Impact of the Low Temperature Ohmic Contact Process on DC and Forward Gate Bias Stress Operation of GaN HEMT Devices

Oguz Odabasi, Amir Ghobadi, Turkan Gamze Ulusoy Ghobadi, Yakup Unal, Gurur Salkım, Gunes Basar, Bayram Butun, and Ekmel Ozbay

***Abstract*— In AlGaN/GaN high electron mobility transistors (HEMTs), high temperature processes (such as ohmic annealing with >800°C value) could deform the crystal structure and induce trap states within the bulk and surface. Expanded defect densities cause crucial problems, such as threshold voltage (V_{th}) instability, current collapse, and high leakages. In this work, a low temperature ohmic contact process (630°C, 10 minutes) is adopted with recess etch, and contact resistances <0.1Ω ·mm with low sheet resistances are achieved. The positive impact of this low thermal budget process on surface morphology, DC operation, long-term stability, and forward gate bias stress of the device is studied.**

***Index Terms*— AlGaN/GaN HEMTs, ohmic contact, stability, surface roughness, annealing temperatures, recessed ohmic contacts.**

I. Introduction

AlGaN/GaN HEMTs are the perfect option for high frequency and high power applications due to the high current capability and electron velocity [1], [2]. Ohmic contact formation is a fundamental step in device fabrication. Especially for high frequency power amplifiers, parasitic resistances have a high impact on RF performance and output power [3]. However, to get low contact resistance (R_c), high temperature annealing is commonly used. [4]. For GaN HEMT, a typical ohmic contact metallization is formed as Ti/Al/Ni/Au stacks [5]. Ti removes the surface oxide and Al diffuses into the bulk to form conductive paths by forming Al-N bonds. The created nitrogen deficiency causes high doping in the contact region, which lowers the barrier and forms an ohmic contact [6]. Ni is also used as a diffusion barrier between the Au and Al layers [7]. Although this approach achieved very low ohmic resistances, it requires very high thermal cycles, might increase to 850°C, and forms alloys and spikes [8]. Such high temperatures can distort GaN crystal and increase the trap densities [9]. In addition, it can cause strain relaxation and reduce the electron density of two-dimensional electron gas (2-DEG) [10].

To address this issue, much effort has been recently devoted to the realization of low temperature ohmic contacts [11]. Tantalum-based ohmic contacts are shown to achieve 0.24 Ω · mm at 500°C [12]. Tungsten (W) based stacks lowered the R_c down to 0.35 Ω · mm with 500°C annealing [13], [14]. However, having a high melting point, W is a hard material for physical vapor deposition (PVD) systems, which is mainly used for most foundries. Ion implantation can provide 0.4 Ω · mm R_c, but post annealing is required to activate the implanted ions [15], [16]. The implementation of MBE or MOCVD growth highly doped (n+) regions for low ohmic contact resistances is also commonly used in highly scaled devices. Low ohmic contact resistances can be achieved without additional annealing due to a high carrier concentration at the regrown region. However, this method requires the sample to enter the MBE or MOCVD chamber after being processed, which can cause contamination in the chamber. It is also relatively expensive and harder to implement. [17]. Among all, the recess etch approach is proven to achieve contact resistances as low as 0.2 Ω · mm at low temperatures [12], [18], [19]. Although much effort has been spent on achieving low contact resistances with minimal thermal budgets, there are very limited studies on the impact of this factor on DC, long-term, and forward gate stress operation of GaN HEMTs. Especially, under a forward bias gate turn on, when a large current density flows, the trapping effects become highly detrimental.

In the present letter, we first develop a recessed low temperature ohmic contact based on Ti/Al/Ni/Au to achieve <0.1 Ω · mm R_c, based on the process described in [19],

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which is one of the smallest reported values so far. Later, conventional high temperature ohmic contacts and the proposed design are brought into HEMT devices. Fabricated devices are tested for surface morphology, DC operation, stability, and forward bias stress conditions. It is found that devices with low temperature ohmic contacts have lower sheet resistance, lower gate leakage currents, and more stable response to DC and long-term stress than a conventional one. Moreover, under forward gate bias stress (which is an important factor for RF amplifiers' large-signal operation), the low temperature HEMT has almost no change in quiescent drain current (I_{DQ}), in gate biases as large as 4 V.

II. Epitaxial-Growth and Device Details

An AlGaN/GaN HEMT epitaxy structure was grown on a 4-H SiC substrate using a metal organic chemical vapor deposition (MOCVD) system. On C-doped GaN buffer, 20 nm AlN nucleation, 200 nm transition and 130 nm channel GaN, 1 nm AlN spike, and 20 nm thick $Al_{0.22}Ga_{0.78}N$ barrier layers were grown, respectively. Electron mobility (μ_n) and concentration (n_s) are 2,000 $cm^2/V{\cdot}s$ and $1.1 \times 10^{13} cm^{-2}$, respectively. The sheet resistance (R_{sh}) of the as-grown HEMT structure was measured as 310Ω/□. For mesa isolation, 100 nm Cl-based etching was used via inductively coupled plasma reactive ion etching (ICP-RIE) on patterns defined by optical lithography. Alloyed ohmic contacts were used for reference devices. Ti/Al/Ni/Au metal stack was deposited by an e-beam evaporator with 12 nm/100 nm/50 nm/50 nm thicknesses, respectively. 830°C, 30 s rapid thermal annealing was applied in a nitrogen environment for ohmic contact formation.

For the low temperature ohmic contacts, a recess etch was applied by ICP-RIE. A 22 nm etch was achieved by using BCl_3/Cl_2 chemistry with low RF power (5 W) to minimize the etching-related damages and to increase the process controllability. After the recess etching, samples were cleaned by using diluted HCl (1:10 water) to smooth away etching residues. A Ti/Al/Ni/Au metal stack was deposited by using an e-beam evaporator, in which the only difference with the reference metal stack was the thickness of the Ti and Al layers. A 3 nm of Ti and 140 nm of Al were deposited while Ni and Au thicknesses were kept the same. These devices were annealed at 630°C for 10 minutes in an N-environment in a rapid thermal annealing chamber.

III. Results and Discussion

R_c and R_{sh} measurements were taken from the transfer length method (TLM) patterns with a 200 μm width and different spacing. The spacings of patterns are verified by using a scanning electron microscope after fabrication. The linear fit of measurements from several patterns was used to calculate the R_c and R_{sh}. TLM patterns were isolated from the rest of the sample by a 100 nm mesa etch. The measured data for the conventional and low temperature ohmic contacts are provided in Fig. 1 (a, b). The linear fit of the total resistances of several channel-distanced ohmic contacts perfectly matches the data for both high temperature ohmic contact and low temperature ohmic contact in Fig. 1 (a). Low temperature ohmic contact shows an R_{sh} of 350Ω/□ and R_c of 0.078 Ohm·mm, while these are found to be 430Ω/□ and R_c

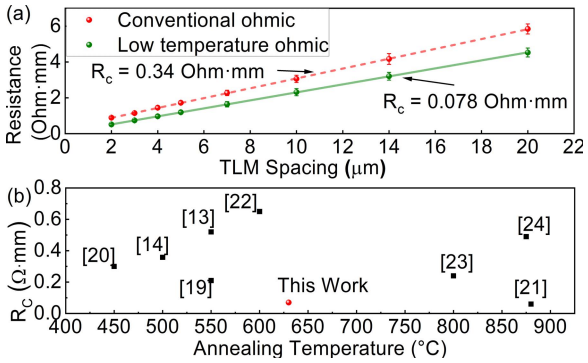

Fig. 1. (a) TLM measurement results with measurement error bars and linear fits of low temperature ohmic contacts and reference contacts, (b) comparison of R_C and anneal temperature of Ti/Al-based annealed ohmic contacts in the literature.

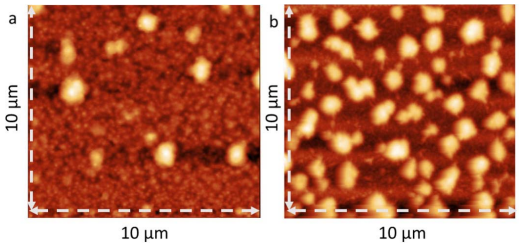

Fig. 2. AFM measurements from (a) low temperature ohmic contact and (b) reference device.

of 0.34 Ohm·mm for conventional HEMT. A contact resistivity of $2.73 \times 10^{-7}\ ohm.cm^2$ is calculated for the low temperature ohmic contacts. The reduction in ohmic contact resistances compared to [19] can be associated with the implementation of Au in the metal stack instead of TiN and a slightly higher annealing temperature.

Besides lower R_c, exposing GaN HEMT to lower temperatures mitigated the formation of surface traps, and this, in turn, shows its impact as lower R_{sh}. Hall effect measurements also gave 15% higher conductivity in low temperature annealed samples compared to high temperature annealed ones. In Fig. 2 (b), the achieved R_C with the proposed method is compared with the previously reported work. R_C of this work is below any reported contact resistance at the below 700-degree range.

Surface roughness is another figure of merit for ohmic contacts. Smoother contact surfaces are desired to prevent device failure, which is related to the long-term diffusion phenomena [25]. Furthermore, it is an important issue in scaling down considerations [26]. Based on the literature, contact with a higher Al/Ti ratio tends to have rougher and bumpy surfaces, although a higher Al/Ti ratio enables lower anneal temperatures [27]. To analyze the surface morphology, atomic force microscopy (AFM) is used in AC surface mode. Fig. 2 (a, b) shows the results of low and high temperature ohmic contacts for a 10 μm × 10 μm area, respectively. The surface of a high temperature sample is rougher, mainly due to alloy formation between gold and aluminum [28]. On the other hand, a low temperature contact surface is quite smooth with sparse bumps. This can also be seen in the numbers. Low temperature ohmic contact has 42 nm surface roughness, while the high temperature one has 104 nm surface roughness.

After surface characterization, to understand the impact of this process on transistor performance, GaN HEMT devices

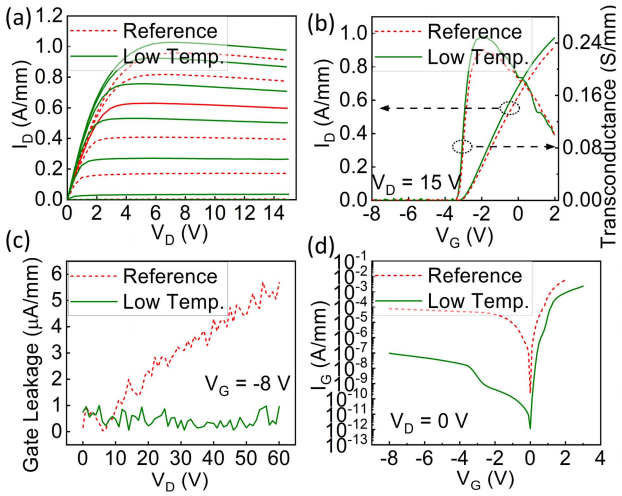

Fig. 3. (a) I_D vs. V_D measurement for V_G from −8V to 1V with 1 V steps, (b) I_D vs. V_G measurement for $V_D = 15$ V, (c) I_G vs. V_D measurements when $V_G = -8$V, (d) I_G vs. V_G when the drain contact is grounded, of low temperature ohmic contact and reference devices.

were fabricated. Device fabrication for both reference and low temperature ohmic contact samples are identical except for ohmic contact formation. 75 nm SiN was deposited by plasma-enhanced chemical vapor deposition (PECVD) after the mesa etch and ohmic contact formation steps. Therefore, both samples have identical passivation that enables the observation of the effects of the ohmic contact formation process. To define the gate patterns, E-beam lithography (EBL) was used with 100 keV. F-based chemistry was used in ICP-RIE for SiN etching. O_2 descum was applied before gate metal deposition to clean the resist residues. 50 nm Ni and 300 nm Au were deposited via an e-beam evaporator as gate metal. Devices have a 5 μm drain to source distance. Gate has a 500 nm foot and an 800 nm gate connected field plate, which is also named gate head. The gate to source and gate to drain distances are 2 μm and 2.75 μm, respectively. Every device has 2 fingers with a 250 μm total gate periphery.

The I_D-V_D characteristics of both devices for different gate voltages (V_G) are plotted in Fig. 3 (a). For 0 V gate bias, improvement in R_{on} from 1.92 Ohm·mm to 1.53 Ohm·mm and an increase of the drain saturation current (I_{DSS}) from 0.95 A/mm to 1.03 A/mm are observed in the low temperature device compared to the reference device, in line with R_c and R_{sh} reduction. As shown in Fig. 3 (b), low temperature HEMT shows a higher maximum transconductance (g_m), which is desired for high frequency operation. Moreover, the proposed design has a lower and V_D invariant gate leakage current at all measured V_D values (Fig. 3 (c)), which offers higher long-term stability. A better leakage and diode turn-on performance can be also seen from the I_G-V_G characteristics of the samples, see Fig. 3 (c). This better Schottky performance and low reverse current prove again the fact that the low temperature process reduces the density of generated bulk and surface traps. This, in turn, leads to a stable and long-term operation of the design [29].

Proposed and reference devices are biased under $V_D = 40$ V. V_G was tuned to flow the same amount of current initially and the biasing was kept constant. Because there was an insignificant V_{TH} difference between devices, the V_G was nearly the same. The change of the current with

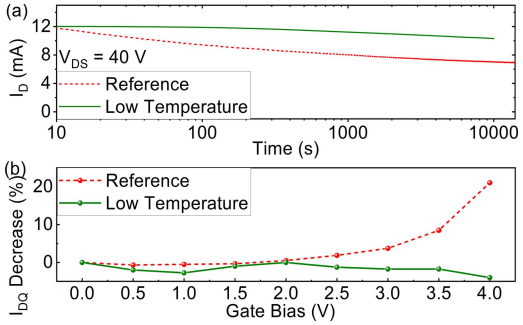

Fig. 4. (a) Long-term I D measurements, (b) forward gate bias I_{DQ} measurements, of low temperature ohmic and reference devices.

time was recorded. As can be seen in Fig. 4 (a), a device with low temperature ohmic contacts only experienced a 1.7 mA I_D decrease, which corresponds to 14%, while this was 5.1 mA, 42% for the reference sample.

The stability of I_D under device operation conditions is an important factor that is satisfied in the proposed design. However, under RF operation, the device experiences positive V_G while V_D is nearly zero volts due to RF swing, which resembles the gate forward current measurements. V_{TH} instability causes a change in the biasing point of the RF signal that can result in instabilities in the output power and turning off the device due to a positive V_{th} shift in extreme cases [30]. To have a better qualitative comparison, their turn-on stress operation is studied.

Consecutive DC measurements by a stressing gate with a positive bias and returning to operation voltage are taken from each device and the quiescent drain current (I_{DQ}) is compared with the initial value. The change in I_{DQ} after these measurements are plotted with respect to the maximum gate voltage in Fig. 4 (b). The device with low temperature ohmic contact showed less than a 5% change in I_{DQ} up to 4 V forward gate bias, which indicates that there is still room for improvement. However, the reference device sees a 20% decrease in I_{DQ}. When the gate is turned on, gate current flows and fills the acceptor type of traps in the vicinity of the gate contact, which leads to a threshold voltage shift. In our proposed device, this effect is minimized due to the reduction of the formation of trap states.

IV. Conclusion

In the present letter, <0.1 Ohm·mm ohmic contact resistance is achieved on GaN/AlGaN/GaN epitaxy by using recess etch and the low temperature anneal process. It is shown that the low temperature improved the sheet resistance. Surface roughness is also decreased in ohmic contacts. GaN HEMT devices are fabricated to test the effect of the proposed contacts on device performance. A combination of a decrease in R_{on} and gate leakages with improvement in transconductance is observed. Long-term DC tests and forward bias gate measurements showed that the devices with proposed ohmic contacts are more stable and reliable under DC operation.

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