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Charge Trapping Memory with 2.85-nm Si-Nanoparticles Embedded in HfO_2

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In this work, the effect of embedding 2.85-nm Si-nanoparticles charge trapping layer in between double layers of high-κ Al_2O_3/HfO_2 oxides is studied. Using high frequency (1 MHz) C-V_{gate} measurements, the memory showed a large memory window at low program/erase voltages due to the charging of the Si-nanoparticles. The analysis of the C-V characteristics shows that mixed charges are being stored in the Si-nanoparticles where electrons get stored during the program operation while holes dominate in the Si-nanoparticles during the erase operation. Moreover, the retention characteristic of the memory is studied by measuring the memory hysteresis in time. The obtained retention characteristic (35.5% charge loss in 10 years) is due to the large conduction and valence band offsets between the Si-nanoparticles and the Al_2O_3/HfO_2 tunnel oxide. The results show that band engineering is essential in future low-power non-volatile memory devices. In addition, the results show that Si-nanoparticles are promising in memory applications.

Silicon-nanoparticles have been extensively investigated and considered as good candidates for storage elements in next-generation low power and high density non-volatile charge trapping memory devices (1-7). However, the size of the nanoparticles greatly affects the memory performance. In fact, as the size of the nanoparticle is reduced, its bandgap, work-function, and charging energy increase, while its electron affinity and dielectric constant reduce (8-11). Earlier, we demonstrated memory devices with 2-nm Si-nanoparticles and holes storage was observed due to the small electron affinity of the nanoparticles and therefore a lack of conduction band offset between charge storage layer and tunnel oxide was obtained (12-14). In this work, 2.85-nm Si-nanoparticles are studied as the charge trapping layer of MOS memory devices with double layer Al_2O_3/HfO_2 tunnel oxide. Mixed charging is observed due to the increased electron affinity. Electrical characterization and energy band diagram analysis of the fabricated memory devices are provided to understand the effect of the 2.85-nm Si-nanoparticles charge trapping layer on the memory performance.

The memory cells are fabricated on an n+-type (111) (Antimony doped, 15-20 mΩ-cm) Si wafer. 5-nm-thick tunnel oxide Al2O3 is deposited at 250°C in Cambridge Nanotech Savannah-100 atomic layer deposition (ALD) system. Then, 1-nm-thick HfO_2 is deposited by Plasma Assisted ALD at 195°C in an Oxford FlexAL system. Next, 2.85-nm Si-nanoparticles are spin coated on the sample. Again, a 1-nm-thick HfO2 is deposited by plasma assisted ALD at 195°C. Finally, an 8-nm-thick Al_2O_3 blocking oxide is deposited by ALD at 250°C. A 400-nm-thick Al layer for the gate contact is e-beam evaporated using a shadow mask with 10 µm feature size which eliminated the need for lithography steps. A cross-sectional illustration of the fabricated memory device is depicted in Figure 1.

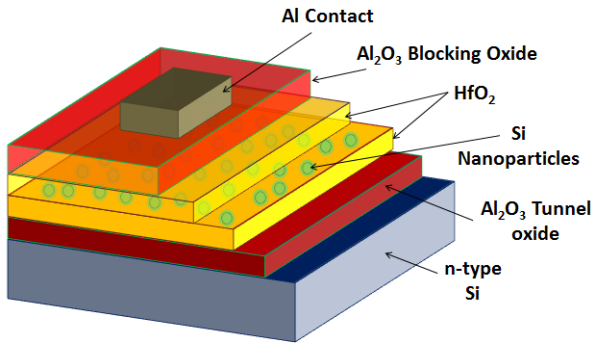

Figure 1: Schematic cross-section of the fabricated charge trapping memory cell with 2.85-nm Si nanoparticles.

The fabricated memory devices are electrically characterized by measuring the high frequency (1 MHz) C-Vgate characteristics of the programmed and erased states. Using the Agilent B1505A Semiconductor Device Parameter Analyzer, the memory cells gate voltage was first swept from -6 V forward to 6 V then backwards. A 1.8 V threshold voltage (V_t) shift is observed. The C-V measurements are repeated at a gate sweeping voltage of 8/-8 V and both erased and programmed states shifted outwards as shown in Figure 2 resulting in a 4.5 V memory window. This indicates that unlike smaller Si-nanoparticles (2-nm) which are found to store only holes due to the smaller electron affinity (6), 2.85-nm Si-nanoparticles in the charge trapping layer are storing mixed charges: electrons and holes, however, more charging is due to holes revealed by the greater shift of the erased state in the negative direction as shown in Figure 2.

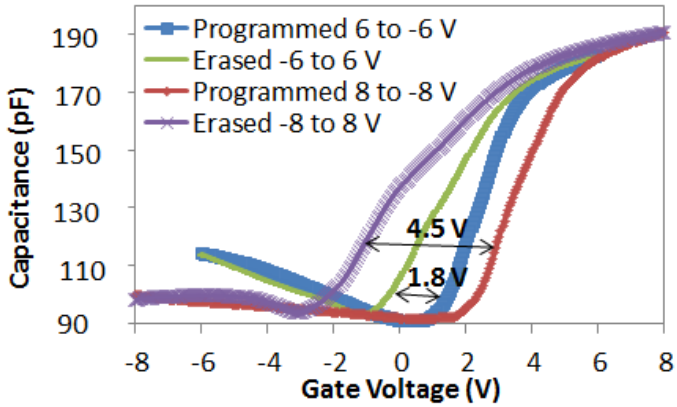

Figure 2: Measured hysteresis behavior using the *C-V_{gate}* characteristic showing a 4.5 V V_t shift at 8/-8 V gate sweeping voltage.

Moreover, the V_t shift is measured at different gate sweeping voltages as sown in Figure 3 and the charge trapping density in the Si-nanoparticles is calculated using the following equation (15-18) and found to be 2.32 $\times 10^{13}$ cm^{-3}:

$$N_t = \frac{C_t \times \Delta V_t}{q} \quad [1]$$

where C_t is the capacitance of the memory per unit area, ΔV_t is the V_t shift, and q is the elementary charge.

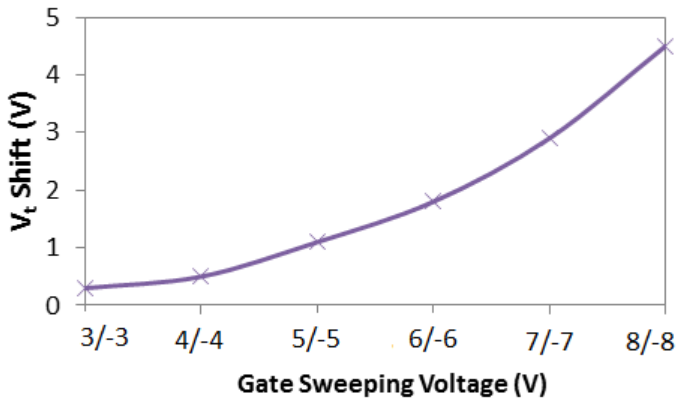

Figure 3: Measured threshold voltage shift using the *C-V*$_{gate}$ characteristic at different gate sweeping voltage.

In addition, the energy band diagram of the memory with Si-nanoparticles is constructed as shown in Figure 4 using the reported electron affinities, band offsets, and band gaps of Al_2O_3, HfO_2, and 2.85-nm Si-nanoparticles (19-32). The changes due to quantization and coulomb charging energy of the 2.85-nm Si-nanoparticles are included. The conduction band offset between Si and tunnel oxide is smaller than the valence band offset (ΔE_C = 2.44 eV < ΔE_V = 3.24 eV), thus the electrons tunneling probability is expected to be higher. However, the conduction band offset between the 2.85-nm Si-nanoparticles and tunnel oxide is much smaller than the valence band offset (ΔE_C = 1.29 eV << ΔE_V = 3.77 eV). This means that stored electrons can leak out and tunnel back to the Si channel much easier than holes. This confirms the observed larger charging due to holes in Figure 2. Moreover, the addition of the high-dielectric constant (κ=20) HfO_2 layer is expected to reduce the leakage of stored charges.

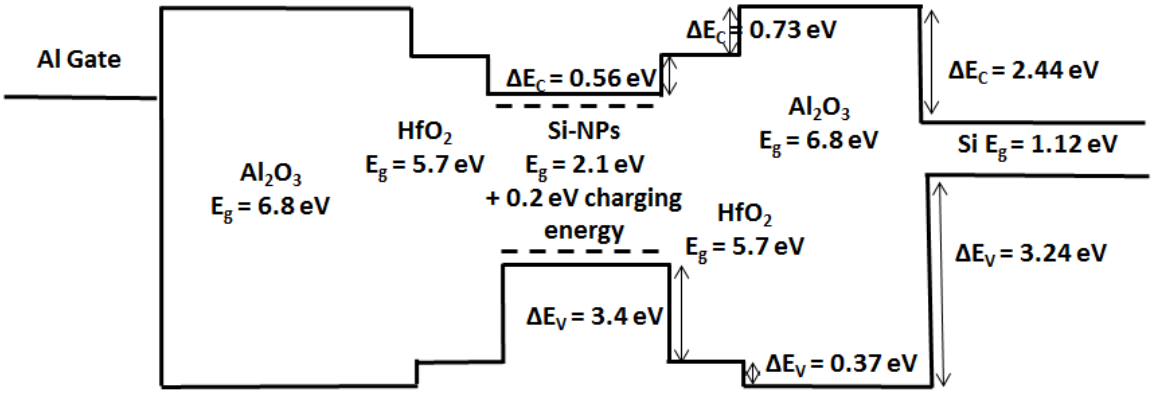

Figure 4: Energy band diagram of the fabricated MOS memory with 2.85-nm Si-nanoparticles.

Moreover, the retention of the memory cells with Si-nanoparticles is characterized by first programming/erasing the memory at 8/-8 V and observing the change in Vt shift in time as shown in Figure 5. The memory with Si-nanoparticles showed a loss of 35.5% of the initial charge in 10 years. Also, Figure 5 shows that the measured V_t of the erased state is almost constant in time which means that holes retention in the Si-nanoparticles after 10 years is excellent, however, the V_t of the programmed state is reducing in time which means that electrons are leaking out at a faster rate. This can be explained from the energy band diagram plot in Figure 4 where the valence band offset between the charge trapping layer and the Al_2O_3 tunnel oxide is much larger than the corresponding valence band offset (ΔE_C = 1.29 eV < ΔE_V = 3.77 eV) which exponentially reduces the back tunneling of holes.

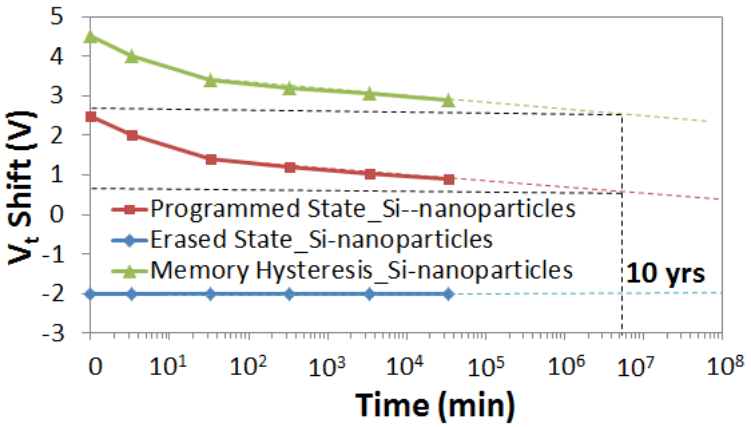

Figure 5: Retention characteristic of the MOS memory with 2.85-nm Si-nanoparticles

In conclusion, 2.85-nm Si nanoparticles charge trapping layer is studied in MOS memory devices with double layer Al_2O_3/HfO_2 tunnel oxide. The results show that a wide memory hysteresis is obtained at low operating voltages due to charging in the Si-nanoparticles. The Si-nanoparticles are found to be storing mixed charges unlike smaller Si-nanoparticles (2-nm). Also, the good retention characteristic of such memory structure is due to the large conduction and valence band offsets between charge storage layer and tunnel oxide. The results show that such memory structures have potential in future low power non-volatile-memory devices.

Acknowledgments

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