A High-Power and Broadband GaN SPDT MMIC Switch Using Gate-Optimized HEMTs

Volkan Erturk, *Graduate Student Member, IEEE*, Armagan Gurdal, and Ekmel Ozbay, *Member, IEEE*

***Abstract*— A high-power, broadband monolithic microwave integrated circuit (MMIC) single-pole double-throw (SPDT) switch is designed with gate-optimized high-electron-mobility transistors (HEMTs) using AlGaN/Gallium nitride (GaN) technology. The foot length of the gate is varied from 200 to 250 nm, and the head length is varied from 500 to 750 nm in the T-gate structure to optimize the radio frequency (RF) performance. The SPDT switch is designed in a series–shunt–shunt topology using gate topology as a design parameter. The switch has achieved an insertion loss better than 0.75 dB throughout the 3.5–13.5-GHz bandwidth. It can transmit 30-W output power at 0.1-dB compression point and handle 47.5-dBm input power at $P_{1\,\mathrm{dB}}$. The isolation is above 25 dB, and the return loss is better than 11 dB. With its low insertion and high power-handling capacity in broadband, the SPDT switch shows state-of-the-art performance for high-power communication systems and radar applications.**

***Index Terms*— Gallium nitride (GaN), high-electron-mobility transistor (HEMT), high power switch, monolithic microwave integrated circuit (MMIC), single-pole double-throw (SPDT).**

I. Introduction

HIGH-POWER radio frequency (RF) switches are critical components for communication systems, commonly placed in satellites, radars, base stations, and transmit/receive (T/R) modules. These high-performance systems require switches with low insertion loss, high power-handling capacity, high isolation between isolated ports, and wide bandwidth.

Micro-electromechanical systems (MEMSs) can provide exceptional RF performance in terms of insertion loss, isolation, and power-handling capacity [1] while suffering from slow switching speed and incompatibility with the monolithic microwave integrated circuit (MMIC) process. Likewise, PIN diode switches are capable of handling high power levels with a disadvantage in dc power consumption [2].

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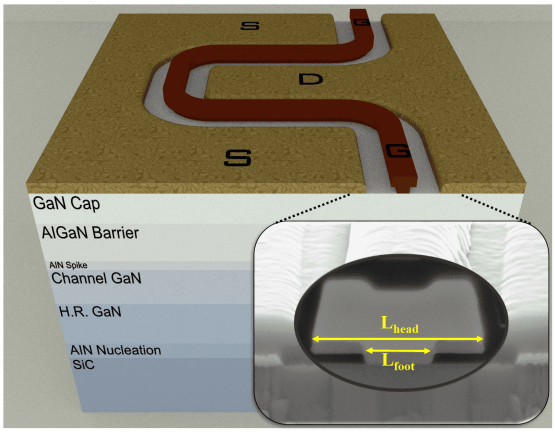

Fig. 1. Drawing of the HEMT structure and SEM image of the fabricated T-gate in the right-bottom corner.

High-electron-mobility transistors (HEMTs), on the other hand, have several advantages in low power consumption, high RF performance, ease of integration in MMIC, and low cost. Gallium nitride (GaN) on silicon carbide (SiC)-based HEMTs are especially preferred in high-power applications because of their extreme electrical and thermal characteristics.

In the past, several studies on switch topology have been reported with enhanced RF performances [3], [4], [5] along with series–shunt switches with quarter-wave transformers. However, circuit topology performance is limited by transistor performance. In this letter, the design and characterization of high-power (45 dBm), broadband (3.5–13.5 GHz), single-pole double-throw (SPDT) RF switches for AM radar applications using gate-optimized GaN on SiC HEMTs are presented. The foot length of the gate (L_{foot}) is varied from 200 to 250 nm, and the head length (L_{head}) is varied from 500 to 750 nm. The gate topology is used as a design parameter for optimum performance. With the optimized gate structure, the symmetric SPDT switch is designed in a series–shunt–shunt topology with gate-optimized 1500-μm series and 500-μm shunt HEMTs. The switch can transmit 30-W output power with insertion loss below 0.75 dB throughout the bandwidth. The return loss and isolation are better than 11 and 25 dB, respectively.

II. GaN-Based MMIC Process

In this study, switch HEMTs and MMICs are fabricated using Bilkent University Nanotechnology Research Center (NANOTAM) GaN on SiC fabrication technology with a substrate thickness of 100 μm. The epitaxial structure is

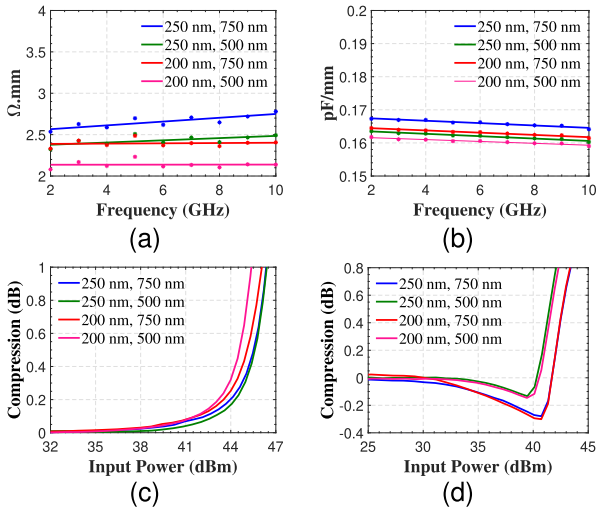

Fig. 2. Measured (a) R_{ON}, (b) C_{OFF}, (c) power-handling of ON-state, and (d) OFF-state for different gate structures (legend shows L_{foot} and L_{head}, respectively).

grown on SiC substrate using metal-organic chemical vapor deposition (MOCVD), which can be seen in Fig. 1. The 2-D electron gas density has 1.1×10^{13} cm^{-2} density and 2×10^{3} cm^{2}/V-s mobility.

The ohmic contacts are formed with Ti/Al/Ni/Au (20/100/40/50 nm) metal stack. Transmission line measurements show 0.25-Ω·mm contact resistance. Switch transistors have T-shaped Ni/Au gates. L_{foot} is varied from 200 to 250 nm, and L_{head} is varied from 500 to 750 nm. Fig. 1 shows the scanning electron microscope (SEM) image of the fabricated T-gate structure. The gate feet and head thicknesses are 50 and 300 nm, respectively. The source-to-drain region of HEMTs is 2.5 μm. The gate foot and the gate heads are positioned in the middle of the drain–source region for a symmetric gate structure.

III. HEMT Performance Optimization

The performance of the transistor depends on its R_{ON} and C_{OFF} values and maximum power-handling capacity, which can be optimized by changing its T-gate structure. To observe the performance variation, four different transistors are fabricated and characterized using the two-port measurements from the drain and source sides. When gate head and foot sizes are reduced, drain–source ON-state resistances should reduce due to the smaller footprint of the gate. Likewise, OFF-state capacitance is also reduced when the gate shrinks in size [6]. Fig. 2(a) and (b) shows R_{ON} and C_{OFF} values of different gate structures measured at 0 and −28 V gate voltage, respectively. Thus, the performance figure of the transistors is improved at the expense of power-handling capacity. R_{ON} and C_{OFF} values are calculated using the following equations:

$$R_{\text{ON}} = 2Z_0(10^{-S_{21\,\text{dB}}/20} - 1) \tag{1}$$

$$C_{\text{OFF}} = \frac{1}{2Z_0 w\sqrt{10^{-S_{21\,\text{dB}}/10} - 1}}. \tag{2}$$

From Fig. 2(a) and (b), the ON-state resistance is reduced by 0.5 Ω·mm while the OFF-state capacitance is reduced by 0.08 pF/mm. On the other hand, reducing gate foot and head lengths also leads to early compression of the device [7] compared with devices with larger T-gates and field plates. The reason is that a larger T-gate improves the breakdown voltage and maximum current-handling capacity of switch HEMTs [8]. Thus, RF power handling could be estimated to be improved with higher breakdown voltage and maximum current [7].

TABLE I
Performance Summary of HEMT in Different Gate Topologies

Gate Type	R_{on} (Ω.mm)	C_{off} (pF/mm)	FOM (GHz)	P_{1dB} (dBm)	OIP3 (dBm)
250 nm L_{foot} 750 nm L_{head}	2.658	0.163	367	46.39	46.054
250 nm L_{foot} 500 nm L_{head}	2.431	0.161	407	46.37	45.81
200 nm L_{foot} 750 nm L_{head}	2.406	0.1597	414	46.06	45.39
200 nm L_{foot} 500 nm L_{head}	2.116	0.158	476	45.33	45.065

The power-handling of the transistors is measured at 10 GHz by varying the input power up to 1-dB compression point. The measured output power and compression results are shown in Fig. 2(c) and (d) for both the ON-state and OFF-state devices. Devices with 200-nm L_{foot} compress at a lower power level compared with 250-nm L_{foot} devices. Therefore, it does not provide the best performance for large input power levels. In the OFF-state, devices with 500-nm L_{head} compress at higher power levels compared with 750-nm L_{head} devices. The negative gain compression of the OFF-state HEMTs is due to nonlinear drain-to-source capacitance variation with respect to drain voltage [9]. The linearity of the transistors is also characterized by their OIP3 points. Two-tone signals are generated at 10-GHz ± 5 MHz. The performance summary of HEMTs is given in Table I. Transistors with larger gate dimensions showed better linearity characteristics. Figure-of-merit (FOM) [10] of switches which is inversely proportional to C_{OFF} and R_{ON} is also included in Table I. Considering the measured performance parameters, the transistor with the optimum performance is 250-nm L_{foot} and 500-nm L_{head} which outputs the highest RF power with a good insertion loss and isolation. The gate-optimized HEMTs are used in the SPDT switch design.

IV. SPDT Switch Design

The SPDT switch is designed to be symmetrical with two identical branches in the series–shunt–shunt topology. Transistors with 250-nm L_{foot} and 500-nm L_{head} gate structures are chosen to maximize the switch performance. The 1500-μm device is connected in series to improve isolation and keep insertion loss low with high power-handling capacity. An inductor that tunes out the OFF-state capacitance of series HEMT is placed in parallel to improve isolation and insertion loss at higher frequencies [11]. This design choice enables an insertion loss with low variation throughout the whole X and C bands. HEMTs with 500-μm gate peripheries are used in shunt configuration so that the isolation of the switch is improved further. Sizes of transistors are chosen to transmit 30-W output power at below 1-dB compression. Although

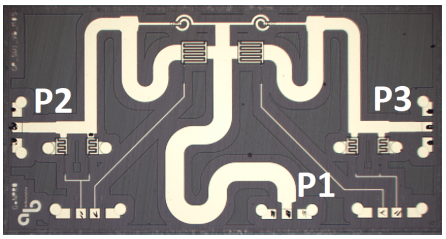

Fig. 3. Microscope image of the MMIC SPDT switch.

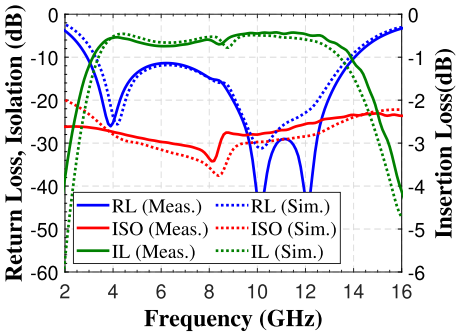

Fig. 4. Measured and simulated small-signal performance of the SPDT switch.

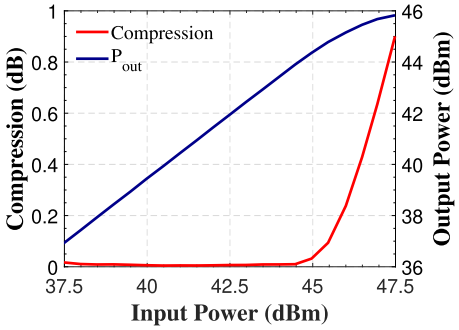

Fig. 5. Measured large-signal performance at 10 GHz of the SPDT switch.

increasing transistor size improves the power performance, the bandwidth of the switch starts to shrink due to higher C_{OFF}.

The gate control resistances of the HEMTs are chosen to be 3.6 kΩ. A gate control voltage of 0 and −28 V is applied to switch between OFF-state and ON-state, respectively. The gate voltages are controlled by V_{G1} and V_{G2} from the dc pads. Fig. 3 shows the image of the fabricated SPDT switch. The bandwidth of the SPDT switch is chosen to be 3.5–13.5 GHz to cover the entire *C*-band and *X*-band. The overall area of the switch is 2×4 mm^2.

V. SPDT Switch Performance

The small-signal performance of the SPDT MMIC switch is characterized under continuous wave (CW) conditions. In the small-signal setup, the standard two-port TOSM calibration method is used. The −28 V is applied to V_{G1} while V_{G2} is kept at 0 V to direct the signal from Port 1 to Port 2. The base temperature is kept at 25°C. Fig. 4 shows the switch's measured and simulated return loss and isolation performances. Return loss is better than 11 dB throughout the bandwidth, while isolation ranges between 25 and 34 dB.

TABLE II
Performance Comparison of SPDT Switches

Ref	Freq. (GHz)	IL (dB)	ISO (dB)	RL (dB)	P_{1dB} (dBm)
[12]	8-12	< 1.6	< 20	< 15	38
[13]	0-12	< 1	< 30	< 14	42
[14]	8.4-10.6	< 1.1	< 28	< 13	42
[15]	8-12	< 0.8	< 44	< 13	43.3
[16]	6-18	< 1	< 30	< 10	45
[17]	8-12	< 3.5	< 35	< 10	44*
This Work	3.5-13.5	< 0.75	< 25	< 11	47.5

* Measurement frequency and compression level are not specified.

The insertion loss of the switch is less than 0.75 dB over the 3.5–13.5-GHz bandwidth. The large-signal performance of the SPDT switch is determined by varying the input power. The input power is injected from Port 1, and the output power is measured from Port 2. As shown in Fig. 5, the input power is increased up to 47.5 dBm. At $P_{0.1\,\text{dB}}$ point, the switch is able to transmit 30-W power.

The ON time of the switch is characterized by the time period between 50% of the input signal and 90% of the square-law detector RF power. The OFF time of the switch is characterized by the time period between 50% of the input signal and 10% of the square-law detector RF power. The switching time of the MMIC is measured to be 49 ns for OFF-state transition and 24 ns for ON-state transition.

The performance comparison of this work with the state-of-the-art GaN SPDTs is shown in Table II. Our design provides excellent insertion loss in broadband. Compared with other competitive switches in the literature, this design is able to transmit significantly higher RF power with GaN technologies due to its optimized gate structure. Especially when compared with high-performing switches in [15] and [16] with similar shunt–shunt and series–shunt topologies, our work outperforms, thanks to the gate-optimization technique. While keeping the power-handling high, the insertion loss is kept low with gate topology selection.

VI. Conclusion

In this letter, switch HEMTs with different gate foot and head lengths are fabricated with AlGaN/GaN on SiC technology to optimize their RF performance. The HEMT with 200-nm foot and 500-nm head lengths showed the most promising result. Using the gate-optimized HEMTs, an SPDT switch is fabricated with an insertion loss of 0.75 dB for AM radar applications. Isolation and return losses are better than 25 and 11 dB, respectively. The switch can transmit 30-W output power at $P_{0.1\,\text{dB}}$. The total area of the chip is 2×4 mm^2. The gate-optimized HEMTs and SPDT switches can be used in high-power communication systems and radar applications.

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