A Performance Enhanced Power Divider Structure

Vahdettin Tas[1,2], Abdullah Atalar[1]
[1]Department of Electrical and Electronics Engineering, Bilkent University, Ankara, Turkey
[2]Power Amplifier Technologies Divison, REWIS, Aselsan Inc., Ankara, Turkey
vtas@ee.bilkent.edu.tr, aatalar@bilkent.edu.tr

***Abstract*—We analyze the bandwidth capability of a divider with a series RLC circuit at the isolation arm. Analytical expressions for optimal component values are given. Bandwidth limiting effect of the pad capacitances of the chip resistors is analyzed. These parasitic capacitors are compensated by the proposed structure. Broadband characteristic of the new divider is verified by experimental results.**

***Index Terms*—wideband power divider, isolation resistor parasitics, pad capacitance.**

I. INTRODUCTION

Power dividers are used at microwave frequencies to direct the power to two or more loads with minimal loss. The Wilkinson power divider was introduced in 1960 [1]. It is matched at all ports and has good isolation between the output ports within a frequency band. Cohn [2] introduced the multisection hybrids to overcome the bandwidth deficiency of the Wilkinson dividers. Broadband power division using multisection structures was revealed in several works [3], [4]. RLC networks in series or parallel configuration have been used to design dividers for dual band operation [5], [6], [7]. In these studies, a detailed analysis for broadband operation is not available. In [8], wideband isolation characteristic was analyzed using series RLC network but the final design lacks a good input return loss and insertion loss characteristic.

In this work, the divider with a series RLC network in the isolation arm is analyzed with a special focus on the tradeoff between bandwidth and desired S-parameter level of the isolation and input-output return losses. Analytic expressions for the required component values are derived. Bandwidth limiting effects of the parasitics of the isolation resistor is discussed. A divider structure is designed to eliminate the dominant parasitic effects.

II. ANALYSIS AND DESIGN OF THE DIVIDER

In Fig. 1, a symmetrical multisection 2-way divider network is depicted. The network is composed of lossless quarter-wave transmission lines apart from the isolation arms shown with gray boxes. For a classical multisection Wilkinson divider, the gray boxes are composed solely of the isolation resistors.

Inclusion of reactive elements in the gray box in addition to the resistor can increase the bandwidth performance of the divider considerably. Fig. 2-a illustrates the odd mode equivalent circuit of the divider in Fig. 1. The transmission lines are quarter wavelength at the center frequency of f_0. Z_{in-1} is inductive for $f < f_0$ and capacitive for $f > f_0$. This limits the bandwidth of the divider. For compensation, a

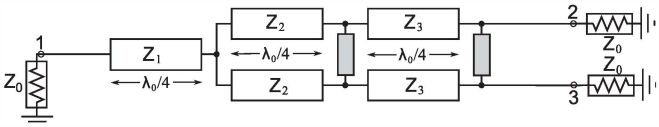

Fig. 1. A symmetrical 2-way power combiner/divider network. White boxes are quarter-wave transmission lines. Gray boxes represent the lossy isolation arms.Possible contents of a gray box: Symmetrical lossless components with isolation resistors in the middle.

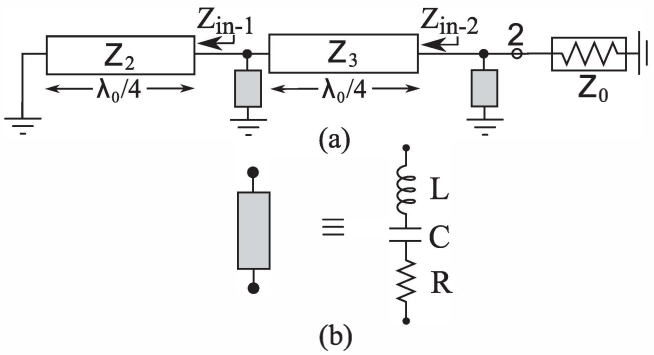

Fig. 2. a) Odd mode equivalent circuit of the divider in Fig 1. b) Possible content of a gray box for wideband operation: Series RLC network.

resonator with the opposite characteristic is required. A series RLC network shown in Fig. 2-b is suitable for this purpose.

Fig. 3-a shows the overall structure for the two-section case. Even mode tuning element is a transmission line and odd mode tuning element is a series LC circuit. To preserve the symmetry, capacitors and inductors are placed at two sides of the resistor. We analyze the trade off between bandwidth and the S-parameter levels. The even mode equivalent circuit is illustrated in Fig. 3-b. To maximize the bandwidth of the impedance conversion from Z_0 to $2Z_0$, the parameters $2Z_1$ and Z_2 are chosen to satisfy the following equation [9]:

$$2Z_1Z_2 = 2Z_0^2 \tag{1}$$

By allowing a nonzero reflection coefficient $|\Gamma_e| \leq \delta$ ($\delta \ll 1$), the bandwidth of operation can be extended. At the band center, f_0, we have:

$$\frac{Z_2^2}{4Z_1^2}\frac{2Z_0}{} = Z_0\frac{1+\Gamma_e}{1-\Gamma_e} \tag{2}$$

With the condition $\Gamma_e = \delta$ at f_0 (reducing the impedance conversion ratio), (2) can be rewritten as:

$$\frac{Z_1}{Z_2} = \sqrt{\frac{1-\delta}{2(1+\delta)}} \approx \frac{1}{\sqrt{2}}\left(\frac{1-\delta/2}{1+\delta/2}\right) \tag{3}$$

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Using (1) and (3), Z_1 and Z_2 are calculated as:

$$\frac{Z_1}{Z_0} = 2^{-1/4}(1-\delta/2) \tag{4}$$

$$\frac{Z_2}{Z_0} = 2^{1/4}(1+\delta/2) \tag{5}$$

The odd mode equivalent circuit is shown in Fig. 3-c. $L/2$

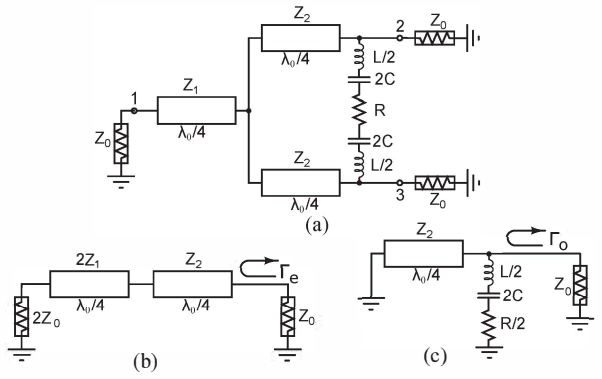

Fig. 3. a) Broadband 2-way divider. b) Even-mode equivalent circuit. c) Odd-mode equivalent circuit.

and $2C$ resonate at the band center:

$$\frac{1}{\sqrt{LC}} = 2\pi f_0 \tag{6}$$

At f_0, we impose $|\Gamma_0| = \delta$. So, R can take two values: $R = 2Z_0(1 \pm \delta)/(1 \mp \delta)$. The smaller one results in a wider band, since the resistive component gets dominant with respect to the shorted transmission line. So, we find

$$\frac{R}{Z_0} = 2\frac{1-\delta}{1+\delta} \approx 2(1-2\delta) \tag{7}$$

To calculate L and C analytically, we follow the approach in [2]. We define the bandwidth condition of $|\Gamma_e| < \delta$ as $f_0(1-k) < f < f_0(1+k)$. Since Z_1 and Z_2 are calculated using (4) and (5), k is a known parameter. To maximize the overall bandwidth, we assume that the $|\Gamma_0| < \delta$ condition covers the same frequency range and calculate L as

$$\frac{w_0 L}{Z_0} = \frac{(1-k)(b+\sqrt{b^2-4ac})}{ak(2-k)} \tag{8}$$

where

$$a = 1 + t^2\sqrt{2}(1+\delta) \quad , \quad b = 2^{5/4}t(1+\delta/2) \tag{9}$$

$$c = 1 - 4\delta \quad , \quad t = \tan(\pi/2 - k\pi/2) \tag{10}$$

Fig. 4 shows the bandwidth performance of the divider. Between the frequencies f_1 and f_2, the parameters $|S_{11}|$, $|S_{22}|$, $|S_{32}|$ stay below the prescribed S-parameter level. Fig. 5 is a plot of the required component values to achieve the bandwidth ranges expressed in Fig. 4.

The implementation of this circuit is difficult due to the parasitics of the lumped components. Even the small pad capacitors to ground of the serial components significantly affect the performance. Fig. 6 shows a high frequency model of a chip resistor. For the even mode, the components R, L_s, C_s

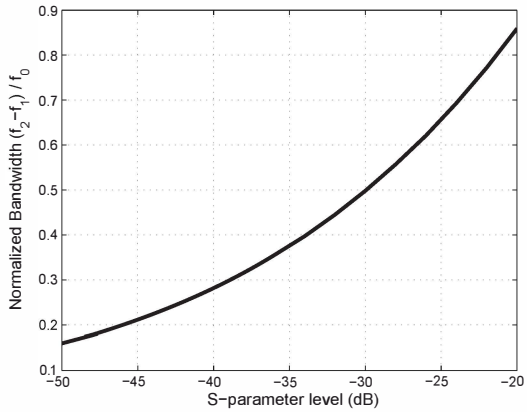

Fig. 4. Achievable bandwidth versus the desired S-parameter level for the divider in Fig. 3. The bandwidth is normalized with the center frequency.

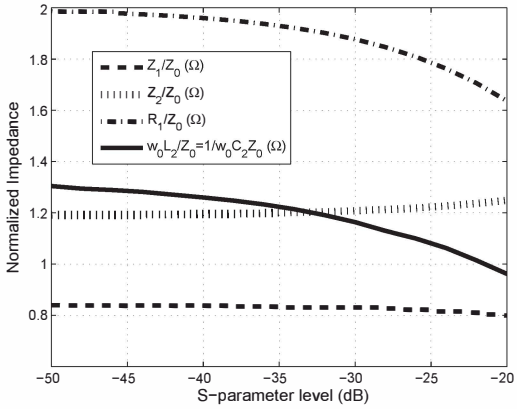

Fig. 5. The component values to achieve the bandwidth ranges expressed in Fig. 4.

are not in the picture, but the pad capacitance C_p results in a path to the ground which degrades the bandwidth performance of the divider. To prevent this, C_p should be tuned out. For this purpose, we propose the structure in Fig. 7 where C_p is tuned out using a shorted transmission line, Z_p. The inductor, L, is implemented with a high impedance transmission line, Z_s that also compensates the parasitics of the capacitor, C. The new configuration of the isolation arm affects also the even mode circuit. The insertion loss due to the resistor is avoided by placing it at the mid point. Being effective also in the even mode, the network in the isolation arm is optimized to enhance the bandwidth of the input return loss as well as the output return loss and isolation. This extra degree of freedom allows the input transmission line, Z_1, to be eliminated. Analysis of these results will be presented in an extended version of this paper.

III. EXPERIMENTAL RESULTS

The divider structure introduced in Fig. 7 was implemented on an AD250 substrate with a thickness of 1.6mm. Fig. 8 shows the photo of the divider. It was designed to achieve over

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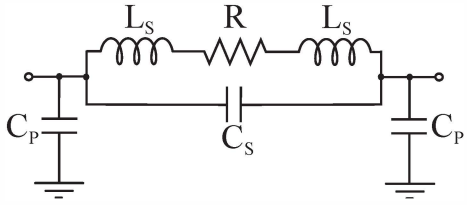

Fig. 6. Equivalent circuit of a chip resistor.

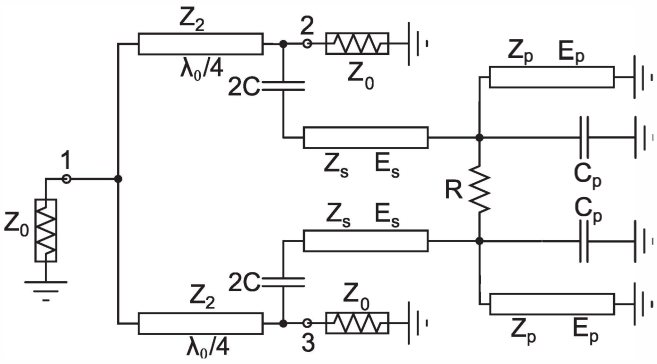

Fig. 7. Schematic diagram of a 2-way divider with symmetric transmission lines in the isolation arm to enhance the band and to compensate the parasitics of the resistor.

25dB isolation and return loss in the band of 675–1325MHz. Figs. 9 and 10 show the measured results. Return loss values are better that 18.5dB in a bandwidth of 625–1500MHz. In a wider band the isolation is over 20dB. Extra insertion loss is lower than 0.2dB and the amplitude mismatch between the output ports is lower than 0.1dB.

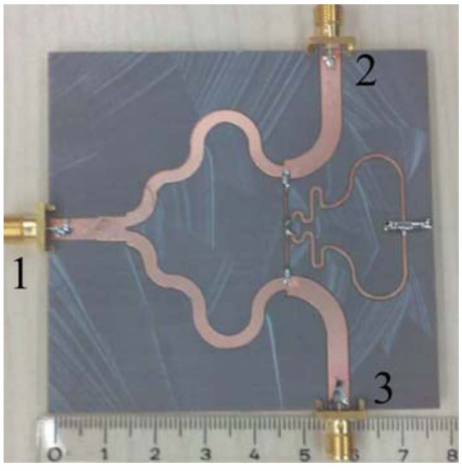

Fig. 8. Implemented 2-way power divider (Fig. 7).

IV. CONCLUSIONS

A series RLC circuit is utilized in the isolation arm of a Wilkinson divider to improve its bandwidth. Parasitic shunt capacitances of the isolation resistors affect the performance negatively. This effect is eliminated using a new power divider

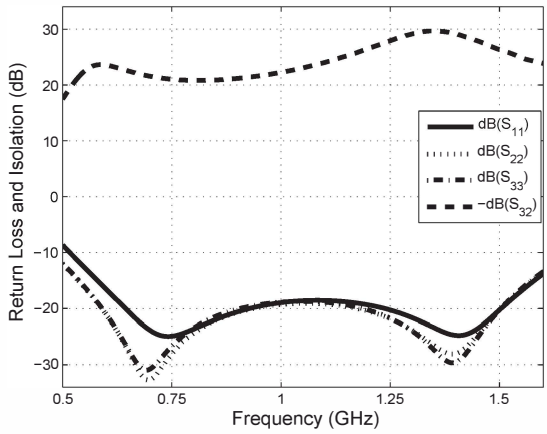

Fig. 9. Measured return loss and isolation characteristic of the divider in Fig. 8.

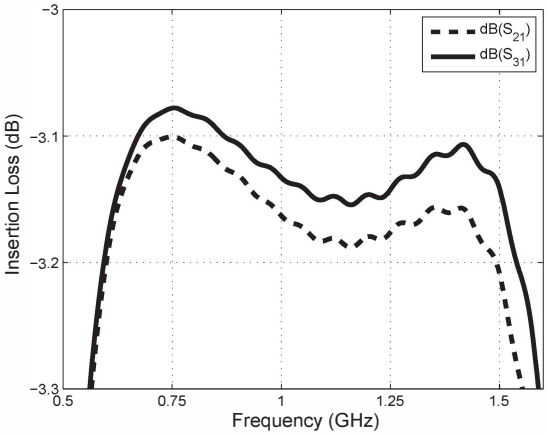

Fig. 10. Measured insertion loss characteristic of the divider in Fig. 8.

structure. Bandwidth response of the divider is promising for wide band applications.

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