

HIGH POWER HIGH EFFICIENCY MICROWAVE  
POWER AMPLIFIER DESIGN USING CLASS-E  
TOPOLOGY

A THESIS

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By

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July 2010

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## ABSTRACT

# HIGH POWER HIGH EFFICIENCY MICROWAVE POWER AMPLIFIER DESIGN USING CLASS-E TOPOLOGY

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M.S. in Electrical and Electronics Engineering

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Power consumption is a major problem in wireless technology. Since power amplifier is one of the most power consuming element, efficiency of the power amplifier should be optimized. Switching amplifiers typically offer very high efficiency. As the frequency increases, the efficiency drops. Class-E is a switching amplifier which is suitable for microwave frequencies. It attains a very high efficiency with proper voltage and current characteristics. Different techniques to obtain these characteristics are possible. In this work, we implement a 38 dBm power amplifier at 2 GHz. Different methods are examined to obtain a high efficiency behavior. We obtained a power added efficiency of 60%.

Keywords: Class-E, Microwave Frequency, High Power, High Efficient

## ÖZET

# YÜKSEK GÜÇLÜ YÜKSEK VERİMLİ MİKRODALGA GÜÇ KUVVETLENDİRİCİSİNİN E-SINIFI TOPOLOJİ KULLANILARAK TASARIMI

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Elektrik ve Elektronik Mühendisliği Bölümü Yüksek Lisans

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Güç tüketimi kablosuz teknolojilerde önemli bir problemidir. Güç kuvvetlendiricisi en çok güç harcayan elemanlardan biri olduğu için, güç kuvvetlendiricisinin verimi optimize edilmelidir. Anahtarlama kuvvetlendiriciler genel anlamda çok yüksek verimler sağlarlar. Frekans arttıkça, verim düşer. E-sınıfı, mikrodalga frekansı için uygun bir anahtarlama kuvvetlendiricidir. E- sınıfı, uygun gerilim ve akım karakteristikleri ile oldukça yüksek verimlere ulaşır. Bu karakteristikleri elde etmek için değişik teknikler bulunur. Bu çalışmada, 2 GHz frekansında, 38 dBm çıkışlı bir güç kuvvetlendiricisi gerçekleştirilmiştir. Yüksek verimli davranışı elde etmek için değişik teknikler incelenmiştir. Elde edilen güç katılmış verim %60'tır.

Anahtar Kelimeler: E-Sınıfı, Mikrodalga Frekansı, Yüksek Güç, Yüksek Verim

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**To my beloved family**

## LIST OF ABBREVIATIONS

RF	Radio Frequency
PA	Power Amplifier
BW	Band Width
PAE	Power Added Efficiency
PCB	Printed Circuit Board
OFDM	Orthogonal Frequency-Division Multiplexing
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase-Shift Keying
CMCD	Current Mode Class D
VMCD	Voltage Mode Class D
RFC	Radio Frequency Choke
LDMOS	Laterally Diffused Metal Oxide Semiconductor
GAN	Gallium Nitride
IMD	Intermodulation Distortion
OIP3	Output Intercept Point Third
TL	Transmission Line
IMC	Input Matching Circuit
OMC	Output Matching Circuit
PAPR	Peak-to-Average Power Ratio

# Chapter 1

## INTRODUCTION

### 1.1 General Introduction

As the wireless communication takes important place in everyday life, an optimized design of power amplifiers (PA) becomes a necessity. High power, high efficiency and highly linear amplification can not be easily achieved at the same time. In wireless communication, portable devices are widely used. These portable devices are battery consuming and the life time of the battery is very important. This reason forces designers to design more efficient amplifiers. Since power amplifier is one of the most power consuming element in such a system, the efficiency of the power amplifier is one of the most important design considerations. More efficient power amplifiers give a way to the portable devices with a longer the battery life time and enable a smaller battery.

Especially in high power applications, the need for efficiency increases due to an increase in the dissipated power of power amplifier. So, achieving a high output power requires a high efficient amplification in PA. The main concern

in high power amplification is achieving high efficiency without degrading the quality of the output signal.

## 1.2 Power Amplifiers (PAs)

Generally, power amplifiers are classified with ‘Capital Letters’ starting with A. Mode of operation determines the class of amplifiers and the most general classification of power amplifiers are according to their **linearity** and **efficiency**. These two important criteria directly affect which class of amplifiers to be chosen for a design.

Linearity of the power amplifier directly affects the quality of the output signal. According to the modulation used in wireless communication, demand on linearity changes. Some modulation techniques do not require amplitude transmission where non-linearity is not the main issue. For instance, Gaussian Minimum Shift Keying (GMSK) is an example of constant envelope modulation [1]. The data is transmitted by the phase of the signal with a constant envelope. The same condition is valid for FM (Frequency Modulation) where signal is transmitted by its frequency. However, for high data rate in data and video transmission, more adaptive modulation techniques are needed which are OFDM, QAM, QPSK. Contrary to GMSK or FM, these techniques are named as non-constant envelope modulation and obviously require a linear amplification [2].

### 1.2.1 Linear Amplifiers

Class A, AB and B amplifiers are considered as linear amplifiers. Class A power amplifiers directly transmit the input signal to the output without distorting

it. The transistor is biased in its active (or saturation in MOS) region that the transistor never enters to its cut-off or saturation (or linear in MOS) region. For no input signal, transistor has a DC current flowing. As a result, transistor is always ‘ON’ and its conduction angle is  $360^\circ$ . This results in a very linear but not very efficient amplification. The maximum drain efficiency that can be obtained from a class-A amplifier is 50%.

Class B power amplifiers use two complementary transistors and every transistor conducts only one cycle of RF input signal. For positive cycle of RF sine-wave, upper transistor (NPN or NMOS) conducts (PNP or PMOS is in cut-off), for negative cycle of RF sine-wave, lower transistor (PNP or PMOS) conducts (NPN or NMOS is in cut-off). That means there exists a time which current and voltage does not exist at the same time which increases the efficiency. So, each transistor’s conduction angle is  $180^\circ$ . The maximum drain efficiency that can be obtained from a class-B amplifier is 78.5%.

For the input signal applied to transistors, there occurs a time the gate-source (base-emitter) voltage is below the threshold. That causes both transistors to be ‘OFF’ at the same time and this situation results in a crossover distortion. To solve this, class-AB mode biasing can be offered which is an intermediate amplification mode between A and B classes. With class-AB biasing, a permanent biasing voltage (diodes or more clever transistor biasing circuits can be implemented to apply proper threshold voltage) forces ‘ON’ transistor to continue to be ‘ON’, until the ‘OFF’ transistor changes its situation to ‘ON’. So, there is no time both transistors are ‘OFF’ at the same time and distortion is avoided.

As it can be seen above, going from Class A to B, linearity decreases while the efficiency increases.

## 1.2.2 Switch Mode Amplifiers

Switch mode power amplifiers use transistors as switches. Ideally, there is no power consumption at the transistor and the theoretical efficiency of the amplifier reaches to the level of 100% . Since using transistor as a switch means driving it into deep saturation, the analog interaction between the input and output signal will be lost [3] that results in a nonlinearity [4]. Widely used switch mode amplifiers are Class-D, E and F.

A typical Class-D amplifier uses the push-pull configuration. Two transistors will work consecutively where if one is ‘ON’ other is ‘OFF’ and vice versa. So, no power is consumed by the transistors. There are two possible configurations: *Voltage mode* and *Current mode*.

In voltage mode class-D amplification (VMCD), the voltage is switched and the current through the transistor is forced to be sinusoidal by the resonator at the output. But, the output capacitance and finite resistance of the transistor results in a RC time constant which slows down the ‘ON’ and ‘OFF’ transition times. With overlapping current and voltage waveforms, the *switching loss* comes into the picture whose effect becomes significant at high frequencies.

In the current mode class-D amplification (CMCD) roles of voltage and current are reversed. The advantage of current mode is using output capacitance as a resonant circuit but this diminishes switching loss only up to a point. In CMCD, current is switched and voltage is forced to be sinusoidal by the resonant circuit. The rise and fall losses resulting from the output capacitance and finite resistance of the transistor are now eliminated but the same *switching loss* rule becomes valid for current switching. [4]

In a Class-F power amplifier, not to overlap voltage and current at the same

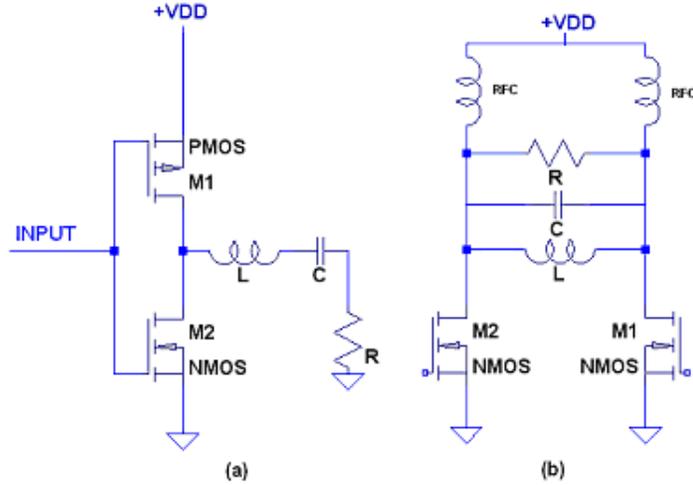


Figure 1.1: a) Voltage mode Class-D (VMCD) b) Current mode Class-D (CMCD)

time, voltage and current characteristics are designed with a proper output resonant circuit. Current through the transistor is a half-sine wave and voltage over the transistor is square wave resulting in a theoretical 100% efficiency.

Half-sine wave is the sum of fundamental frequency and infinite number of even harmonics. So, to obtain a half-sine wave current flowing through the transistor, only even harmonic frequencies of current should be allowed (No odd harmonics should flow through the transistor.) On the other hand, square wave is the sum of fundamental frequency and infinite number of odd harmonics. So, to obtain a square-wave voltage over the transistor, even harmonic frequencies of voltage should be short-circuited. Consequently, input of the resonant circuit should be high impedance resulting no current flow through load at odd harmonics and input of the resonant circuit should be short circuited resulting no voltage existing on the load at even harmonics.[5]

Since it is not easy to tune the resonant circuit for each harmonics, a theoretical analysis may give how the maximum efficiency changes according to the

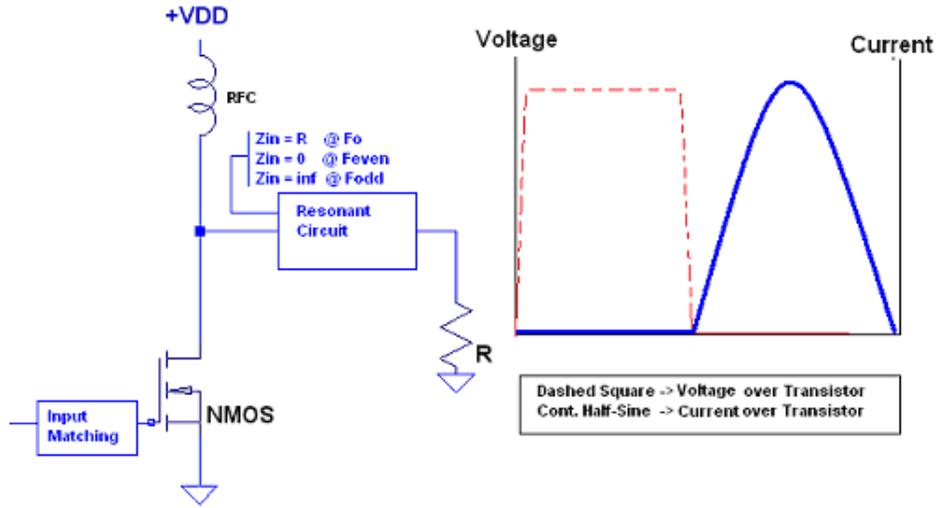


Figure 1.2: Class-F PA and its Current-Voltage Characteristics

tuning of a number of harmonics. It is found that tuning of second and third harmonics gives a theoretical maximum efficiency of 81.65% and tuning up to fifth harmonics gives a theoretical maximum efficiency of 90.45% [6]. As a result, for Class-F amplification it is not easy to obtain a very high efficiency without tuning the resonant circuit up to the fifth harmonic .

Class-E amplifier is introduced by Sokal [7] at 1975. To obtain a theoretical efficiency of 100%, the voltage and current behaviors are tuned with a proper output resonant circuit design. Besides, the output capacitance of the transistor directly enters into design parameters. By using the appropriate harmonic control, a harmonic suppression can be achieved.

Class-E and Class-F amplifiers have many similarities. The main difference is their output resonance circuit design. According to the design of the output resonance circuit, current and voltage waveforms show differences which directly affect the amplification principle of these classes. Two 1 GHz designs implemented

by the same designers with the same transistors show very close performances [8], [9]. But, the complicated resonant circuit design of Class-F carries Class-E PA one step forward.

Since there is a limit of efficiency in linear mode power amplifiers, it is more convenient to design a high efficiency switched mode power amplifier and if necessary increase the linearity of PA using an appropriate linearization method. Class-E power amplifier is a convenient amplification mode to obtain high efficiencies at microwave frequencies.

### 1.3 Contributions of the Thesis

In this thesis, the aim is to obtain 38 dBm output power with approximately 60% efficiency. While achieving this, some critical issues will be considered.

Switching mode power amplifiers usually aim to have a very high efficiency. But, this high efficiency behavior is obtained at the saturation region of the amplifier. Designers declare this maximum efficiency as a performance figure, despite being at the saturation region. However, the linearity is an important concern in an amplifier circuit. Although there is a trade-off between linearity and efficiency, both should be examined carefully during a PA design.

To avoid the power amplifier to operate in saturation,  $P_{1dB}$  point will be chosen as the maximum output power and we define the efficiency at this point. The design aim of this Class-E amplifier will be to increase the output power and the efficiency at  $P_{1dB}$  point. So, without using any other linearization technique, a more linear Class-E amplifier will be achieved with only a little decrease in efficiency. We will also try to maximize the efficiency at the output power level

which is 10 dB lower than the  $P_{1dB}$  point.

Secondly, the harmonic suppression will be considered. By using a proper output matching network, the harmonic suppression of approximately -40 dBc will be obtained. So, the quality of the output signal will be improved.

## 1.4 Outline

In the following chapter, a detailed explanation about Class-E power amplifiers will be presented. The behavior of Class-E amplifier will be given and detailed formulas will be obtained to force a PA to work as a Class-E amplifier. At last, a generic SPICE simulation will be made to show how a class-E amplifier works.

In the third chapter, different design techniques will be considered. Each technique will be handled in detail and a theoretical comparison will be given. In this chapter, we will also give the simulation and measurement results. The design methods mentioned here will be simulated and a comparison will be made. Finally, the measurement results for the implemented Class-E PA will be given.

The last chapter is the conclusion of the thesis.

# Chapter 2

## CLASS-E POWER AMPLIFIERS

### 2.1 Operation Principle of Class-E Power Amplifiers

Class-E power amplifier operates on the principle that no power should be consumed over the transistor. There is no time interval that a finite current and a finite voltage exists at the transistor at the same time. This results in a zero power consumption over the transistor. Since other components are reactive elements (inductance or capacitance), all the power supplied from the source will be delivered to the output load resistance resulting in a high efficiency.

A generic Class-E power amplifier is shown in Figure 2.1. In (a), the basic circuit is given. The circuit consists of a switching transistor (M1), a series-tuned output circuit ( $L_0$ - $C_0$ ), shunt capacitors ( $C_t$ + $C_2$ ), an RF choke inductance (RFC) and a load resistance ( $R_{opt}$ ). In (b), the equivalent of series-tuned output circuit

is given. It consists of a resonant circuit (LC) and an additional reactance ( $jX$ ). All these elements will be optimized to force the PA to work in class-E mode.

- The **transistor** will be used as a switching element. When it is ‘ON and when a current flows through it, the voltage over the transistor will be *zero*. When the transistor is ‘OFF’, a voltage appears on it, but no current flows through it.

- The **load resistor** at the output of the circuit is calculated to achieve the high efficiency for a desired supply voltage and output power.

- The **series-tuned output circuit** consists of an LC resonant circuit and an additional reactance. The series LC resonant circuit is tuned at the fundamental frequency of the circuit. So, only fundamental components will pass through the load. There is an additional  $jX$  reactance used for a phase shift between the current through the tuned circuit and the voltage at the input of the tuned circuit. This phase shift is necessary to obtain the maximum efficiency.

- The **RF choke inductor** should be high enough to result in only DC current flowing through the supply. But, some researchers mathematically proved that a finite DC-feed inductance could also be used to obtain Class-E topology and achieve high efficiency [10]. It is shown that, by using a finite DC-feed inductance, the output capacitance of the switching transistor can also be compensated [11].

- The **total parallel capacitor** at the output of the transistor consists of the output capacitance of the transistor and an additional parallel capacitor. This capacitor is needed to obtain proper voltage-current characteristic over the transistor. At low frequencies, to obtain the high efficiency circuit, an additional parallel capacitor should be added. However, as the frequency increases, the needed total parallel capacitor value decreases and the output capacitance of the transistor becomes high with respect to the needed value. So, one of the

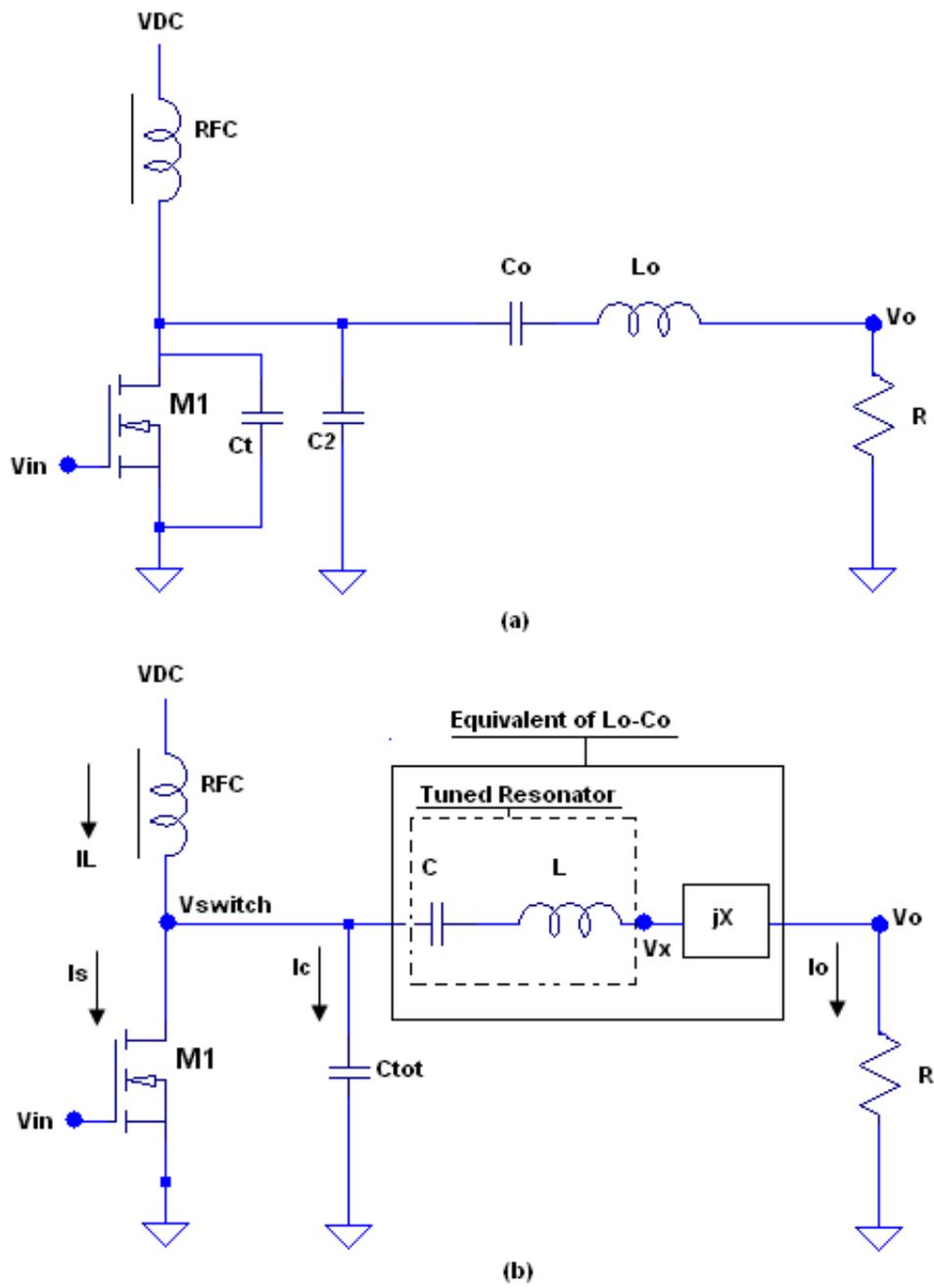


Figure 2.1: Class-E Power Amplifier (a)Basic Circuit (b)Equivalent Circuit

drawbacks at high frequencies is this parallel output capacitance.

There are three conditions that should be satisfied to obtain the high efficiency.

[7]

1. When the transistor is 'ON', a current flows through it. When it is turned 'OFF', the current continues to flow through the capacitor. If the voltage over the capacitor immediately starts to rise, there will be a possibility of the current and voltage overlap. So, the rise of the voltage over the capacitor should be delayed and should not rise immediately after the turn-off.
2. When the transistor is 'OFF', no current flows through it and there exists a voltage over the capacitor (so, over the transistor). Whenever it is 'ON', current starts to flow through it. If there exists a voltage over the capacitor at the time transistor is 'ON', then this voltage will be discharged over the transistor with a dissipation of  $\frac{1}{2}CV^2$ . Avoiding this, the voltage over the capacitor should be guaranteed to be zero just before the transistor turns on.
3. To guarantee the second condition, the slope of the voltage over the capacitor should be zero at the time the transistor turns on.

Fig. 2.2 shows all the current and voltage waveforms of the transistor that satisfies the conditions mentioned above. This figure shows that the voltage over the transistor reaches zero just before the turn-on. Since the current flowing through the capacitor is zero at the turn-on time, the slope of the voltage over the capacitor has to be zero, too ( $I_{cap} = C \frac{dV_{cap}}{dt}$ ).

Assuming that  $I_o = I_{RF} \sin(\omega t)$  is the load resistor current, and  $I_L$  is the DC

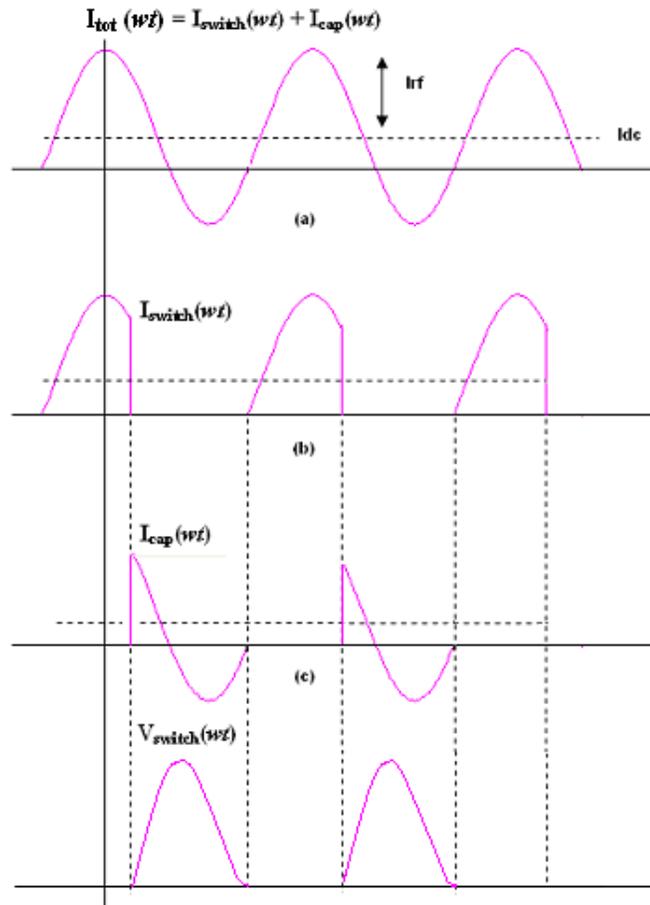


Figure 2.2: Transistor's Voltage-Current Waveforms (a) The sum of currents through the transistor and the parallel capacitor (b) Current through the transistor (c) Current through the parallel capacitor (d) Voltage over the transistor

supply current, we have [5]

$$I_{tot} = I_s + I_c = I_L - I_{RF} \sin(\omega t) \quad (2.1)$$

The current is partitioned in time between the transistor and the parallel capacitor. Either the transistor or the capacitor carries the current, but not both. Figure 2.2 shows the current flowing through the transistor and the capacitor.

The class-E topology has the operation principle as explained below:

When the transistor is ‘ON’, the total current  $I_{tot}$  flows through the transistor. At that time, the voltage over the transistor (also over the parallel capacitor) is zero, so no current flows through the capacitor. When the transistor is ‘OFF’, no current flows through the transistor and the total current  $I_{tot}$  flows through the capacitor. This voltage-current characteristics result in no power dissipation over the transistor.

The resonant circuit of the series-tuned output circuit provides fundamental current flowing through the load. Since the reactance of the resonant circuit is very high at the harmonic frequencies, no harmonic power dissipation occurs. All these properties provide Class-E topology to achieve 100% theoretical efficiency.

## 2.2 Mathematical Analysis

### 2.2.1 Design Formulas

The following assumptions are made to determine the values of the elements [12]:

- The RF choke provides **only DC current** and no power dissipation occurs on it. (No series resistance)
- The series-tuned output circuit has a sufficiently **high Q** to obtain a pure sinusoidal signal at the load resistance.
- The transistor acts as an ideal switch. It has a **zero on-resistance, infinite off-resistance** and its **saturation voltage is zero**.

Referring to voltage and current notations of Figure 2.1:

$$v_o(t) = V \sin(\omega t + \phi) \quad (2.2)$$

$$i_o(t) = \frac{V}{R} \sin(\omega t + \phi) \quad (2.3)$$

where  $V$  is the magnitude of the voltage and  $\phi$  is the phase of the output signal.

The voltage at the node  $x$  is given by

$$\begin{aligned} v_x(t) &= v_o(t) + v_{LA}(t) \\ &= V \sin(\omega t + \phi) + X(V/R) \cos(\omega t + \phi) \end{aligned} \quad (2.4)$$

Defining

$$v_x(t) = V_x \sin(\omega t + \phi_1) \quad (2.5)$$

and using trigonometric identities, we can write

$$\begin{aligned} V_x &= V \sqrt{1 + \frac{X^2}{R^2}} \\ \phi_1 &= \phi + \psi = \phi + \tan^{-1}\left(\frac{X}{R}\right) \end{aligned} \quad (2.6)$$

After obtaining voltages over the load and additional reactance, the voltage over the capacitor (transistor) can be solved. For this purpose, we define new quantities as

- $y$  : Half of the time of which transistor is off.
- $\frac{\pi}{2}$  : Mid point of the off time.
- $\theta_{close}$  : The time when the transistor turns on ( $\frac{\pi}{2}+y$ )
- $\theta_{open}$  : The time when the transistor turns off ( $\frac{\pi}{2}-y$ )

and these values are shown in Figure 2.3.

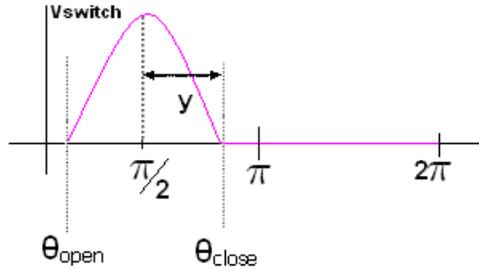


Figure 2.3:  $y$  and turn on/off times

Using the capacitance formula:

$$\begin{aligned}
 i_{cap}(t) &= C dv_{cap}(t)/dt \\
 &\Downarrow \\
 v_{cap}(t) &= \frac{1}{C} \int i_{cap}(t) dt
 \end{aligned}
 \tag{2.7}$$

With  $\omega t = \theta$ ,  $t = \frac{\theta}{\omega}$ , we can write

$$v_{cap}(\theta) = \frac{1}{\omega C_{tot}} \int i_{cap}(\theta) d\theta
 \tag{2.8}$$

where  $v_{cap}(\theta) = v_{switch}(\theta)$ . To obtain the voltage over the switch at  $\theta$ , the boundaries of the integral should be  $\theta_{open}$  and  $\theta$ . It will be integrated later between  $\theta_{open}$  and  $\theta_{close}$  to satisfy the conditions given in the previous section. Then, using Eq. (2.1), it is known that the total current flows through the capacitor when the transistor is off. Also, at the fundamental frequency, the total impedance of the series-tuned output circuit will be zero. That means the RF current in the Eq. (2.1) will be the current derived in Eq. (2.3). Hence,

$$\begin{aligned} v_{cap}(\theta) &= \frac{1}{wC_{tot}} \int_{\frac{\pi}{2}-y}^{\theta} i_{cap}(\theta) d\theta \\ v_{cap}(\theta) &= \frac{1}{wC_{tot}} \int_{\frac{\pi}{2}-y}^{\theta} (I_L - i_o(\theta)) d\theta \\ v_{cap}(\theta) &= \frac{1}{wC_{tot}} \int_{\frac{\pi}{2}-y}^{\theta} (I_L - \frac{V}{R} \sin(\theta + \phi)) d\theta \end{aligned} \quad (2.9)$$

the capacitor voltage is obtained. (Detailed formula is given in Eq. (A.1))

At the fundamental frequency, the impedance of the series-tuned circuit will be zero. That results in an equivalence of capacitor(transistor) voltage and  $v_x$  at the fundamental frequency. By using the Fourier integral, the magnitude of the capacitor voltage can be determined and two equations are obtained as:

$$\begin{aligned} V_x &= \frac{1}{\pi} \int_0^{2\pi} v_x(\theta) \sin(\theta + \phi_1) d\theta \\ 0 &= \frac{1}{\pi} \int_0^{2\pi} v_x(\theta) \cos(\theta + \phi_1) d\theta \end{aligned} \quad (2.10)$$

Since  $v_{cap} = v_x$ , by using Eq. (2.9), Eq. (2.10) will result in two solutions for  $V_x$ . Again by using Eq. (2.6), the solutions for the magnitude of the output voltage are found as

$$\begin{aligned} V &= I_L R h(\phi, \psi, y, C_{tot}, R, X) \\ V &= I_L R g(\phi, \psi, y) \end{aligned} \quad (2.11)$$

where  $h()$  and  $g()$  are analytical functions calculated in [12] and given in Eq. (A.2) and Eq. (A.3). In these equalities, the element values,  $y$  and  $\phi$  values are the unknown parameters.

The drain efficiency is the ratio of the power delivered to output and the power supplied from the DC supply. So

$$\begin{aligned} P_o &= \frac{1}{2} \frac{V^2}{R} \\ P_{DC} &= V_{DC} I_L \\ \eta &= \frac{P_o}{P_{DC}} \end{aligned} \quad (2.12)$$

- **Output Power** : For output power calculation, the magnitude of the output power should be determined by using the result of Eq. (2.11):

$$\begin{aligned} P_o &= \frac{1}{2} \frac{I_L g() R^2}{R} \\ &= \frac{1}{2} (I_L g())^2 R \end{aligned} \quad (2.13)$$

- **DC Power** : For DC power calculation, the DC voltage should be determined. One can say that this voltage is an input for element calculations, but DC voltage value can be determined as a function of the parameters used in the circuit. Since DC voltage directly affects the voltage over the transistor, by taking the average of the voltage over the transistor (no dissipation over RF choke is assumed in the beginning of the this section), DC voltage can be found. Average value of a function defined in an interval of [m,n] is:

$$Avg = \frac{1}{m - n} \int_n^m f(x) dx \quad (2.14)$$

So, DC voltage can be calculated as:

$$\begin{aligned} V_{DC} &= \frac{1}{2\pi} \int_0^{2\pi} v_{cap}(\theta) d\theta \\ &= \frac{1}{2\pi} \int_{\frac{\pi}{2}-y}^{\frac{\pi}{2}+y} v_{cap}(\theta) d\theta \\ &= I_L R_{DC} \end{aligned} \quad (2.15)$$

where  $R_{DC}$  is defined in [12] and given in Eq. (A.4). Boundaries are diminished to the period where voltage exists over the transistor. Finally the DC power is:

$$P_{DC} = V_{DC} I_L = I_L^2 R_{DC} \quad (2.16)$$

- **Drain efficiency** : The efficiency is calculated from

$$\eta = \frac{P_o}{P_{DC}} = \frac{\frac{1}{2}(I_L g())^2 R}{I_L^2 R_{DC}} = \frac{g()^2}{2} \frac{R}{R_{DC}} \quad (2.17)$$

To achieve 100% efficiency;

$$\eta = 1 = \frac{g()^2}{2} \frac{R}{R_{DC}} \quad (2.18)$$

should be obtained. But, up to now, no optimization is made. All the parameters remain as unknowns. From now on, the conditions of the previous section will be used to obtain the optimal parameter values to achieve the 100% efficiency.

Equalizing Eq. (2.18) to 1, the following is obtained.

$$R_{DC} = \frac{g()^2 R}{2} \quad (2.19)$$

There are too many unknowns to solve this equation. To find the solutions, two conditions will be added. The first one is about the slope of the voltage over the transistor at the time of turn on. The second is about the turn-off duty cycle(y). [12] made an analysis to obtain optimal values for these two parameters.

- **Determining the Slope**: In the third condition in the previous section, it is declared that the slope of the voltage over the transistor at the time of turn on should be zero to guarantee the voltage to be zero. [12] presents an analysis that if both voltage-current characteristics of the transistor and the output power-maximum power capability is plotted with respect to the slope, the optimal operation is obtained when this slope is **ZERO**. During this analysis, he uses the y value as 50% which corresponds to  $\frac{\pi}{2}$ .

- **Determining the OFF duty-cycle (y)**: [12] gives an analysis that if both voltage-current characteristics of the transistor and the output power-maximum

power capability is plotted with respect to the OFF duty-cycle ( $y$ ), optimal operation is obtained when  $y$  value is  $\frac{\pi}{2}$  or **50%**. During this analysis, he uses the slope value as 0.

Using the first condition, the voltage over the capacitor should be zero whenever the transistor becomes on. So, using the derived formula of  $v_{cap}$  in Eq. (A.1), it is known that this voltage should be zero at the close time  $\theta_{close} = \frac{\pi}{2} + y$ . This results in

$$\cos(\phi) = \frac{y}{g() \sin(y)} \quad (2.20)$$

Using the third condition and the analysis above, the slope of the voltage over the transistor at the time of turn on should be zero. Taking the derivative of Eq. (A.1) at the time  $\theta_{close} = \frac{\pi}{2} + y$ ,

$$slope = \left( \frac{dv_{cap}(\theta)}{d\theta} \right)_{\theta=\frac{\pi}{2}+y} = 0 \quad (2.21)$$

Now, it is time to find appropriate angles:

- Rearranging Eq. (2.21) and Eq. (A.4), the Eq. (A.7) is obtained where  $slope = 0$  and  $y = \frac{\pi}{2}$ . This results in  $\tan(\phi) = -\frac{2}{\pi} \Rightarrow \phi = -32.5^\circ$ .
- Using Eq. (2.20),  $g()$  is calculated as  $g() = \sin(y) \cos(\phi) / y = 1.86$
- Using Eq. (A.2) and defining coefficients in Eq. (A.5), Eq. (A.6) is obtained, so  $\psi$  is calculated as  $\tan(\psi) = 1.152 \Rightarrow \psi = 49.05^\circ$ .

Table 2.1 summarizes the optimal values:

Using the formulas given in Table 2.1, the optimal element values will be obtained. The element values first will be calculated with respect to optimal resistance  $R$ . Then an optimal calculation for load resistance will be given.

slope	y	$\phi$	$g()$	$\psi$
0	$\frac{\pi}{2}$	$-32.5^\circ$	1.86	$49.05^\circ$

Table 2.1: Optimal values for Class-E PA

- **Design element values:**

- Using Eq. (2.19),  $R_{DC}$  is calculated as  $R_{DC} = 1.73R$
- Using Eq. (2.6),  $X$  is calculated as  $X = \tan(\psi)R = 1.15R$
- Using Eq. (A.4) and Eq. (2.19),  $C_{tot}$  is calculated as  $C_{tot} = 1/(5.45R\omega)$ .
- Finally, using Eq. (2.13) and Eq. (2.15),  $R$  will be calculated from  $R = 2P_o R_{DC}^2 / (V_{DD}^2 g())^2 = 0.577V_{DD}^2 / P_o$  with the intended output power and supply voltage.

- **Maximum Ratings and Output Voltage:** To obtain the maximum voltage over the transistor and the maximum current flowing through the capacitor, the time when the slope of the voltage over the transistor is zero should be found.

- Using Eq. (2.11), magnitude of the output voltage is calculated as  $V = I_L R g() = \frac{V_{DD}}{R_{DC}} R g() = 1.07V_{DD}$
- Using Eq. (A.1):

$$\begin{aligned}
 \left(\frac{dv_{cap}(\theta)}{d\theta}\right)_{\theta=\theta_{max}} &= 0 \\
 &\Downarrow \\
 \theta_{max} &= \arcsin(1/g()) - \phi
 \end{aligned} \tag{2.22}$$

is obtained. Solving Eq. (A.1) at the time of  $\theta_{max}$ , maximum voltage over the transistor is obtained as  $V_{trmax} = 3.56V_{DD}$

- Using Eq. (2.1) and Eq. (2.3), it's obvious that maximum current occurs when sine value is -1. So, maximum current flowing through the transistor is obtained as  $I_{trmax} = I_L + \frac{V}{R} = I_L + \frac{I_L R g()}{R} = I_L(1 + g()) = 2.84I_L$

In the beginning of this section, we gave three assumptions for making calculations easier. But, in real life these assumptions can not be valid. So, the real life calculations should be given for the remaining elements. Also, empirical formulas derived by [7] and [13] will be given for  $X$  and  $C_{tot}$ .

**- Finite Q value:**

A series RLC circuit's Q-value can be determined from

$$Q = \frac{1}{R} \sqrt{\frac{L}{C}} \quad (2.23)$$

So, a high Q value can only be obtained with very high  $L$  value or very low  $C$  value. Practically, a  $Q$  value of 3-10 is meaningful for Class-E circuits. (A detailed  $Q$  value analysis will be made in the next section.) We have so far calculated formulas for high quality factor. Now, we repeat for finite  $Q$  values. - First, the easiest calculation is the  $L_0$  formula.

$$L_0 = \frac{QR}{\omega} \quad (2.24)$$

- In [13], empirically derived formulas are obtained for  $X$  (additional reactance) and  $C_{tot}$  (parallel capacitance) for a finite  $Q$ -value.

$$\begin{aligned} X &= \frac{1.42Q}{Q-0.67} R \\ C_{tot} &= \frac{0.1836}{R\omega} \left(1 + \frac{0.81Q}{Q^2+4}\right) \end{aligned} \quad (2.25)$$

- The next value is  $C_0$ . Instead of using discrete C, L and X values in Fig. 2.1-b, it is more convenient to use the circuit in Figure 2.1-a. So,  $X$  reactance can

be absorbed into  $C_0$  value as [14] ( $L_0$  remains same):

$$\begin{aligned} Z_{C_0} + Z_{L_0} &= Z_C + Z_L + Z_X \\ Z_{C_0} &= Z_C + Z_X \end{aligned} \quad (2.26)$$

Since  $L_0$  and  $C$  are resonant at  $\omega$ ;

$$C = \frac{1}{\omega^2 L_0} \quad (2.27)$$

So,

$$C_0 = \frac{1}{\omega(\omega L_0 - X)} \quad (2.28)$$

In fact using formulas Eq. (2.24) and Eq. (2.25),  $C_0$  can be found as a function of  $Q$  and  $C_{tot}$ . [7] again produced an empirical formula very close this calculation as:

$$C_0 = C_{tot} \frac{5.4466}{Q} \left(1 + \frac{1.42}{Q - 2.08}\right) \quad (2.29)$$

#### - Finite RF Choke:

As the frequency increases, the needed total parallel capacitance  $C_{tot}$  will be smaller and transistor output capacitance will be dominant. This will result in deviation from the optimal values. Instead of using a high RF Choke inductor, using a finite choke inductor will provide a compensation for output capacitor [11]. The same authors gave a way to calculate this inductance value. Using these calculations, a MATLAB code is written. In this code, starting from an initial value of DC Feed inductor and using the design inputs, a set of recursive calculations are made which finish when a very small calculation error is achieved (See App B).

#### - Finite Transistor Resistance:

Since a transistors' 'ON' resistance can not be 'zero', an analysis should be made

to determine the effect. [15] gave an analysis about the finite ON resistance of the transistor. Defining two values  $\mathbf{y}$  and  $\mathbf{k}$  as:

$$\begin{aligned} y &= \omega C_{tot} R_{ON} \\ k &= P_{OUT} R_{ON} / V_{DD}^2 \end{aligned} \quad (2.30)$$

an equation with respect to these two constants is obtained in Eq. (A.8). Solving this fourth-degree equation numerically, no positive roots are found when the value of  $\mathbf{k}$  is above 0.1. So, this result concludes this analysis as:

$$R_{ON} < 0.1 V_{DD}^2 / P_{OUT} \quad (2.31)$$

In conclusion of these mathematical analysis, Table 2.2 summarizes design element formulas for a finite Q-value to obtain the optimal Class-E topology:

Input Parameters: $V_{DD}, P_{OUT}, Q, \omega$	
Element	Formula
$R$	$0.577 V_{DD}^2 / P_{out}$
$C_{tot}$	$\frac{0.1836}{R\omega} \left(1 + \frac{0.81Q}{Q^2+4}\right)$
$C_0$	$C_{tot} \frac{5.4466}{Q} \left(1 + \frac{1.42}{Q-2.08}\right)$
$L_0$	$QR/\omega$
$X$	$\frac{1.42Q}{Q-0.67} R$
$L_{feed}$	Use MATLAB code

Table 2.2: Class-E Design Formulas

### 2.2.2 Sensitivity of Design Parameters

To obtain the sensitivity of design parameters, the formulas in Sec. 2.2.1 will be used. Efficiency ( $\eta$ ) which is  $\frac{g(\omega)^2}{2} \frac{R}{R_{DC}}$  can be written as a function of any design parameter. For example, if the efficiency is intended to be written only as a

function of  $R$ ,  $g()$  and  $R_{DC}$  should be written as a function of  $R$ . These two parameters are derived in Sec. 2.2.1 as a function of  $g(y, \phi, \psi)$ ,  $R_{DC}(\omega, C_{tot}, y, g(), \phi)$  and  $C_{tot}(R, \omega)$ . Using the calculated values of  $y$ ,  $\phi$ ,  $\psi$  and under the assumption of high  $Q$  and normalization of  $\omega = 1$ , the efficiency can be written as a function of  $R$ . Plotting the graph of  $\eta$  with respect to  $R$  gives how efficiency changes with the changing value of  $R$ . The same derivation can be done for the remaining design parameters. [16] has done an analysis for these design parameters and showed how the efficiency changes with the change of the design parameters.

**- Sensitivity of Load Resistance ( $R$ ):**

Normalization of the load resistance value to 1 when the efficiency is 100%, an analysis can be done with changing this optimal value of  $R$  and determining how the efficiency changes. As a result, between the values of  $R = 0.67$  and  $R = 1.55$ , efficiency is more than 95%. Obviously 100% efficiency is obtained when  $R = 1$ .

**- Sensitivity of Parallel Capacitor ( $C_{tot}$ ):**

It's found in Sec. 2.2.1 that  $C_{tot} = 0.1836/(wR)$  when the efficiency is 100% . To normalize  $R$  and  $w$  to 1, an analysis can be done with changing this optimal value of  $C_{tot}$  and determining how the efficiency changes. As a result, between the values of  $C_{tot} = 0.06$  and  $C_{tot} = 0.3$ , efficiency is more than 95%.

**- Sensitivity of Additional Reactance ( $X$ ):**

It's found in Sec. 2.2.1 that  $\psi = 49.05^\circ$  (where  $\psi = \arctan(X/R)$ ) when the efficiency is 100% . To normalize  $R$  to 1, an analysis can be done with changing this optimal value of  $\psi$  and determining how the efficiency changes. As a result, between the values of  $\psi = 40^\circ$  and  $\psi = 70^\circ$ , efficiency is more than 95%.

**- Sensitivity of Operation Frequency ( $f$ ):**

Operation frequency directly affects design parameters to achieve the maximum efficiency. Besides, the effect of  $Q$ -value of the series-tuned output circuit to the efficiency must be considered with frequency effect. Normalizing  $f = 1$  when 100% efficiency is obtained, an analysis can be done with changing this optimal value of  $f$  and determining how the efficiency changes. As a result, for  $Q = 0$ , between the values of  $f = 0.5$  and  $f = 2$ , efficiency is more than 95%. For  $Q = 5$ , between the values of  $f = 0.96$  and  $f = 1.04$ , efficiency is more than 95% . For  $Q = 10$ , between the values of  $f = 0.98$  and  $f = 1.02$ , efficiency is more than 95% .

**- Sensitivity of OFF duty-cycle ( $y$ ):**

It is found in Sec. 2.2.1 that  $y = \pi/2$  (where  $y = 50\%$ ) when the efficiency is 100% . An analysis can be done with changing this optimal value of  $y$  and determining how the efficiency changes. As a result, between the values of  $y = 2\pi/5$  and  $y = 3\pi/5$ , efficiency is more than 95%.

**- Sensitivity of Q-value and RF Choke ( $RFC$ ):**

$Q$ -value of the series-tuned output circuit and the DC feed inductor are important design parameters. As it is mentioned in Sec. 2.2.1, a very high  $Q$ -value for the series-tuned output circuit is not easy, so design parameters are updated for a finite  $Q$ -value. [17] gave an analysis for finite a  $Q$ -value and DC feed inductor. In this analysis, it is seen that for a  $Q$ -value of 10 and for a ratio  $L_0/L_{feed}$  of 0.001, a DC supply current and a sinusoidal output voltage is obtained. For a  $Q$ -value of 3 and for a ratio  $L_0/L_{feed}$  of 0.5, a non-constant DC supply current and a non-sinusoidal output voltage is obtained. In Sec. 2.2.1, a DC feed inductor calculation in MATLAB is given for 100% efficiency.

## 2.3 Spice Simulations

In this section, using the formulas obtained in Sec. 2.2, a Spice simulation will be given. The Spice simulation will be done at 900 MHz. A calculator code is written for that purpose. This calculator finds the exact values and a range of values for design parameters to obtain optimum Class-E configurations. The inputs are  $V_{DD}$ ,  $P_{OUT}$ ,  $Q$  and  $f$ .

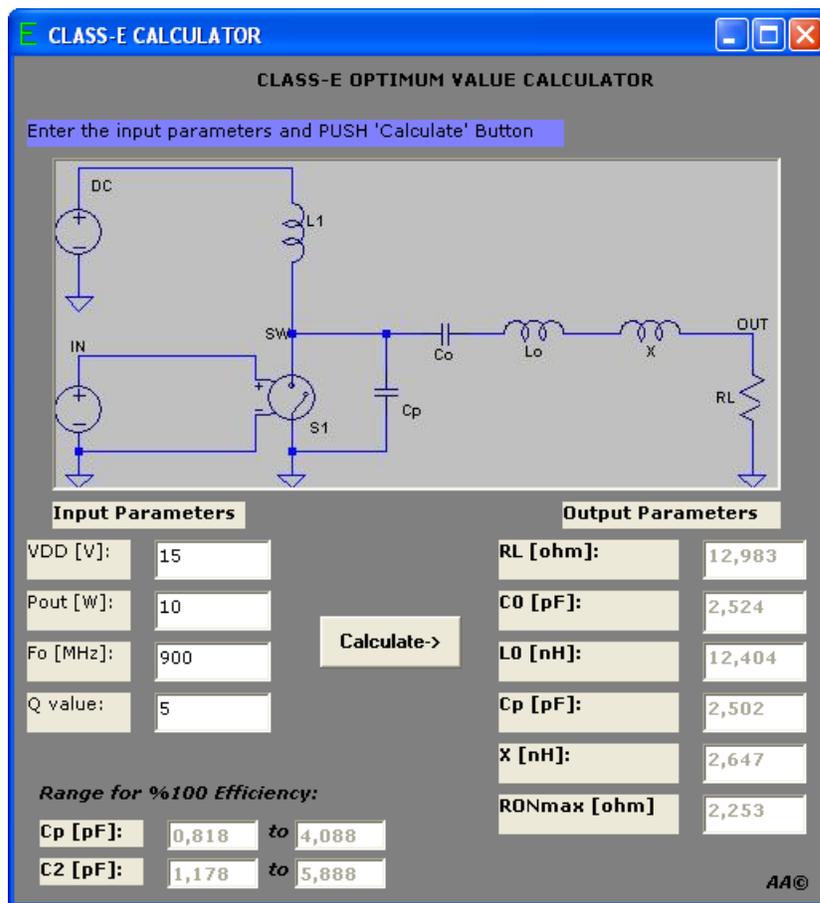


Figure 2.4: Class-E Optimum Value Calculator

For the chosen design inputs, the anticipated results are calculated below:

- $V_{trmax} = 3.56V_{DD} = 54V$

- $I_{trmax} = 2.84I_L = 1.8A$
- $V_{out} = 1.074V_{DD} = 16.1V$

Using this calculator, the optimum values are calculated as in Fig. 2.4 and a Spice analysis is made according to these values. The voltage-current characteristics of the transistor, the input-output phase difference, the output power and the efficiency is measured. An ideal switch with on resistance 4 mΩ is used as the transistor. Fig. 2.6 and Fig. 2.5 are the obtained characteristics. A proper

Parameter	Value
$V_{trmax}$	55.43V
$I_{trmax}$	1.75A
$\phi$	$2\pi f \Delta t = -32.6^\circ$
$I_L$	0.646A
$V_{out}$	16.56V
$P_{out}$	9.6W
$\eta$	99.02%

Table 2.3: Class-E Spice Calculated Values

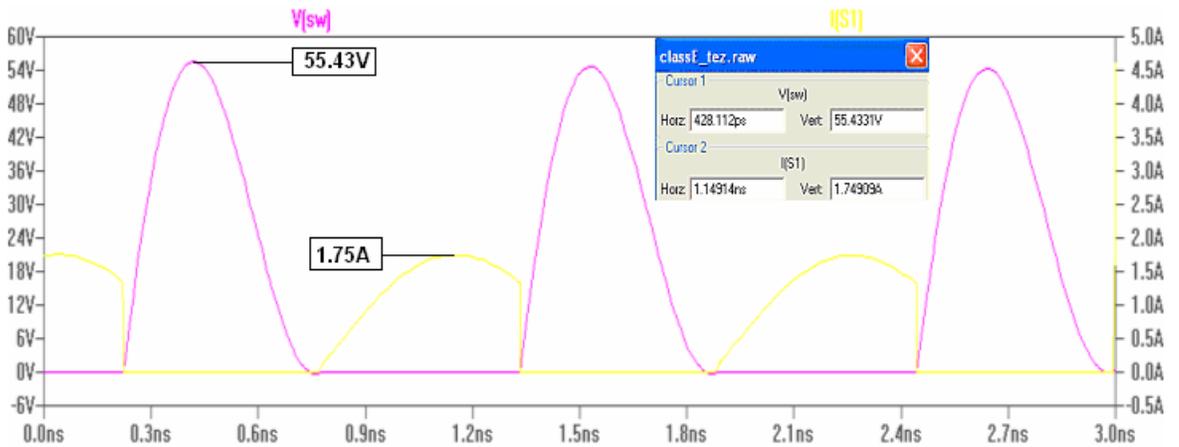


Figure 2.5: Current-Voltage characteristics over the Transistor

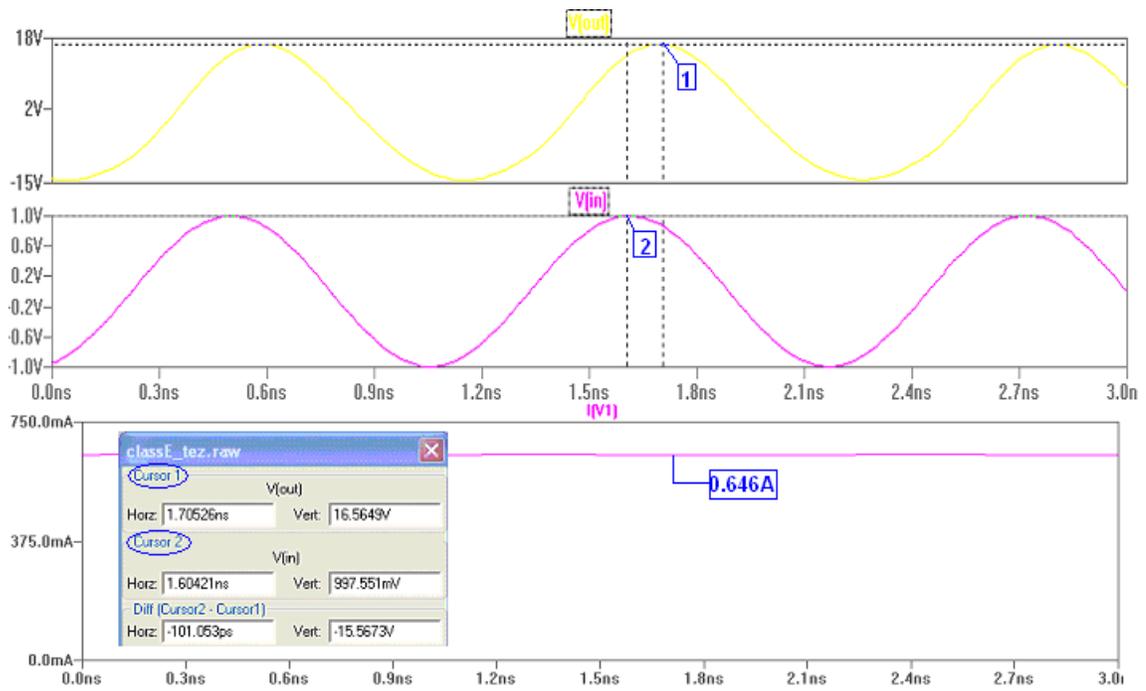


Figure 2.6: Output Voltage, DC current and Phase Difference ( $\phi = -32.5^\circ$ )

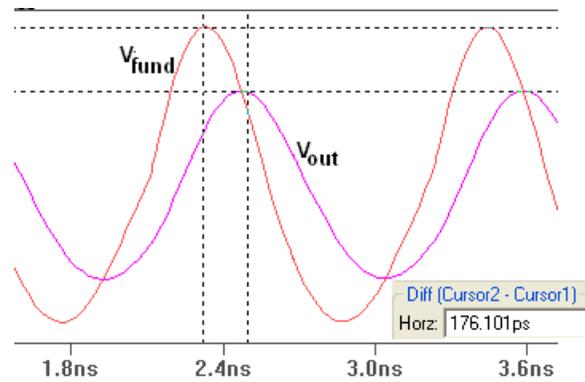


Figure 2.7: Fundamental Component of the Switch Voltage ( $V_{fund}$ ) versus Output Voltage (Phase Difference =  $-57.5^\circ$ )

measurement code is written in SPICE to calculate output power and efficiency. The measured values are given in Table 2.3.

The anticipated and simulated results are very close. The small difference is due to finite Q-value and ON resistance. The current supplied from the DC supply is very close to DC (4mA swing). Now, an analysis will be done to validate the explanation in Sec. 2.2.2.  $R$ ,  $C_{tot}$  and  $X$  values will be varied and the change in the voltage-current characteristics and the efficiency will be determined. Fig. 2.5 is the voltage-current characteristics over the transistor when normalized values are  $R = 1$ ,  $C_{tot} = 0.1836$  and  $\psi = 49.05^\circ$ .

According to Fig. 2.8, Fig. 2.9 and Fig. 2.10:

- For  $R$  values smaller than optimum (1), there occurs a voltage swing and negative current is needed. Since there is a negative voltage over the transistor (capacitor) just before turn-on, with the turn-on, voltage over the transistor(capacitor) goes from negative to zero which results in negative current. Peak voltage value also increases. For  $R$  values bigger than optimum (1), a ramp behavior for voltage is obtained. The efficiency decreases in both cases.
- For  $C_{tot}$  values smaller than optimum (0.1836), there occurs a voltage swing and negative current is needed (Same reason explained for  $R$  is valid here). Peak voltage value also increases. For  $C_{tot}$  values bigger than optimum (0.1836), a ramp behavior for voltage is obtained. The efficiency decreases in either direction.
- For  $X$  values smaller than optimum ( $49.05^\circ$ ), there occurs a voltage swing. The peak voltage value also increases. For  $X$  values bigger than optimum

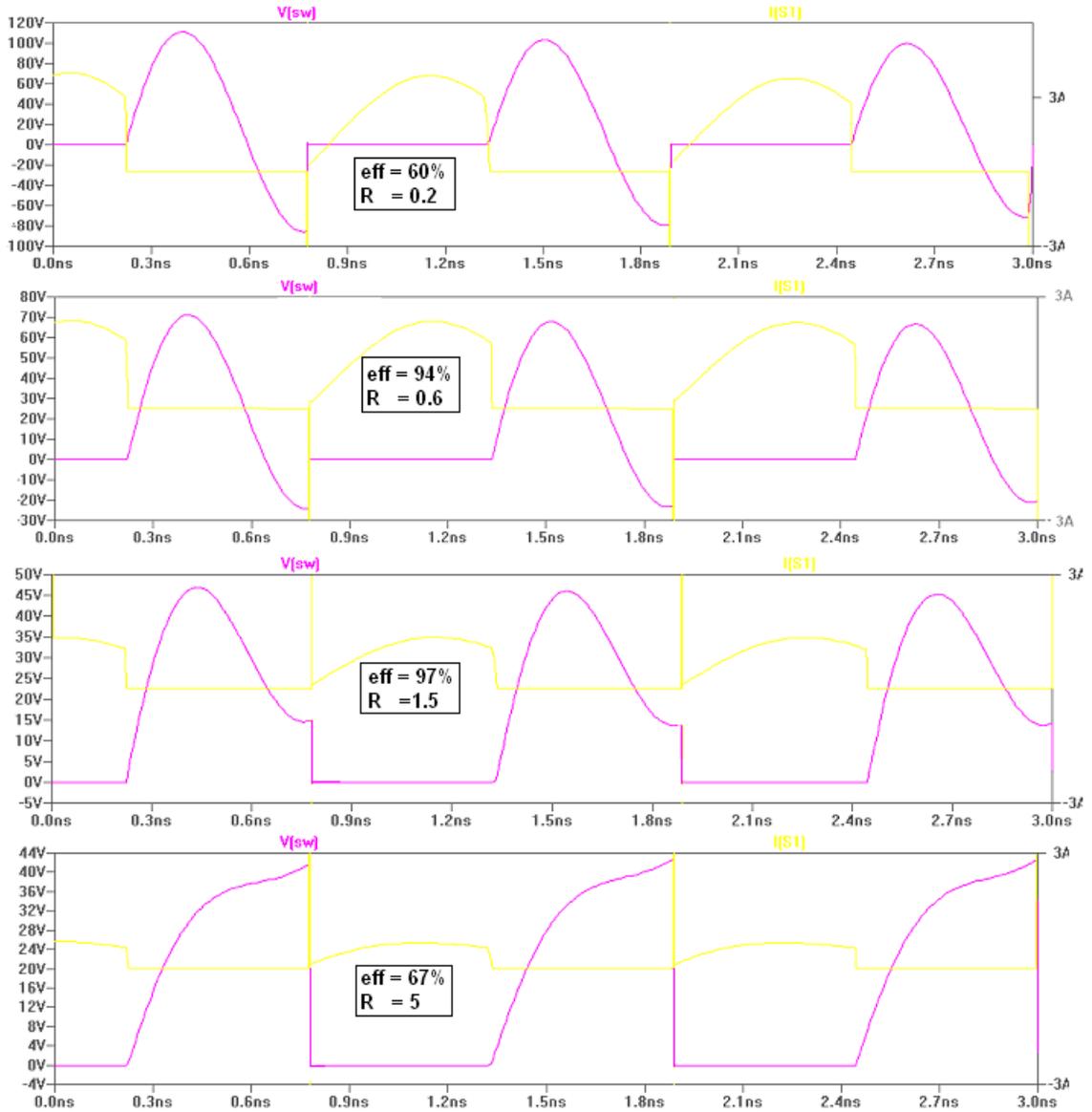


Figure 2.8: Efficiency and Voltage-Current Characteristics over Transistor to R-value variation

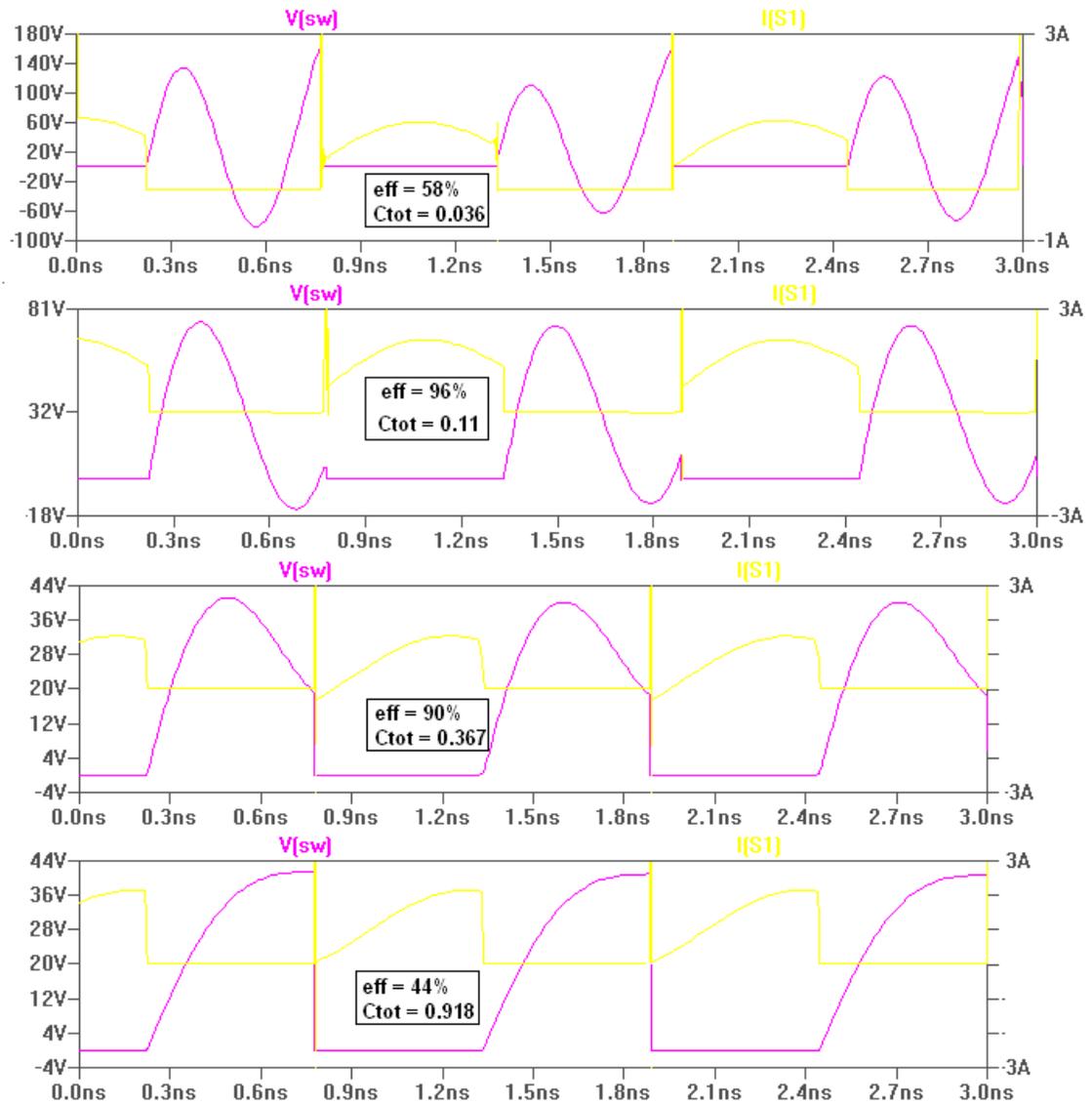


Figure 2.9: Efficiency and Voltage-Current Characteristics over Transistor to  $C_{tot}$ -value variation

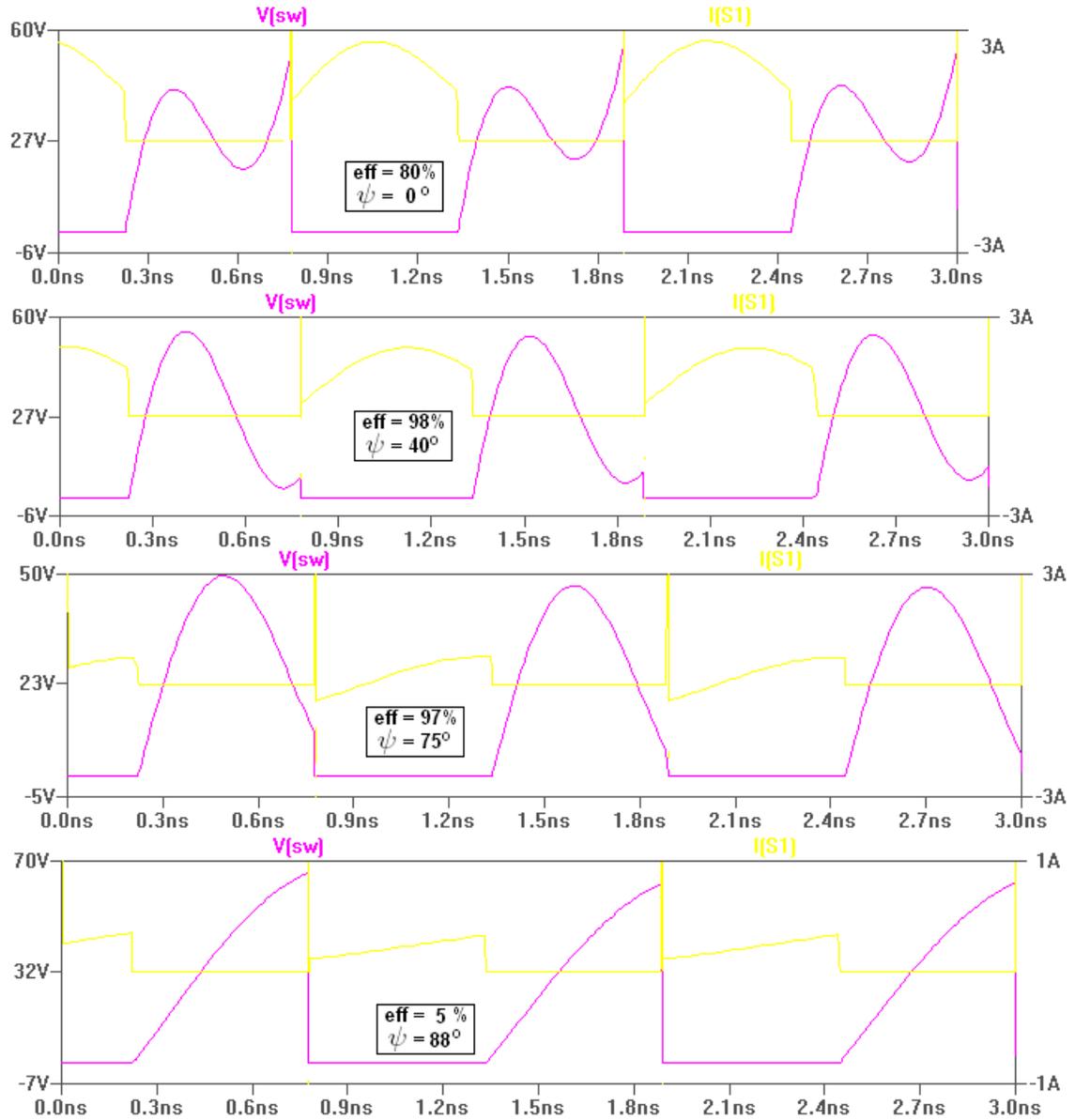


Figure 2.10: Efficiency and Voltage-Current Characteristics over Transistor to X-value variation

( $49.05^\circ$ ), a ramp behavior for voltage is obtained. The efficiency decreases in either case.

Consequently, analysis in Sec. 2.2.2 is validated via the Spice simulations. For efficiency, exact values for design parameters are not necessary. There exists a range of values for obtaining a relatively high efficiency.

# Chapter 3

## CLASS E POWER AMPLIFIER DESIGN

In this chapter, some design techniques will be examined and according to the design inputs, a transistor will be chosen. Then, using the large signal model of this transistor, a harmonic balance microwave simulation will be given. A comparison will be made and the best performing design will be implemented.

### 3.1 Class-E Design Techniques

#### 3.1.1 Design Techniques

The real transistor used in the design will directly affect the calculations and lumped elements will differ from their lossless behavior. But, Class-E topology offers designers to use some spurious elements of the transistor parameters as a design element.

- **50  $\Omega$  matching:** An optimum load resistance is used to obtain the desired

output power and high efficiency. But very likely, the value of this resistance is not a  $50 \Omega$ . Since the inputs or outputs of most RF stages require a  $50 \Omega$  resistance, the calculated optimal load resistance should be converted to  $50 \Omega$  using a proper matching network. Similarly, a proper matching network is needed to match the gate of the transistor to.

- **Biasing:** The sinusoidal input signal given to the power amplifier will drive the transistor. To use the transistor as a switch, the sinusoidal signal should symmetrically drive the transistor and quickly open and close it. Hence, the transistor is biased at the threshold of gate-to-source voltage.

After explaining these common topologies, different design techniques will be considered.

### **1. Using lumped elements with Capacitor Compensation:**

At very high frequencies, the actual output capacitor of the transistor may be greater than the needed parallel capacitor. So, an inductive compensation may be needed to decrease the level of the transistor output capacitor. But, it may not be very easy to directly add a shunt inductor to the drain of the transistor. Instead a series-capacitor and a shunt inductor can achieve the capacitor compensation [18], [19].

### **2. Transmission line with Harmonic Suppression:**

Output capacitor compensation can also be achieved with only a series capacitor. The main point of this technique is the harmonic controlled output circuit with the additional reactance  $X$ . It is known that the optimal resistance should be matched to 50-ohm. So there will be a conversion from  $R$  to 50-ohm by using LC networks (series L, parallel C: A basic L-match circuit). If this matching circuit can be used as a harmonic controlled circuitry, a series-tuned output circuit

will be achieved. Due to loss, no lumped elements will be used (except bypass capacitors and a high-value compensation capacitor) and all elements will be converted to transmission lines.

For an open stub transmission line, if the electrical length is chosen as  $90^\circ$ , the input of the transmission line will be a short-circuit. In the harmonic control circuitry, this property can be used to short circuit each harmonic component [20]. Parallel capacitor can be designed with a transmission line with an open-stub, low characteristic impedance  $Z_0$  and a length smaller than  $\lambda/8$ . Also, a series inductor can be designed with a transmission line with a high characteristic impedance  $Z_0$  and a length smaller than  $\lambda/8$  [21]. So, the shunt capacitor in the L-match circuit can be designed with a transmission line as an open-stub harmonic suppressor. Formulas for the series inductor and the shunt capacitor are given as:

$$\begin{aligned} L &= Z_0 E_L / (f 360^\circ) \\ C &= E_L / (Z_0 f 360^\circ) \end{aligned} \tag{3.1}$$

where  $E_L$ : electrical length (in degrees) and  $Z_0$ : characteristic impedance. For both elements electrical length should be chosen less than  $\lambda/8$  or  $45^\circ$ . The characteristic impedance of the transmission line should be chosen as high as possible for an inductor, and as low as possible for a capacitor.

Using an open stub transmission line with electrical length of  $90^\circ$  at the related harmonic frequency, this harmonic content is short circuited. For Class-E amplifier, if first four harmonic suppression is achieved with the open-stub topology,  $(2f_0, 3f_0, 4f_0, 5f_0)$ , sixth, ninth, tenth and higher harmonic suppression will also be achieved [22]. These higher harmonics will be suppressed more than 40 dB with respect to the fundamental frequency.

So, to obtain a four step harmonic suppressor, a two step L-match circuit

should be designed. Each capacitor in the matching circuit will be replaced with two open stubs. Consequently, the lumped elements will be replaced with transmission lines, a harmonic suppression is achieved and the optimal load resistance is matched to 50-ohm resistance.

An example conversion is given in Figure 3.1.

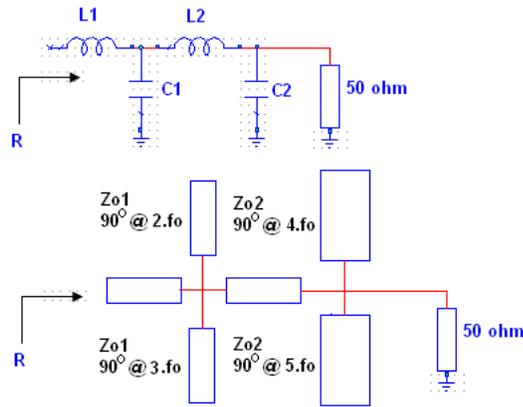


Figure 3.1: L-match to Transmission line conversion

### 3.1.2 Selection of the Transistor

The intended Class-E power amplifier will have an output of 10W (40 dBm). The operating frequency is chosen as 2 GHz which is compatible with 3G systems. The supply voltage is 15 volts. So, these design inputs will be used to find the element values and maximum ratings for the transistor.

To choose the proper transistor technology, two technologies are compared: LDMOS and GaN. LDMOS is a transistor technology that is heavily used in wireless systems. The most important reason of its dominance is its high performance to cost ratio. Besides, its reliability is proven by the manufacturers. However, its

relatively large and lossy output capacitance may result in a disadvantage [23].

GaN is a relatively new technology used in wireless systems. It offers a high transition frequency and a high current density. Besides, its breakdown voltage is high and output capacitance is low with respect to LDMOS [24].

That seems a great improvement in transistor characteristics compared to LDMOS. But, there are important technical drawbacks in GaN technology. First, its high cost results in a very small performance to cost ratio with respect to LDMOS. The high memory effect decreases the linearity performance and high current density forces designer to be more careful in high power designs due to thermal effects. Moreover, the reliability of GaN transistor are declared by its manufacturers only recently. Because of this, designers can not easily obtain valid design parameter files for simulation using electronic tools and programs. Although GaN shows promising development for future technologies, LDMOS is still the leading technology especially for designs at lower frequencies than 3GHz [23], [24].

After determining the design inputs and deciding the proper transistor technology, the only remaining part is choosing the proper transistor. First, operation properties and the maximum ratings should be determined. The transistor should work at 2GHz and should provide a power of 10W. The 15 V supply voltage requires a maximum drain voltage of 53 volts. With these data, **Freescale Semiconductor's MRF6S20010N** transistor is chosen. It is a 10W N-Channel Enhancement-Mode Lateral MOSFET and its operation frequency is between 1600 - 2200 MHz. The maximum drain to source voltage is 68 V. The maximum junction temperature is 225°C and the maximum case temperature is 150°C. The junction to case thermal resistance is 5.9°C/W for 10W operation.

## 3.2 Simulation & Measurement Results

### 3.2.1 Simulation Results with a Harmonic Balance Simulator

An amplifier circuit designed using the first technique is shown in Fig. 3.2. The circuit consists of two matching circuits at the gate and at the drain of the transistor. The input matching circuit (IMC) is for matching the input port 50 ohm to the gate of the transistor. A blocking capacitor is needed to block the DC signal from input. The gate biasing voltage is chosen as 2.7 V (Datasheet value is 2.2V typically and 3.5V maximum).

In the output matching circuit (OMC), the capacitor compensation is made with a series capacitor and a shunt inductor. First, the drain of the transistor is analyzed and using a Smith Chart, the output capacitance of the transistor is decreased to the intended design value. Then, a series-tuned output circuit is designed. Last, the calculated optimal output resistance is matched to 50 ohm output by using a 2-stage L-match circuit.

The gain, the power added efficiency and the output power with respect to the input signal are given in Fig. 3.3. The results are satisfactory but, there are some drawbacks. All design elements are lumped and after implementation, the loss over these lumped elements will result in a degradation in performance of the circuit. Also, it may not be easy to find the intended lumped element value (for capacitor and inductor) for each design element. To minimize loss, most elements can be replaced by transmission lines. But, large values of inductors make the replacement with a transmission line difficult. So, all these drawbacks force us to use the second design technique.

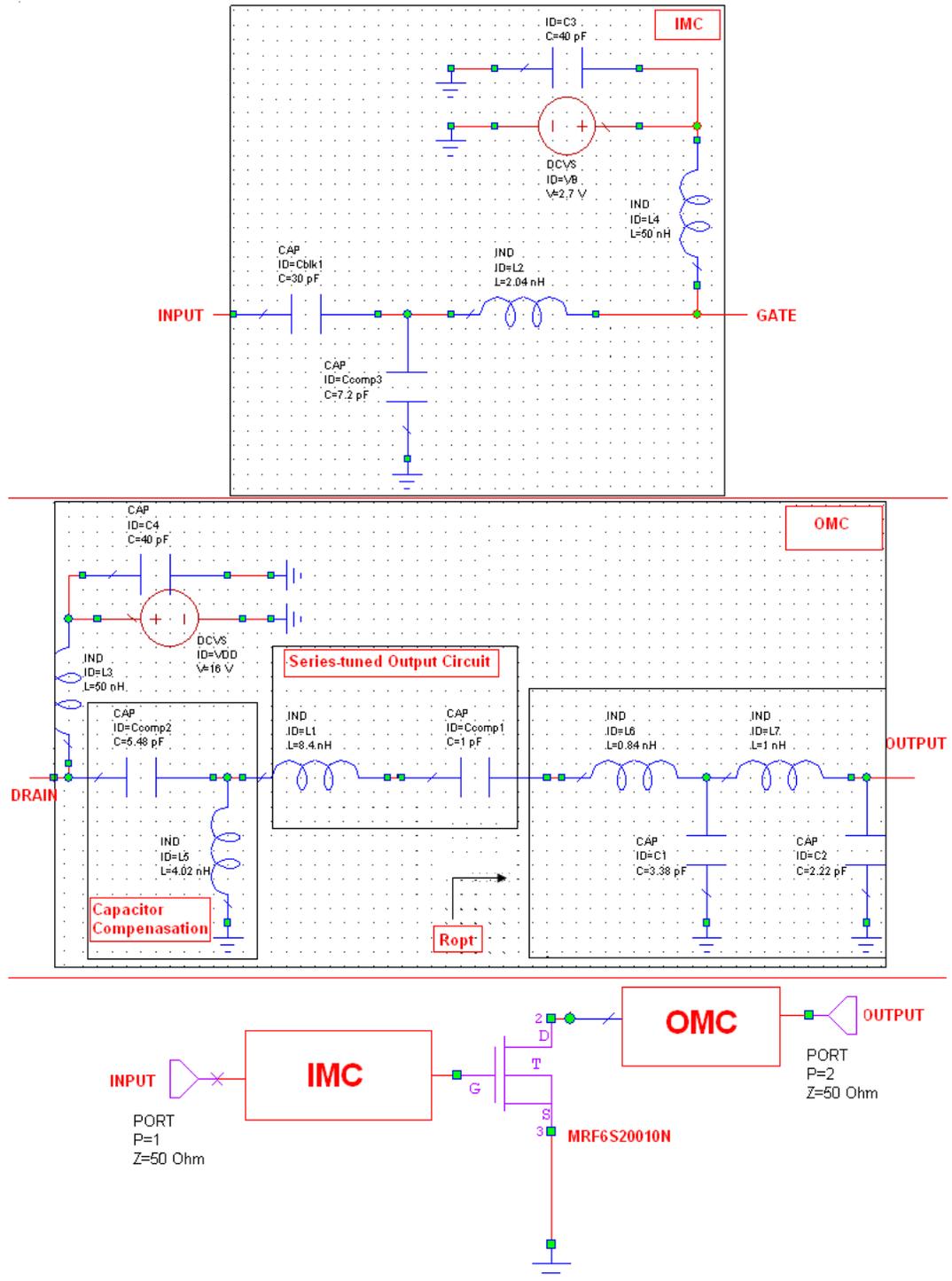


Figure 3.2: IMC, OMC and the Full Circuit for the First Technique

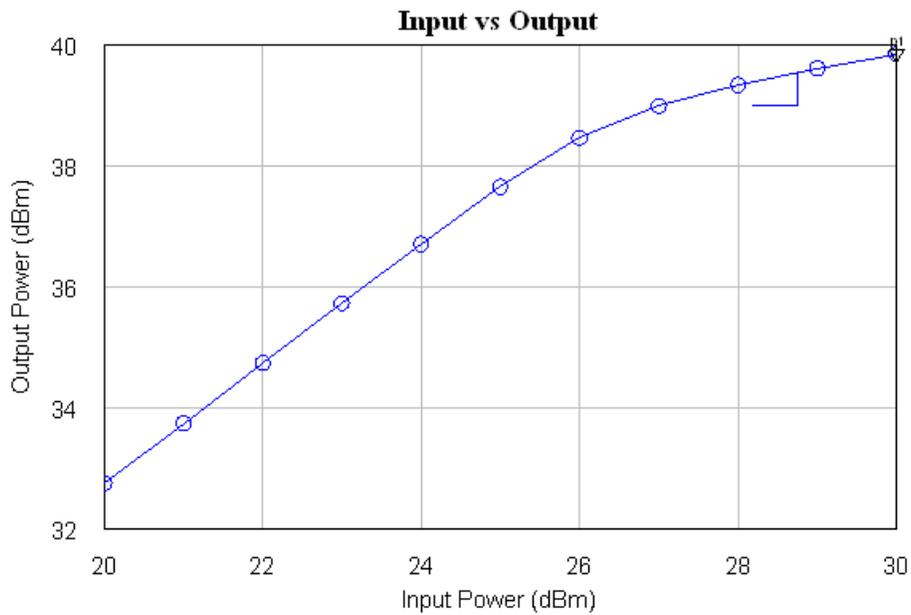
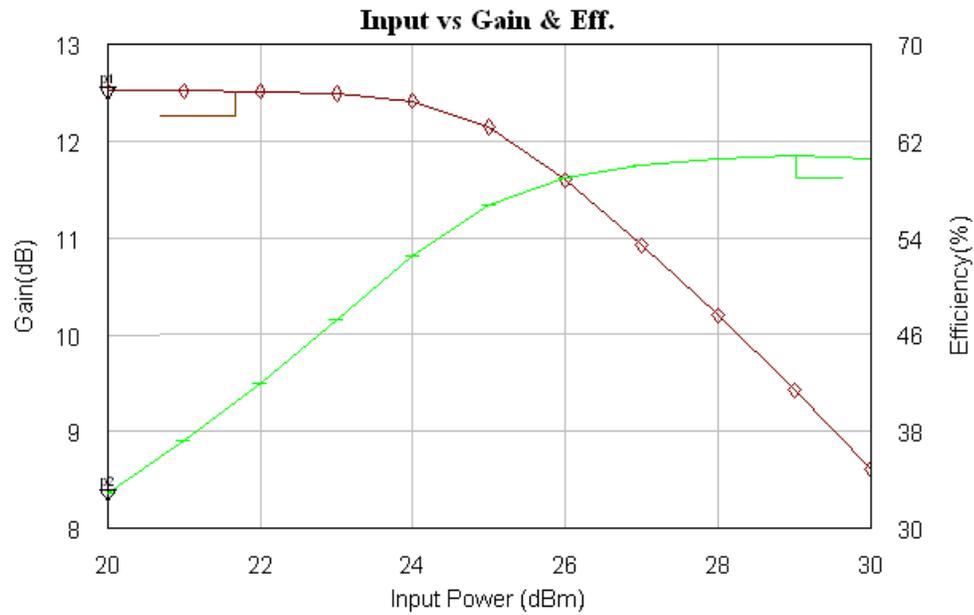


Figure 3.3: Input Power(dBm) versus Gain(dB), PAE(%) and Output Power(dBm) for the First Technique

Fig. 3.4 shows the output circuit and its harmonic behavior for the second technique. The difference of power between the fundamental and the second harmonic is 23 dBm. So, the harmonic control circuit technique in Sec. 3.1.1 should be applied to the 2-stage L-match circuit.

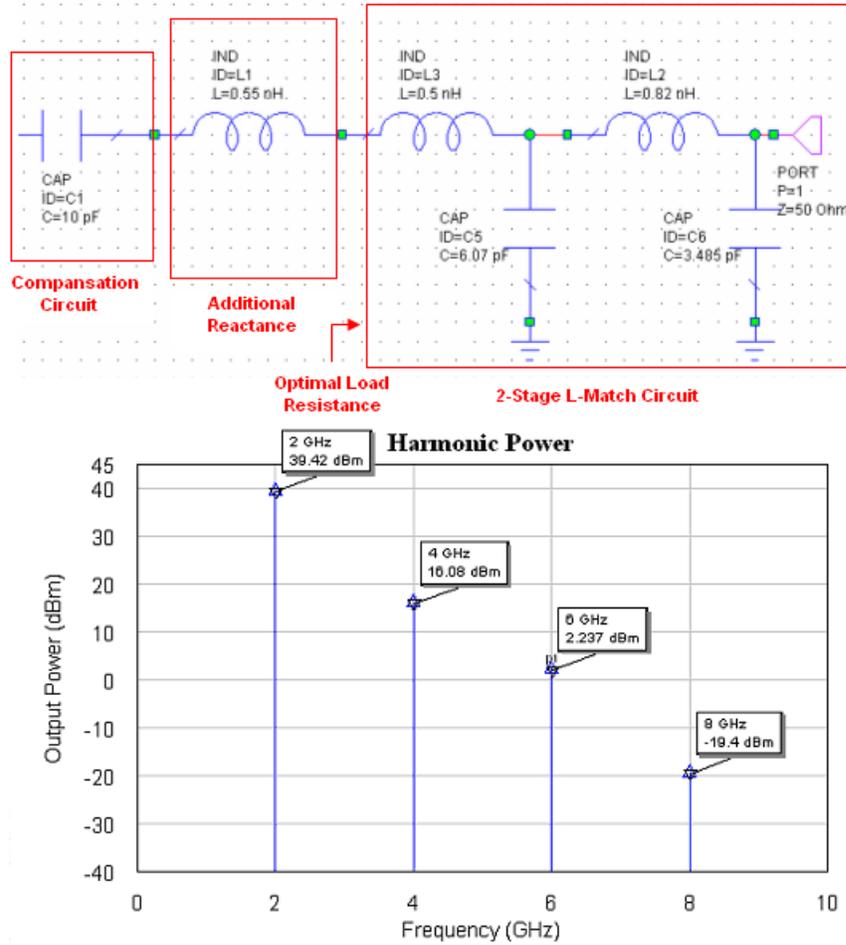


Figure 3.4: Output Circuit with Lumped Elements and its Harmonic Behavior

After applying L-match to transmission line conversion in Fig. 3.5, Fig. 3.6 shows the harmonic power at the output and the impedance for the output circuit. It is obvious that the difference of power between the fundamental and the second

harmonic increased to 43 dBm and the impedance at the second harmonic is six times more than the impedance at the fundamental frequency.

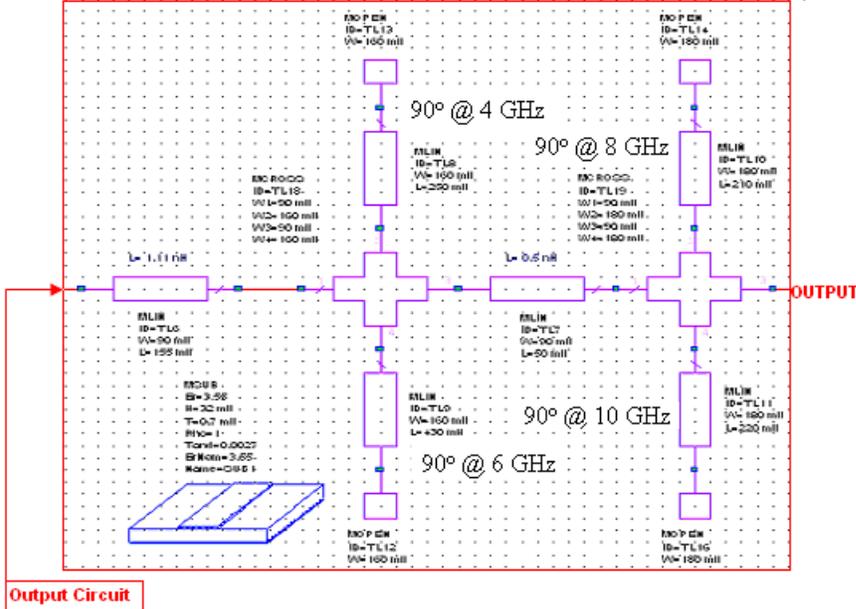


Figure 3.5: Output Circuit with Transmission Line

Fig. 3.5 shows the circuit schematic of the output circuit of the Class-E power amplifier. The transmission lines are made from microstrips. The input and output of the circuit is extended with 50-ohm lines. The gate of the transistor is matched to 50 ohms with an input matching circuit. The compensation is provided with a series capacitor as mentioned before. The gate bias voltage is 2.7 V and a DC feed transmission line is added to the biasing line. The supply voltage of the power amplifier is 15 V and the same DC feed transmission line is added to this supply line. Since, the transistor’s gate and drain have large pads, effect of these pads are included using two large transmission lines.

From Fig. 3.8, the output power at  $P_{1dB}$  point is approximately 38 dBm and efficiency is 58.5% . On the other hand, the efficiency at the power level 10 dB

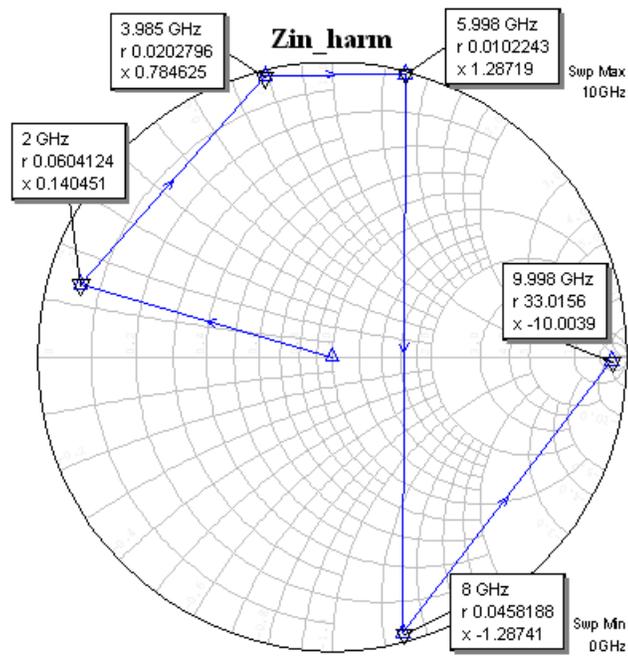
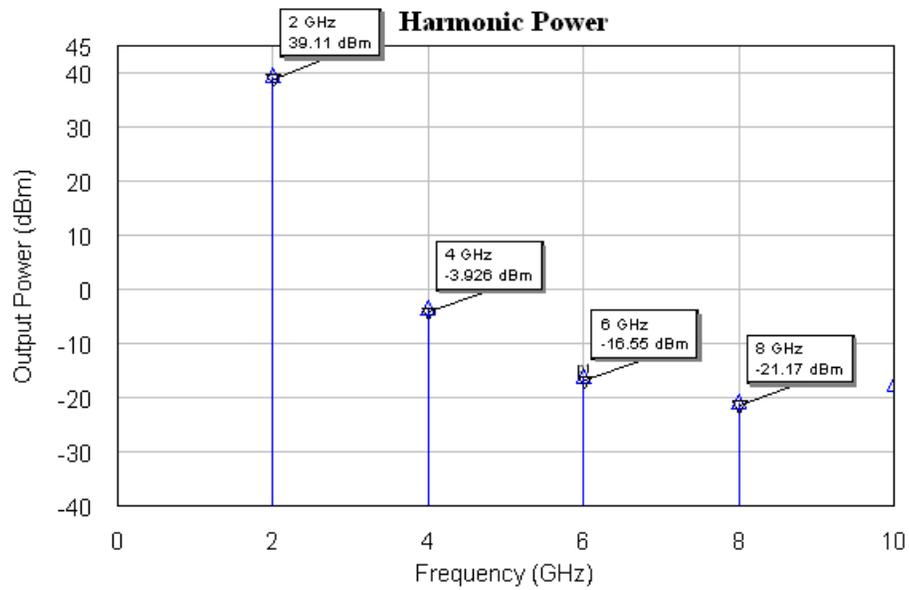


Figure 3.6: Harmonic Behavior and Impedance of Output Circuit made from Transmission Lines

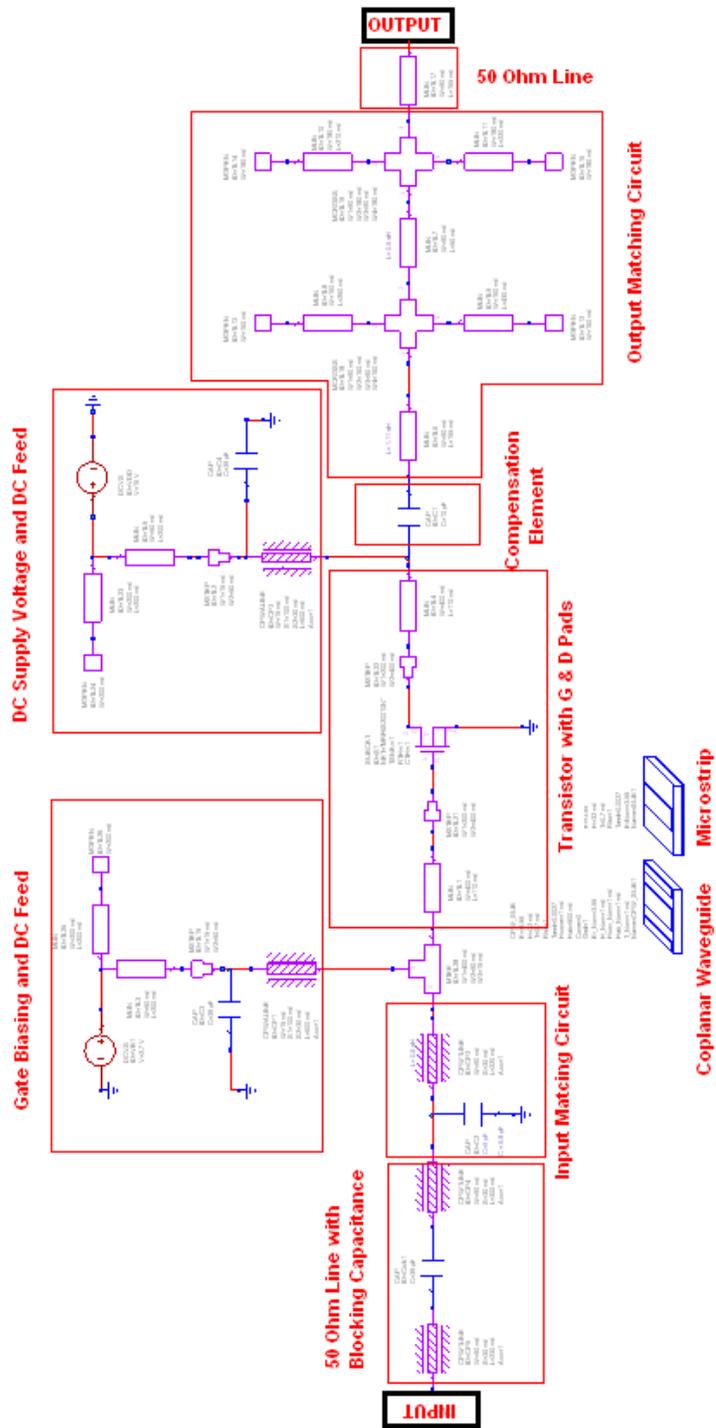


Figure 3.7: Class-E Power Amplifier Circuit Diagram

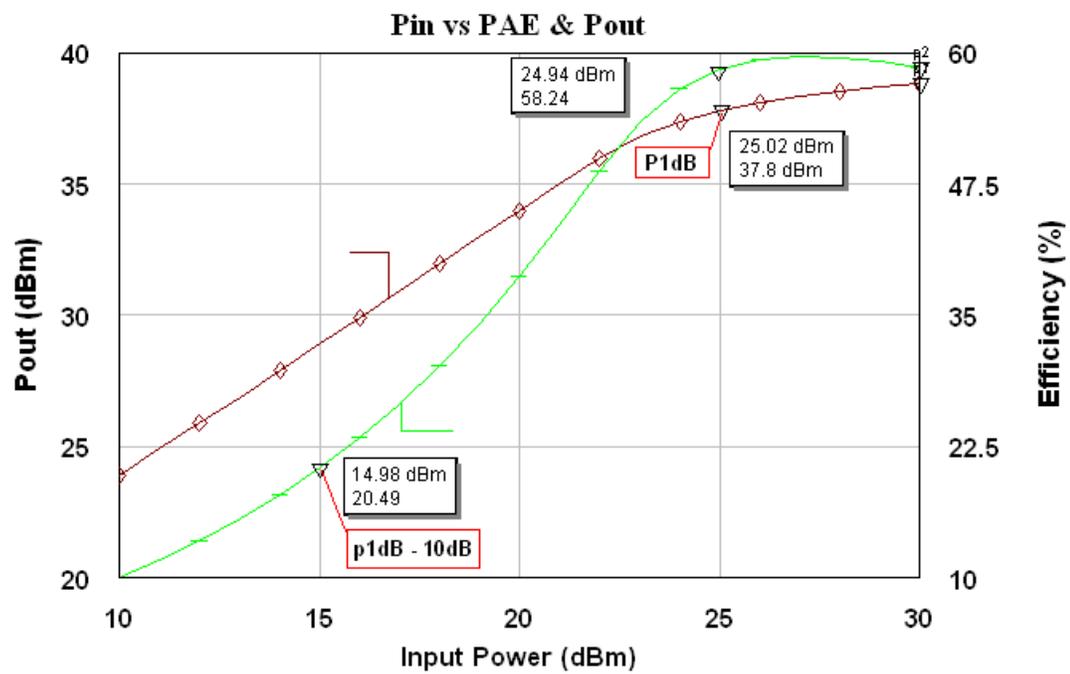


Figure 3.8: Input Power vs. Output Power & Efficiency

less than  $P_{1dB}$  (at 10 dB back-off) is more than 20%. In some techniques like OFDM, the peak-to-average-power-ratio (PAPR) is high. In other words, the output signal's envelope changes in a large range. For example, PAPR for a QPSK modulated OFDM signal with 256 sub-carriers is more than 10 dB for 3% of the possible transmitted signals [25]. That means, the efficiency must be considered in a wider range of output power levels. So, we should try to increase not only the  $P_{1dB}$  efficiency, but also the efficiency at some back-off point.

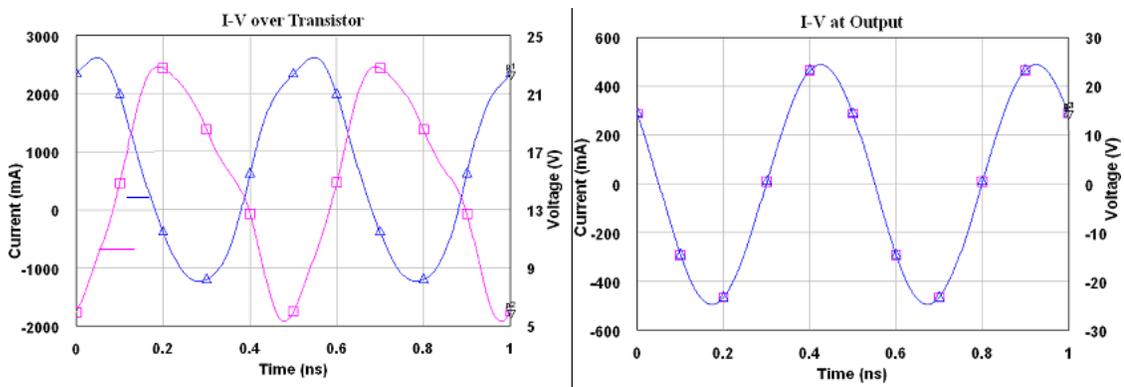


Figure 3.9: Voltage-Current Characteristics over Transistor & Output

Fig. 3.9 shows the current-voltage characteristics over the transistor and at the output of the circuit. With the proper harmonic suppression, the signal quality at the output is increased. The maximum voltage over the transistor is 25 V which is less than the maximum rating given in the transistor datasheet.

In Fig. 3.10, a flat gain behavior which results in a constant  $V_{out}/V_{in}$  ratio is obtained for the input signals below than 1 dB compression point. For the switching-mode power amplifiers, the gate-to-source voltage should be applied high enough to force the transistor to work as a switch. So, this lowers the overall gain of the switch-mode PAs. On the other hand, the stability factor  $K$  is always larger than unity and  $B$  is always larger than zero for all frequency

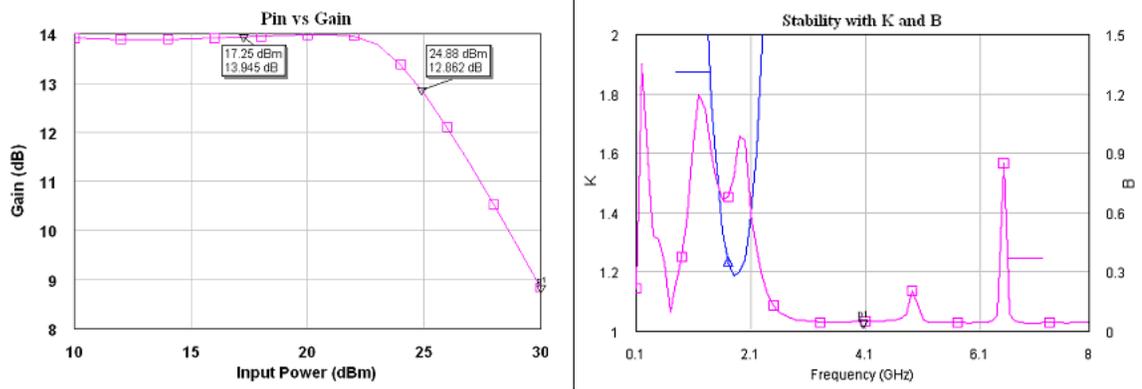


Figure 3.10: Gain vs. Input Power and Stability

components. That is, the designed Class-E power amplifier is unconditionally stable. In Fig. 3.11, an AM to PM conversion graph is given. In this figure, the

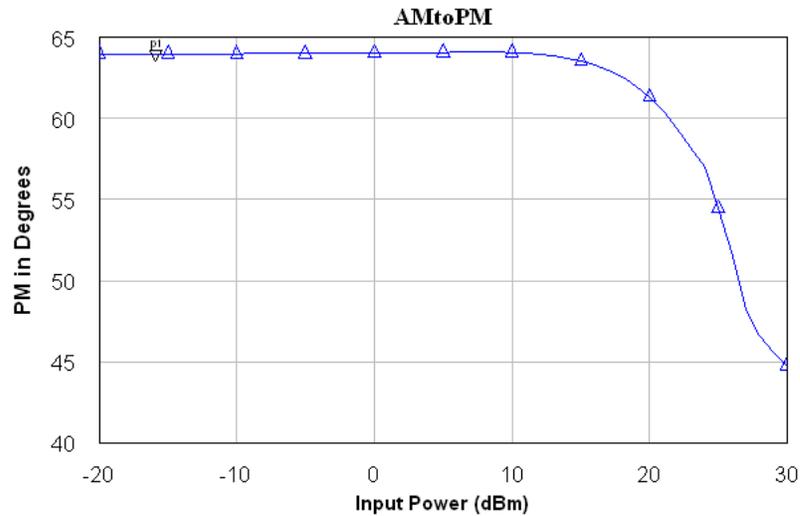


Figure 3.11: AM to PM conversion graph as a function of input signal level

angle of the output voltage is plotted in degrees with respect to the input signal level. Defining the bandwidth as the the frequency range where the efficiency drops 10%, a 150 MHz bandwidth is obtained where the gain varies within 2 dB. Fig. 3.12 shows the frequency response of the amplifier.

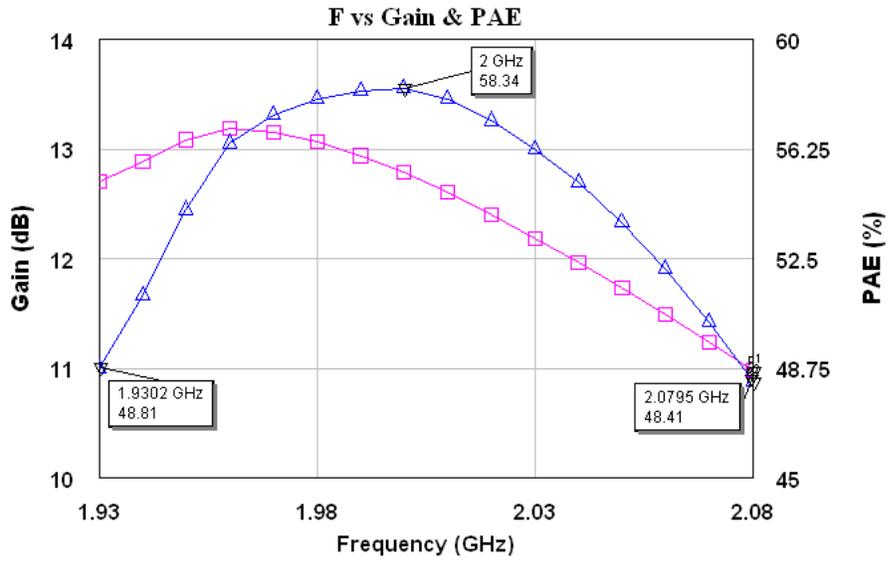


Figure 3.12: Frequency response of the amplifier

Fig. 3.13 shows a two-tone analysis of the Class-E power amplifier. As the input power is reduced, the power difference between the fundamental and the third order components <sup>1</sup> increases. The results are satisfactory and the designed class-E circuit will be implemented on a PCB.

<sup>1</sup>For two tone  $f_1$  and  $f_2$ , the important third order components are at  $2f_1 - f_2$  and  $2f_2 - f_1$

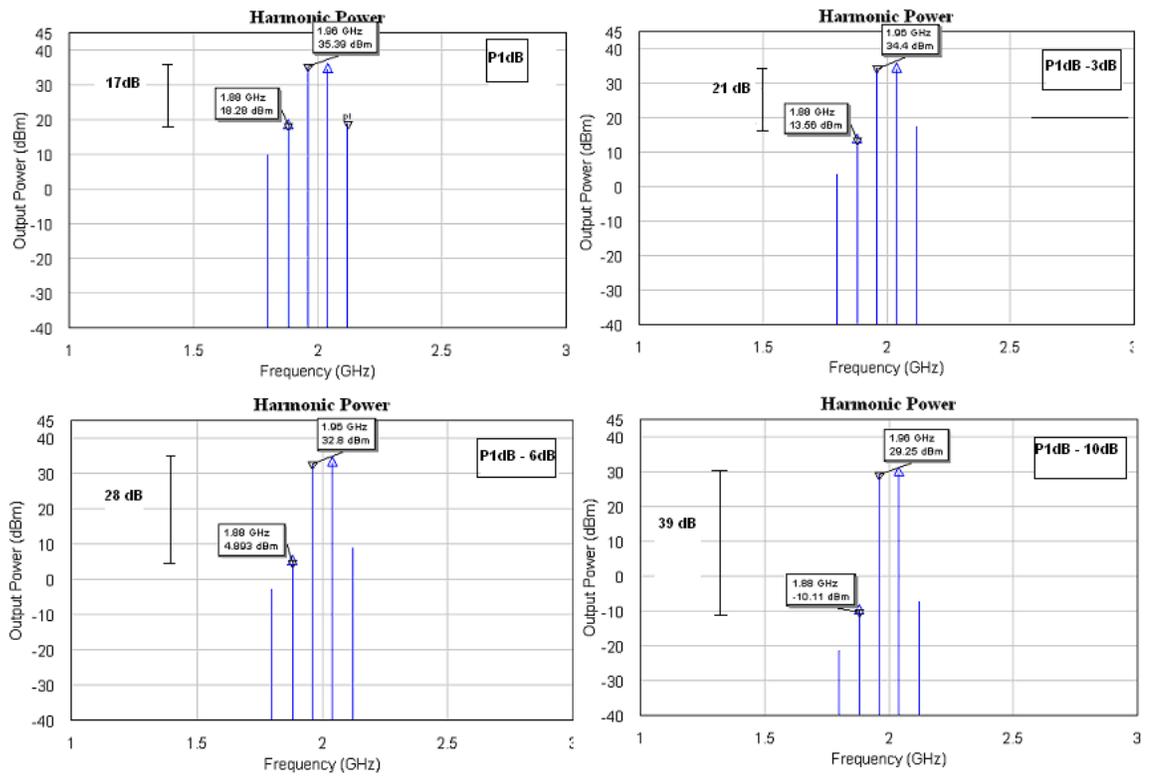


Figure 3.13: Two-tone Analysis for the Designed Circuit

### 3.2.2 Measurement Results of Implemented Circuit

To implement the designed power amplifier, first the PCB substrate should be chosen. To achieve the simulated performance, the substrate should be chosen which has a very near behavior to the given specifications in datasheet. The loss tangent should be low and it should have a stable dielectric constant in RF. So, ROGERS 4003C substrate is chosen which has a loss tangent of 0.0027 and a dielectric constant of 3.55. Our transistor's S-parameters are given for the intersection of the pad and the package. So, it is aimed to use TO-270 package surface mount to obtain the given S-parameters. It needs a rectangular hole on the PCB to place the transistor's GROUND. The height of the transistor from PAD to SOURCE is 40 mils, so a PCB substrate of 40 mils height is used. To achieve a perfect ground, a metal plate is added below the circuit. Also, the transistor's top is pushed down using a teflon piece with two screws to provide a better ground to the transistor. Some additional tuning pads are included to tune the circuit for optimization.

The layout of the implemented power amplifier is given in Fig. 3.14 and the produced board is given in Fig. 3.15. For the implemented circuit, the following measurements are made:

- Output Power vs. Input Power
- Gain vs. Input Power
- Power Added Efficiency vs. Input Power
- Output Power vs. Frequency
- IMD Analysis to obtain OIP3.

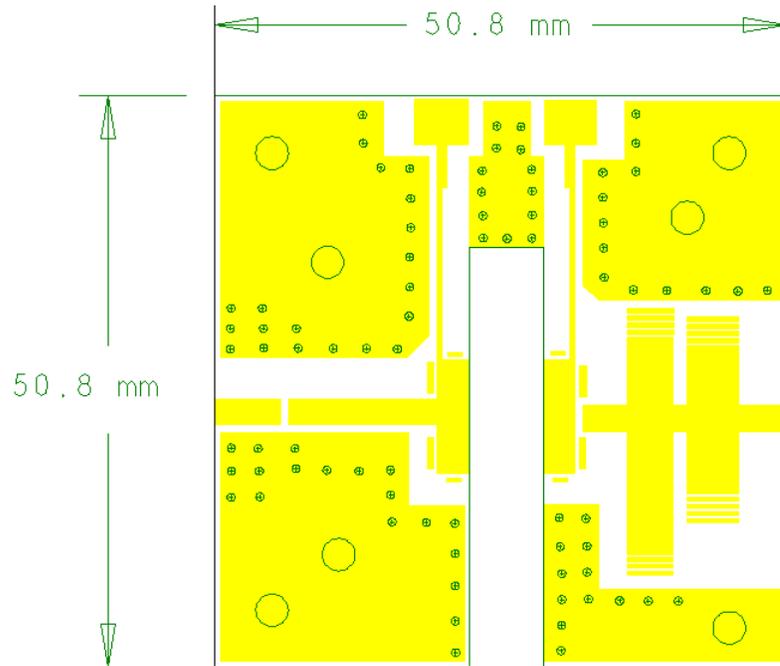


Figure 3.14: Layout of the Power Amplifier

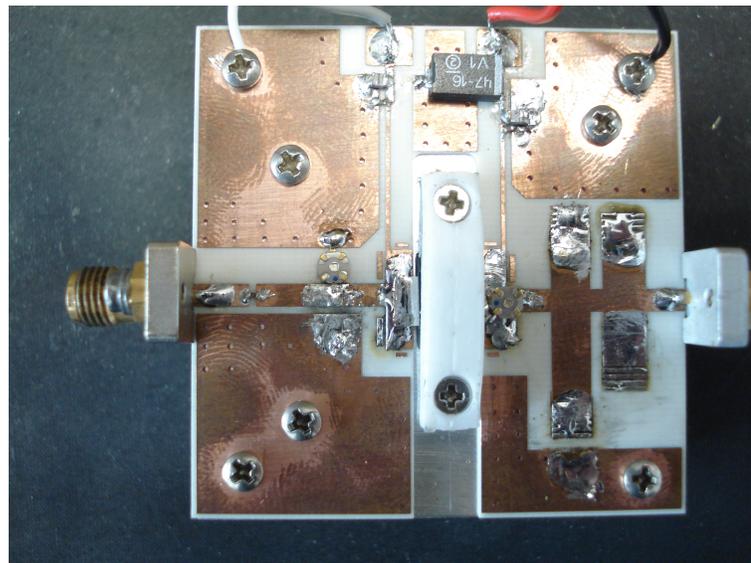


Figure 3.15: Photo of the Implemented Board

**- Simulation & Measurement Comparison:**

After producing the PCB using Rogers 4003 substrate, the amplifier is tuned to achieve its best performance. After proper tuning, the following results are obtained:

- The output power with respect to the input power is measured. The resulting measurement is given in Fig. 3.16 which compares the simulations and the measurements. The measurement results are pretty close to the simulations.  $P_{1dB}$  point is measured as 38 dBm.

- The gain behavior with respect to the input power is measured. The resulting measurement is shown in Fig. 3.17. The measurement results are again pretty close to the simulations. The linear region gain is measured as 14 dB.

- The power added efficiency with respect to the input power is measured. The resulting measurement is depicted in Fig. 3.18. The results are satisfactory for the power added efficiency.  $P_{1dB}$  point has the power added efficiency of 58.41%. The PAE value at 10 dB back-off point is measured as 19%.

- The output power with respect to the frequency is measured. The resulting measurement is given in Fig. 3.19. The output power has a ripple of 1 dB between the frequencies 1.96 GHz and 2.03 GHz.

- To measure the intermodulation distortion, a two-tone measurement is needed. To achieve this, two RF signal generators are used. The signals are combined with a combiner. To increase the isolation between input ports, 20 dB attenuators are used at the inputs of the combiner. Then, the signals are observed with a Spectrum Analyzer. For 3 different input levels, the output power at the fundamental frequencies ( $f_1$  and  $f_2$ ) and the output power at the harmonics ( $2f_1 - f_2$  and  $2f_2 - f_1$ ) are measured and using these data points, the line is

extrapolated to obtain OIP3. This value is found as 47.3 dBm.

To summarize, the simulation and measurement results are consistent with each other. With a proper tuning of the implemented circuit, satisfactory measurement results are obtained. As a result, at the  $P_{1dB}$  point of nearly 38 dBm, 58% power added efficiency is achieved at 2 GHz. Besides, the power added efficiency at 5 dB back-off point nearly achieved as 38%. The power added efficiency at 10 dB back-off point is nearly 20%.

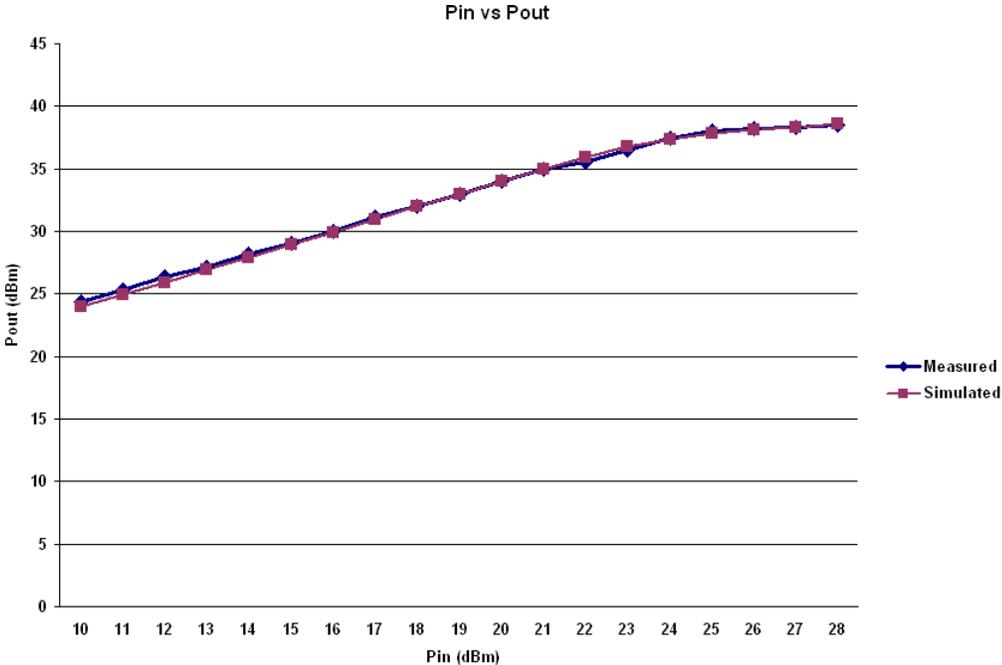


Figure 3.16: Output vs. Input Power for Simulation and Measurement

The summary of results for simulations and measurements is given in Table 3.1.

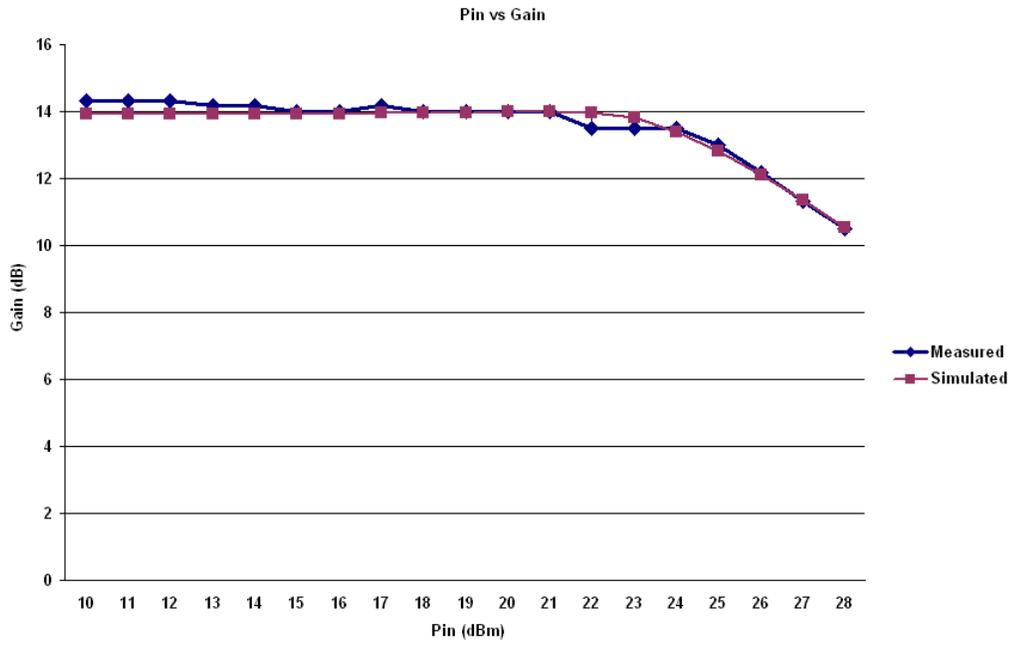


Figure 3.17: Gain vs. Input Power for Simulation and Measurement

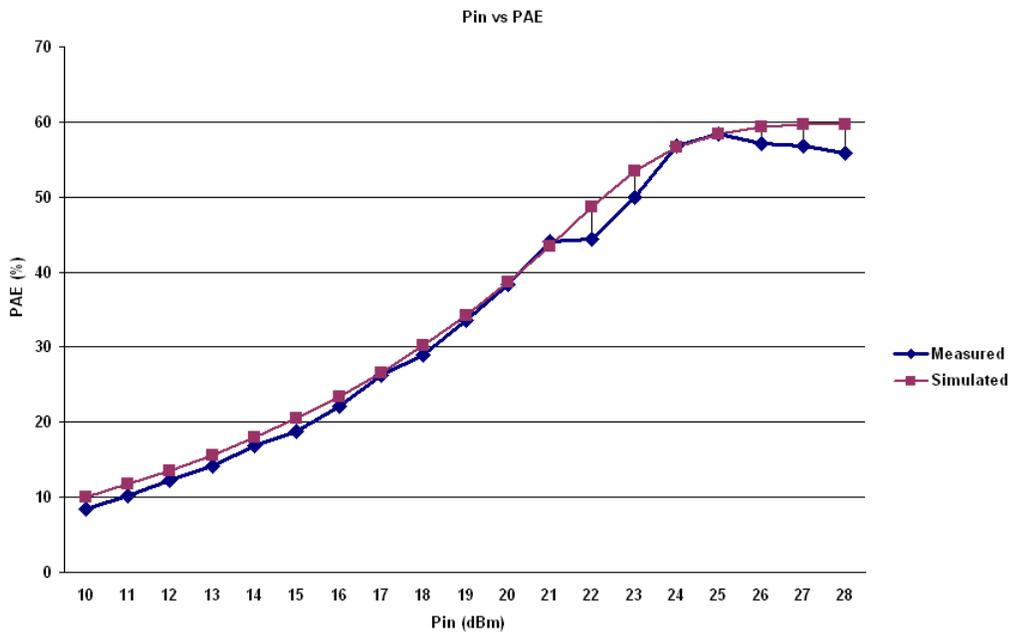


Figure 3.18: Power Added Eff. vs. Input Power for Simulation and Measurement

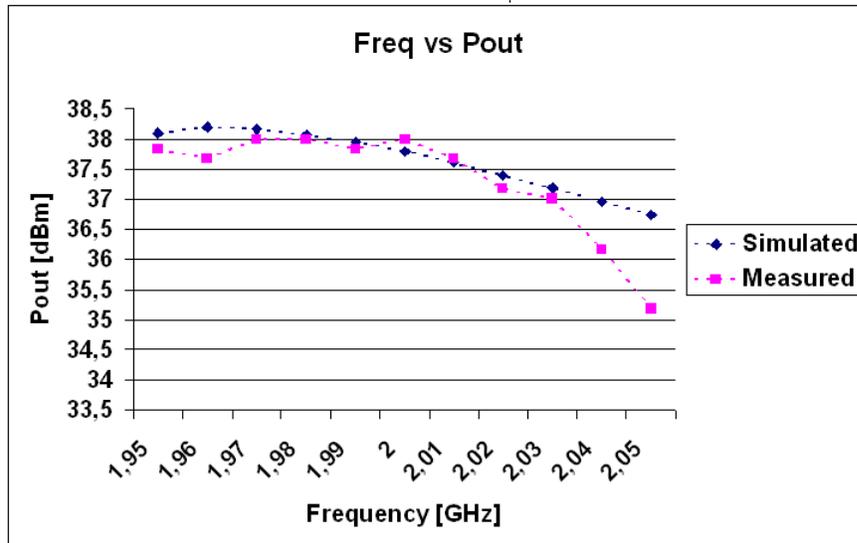


Figure 3.19: Output Power vs. Frequency for Simulation and Measurement

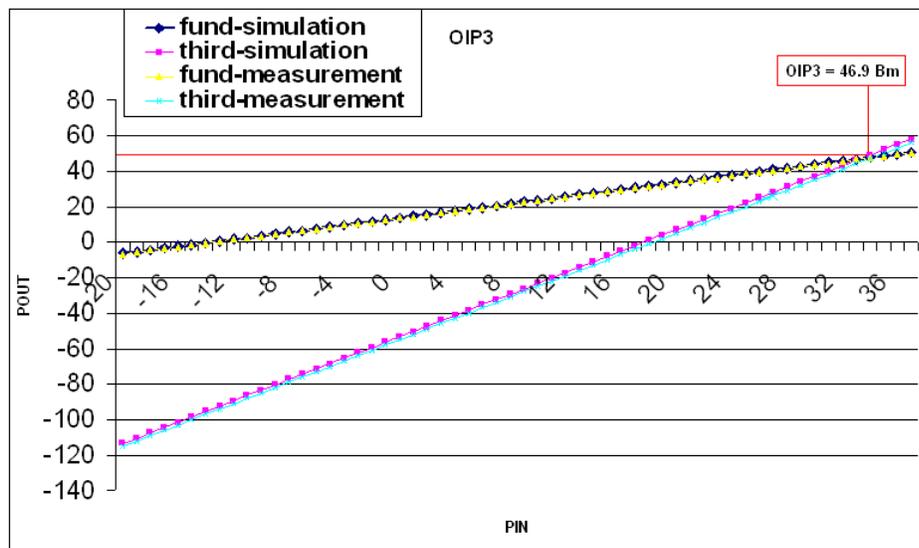


Figure 3.20: Output Third Intercept Point for Simulation and Measurement

<b>Quantity</b>	<b>Simulated</b>	<b>Measured</b>
$P_{1dB}$	37.811 dBm	38 dBm
PAE @ $P_{1dB}$	58.34%	58.41%
PAE @ $P_{1dB} - 5dB$	38.63%	38.28%
PAE @ $P_{1dB} - 10dB$	20.54%	18.83%
Gain	14 dB	14 dB
OIP3	47 dBm	47.3 dBm

Table 3.1: Summary of Simulation & Measurement Results

# Chapter 4

## Summary and Future Work

### 4.1 Conclusion

In this thesis, we aim to design a high power, high efficiency power amplifier at microwave frequencies. For this purpose, an appropriate topology is investigated and shown that Class-E power amplifier topology is very convenient for high efficient design at microwave frequencies.

After obtaining the satisfactory simulation results, the designed and simulated Class-E power amplifier circuit is implemented on the PCB. Measurement results along with the simulation results are given.

After proper tuning of the implemented circuit, the measurement results are obtained pretty close to the simulation results. To conclude, a 2 GHz, 38 dBm power amplifier (at 1dB compression point) is designed and implemented with approximately 60% power added efficiency. The power added efficiency at 10 dB back-off point is nearly 20%.

For future work, improving the linearity of the amplifier can be tried. As it can

be seen from the results, the Class-E power amplifier has the maximum PAE value at the saturation point. As escaping from the saturation point, linearity increases but with the reduction of the PAE. There are some linearization methods like digital envelope predistortion [26] or envelope following [27]. In the envelope following method, the output power and PAE is plotted with respect to  $c = V_{in}/V_{DD}$  (with a constant supply voltage ( $V_{DD}$ ) and changing input signal) and the  $c$  value is found where maximum PAE is achieved. Then, the supply voltage is changed without changing the  $c$  ratio (input is applied proportional to supply voltage to achieve the constant  $c$  ratio), and by that way a linear input to output voltage change is achieved by holding PAE constant at its maximum value.

# APPENDIX A

## Class-E Detailed Formulas

$$v_{cap} = \left[ \frac{I_L}{wC_{tot}} \left( -\frac{\pi}{2} + y \right) + \frac{V}{wC_{tot}R} \sin(\phi - y) \right] + \frac{I_L}{wC_{tot}} wt + \frac{V}{wC_{tot}R} \cos(wt + \phi) \quad (\text{A.1})$$

$$g() = \frac{[2y \sin(\phi_1) \sin(y) - 2y \cos(\phi_1) \cos(y) + 2 \cos(\phi_1) \sin(y)]}{[-2 \sin(\phi - y) \sin(y) \sin(\phi_1) - \frac{1}{2} \sin(2y) \cos(2\phi + \psi) + y \cos(\psi)]} \quad (\text{A.2})$$

$$h() = \frac{[2y \cos(\phi_1) \sin(y) + \sin(\phi_1)(2y \cos(y) - 2 \sin(y))]}{[\pi wC_{tot}R \frac{V_x}{V} + \frac{1}{2} \sin(2\phi + \psi) \sin(2y) - y \sin(\psi) + 2 \sin(y - \phi) \cos(\phi_1) \sin(y)]} \quad (\text{A.3})$$

$$R_{DC} = \frac{1}{2\pi wC_{tot}} [(2y^2 + 2yg() \sin(\phi - y)) - (2g() \sin(\phi) \sin(y))] \quad (\text{A.4})$$

$$\begin{aligned} q1 &= -2g() \sin(\phi - y) \sin(y) - 2y \sin(y) \\ q2 &= 2y \cos(y) - 2 \sin(y) \end{aligned} \quad (\text{A.5})$$

$$q3 = -\frac{g()}{2} \sin(2y)$$

$$\tan(\psi) = \frac{q1 \sin(\phi) + q2 \cos(\phi) + q3 \cos(2\phi) + g()y}{q2 \sin(\phi) + q3 \sin(2\phi) - q1 \cos(\phi)} \quad (\text{A.6})$$

$$\tan(\phi) = \frac{\frac{\sin(y)}{y} - \cos(y)}{\frac{\text{slope} \cdot y}{\pi} \cos(y) - (1 + \frac{\text{slope}}{\pi}) \sin(y)} \quad (\text{A.7})$$

$$y^4(k + \frac{\pi^2}{4}) + y^3(3\pi k + \pi + \frac{\pi^3}{4}) + y^2(2k + 9\frac{\pi^2}{4}k + \frac{\pi^2}{4} + \frac{\pi^4}{16}) + y(3\pi k - \pi) + k = 0 \quad (\text{A.8})$$

## APPENDIX B

### MATLAB code for Feed Inductor Calculation

```
Pout = 10;
Vcc = 18;
f = 2e9;
Cp = 0.8e-12;
L1 = 50e-9;
hedef = Pout / Vcc

for L1 = 40e-9:0.1e-9:60e-9

    w0 = (L1*Cp)^(-0.5);
    w = 2*pi*f;
    b = w/w0;
```

```

fi = acot( ( pi*w0*cos(pi/b)+w*sin(pi/b)) /
            (w*b*(1-cos(pi/b)+sin(pi/b)*pi/(2*b))
            - ((2/b)*cot(pi/b)) - (b*(1-cos(pi/b))
            /sin(pi/b)) );
I0 = ( Vcc * ( 1-cos(pi/b)+sin(pi/b)*pi/(2*b) )
      * (1-b^2) ) / (L1*w0*sin(fi)*sin(pi/b)) ;

A = (1/(1-cos(pi/b))) * ( (Vcc/(L1*w0)) -
      ((I0*b*cos(fi)) / (1-b^2)*sin(pi/b)) -
      (2*I0*sin(fi)/(1-b^2)) + (Vcc*pi/(L1*w)) );
B = (Vcc/(L1*w0)) - (I0*b*cos(fi)/(1-b^2));

sonuc = sin(pi/b)*b*A/(2*pi) + (1-cos(pi/b))*b*B/
      (2*pi) + I0*cos(fi)/(pi*(1-b^2)) +
      Vcc*pi/(L1*4*w) - I0*sin(fi)/2
hata = hedef - sonuc

```

**end**

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