DESIGN OF GaN-BASED COPLANAR MULTI-OCTAVE BAND MEDIUM POWER MMIC AMPLIFIERS

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MASTER OF SCIENCE

By
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July, 2013

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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Wideband amplifiers are employed in many applications such as military radar, electronic warfare and electronic instrumentations and systems, etc. This thesis project aims to build a wideband medium power monolithic microwave integrated circuits (MMIC) amplifier which operates between 6 and 18 GHz by using 0.25 μm Gallium Nitride (GaN) based high electron mobility transistor (HEMT) technology. Fully monolithic microwave integrated circuits realized with gallium nitride (GaN) high electron mobility transistors are preferred for designing and implementing microwave and millimeter wave power amplifiers due to its superior properties like high breakdown voltage, high current density, high thermal conductivity and high saturation current. Large band gap energy and high saturation velocity of AlGaN/GaN high electron mobility transistors (HEMTs) are more attractive features for high power applications in comparison to the conventional material used in industry for power applications- gallium arsenide (GaAs). Besides the high power capability of GaN enables us to make devices with relatively smaller sizes than of GaAs based devices for the same output power. Device impedances in GaN technology are higher than the GaAs technology which makes broadband matching easier.

Firstly, GaN material properties are overviewed by mentioning the design and characterization process of the AlGaN/GaN epitaxial layers grown by Bilkent NANOTAM. After the microfabrication process carried out by Bilkent

NANOTAM is explained step by step. It is followed by characterization of the fabricated HEMTs. As a final step before going through the design phase, the small signal and large signal modeling considerations for GaN based HEMTs are presented. In the last part, designs of three different multi-octave MMIC amplifier realized with coplanar waveguide (CPW) elements are discussed. In order to extend the bandwidth and to obtain a flat gain response, two different design approaches are followed, the first one is realized with Chebyshev impedance matching technique without feedback circuit (CMwoFB) and the other one is utilized by Chebyshev Impedance matching technique with negative shunt feedback (CMwFB), respectively. To maximize the output power, two transistors in parallel (PT) are used by introducing Chebyshev matching circuit and negative feedback circuit. The design topology which consists of two parallel transistors (PT) is modified to fulfill all the design requirements and it is implemented by taking process variations and the previously obtained measurement results into account. The measurement and the simulation results match each other very well, the small signal gain is 7.9 ± 0.9 dB and the saturation output power in the bandwidth is higher than 27 dBm in this second iteration.

Keywords: GaN HEMT, CPW, epitaxial growth, microfabrication, large signal modeling, Chebyshev matching, wideband MMIC PA design.

ÖZET

GaN TABANLI 1 OKTAVDAN FAZLA BANT GENİŞLİĞİNE SAHİP OLAN ORTA GÜÇLÜ MMIC YÜKSELTEÇLERİN TASARIMI

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Geniş bantlı yükselteçler askeri radar, elektronik harp, elektronik ürün ve sistemlerde olmak üzere birçok uygulamada kullanılmaktadır. Bu tez projesi 0.25 μm GaN tabanlı HEMT teknolojisini kullanarak, 6 ve 18 GHz frekans aralığında çalışan geniş bantlı MMIC yükselteci inşa edilmesini amaçlamıştır. GaN HEMT kullanılarak gerçekleştirilmiş tam monolitik mikrodalga entegre devreler yüksek akım yoğunluğu, yüksek ısıl iletkenliği ve yüksek elektron hızı gibi üstün özelliklerinden dolayı mikrodalga ve milimetre dalga yükselteçlerin tasarımında ve uygulamasında tercih edilmektedir. AlGaN/GaN HEMT' lerin yüksek enerji bant aralığı ve yüksek elektron hızı, yüksek güç uygulamaları için GaAs la karşılaştırıldığında daha ilgi çekici özelliklerdir. Bunun yanı sıra, aynı çıkış gücü için, GaN' ın yüksek güç kapasitesi, GaAs tabanlı aygıtlara oranla daha küçük boyutlarda aygıt yapımına olanak verir. GaN teknolojisinde aygıt empedansları GaAs teknolojisinde olduğundan daha yüksektir, bu geniş bant uyumlama devrelerini daha kolaylaştırır.

İlk olarak, Bilkent NANOTAM tarafından büyütülen AlGaN / GaN epitaksiyel katmanlarının tasarım ve karakterizasyonu sürecinden bahsedilerek, GaN malzeme özellikleri gözden geçirilmiştir. Daha sonra yine Bilkent NANOTAM tarafından sürdürülen mikrofabrikasyon süreci adım adım

açıklanmıştır. Onu HEMT karakterizasyonu fabrikasyonu takip etmiştir. Son adım olarak tasarım aşamasına geçmeden önce GaN tabanlı HEMT ler için küçük sinyal ve büyük sinyal modellemesinde dikkat edilecek noktalar sunulmuştur. Son bölümde ise, 3 adet 1 oktavdan fazla bant genişliğine sahip eşdüzlemli dalga kılavuzu (CPW) ile gerçekleştirilmiş MMIC yükselteçleri tartışılmıştır. Bant aralığını genişletmek ve daha az dalgalı bir kazanç elde etmek için, 2 farklı tasarım yaklaşımı izlenmiştir, sırasıyla birinci devre Chebyshev empedans uyumlama tekniği ile geri besleme olmaksızın (CMwoFB), diğerinde ise Chebyshev empedans uyumlama tekniği ve paralel geri beslemesinden (CMwFB) faydalanmıştır. Çıkış gücünü arttırmak için, iki paralel transistor Chebyshev empedans uyumlama tekniği ve paralel geri beslemesi (PT) ile kullanılmıştır. Bu iki paralel transistor içeren tasarım topolojisi bütün tasarım isterlerini sağlayabilmek için fabrikasyona bağlı değişiklikler ve önceden elde edinilen ölçüm sonuçları göz önünde bulundurularak düzenlenmiştir. Benzetim sonuçları ile ölçüm sonuçları birbirleriyle oldukça uyumludur, küçük sinyal kazancı 7.9 ± 0.9 dB ve satürasyondaki çıkış gücü ise 27 dBm dir.

Anahtar kelimeler: GaN HEMT, CPW, epitaksiyel büyütme, mikrofabrikasyon, büyük sinyal modelleme, Chebyshev uyumlama, genişbant MMIC güç yükselteç tasarımı

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Finally, I am deeply indebted to my family for their unconditional love, understanding and encouragement. I hereby dedicate this work to my lovely parents, Suna Eren and Bektaş Eren and to my brother, Atalay Eren.

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Chapter 1

Introduction

Wide-band amplifiers are critical for a wide range of general purpose applications such as radar, electronic warfare (EW) and electronic instrumentation [1],[2]. Gallium-Nitride (GaN) has become the promising material choice for wideband power amplifiers due to its highly demanded physical and electrical properties. Fully monolithic microwave integrated circuits (MMICs) realized with GaN high electron mobility transistors (HEMTs) provide some superior material properties such as high breakdown voltage, high current density, high thermal conductivity and high saturation current [3],[4],[5],[6],[7]. For high power applications, large bandgap energy and high saturation velocity of AlGaN/GaN HEMTs are attractive features. Large bandgap nature of GaN also makes the material more advantageous than the conventional material Gallium Arsenide (GaAs) for the device operation that requires high voltage, power and temperature. In addition, high power capability of GaN enables us to make devices with smaller size than of GaAs based devices for the same output power requirement. Device impedances in GaN technology are higher than the GaAs technology which makes matching easier.

In this thesis, design, fabrication and measurement of a single stage 6 GHz - 18 GHz monolithic microwave integrated circuit (MMIC) medium-power amplifier is explained. The amplifier is realized with coplanar waveguide (CPW) circuit elements using 0.25 µm-gate Gallium Nitride (GaN) HEMT technology by implementing two- and- a- half dimensional (2.5D) Momentum simulation tool in ADS. The 4x75 µm HEMTs used in this technology have a

cutoff frequency (f_t) of higher than 40 GHz which indicates that these active devices can be comfortably used for the frequency range of 6 GHz to 18 GHz.

In Chapter 2, material properties of GaN based HEMTs will be investigated by explaining what makes GaN based devices more advantageous than its conventional competitors like GaAs, Si for high power and high frequency applications. Formation of two dimensional electron gas (2DEG) region is overviewed with a strong emphasis on the concept of the polarization induced sheet charge density at the interface of AlGaN/GaN HEMTs. Next, AlGaN/GaN heteroepitaxial layer growth using metal organic chemical vapour deposition (MOCVD) system will be provided in a step by step manner by emphasizing the design of epitaxial structure and characterization techniques for the grown layers.

In Chapter 3, transistor mask design considerations will be revisited in detail by indicating the HEMT structure and the transistor mask layout which is composed of those HEMTs. Afterwards, the micro fabrication process will be presented by examining each fabrication steps specifically from beginning to end. The MMIC fabrication process includes mesa isolation, ohmic contact metallization, NiCr resistor formation, Schottky contact metallization, first metal formation, device passivation (Si_3N_4), dielectric opening, airbridge post and interconnect metallization steps. Device passivation is an essential need to enhance the device performance by about 20% to suppress the traps thus it prevents the degradation in maximum current density and transconductance due to surface charges and traps. In pursuit of fabrication of GaN based HEMT structures, DC and RF characterization process of the fabricated HEMTs will be explained by giving the performance results of the transistors. This chapter will be continued by examining the GaN based HEMT modeling techniques including the small signal modeling and the large signal modeling of the AlGaN/GaN HEMTs. Additionally, the details of the modeling software, which is called as TOPAS produced by IMST GmbH, will be mentioned. This section

will be concluded by checking the small-signal and large-signal model consistency.

In Chapter 4, small-signal and large-signal modeling considerations are discussed by examining the various modeling approaches. In the mean time, the model validations with measurement results are shown.

In Chapter 5, design of a wideband (6 GHz-18 GHz) medium power monolithic microwave integrated circuit (MMIC) amplifier using a 0.25 μm gate length Gallium Nitride (GaN) HEMT technology will be explained by revisiting general wideband amplifier design considerations and techniques. Wideband Coplanar Waveguide (CPW) MMIC amplifier designs with the network synthesizer method and the negative feedback method will be presented. Furthermore, the small-signal and large-signal measurement results for the realized amplifiers are compared with the 2.5D electromagnetic Momentum simulation results obtained in ADS. General design considerations for wideband MMIC amplifier are overviewed and then the design, realization and measurement results for the first wideband amplifier topology without negative feedback (CMwoFB) is assessed, after that, the design and realization of the amplifier by using Chebyshev matching network with negative feedback (CMwFB) is explained including the simulations and measurements, following that design, realization and measurements of two parallel transistors with negative feedback topology (PT) is presented. Lastly, the final wideband amplifier, which satisfies all the specifications, is provided with measurement results.

Finally, in chapter 6 the measurement results of the amplifier will be summarized by determining what we can do for the further GaN HEMT model improvement. In a nutshell, work done throughout this thesis will also be overviewed.

Chapter 2

GaN based High Electron Mobility Transistors

2.1 Properties of GaN Based HEMTs

A literature study of Gallium Nitride based HEMT technology begins with electrical and physical material properties of GaN based devices and continuing with two dimensional electron gas formation (2DEG) mechanism in AlGaN/GaN HEMTs, moving to MOCVD growth and finally to characterization of epitaxial layers.

In this chapter, the material properties including the working principle of Gallium Nitride (GaN) HEMTs are explained providing the benefits of GaN HEMT technology. Gallium Nitride, III/V direct bandgap semiconductor, has been seen as the key material for the next generation of high frequency and high power transistors due to its advantageous material properties [7]. The wide bandgap semiconductors are much more preferable for microwave power applications since employing a large bandgap material increases the temperature tolerance of the device while struggling with the large power levels and large bandgap also enables operating at higher voltage levels compared to smaller bandgap semiconductors. As can be seen in Table 2.1, the bandgap energy of GaN is higher than the bandgap energy of Gallium Arsenide (GaAs), which is the conventional material used in microwave amplifier applications. Therefore GaN can handle much higher voltages and operate at much higher temperatures.

Besides the wide bandgap nature of GaN material, GaN HEMT technology has several advantageous and superior properties in terms of higher power capability, higher efficiency, easier matching circuit design than the principal competing material GaAs. Large bandgap (3.4 eV), large electric breakdown field (3.3 MV/cm) and high saturation electron drift velocity (> $2x10^7$ cm/s) of GaN devices are very decisive properties on electrical performance of active devices [8],[9]. High saturation electron drift velocity (V_{eff}) results in high saturation current as desired in power applications and short circuit current gain cutoff frequency is proportional to the saturation electron velocity. In addition, GaN has a good thermal conductivity which is around 1.3 W/cm.K [10]. In Table 2.1, a commonly used range of semiconductors are provided to be able to compare the material properties of the GaN with its widely used conventional competitors like GaAs, Si and SiC in the semiconductor industry.

Material Property	Si	GaAs	6H-SiC	6H-SiC	GaN
Band gap (eV)	1.12	1.42	3.02	3.3	3.4
Dielectric Constant	11.7	12.9	9.66	9.7	8.9
Breakdown Electric Field Strength (MV/cm)	0.3	0.4	3.2	3	3.3
Electron Mobility(cm2/V.s)	1400	8500	400	900	1000
Thermal Conductivity (W/cm.K)	1.3	0.55	4.9	3.7	1.3
Electron Drift Velocity(10^7cm/s)	1	1	2	2	2.2

Table 2.1 Crucial physical properties of some conventional materials used in power applications [10],[11].

AlGaAs and AlGaN are the ternary materials that are commonly used in power HEMT devices. The conducting layers are grown over a semi-insulating

substrate such as SiC using epitaxial growth techniques. GaN can be grown in zincblende or wurtzite crystal structures. Wurtzite crystal structures are much more preferable than zincblende structures since the bandgap of the wurtzite crystal structure is higher than the zincblende crystal structure. The wurtzite crystal structure of nitride based semiconductors is a part of the hexagonal crystal system and it is an example of non-centrosymmetric structure which characterizes the symmetry of a crystal lattice with no inversion center [12]. The wurtzite structure lacking inversion layer leads to macroscopic polarization due to the strong ionicity of the semiconductor [13]. The wurtzite crystal structure is provided in Figure 2.1. Non-centrosymmetric wurtzite crystal structures of GaN can be classified as Ga-faced and N-faced polarity depending on the epitaxial growth direction of the crystal. The growth direction for wurtzite GaN crystal structures is along the c-axis and the spontaneous polarization exhibits along the c-axis by causing strong electric fields. In Figure 2.1, Ga-faced GaN((0001) atomic layering) and N-faced GaN ($(000\bar{1})$ atomic layering) are shown [14].

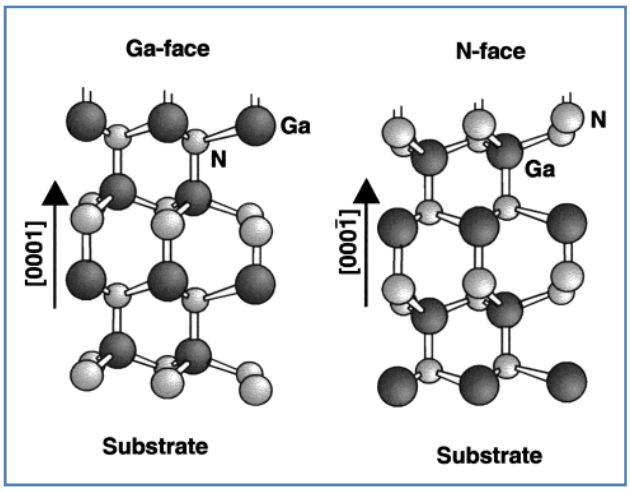


Figure 2.1 Crystal structures of GaN wurtzite for Ga-faced (left) and N-faced (right) polarity crystals [14].

Typical crystal structure used in AlGaN/GaN HEMT is Ga-faced surface in the (0001) orientation since growing a Ga-faced crystal structure forms electron channel (2DEG) at the heterojunction as a result of the polarity of spontaneous

and piezoelectric polarization components, which are parallel to each other. In the case of an N-face GaN structure, there is no electron channel formation at the AlGaN/GaN interface because of the change in the orientation of polarization components [14], [15].

For the AlGaAs/GaAs heterojunction, intentional doping is required to form charges. However, it should be noted that no intentional doping is needed for the AlGaN/GaN interface due to the polarization induced charges introduced by spontaneous and piezoelectric polarization effects. Microscopic polarization, which arises from the strong ionicity of metal-nitrogen covalent bond due to high electro-negativity of nitrogen, constitutes macroscopic polarization when the nature of the crystal structure is non-centrosymmetric [12], [14]. Along the c-axis of the wurtzite crystal structure, the macroscopic electrical polarization, which is called as spontaneous polarization (P_{SP}), occurs due to the intrinsic asymmetry of the bonding in the equilibrium. Throughout this thesis, polarizations along the (0001) direction will be considered, since it is the direction of the epitaxial growth to form an electron channel at the interface of AlGaN/GaN layer. The spontaneous polarization constant (c_0) in GaN and AlGaN semiconductors is large so the polarization dipole and electric field appears in an unstrained crystal structure [16], [17]. The difference among spontaneous polarization coefficients leads to spontaneous polarization induced sheet charge in AlGaN and the direction of the spontaneous polarization occurred in Ga-face heterostructure is negative since it points toward the substrate. In addition to spontaneous polarization, piezoelectrically induced charges, which are formed due to piezoelectric polarization (P_{PZ}), contribute to the formation of polarization induced charges at the interface of AlGaN/GaN. Strained AlGaN layer leads to the piezoelectric polarization field and related electrostatic charge. That is, lattice mismatch between GaN and AlGaN gives rise to piezoelectric polarization induced sheet charges in AlGaN [15], [17]. In Figure 2.2, directions of spontaneous polarization field for and piezoelectric

polarization field for AlGaN/GaN crystals on c-axis in a Ga- faced polarity crystal are shown [17].

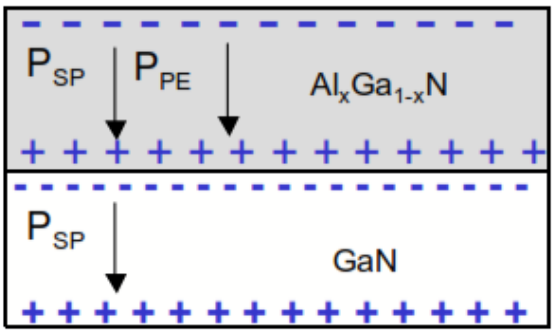


Figure 2.2 Piezoelectric and Spontaneous Polarization observed in AlGaN/GaN [17].

In AlGaN/GaN HEMTs, positive polarization charges accumulated at the undoped AlGaN/GaN heterostructure lead to high channel carrier concentration at the interface, resulting in a two dimensional electron gas (2DEG) (see Figure 2.3). The concept of 2DEG is given detailed in the next subsection.

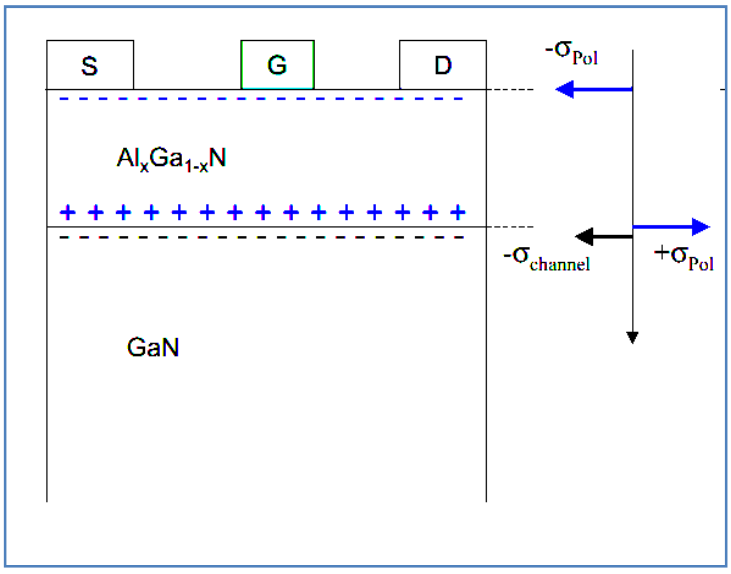


Figure 2.3 Accumulated polarization induced charges and sheet carrier charges occurred at the AlGaN/GaN interface [17].

High sheet carrier concentration at the heterojunction (2DEG concentration) is desirable for high electron mobility transistor (HEMT) structures. The

piezoelectric polarization due to the strained AlGaN top layer in AlGaN/GaN HEMTs causes a worthy increase in sheet carrier concentration in the 2DEG region. Due to the strong polarization effects in AlGaN/GaN structures, doping is not needed to form a 2DEG region at the interface. The piezoelectric polarization occurred in AlGaN/GaN based transistors is more than 5 times larger the piezoelectric polarization induced in AlGaAs/GaAs based transistor [14].

High electron mobility transistor (HEMT), which has drain, source and gate terminals, is one of the members of the MESFET family. The conducting channel between drain and source contacts is due to 2DEG formation at the interface of AlGaN/GaN. The drain current can be controlled by varying the gate voltage, that is, transistor behaves like a voltage controlled current source Similarly, the 2DEG density in the conducting channel can be controlled by the gate voltage for HEMTs.

The total polarization on the AlGaN/GaN heterostructure equals to sum of spontaneous polarization and piezoelectric polarization when the external electric field is not applied as it is given in equation (2.1). The sheet charge density at the interface of AlGaN/GaN is calculated by the given equation (2.2).

$$P = P_{SP} + P_{PE}\,. \tag{2.1}$$

$$\sigma_P = P_{SP,AlGaN} + P_{PE,AlGaN} - P_{SP,GaN}\,. \tag{2.2}$$

Piezoelectric polarization can be calculated by employing the equation (2.4) where e_{33} and e_{31} are piezoelectric constants, ε_z is the strain along the z-axis and $\varepsilon_x = \varepsilon_y$ is the isotropic in-plane strain. The strain through the z-axis can be found by placing elastic constants (C_{13} and C_{33}) in equation (2.5).

$$\varepsilon_z = \frac{c - c_0}{c_0} \;\&\; \varepsilon_{x,y} = \frac{a - a_0}{a_0}\,. \tag{2.3}$$

$$P_{PE} = e_{33}\varepsilon_z + e_{31}(\varepsilon_x + \varepsilon_y)\,. \tag{2.4}$$

$$\varepsilon_z = -2\varepsilon_{x,y}\left({}^{C_{13}}/_{C_{33}}\right). \tag{2.5}$$

When the polarization fields are large enough to ionize the surface donor states, the ionized surface charges pass through the AlGaN barrier by accumulating the these charges at the interface of the heterojunction. By substituting the piezoelectric polarization formula, which is obtained by combining equations (2.3), (2.4) and (2.5), into the sheet charge density equation given in equation (2.2), the accumulated sheet charge density at the interface of AlGaN/GaN HEMT can be obtained. The relation is given by,

$$|\sigma_P| = \left|2\frac{a-a_0}{a_0}\left\{e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right\} + P_{SP,AlGaN} - P_{SP,GaN}\right|, \tag{2.6}$$

$$\text{where } P_{PE} = 2\frac{a-a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right). \tag{2.7}$$

The formula for 2DEG sheet carrier density, which is derived by assuming that the sum of the charges associated with the carriers must equal zero (the charge neutrality), is given in equation (2.8) as a function of Al mole fraction (x) of the AlGaN layer, where σ_P is the polarization induced charge at the interface of the AlGaN/GaN layer, e is the electron charge, ε_0 is the free space permittivity, ε_{AlGaN} is the relative dielectric constant of the AlGaN layer, d is the AlGaN layer thickness, ϕ_b is the Schottky barrier height, E_F is the Fermi level and ΔE_C is the conduction band offset. Alongside of Al mole fraction, critical thickness of AlGaN barrier layer plays a significant role in determining the 2DEG sheet charge density. If the thickness of the grown AlGaN layer is smaller than the critical one, surface donor states would remain below the Fermi level due to the occurrence of low polarization fields. When the AlGaN layer

thickness exceeds the critical thickness given in equation (2.9), the ionized surface charges creates 2DEG region at the interface of AlGaN/GaN layers by filling the triangular like quantum well with the ionized electrons. In this expression, the surface donor energy, the band offset at the interface, the polarization induced charge density, the dielectric constant of AlGaN are denoted by E_D,ΔE_C, σ_P, and ε_{AlGaN}, respectively.

$$n_s(x) = \frac{\sigma_P(x)}{e} - \left(\frac{\varepsilon_0 \varepsilon_{AlGaN}(x)}{de^2}\right)\left(e\phi_b(x) + E_F - \Delta E_C(x)\right). \quad (2.8)$$

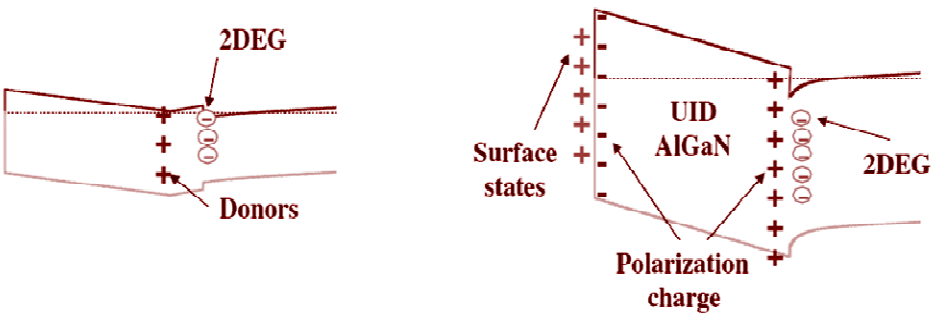
$$d_{critical=}(E_D - \Delta E_C)\left(\frac{\varepsilon_{AlGaN}}{e\sigma_P}\right). \quad (2.9)$$

The closed form of the expression of the 2DEG sheet carrier density is provided by substituting $d_{critical}$ into equation (2.10) to simplify the relationship between the critical barrier thickness of AlGaN and the 2DEG sheet carrier density. As the sheet carrier density increases the conductivity also increases since the conductivity formula, given in equation (2.11), represents that the conductivity increases in direct proportion to the increase of the sheet carrier density. In this equation, e is the electron charge and $\mu_n$is the electron mobility in the 2DEG channel.

$$n_s = \frac{\sigma_P}{e}\left(1 - \frac{d_{critical}}{d}\right). \quad (2.10)$$

$$\sigma = en_s\mu_n. \quad (2.11)$$

As it is mentioned previously, the formation of the sheet charge for the AlGaN/GaN heterostructure is due to the large spontaneous and piezoelectric polarization-induced field and large conduction band offset. 2DEG caused by built-in field occurs at the AlGaN/GaN interface without requiring a doping. However, in the case of GaAs based HEMT, intentional doping is required to form charges at the interface of AlGaAs/GaAs HEMT. Figure 2.4 indicates the energy band diagrams of GaN based and GaAs based HEMT devices.



(a) (b)

Figure 2.4 Energy band diagrams of (a) GaAs based and (b) GaN based HEMT devices.

Quality of the epitaxial layer also plays an important role in formation of 2DEG channel. The quality of the surface donor states is quite dependent to the quality of the AlGaN layer grown on top of a GaN layer. Hence, the quality of epitaxial layers grown on silicon carbide (SiC) substrate is an important criterion, which should be considered carefully. In the subsequent section, the heteroepitaxial layers are examined by pointing out what makes the quality of the material better.

2.2 Heteroepitaxial Growth Using MOCVD

In this subsection, the epitaxial growth of our AlGaN/GaN HEMT wafers using MOCVD system is overviewed. The epitaxial growth of high quality AlGaN/GaN HEMT wafers on SiC substrates has historically been a challenge to succeed. In principle, the epi-layer structure is optimized to grow a thin AlGaN layer on top of a semi insulating GaN layer during the heteroepitaxy growth process. The operating principle of FETs relies on the basis of the flow of electrons from source to drain by applying a positive bias voltage on the drain. The gate controls the current through the channel region. When the channel between source and drain is completely depleted at which the current

flow between these electrodes is fully blocked, the channel is pinched off. This operation principle is valid for all types of FETs. For conventional MOSFETs, the channel can be pinched off by annihilating the channel conductivity at the base layer with opposite type of conductivity to the source and drain regions by charge inversion [18]. However, the base layer conductivity type has to be opposite to the channel or semi insulating in order to get a fully depleted channel for other types of FETs [18]. As a result, a semi insulating substrate layer is selected not to degrade the RF performance of the device.

Before starting to the growth of layers, a suitable semi insulating substrate is needed to be identified. SiC has been traditionally used as substrates due to its high thermal conductivity, while sapphire and Si are also utilized as substrate materials because of their low cost [19],[20],[21]. Semi insulating 6H-SiC is employed as a substrate during our wafer growth due to its superior material properties like excellent thermal conductivity (>330 W/m.K at 300 K), low lattice mismatch (3.4%), and comparatively low thermal expansion coefficient (TEC) mismatch (25%) [22]. For high power densities, the high thermal conductivity of SiC substrates is much more advantageous than the other substrate materials, minimizing self-heating effect.

After the selection of the substrate material, a resistive AlN nucleation layer with a thickness of 10 nm is introduced to isolate device from the SiC substrate. A 120 nm thick high temperature (HT) AlN, a 2.6 µm thick GaN buffer layer stack and an undoped AlGaN barrier layer with 20% Al composition with a thickness of 20-25 nm are grown on the AlN nucleation layer, respectively. The epitaxial layer also includes 1nm thick AlN spacer between GaN buffer layer and AlGaN barrier layer and 3-5 nm thick GaN cap layer after the barrier. Schematic cross section of epitaxial layers is provided in Figure 2.5.

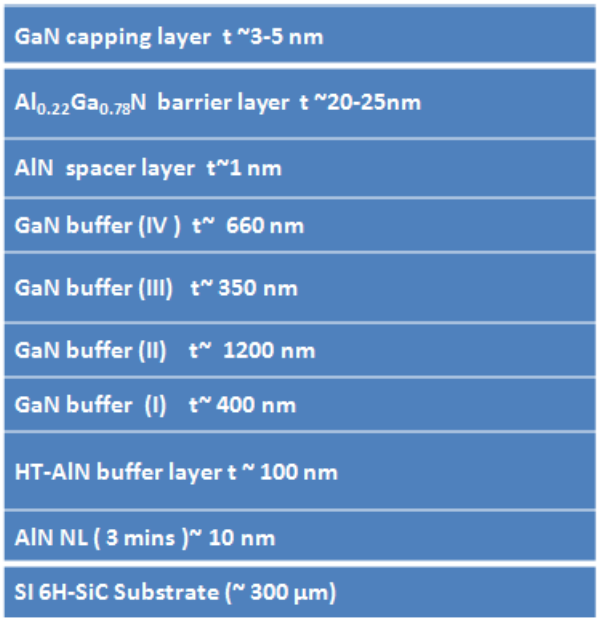


Figure 2.5 Schematic cross section of B-2323 epitaxial layers with related thicknesses.

As mentioned previously, the epitaxial layer growth begins with nucleation layer on top of semi insulating 6H-SiC substrate layer. High lattice mismatch between the substrate and GaN buffer layers increases surface roughness, causing a low quality HEMT structure. Thus, the resistive AlN nucleation layer is used to decrease the density of threading dislocations in the GaN buffer layer. AlN nucleation layer comprises small crystallites which decreases defects in the high temperature GaN buffer layer. Reduction in the number of defects enhances the quality of the surface [23].

The next epitaxial layer is GaN buffer layer. High quality GaN Buffer layer with low defect density and high resistivity is desired to prevent charge trapping of 2DEG electrons. The essential influence of trapping on device performance is to diminish the output power because of producing current collapse [24]. Buffer leakage, which is the other performance limiting factor, can be minimized in case of having a high quality GaN layer. To obtain sharp pinch-off characteristics and high 2DEG mobilities, GaN buffer layer, resulting in smooth AlGaN/GaN heterojunctions, should be optimized. The enhancement of device

performance with GaN buffer layer thickness (approximately 2600 nm) is due to the reduction of defects from SiC substrate and AlN nucleation layer [GaN buffer]. SiC substrate with a thicker crack free GaN buffer layer is promising for high power applications via the enhancement of breakdown voltage [25].

After completing the growth of GaN buffer layer, a ultra thin 1 nm thick AlN spacer layer is grown between GaN buffer layer and AlGaN barrier layer to enhance electron mobility. Two dimensional electron gas (2DEG) is formed at the interface of the buffer layer of GaN and the wide bandgap AlGaN material. The presence of such a spacer layer would decrease the Columbic scattering caused by the electrical interaction between the 2DEG electrons and their ionized atoms in the barrier layer, presenting a better confinement of the electrons in the 2DEG region. The thickness of this layer is optimized according to the electron velocity and the mobility by decreasing impurity scattering [26]. Dislocations, defects, roughness of AlGaN/GaN interface, and different scattering mechanisms lead to decrease in the electron mobility of the 2DEG. In order to obtain high quality of the AlGaN/GaN heterostructures, special attention should be paid on the critical transport parameter which is the 2DEG mobility. The electron mobility of 2DEG goes up to above 1500 $cm^2V^{-1}s^{-1}$ by enhancing the quality of the layer with AlN spacer layer.

Growth of AlN spacer layer is followed by AlGaN barrier layer growth. A 20- 25 nm thick AlGaN barrier layer is grown on top of the spacer layer to form a quantum well at the interface of AlGaN/GaN utilizing from the bandgap difference between these wideband gap materials. AlGaN layer supplies charge for 2DEG forms a Schottky-gate barrier as well. Depending on the Al mole fraction in the AlGaN layer, the optimal 2DEG thickness has been reported in the order of 2-3 nm [27]. The density of 2DEG depends on the thickness of AlGaN layer and Al mole fraction in this layer [28].

A 3 nm thick GaN capping layer is the final epitaxial layer that is suggested to improve the device performance. In addition, GaN capping layer can be employed to further increase the maximum transconductance (g_m), saturation

current (I_{ds}), current gain cutoff frequency (f_t) and maximum oscillation frequency (f_{max}) [29],[30]. Interface roughness scattering can be decreased by making GaN cap layer thicker. Increasing the GaN cap layer thickness alleviates the sheet density of 2DEG and increases the 2DEG electron mobility by causing a larger separation between the 2DEG electrons and AlGaN/GaN hetero-junction [31] .

2.3 Wafer Characterization

We have mentioned the epitaxial layers of AlGaN/GaN HEMT devices and their functions so far. The next part of this chapter is devoted for MOCVD growth and characterization process which are performed in NANOTAM. AIXTRON RF200/4 RF-S MOCVD system is used to grow the epitaxial layers of our GaN HEMT devices as shown in Figure 2.6 and Figure 2.7.

Deposition of epitaxial structures of III-V group materials needs high growth temperatures around 1000-1100°C [32]. MOCVD growth is the most suitable growth technique since it provides thermodynamically favorable growth process allowing high temperature growth. Besides, fast growth time (a few microns per hour), mass production capability (multi-wafer growth) and high quality of epitaxial layers are the other advantageous features of MOCVD growth in comparison to Molecular Beam Epitaxial (MBE) growth [33], [34], [35].

To mention briefly about AIXTRON RF200/4 RF-S MOCVD system with a 1x2” horizontal reactor (see Figure 2.6) used in NANOTAM, gas pipelines, mass flow controllers, pressure gauges and water pool that consists of metal-organic sources take place inside of the blue cabinet as indicated in Figure 2.7 (a) and Figure 2.7 (c). MOCVD system hardware is controlled by a computer program as shown in Figure 2.7 (d). During the growth process, harmful gases

and spinoffs can be created and cleaning mechanism of the MOCVD wipes out these gases via acid solution as given in Figure 2.7 (b).

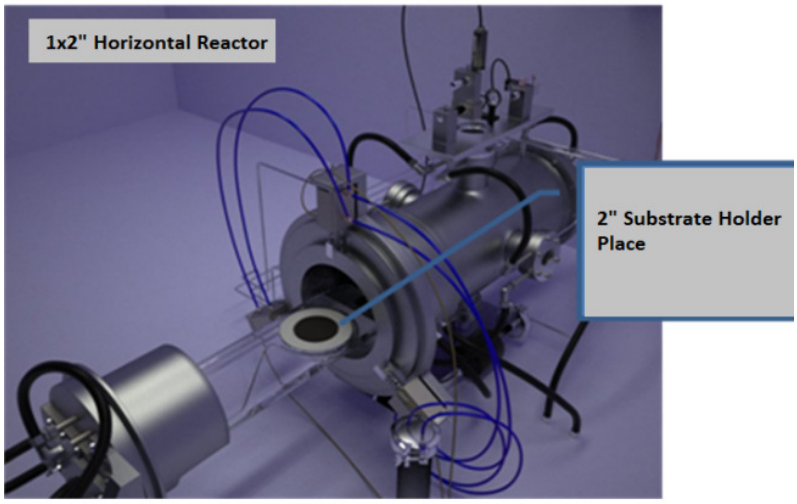


Figure 2.6 The detailed view of 1x2" horizontal reactor.

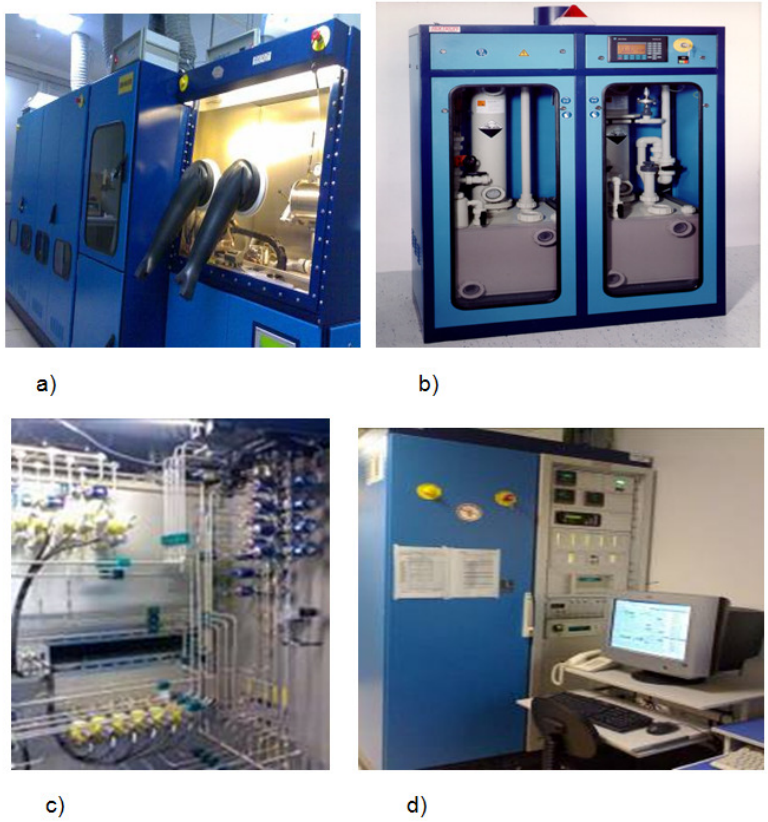


Figure 2.7 Bilkent NANOTAM MOCVD System.

MOCVD growth process begins with cleaning of the substrate material, which is SiC in our case. Since cleanness of the MOCVD reactor is very important since it changes layer quality and crystalline orientation. However, substrate material is very sensitive to physical and chemical cleaning techniques applied. Under hydrogen flow and at high temperatures (1000-1200^{o}C), a set of chemical cleaning techniques is put in MOCVD growth process that is very crucial step before starting the growth process.

Thin film growth is performed by MOCVD, using the pre-cursors trimethylgallium (TMGa), trimethylaluminum (TMAl), and ammonia and hydrogen and nitrogen carrier gases. After completing cleaning process, desorption under hydrogen flow is carried out at around 1100°C for 10 minutes. Finally, the growth conditions are ready for the first thin layer growth. After 20 seconds nitridation process by using NH_3 gas source, AlN nucleation layer growth on SiC substrate gets started at 500°C. It continues at a temperature of 750 °C, TMAl flow is adjusted at 15 sccm, NH_3 flow is set 200 sccm and growth pressure is 50 mbar for 3 minutes. As a result AlN thickness is obtained around 10 nm. In pursuit of nucleation layer growth, the growth conditions are altered for the growth of following high temperature (HT) AlN buffer layer. Reactor temperature and pressure are adjusted as 1130°C and 25 mbar, respectively while the settings of source gases are changed to 20 sccm of TMAl flow and 50 sccm of NH_3 flow. The resulting HT -AlN layer thickness is obtained approximately 100 nm.

Afterwards, the growth of AlGaN/GaN HEMTs proceeds with the first GaN buffer layer growth at 1050 °C. The growth pressure is kept at 200 mbar for all of the GaN buffer layers. TMGa flow and NH_3 flow are set at 10 sccm and 1300sccm for the first desired GaN buffer layer. A 400 nm thick GaN (I) buffer layer is grown with these growth settings. The following GaN (II) buffer layer is grown at 1060°C with 1500 sccm of NH_3 flow while the other growth parameters are kept constant. A 1.2 µm thick GaN buffer layer is deposited on top of the first GaN buffer layer with a 1.21 µm/hour growth rate. The next GaN

(III) buffer layer is deposited by increasing the growth temperature gradually from 1060 °C to 1075 °C. As TMGa flow is increased slowly from 10 sccm to 17 sccm, NH_3 flow is increased up to 1800 sccm. The calculated thickness for the third buffer layer is around 350 nm. GaN (III) buffer layer is followed by GaN (IV) buffer layer growth which is at 1075 °C with 17 sccm of TMGa flow and 1800 sccm of NH_3 flow, respectively. The thickness of this last GaN buffer layer is obtained 660 nm with a 2.01 μm/hour growth rate.

The posterior growth is performed at 1100°C growth temperature and 50 mbar growth pressure to get a 1 nm thick AlN spacer layer. TMGa flow and NH3 flow are set at 10 sccm and 200 sccm to achieve a 1 nm thin layer thickness. After the deposition of this intermediate layer, AlGaN barrier layer with 20% Al composition is deposited to form the 2DEG region. TMGa flow, TMAl flow and NH_3 flow are adjusted as 5 sccm,10 sccm and 500 sccm for 125 seconds, respectively. All the other growth parameters are not changed. Thickness of AlGaN barrier layer is around 20-25 nm. Eventually a GaN cap layer with a thickness of 3-5 nm is grown on top of the barrier layer by keeping the last used parameters same and only disabling the TMAl source flow. The in-situ characterizations of the grown epilayers are provided by the optical reflectance measurements. Crystal quality, thickness and growth rate are analyzed from the reflectance measurements using LaytecEpiSense system. Optical reflectance measurement result of B-2323 HEMT wafer is given in Figure 2.8. These measurements can be made easily and accurately in near real time during the process run. Besides, MOCVD grown layers can be calibrated through optical reflection method.

Determination of growth rate based on reflection measurements is made by employing the following equation below where λ is the wavelength of the optical probe, n is the material index and τ is the oscillation frequency.

$$\text{Growth Rate (GR)} = \frac{\lambda}{2n\tau} \tag{2.12}$$

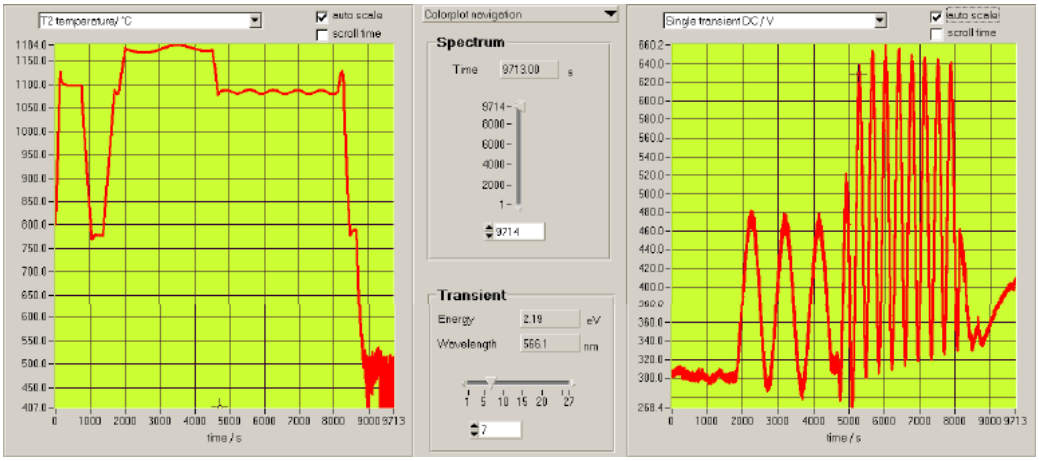


Figure 2.8 Optical reflectance measurement results of B-2323 HEMT wafer.

Optical reflectivity measurements indicate whether the structure has a high quality crystal and low surface roughness, or not. To explain the reflectance profile provided in Figure 2.8, this optical reflectivity measurement begins with the GaN buffer layer deposition at t=0 seconds. Then, a dip in the intensity of the optical reflectivity is observed at the first part of AlGaN barrier layer growth. Afterwards, the intensity starts to increase implying lateral growth of the layers. Finally, the surface with optically low roughness is obtained during the Quasi-two-dimensional (2D) growth. Furthermore, no significant change is observed in the amplitude of reflectivity and the average intensity of the oscillations during this Quasi-two-dimensional (2D) growth.

Further characterization efforts should be made for the deposited structures to determine the quality of the growth process. Atomic force microscope (AFM) provides the map of the surface morphology of the epitaxial layers. A Veeco di CP-II multi-mode AFM characterization system is used to get contact-mode AFM scan graphs of the HEMT structures in Bilkent University, NANOTAM. Photograph of the AFM characterization system and the AFM graph of B-2323 MOCVD growth are shown in Figure 2.9 and Figure 2.10, respectively.

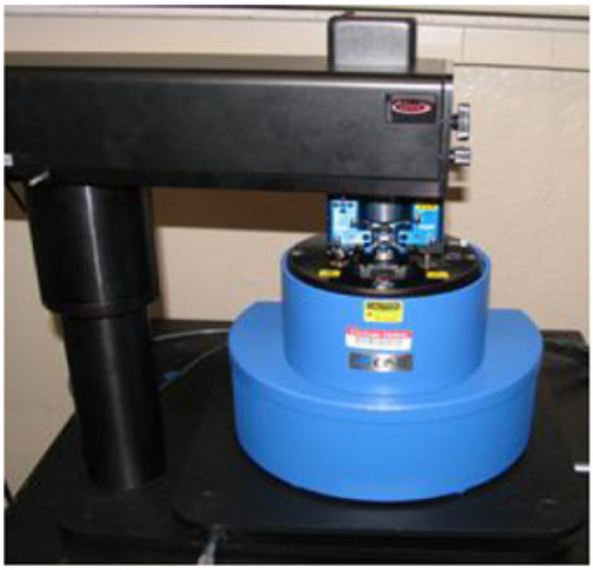


Figure 2.9 Photograph of the AFM characterization system in NANOTAM.

In Figure 2.10, RMS surface roughness value of the grown epitaxial layer is found to be 0.48 nm. In literature, this value is given in the range of 0.2 -0.6 nm [36], [37].

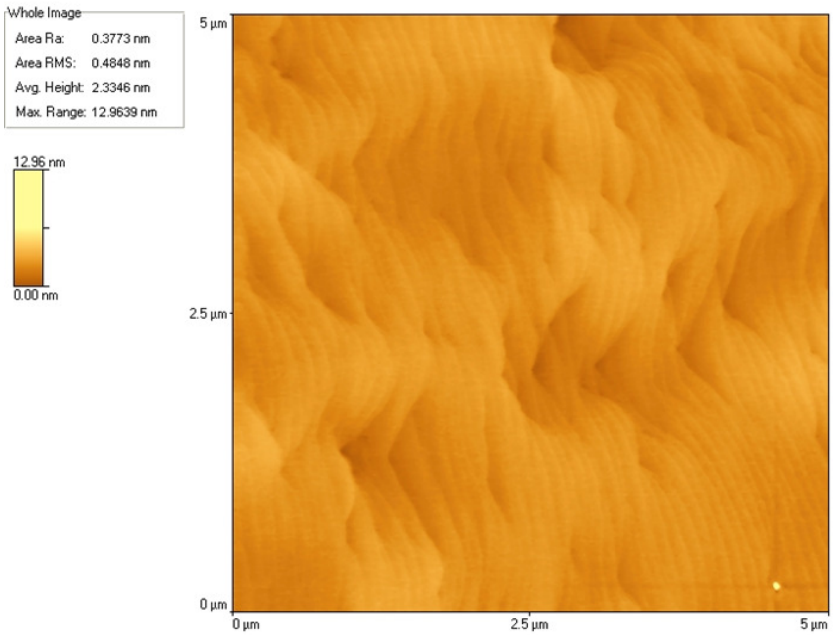


Figure 2.10 Contact-mode AFM scan graph of B-2323 and its RMS surface roughness value is 0.48 nm.

To evaluate the crystal quality of Bilkent University NANOTAM growths and determine the alloy composition of these growths, GaN and AlGaN epilayers are utilized from X-Ray diffraction (XRD) measurements. X-Ray diffractometer can be used in many ways like measuring the spacing between layers, determining the crystal structure and measuring the size, shape and stress of crystalline regions [38]. The principle idea behind XRD method can be explained in a way that the atomic planes of a crystal lead to an incident beam of X-rays to interfere with one another as they go out of the crystal. The phenomenon is called X-ray diffraction (XRD) [39],[40]. In NANOTAM, a Rigaku Smartlab XRD measurement system is used for XRD characterizations. Thin films that are grown by using MOCVD system are examined in terms of the quality of the crystal and rate of material compositions (AlGaN, AlInN, InGaN etc.) through XRD measurements. Peak shaped intensity profiles in XRD determine the growth characteristics. Peak position, peak width, peak intensity values are very deterministic parameters during the XRD measurements. XRD measurement results for our AlGaN/GaN heterostructure are provided in Figure 2.11.

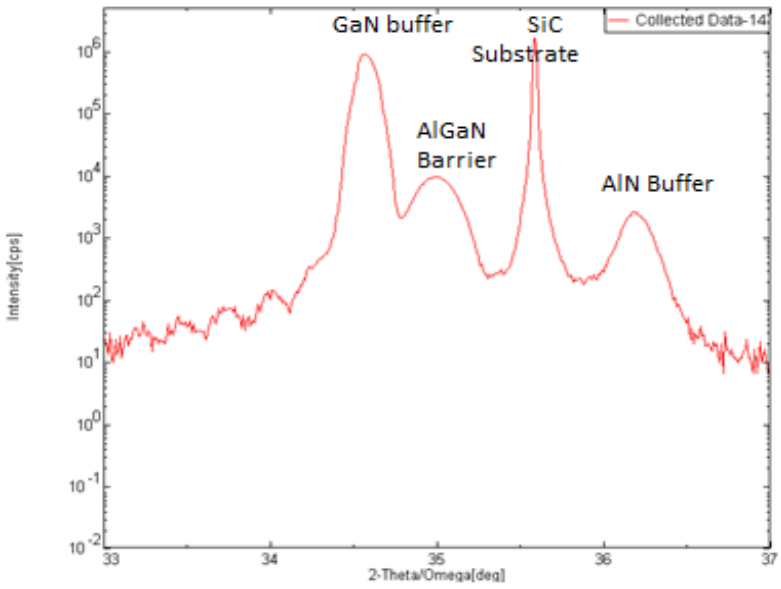


Figure 2.11 XRD Measurement Results for the AlGaN/GaNheterostructures: Intensity vs. Bragg Angle Graph.

Thin Epilayer	FWHM Value (arcsec)		FWHM Value (arcsec) in Literature [41],[42],[43],[44]
AlN Buffer	Symmetrical Axis (002)	320	200-600
	Asymmetrical Axis (102)	1800	200-3200
GaN Buffer	Symmetrical Axis (002)	173	100-400
	Asymmetrical Axis (102)	284	200-500
AlGaN Barrier	Symmetrical Axis (002)	302	300-500

Table 2.2 Comparison of FWHM values of AlN buffer, GaN buffer and AlGaN barrier layers with the FWHM values (arcsec) given in the literature.

In Table 2.2 given, FWHM values are provided for AlN buffer, GaN buffer and AlGaN barrier layers. These values are compatible with the values shown in the literature. Thus, it is understood that Bilkent University NANOTAM can grow the high quality of thin epilayers.

GaN material quality can be also defined by Photoluminescence (PL) measurements. A Jobin Yvon Triax 550 CCD photoluminescence system is used in Bilkent University NANOTAM. The schematic illustration of PL measurement setup is given in Figure 2.12. Photoluminescence is the optical emission created by photon excitation and it is a widely used characterization method in III-V semiconductor materials [45],[46]. In this setup, photon excitation of the GaN material is made by: 1-325 nm HeCd and 2-246 nm NeCu70 DUV lasers.

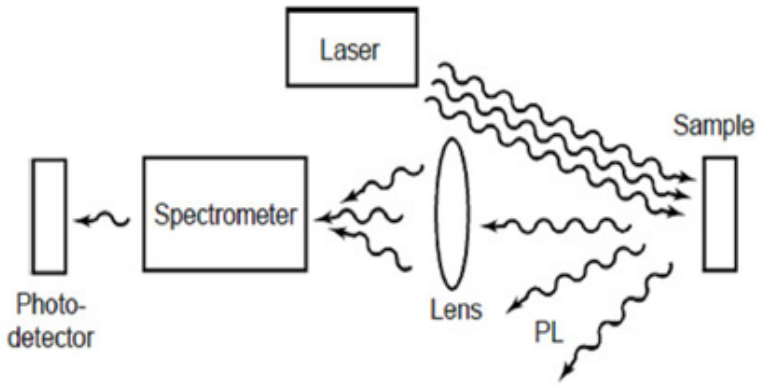


Figure 2.12 Schematic of the Photoluminescence (PL) measurement setup.

Photon excitation of the GaN is made by focusing laser beams on the sample and the sample emits photons if the energy of photons coming from the laser source is greater than the semiconductor energy bandgap (E_g). For Bilkent University NANOTAM grown B-2323 wafer, PL measurement result of GaN buffer layer of the B-2323 wafer is provided in Figure 2.13 with a peak photoluminescence at a wavelength of 361.5 nm.

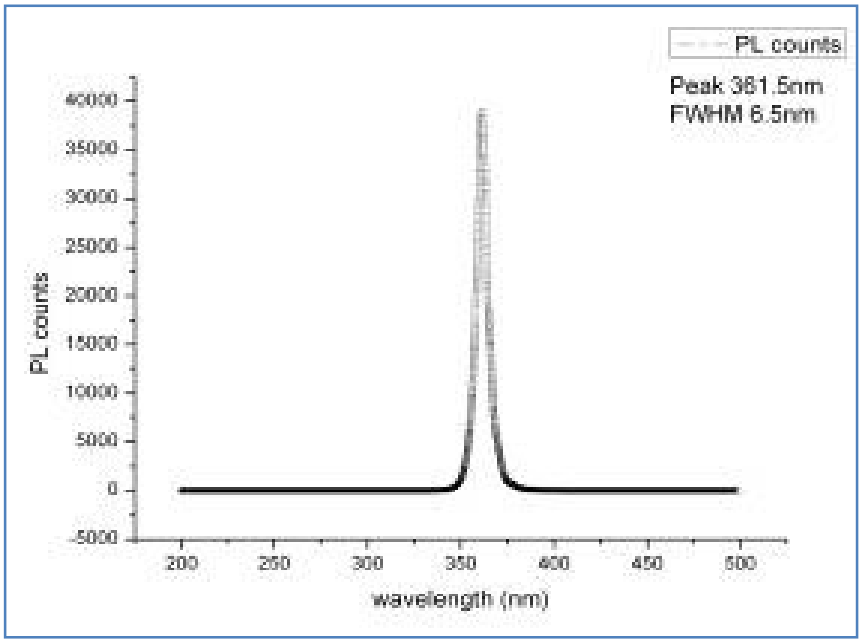


Figure 2.13 PL measurement result of GaN buffer layer of the B-2323 wafer.

To achieve the electrical characterization of the HEMT structures, Hall Effect measurements are performed to measure the mobility (μ_n), the resistance of the semiconductors, and the 2DEG charge carrier density (n_s). The ohmic metal contact pads (Ti/Al/Ni/Au metal stack) are needed to be able to make measurements on the epitaxial layer. These ohmic pads are deposited on the corners of the thin films that are grown in NANOTAM. After forming the required contact pads, the electrical characterization of the epitaxial layers grown in NANOTAM are made using an ECOPIA Hall Effect Measurement System (HMS) 3000 (see Figure 2.14)

Figure 2.14 ECOPIA Hall Effect measurement system (HMS) 3000 in NANOTAM.

Sheet carrier concentration is determined by measuring the magnitude of the Hall Voltage (V_H) and the van der Pauw method is applied to measure the bulk resistivity of the sample [47].To determine the Hall voltage, a current is forced through the opposing pair of ohmic contact pads 1 and 3 that are shown in Figure 2.15 and the Hall voltage V_H (= V_{24}) is measured across the pair of contacts 2 and 4. Schematic representation of a van der Pauw configuration is given in Figure 2.15. The sheet carrier density (n_s) can be found by using the

equation (2.13). In this equation, I is the current, B is the magnetic field, and e (= 1.602×10^{-19} C) is the elementary charge.

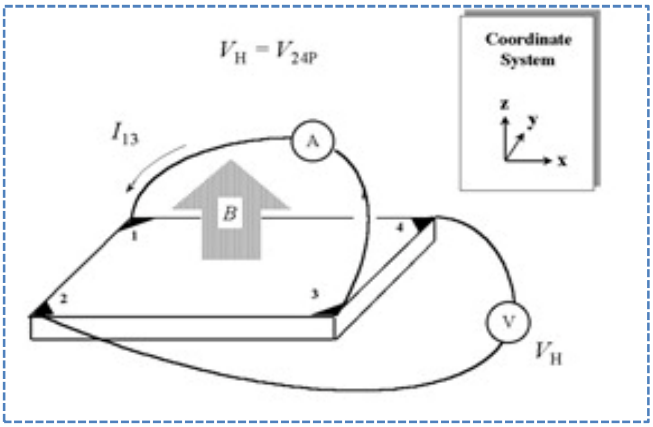


Figure 2.15 Schematic representation of van der Pauw configuration [47].

$$n_s = \frac{IB}{e|V_H|} \tag{2.13}$$

$$R_A = V_{43}/I_{12} \;\&\; R_B = V_{14}/I_{23} \tag{2.14}$$

$$\exp\left(-\pi \frac{R_A}{R_{sheet}}\right) + \exp\left(-\pi \frac{R_B}{R_{sheet}}\right) = 1 \tag{2.15}$$

R_A and R_B are the characteristic resistances which can be calculated by using the equation (2.14). To find the sheet resistance value, the set of equations (2.13), (2.14), (2.15) are gradually provided. If the thin film thickness is known, the bulk resistivity (Ω.cm) can be calculated by using the equation (2.16) given below.

$$\rho = R_{sheet} \times t \tag{2.16}$$

A sheet resistance of 229 Ohms per square is calculated for of B-2323 GaN HEMT structure. If the sheet resistance and sheet carrier concentrations are known, the mobility can be calculated by using the equation (2.17) given below.

$$\mu_n = \frac{1}{e\, n_s R_{sheet}} \tag{2.17}$$

The Hall Effect measurement results of Bilkent University NANOTAM GaN based HEMT structures are compatible with the presented results in literature [41],[42],[43],[44] (see Table 2.2). A Typical AlGaN/GaN HEMT structure has a sheet carrier density of 1-2x$10^{13}$$cm^{-2}$, a carrier mobility of 1000-1700 cm^2/V.s and a resistivity of 3-5x10^{-2} Ω.cm as shown in Table 2.2. A sheet carrier density of 1.7x10^{13} cm^{-2}, a carrier mobility of 1594 cm^2/V.s and a resistivity of 2.29x10^{-2} Ω.cm are obtained from B-2323 HEMT structure.

2.4 Transistor Mask Design Considerations

In this chapter, the main goal is to explain HEMT design considerations by pointing out which device parameters affects device characteristic at which way. There are several basic FET configurations which are also examined for HEMT devices. While designing our HEMTs, the interdigitated FET approach is taken into account. In this configuration there are several gate fingers that are fed from the same gate pad. This approach helps to minimize device area with paralleled many gate fingers by allowing a large amount of total effective gate width. The HEMT structure we proposed is depicted on Figure 2.16. Since we use coplanar waveguide (CPW) elements in our MMIC designs, our HEMT structures are needed to be compatible with CPW passive elements. Also, in our designs we used common source HEMTs so source sides of the HEMTs are designed as ground pads (see Figure 2.16).

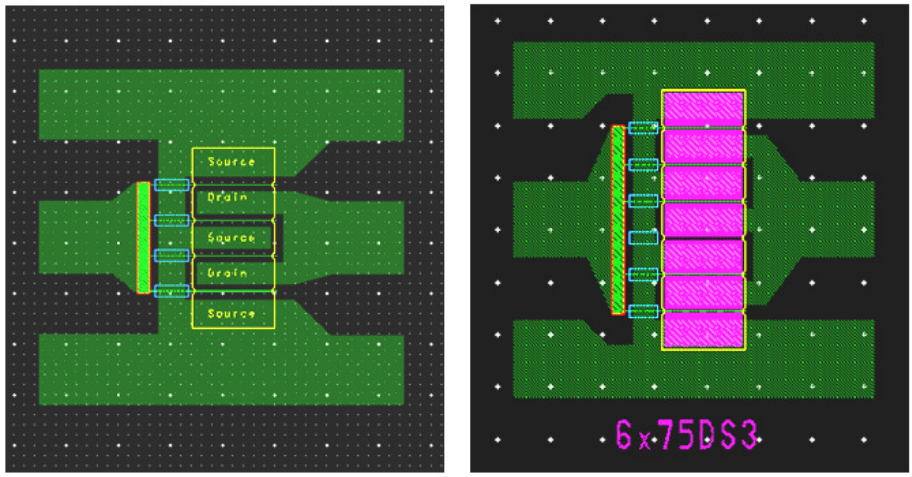


Figure 2.16 Typical layout for a 4x75µm HEMT a) showing the drain and source pad areas b) showing the final layout with ohmic contact metals.

Our active device mask involves transistor layouts with different periphery devices. A large periphery devices is more advantageous than a smaller periphery device in terms of high output power, however, maximum available small-signal gain of large periphery device is smaller than a smaller periphery devices. Number of gate fingers (n), unit gate finger width (W_{gu}), gate length (L_g), total gate width (W_g), gate-source spacing (L_{gs}), gate-drain spacing (L_{gd}), drain-source spacing (L_{ds}) and gate-to-gate pitch length (L_{gg}) are deliberately important parameters while designing the mask layout (see Figure 2.17).

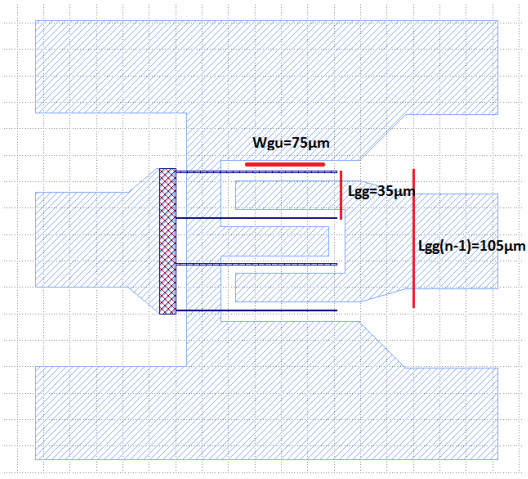


Figure 2.17 Layout of a 4x75µm HEMT with the parameters Wgu, Lgg and Lgg(n-1).

Shrinking the gate length is the essential design method while operating at high frequencies. However, the short channel effect is to be thought as reducing the effective gate length. Short channel limitation on high frequency gives rise to a design rule based on the ratio of gate length (L_g) and the potential barrier thickness (t_{bar}) to eliminate the short channel effects. The minimum limit of the reported aspect ratios (L_g/ t_{bar}) change 6 to 15 not to suffer from the short channel effects for AlGaN/GaN HEMTs with a gate length of larger than 0.1µm [48],[49], [50]. This ratio is determined according to the application. For power applications, large aspect ratios are desired not to degrade the device performance. To decrease the gate-source and gate-drain capacitances, the gate length should be carefully reduced by concerning the reported aspect ratios. Hereby current-gain cutoff frequency (f_t) and maximum oscillation frequency (f_{max}) are increased by decreasing parasitic capacitances i.e., gate length, as stated in equation (2.18). The posture given in equation (2.18) shows that f_t values are highly dependent on effective gate length, including fringing field gate length and effective electron velocity.

$$\mathbf{f_t = \frac{v_{eff}}{2\pi L_{g-eff}} = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \propto f_{max}} \qquad (2.18)$$

Maximum drain current is proportional with the ratio of gate width and gate length. In other words, choosing devices with large total gate width increases power capability of the HEMT.

To increase the drain current and the maximum transconductance, keeping the source-drain spacing as short as possible is required. However, the optimum source-drain spacing value should be carefully controlled not to suffer from increase in the parasitic gate capacitance since the gate capacitance increases as decreasing the spacing between source and drain [51],[52],[53] . Increase in gate capacitance causes reduction in current gain cutoff frequency and maximum oscillation frequency.

0.25µm gate length and 3 µm source-drain spacing are designated as optimum parameter values in our HEMT design. As gate-drain spacing increases, breakdown voltage goes up. Optimum gate-drain spacing (L_{gd}) and optimum gate-source spacing (L_{gs}) are specified as 1.6 µm and 1.4 µm, respectively. We have designed several multi-finger gate HEMT devices since selection of transistors should be made according to our design expectations. When power capability of the device is the prior concern in the design, relatively larger gate periphery devices can be a better option to meet the design requirements. Another parameter which affects device performance is the gate-to-gate pitch length. Gate-to-gate pitch length (L_{gg}), which affects channel temperature by changing thermal resistance value, is defined as 35 µm in our HEMT structures as indicated in Figure 2.17. While trying to make devices with a large number of gate fingers, gate-to-gate pitch length (L_{gg}) should be kept as large enough not to degrade device performance due to thermal issues. Increase in $L_{gg}(n-1)$ lead to decrease in gain by increasing the device periphery. Unit gate finger width (W_{gu}) has an impact on the gain of the device. Increasing unit gate finger width (W_{gu}) for the sake of power degrades gain performance of the device. For a 4x75 µm device, W_{gu} equals to 75 µm where 4 is the number of gate fingers. In photolithography transistor mask, there exists different transistors with different number of gate fingers, gate-to-gate pitch length and unit gate finger width. In addition to that gate length can be changed during fabrication process since gate length is determined during e-beam lithography and can vary from fabrication to fabrication. Optimum transistors are chosen according to the different design requirements, such as output power, gain, operating frequency, etc.

Photolithography mask is prepared using Advanced Design System (ADS) Layout utility by introducing the related layers like mesa, ohmic contact pads, gate pad metal, airbridges. The gates are written by using e-beam lithography so gates are defined by using e-line plus software tool. Alignment marks are introduced to align the mask while performing optical and e-beam Lithography.

Our HEMT mask is given in Figure 2.18 with TLM patterns, control HEMTs (2x100 µm) on the edges of the mask.

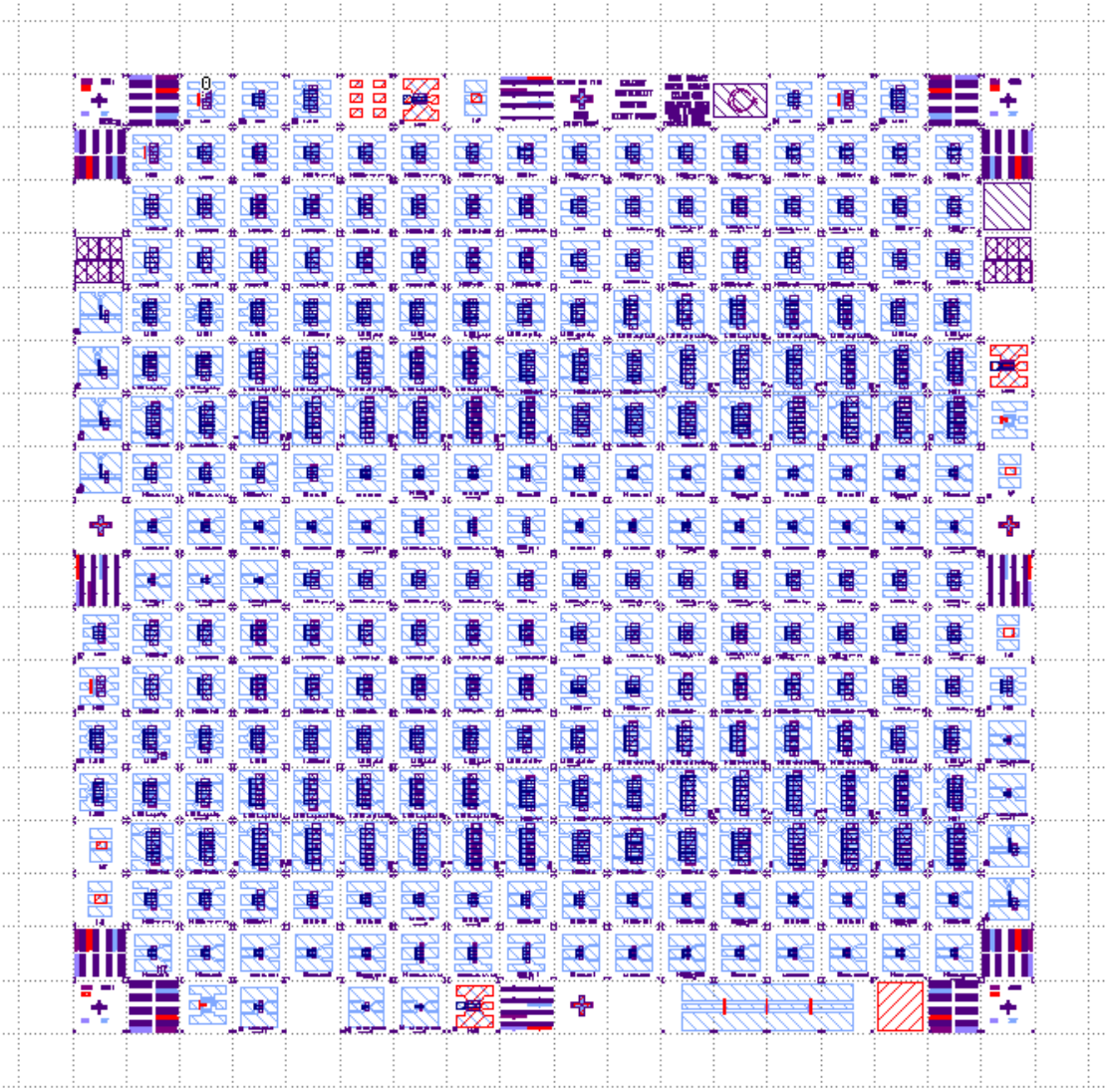


Figure 2.18 HEMT mask layout with alignment marks.

Chapter 3

MMIC Fabrication andCharacterization of GaN HEMTs

3.1 AlGaN/GaN MMIC Fabrication Process

This section is devoted for AlGaN/GaN MMICs fabrication steps. MMIC fabrication starts with wafer cleaning to remove undesired materials from the sample before going through the fabrication process literally. Maintaining the cleanliness is extremely important to avoid device failures since unwanted contamination on the sample can provoke pattern defects by causing electrical failures like shorts in capacitors or opens in the gate fingers. Starting from the beginning, cleaning process should be performed before each major fabrication steps during the device processing. Solvent cleaning is an effective method in removing residual organic contaminants. We employ acetone (CH_3COCH_3) as our organic solvent to prevent contamination on our samples; however, another cleaning step is needed to be taken due to the high evaporation rate of acetone. Therefore, after soaking samples in acetone and floating in ultra-sonic bath in a container filled with fresh acetone, we also use isopropyl alcohol ($CH_3CHOHCH_3$) solvent in order to avoid striations on samples. As the final cleaning operation, samples are required to be dried with nitrogen gas (N_2) so as to uniformly blow all the remaining solvent from the surface.

MMIC fabrication process consists of challenging fabrication steps like mesa isolation, ohmic contact metallization, resistor formation, Schottky contact metallization, first metal formation, partial and full device passivation (Si_3N_4), dielectric opening, airbridge post and interconnect metallization. Details of all of these fabrication steps are discussed in the following sub-sections.

The first major fabrication step in our process flow is the device isolation by mesa etching. The main goal in mesa isolation process is to isolate electrically conductive region of monolithic circuits from each other. Additionally it provides an electrically insulating surface for construction of all the passive elements on monolithic circuits since all the transmission lines, rectangular inductors, capacitors and pads on monolithic circuits need to be fabricated on nonconductive material. In active devices, mesa etching restricts the current flow to only the desired path. For the case of HEMT, the isolation pattern is provided since we do not want to have any current flow that does not pass under the gate metal. If the isolation is not good enough, unwanted current flow occurs causing a parasitic resistance that will degrade the RF performance of our MMICs. Gate pad of the HEMT is excluded from the active pattern in order not to decrease the RF performance of the HEMT with the increased parasitic gate pad capacitance. Therefore, use of Mesa isolation is an effective way to reduce undesirable parasitic capacitances and resistances. A $CCL_2 F_2$ based ICP-RIE (inductively coupled plasma-reactive ion etching) technique is used for etching. The layer to be etched, which is defined by photolithography, is removed by ion bombardment using this dry etching technique. The etch rate for the mesa isolation is 1nm s^{-1} at RF power levels of 200 W. We set the flow rate of the plasma at 20 sccm, the flow pressure at 8 μbar and the RF power level at 200 W. The depth of 2DEG region for a typical HEMT structure is approximately 40-45 nm from the surface of the sample. According to this depth, the mesa etch depth is chosen about 90 nm which is larger than the depth of 2DEG and it takes roughly 90-100 sec to constitute the desired etch profile. Finally we measure our mesa etch depth in order to verify our desired depth by the aid of a Dektak

profilometer which is a commonly used surface contact measurement technique. An etched mesa photograph is shown in Figure 3.1.

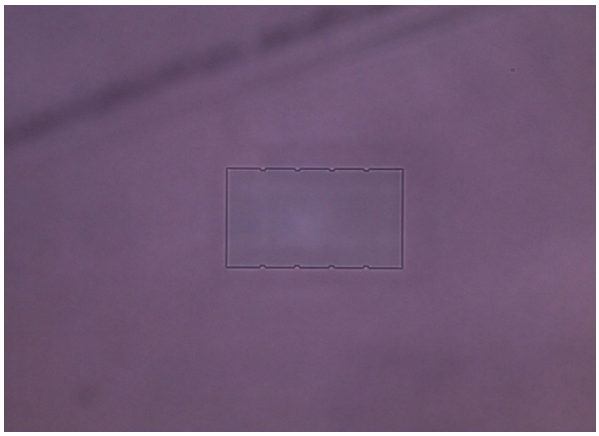


Figure 3.1 An etched mesa photograph.

The next critical fabrication step is ohmic contact metallization which is so important to HEMT devices. The aim of source-drain metallization is to allow current flow into or out of semiconductor. As opposed to Schottky gate contact, source and drain metallization obeys Ohm's Law (V=I*R). That is, ohmic contacts should have a linear I-V characteristic, low contact resistance (Rc), high thermal and electrical stability. In literature, typical ohmic contact resistance value of GaN based HEMT devices vary between 0.2-0.6 Ohm-mm [54],[55],[56],[57]. Contact resistance is related with ohmic metal to semiconductor junction and it has a significant contribution to the total parasitic source resistance in HEMT devices. Therefore, it should be as small contact resistance as possible not to suffer from the performance limiting effects of parasitic resistances. In HEMT devices we have a planar device structure and the contact resistance of a planar source and drain contacts constructed by the resistance between the metallization and an imaginary plane at the edge of the ohmic contact. High quality ohmic contact formation can be achieved by using the highly doped semiconductor to initialize the dominant conduction mechanism which is tunneling. Tunneling (field emission) mechanism occurs when the width of potential barrier decreases sufficiently. In order to have a

lower potential barrier width, doping concentration of the semiconductor should be high enough since the barrier width is inversely proportional with the square root of doping concentration. In our process, a metal stack of Ti/Al/Ni/Au is optimized according to metal thicknesses to achieve good contact metallization. The optimization of the Ti/Al ratio and thickness plays crucial role for ohmic contact fabrication. Basically, Titanium generates nitrogen vacancies in GaN and high n-type region reveals under the contacts due to these nitrogen deficiencies. However, Titanium can be easily oxidized so it needs a stable cap layer. In order to prevent oxidization in Titanium layer, Aluminum is proposed as a second metal layer. Al_3Ti alloy plays a significant role in the metal stack preventing oxidization. After Ti/Al bilayer metallization, two additional layers (Ni/Au) are proposed to increase the quality of the contacts. Nickel is deposited as a diffusion barrier between Al and Au metal layers in order to prevent the inter-diffusion of these two metals [58]. Finally, depositing highly conductive and protective layer of Au improves the quality of ohmic contacts. The basic principle behind the formation of this metal stack is that the interfacial reaction helps in decreasing the contact resistance [59],[60]. In our processes, photolithography techniques are used to define the ohmic contact areas. Before starting the photolithographic process, the mask is accurately aligned with the pattern on the wafer's surface. As a next step, the negative photoresist is exposed through the pattern on the mask with a high intensity ultraviolet light. Development processes applied as a last part of photolithographic process after the UV exposure. UV light makes negative resist more difficult to dissolve so developer solution removes only the unexposed regions. Afterwards, we used the e-beam evaporator to deposit a Ti/Al/Ni/Au metal stack. The related thicknesses for this ohmic contact stack is 150/1500/400/700 Å, respectively. After deposition of metals, the photoresist is dissolved using a solvent and eventually the metal stack deposited on top of the resist is lifted off so that the unwanted metal parts are removed. After all, multi-layer ohmic contact metal stack of Ti/Al/Ni/Au on n-GaN is annealed at temperature of 850^{o}C for 30 sec in a Rapid Thermal Annealer (RTA) to lower the specific contact resistance value.

An optic microscope photograph of the fabricated ohmic contacts is shown in Figure 3.2.

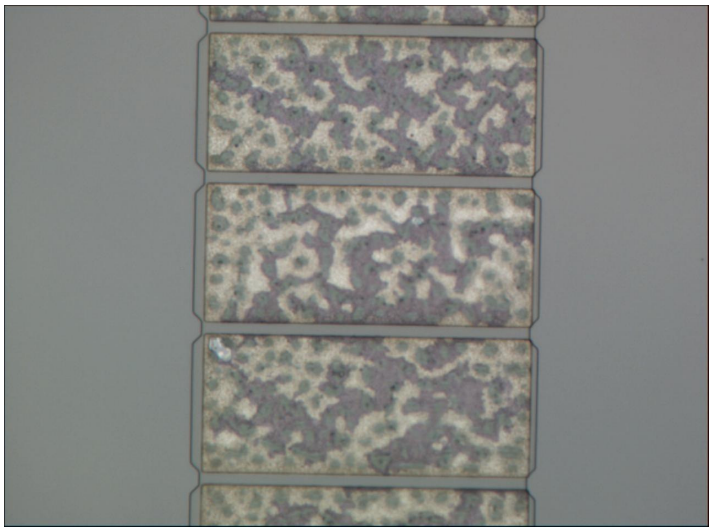


Figure 3.2 Ohmic contact metallization photograph

After ohmic contact metallization, the next step is formation of resistor (see Figure 3.3). Resistors are used in MMICs for many reasons including feedback, stabilization, isolation, self-biasing, terminations (power combiners) [61]. Ni-Cr is chosen as a suitable metal stack for synthesizing resistors. A sheet resistance of 15Ω/square is obtained from the fabricated Ni-Cr.

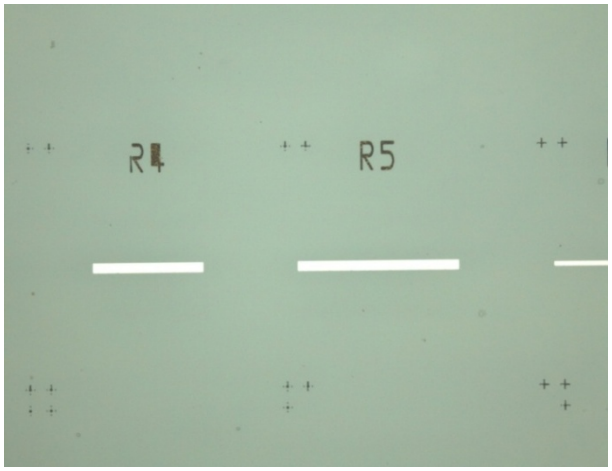


Figure 3.3 Fabricated Ni-Cr Resistor image

The Schottky gate formation is the other essential process in AlGaN/GaN HEMT fabrication after the ohmic contact formation. When a metal is placed in intimate contact with a large bandgap semiconductor (AlGaN), the junction shows a rectifying behavior for moderate doping levels. In the case of AlGaN/GaN heterostructure, the 2DEG channel occurs due to the strong strain induced piezoelectric polarization field in the AlGaN/GaN junction since polarization effects cause high carrier densities even in undoped structures. Therefore, the Schottky barrier can be made larger due to high polarization field in nitrides. There are a lot of dislocations in AlGaN/GaN heterostructures because of the lattice mismatch between the semiconductors. These dislocations under the gate metal lead to a large leakage current of AlGaN/GaN devices. The low gate leakage current through the GaN buffer is very important to obtain high breakdown voltage and high power efficiency. In order to guarantee a lower leakage current, a high Schottky barrier height is required. A high Schottky barrier can be constructed by using a metal with a large work function. Thermal stability is extremely important for Schottky contact so Ni does not react with GaN below 600°C which means Ni is a good material choice; however, it can be oxizidized easily. Therefore an additional Au metal layer is optimized to obtain high quality Schottky contacts. This second metal layer improves the conductivity of Ni and prevents oxidization. E-beam lithography technique is applied to form 0.25 μm gate contacts since it is a specialized technique for creating extremely fine patterns (~ 50 nm)[62]. The AlGaN/GaN substrate is coated with a thick layer of PMMA positive resist, which is chemically changed under exposure to the electron beam. Schottky metal thicknesses are 50nm and 250 nm for Ni and Au, respectively. Gate metals are coated by using e-beam evaporator system. The following figure demonstrates an optic microscope photograph of formed Schottky contacts (see Figure 3.4).

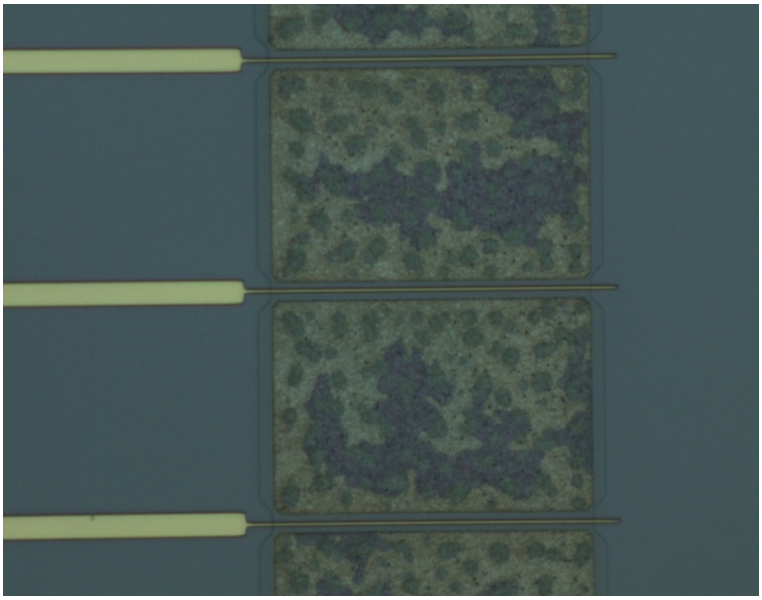


Figure 3.4 Photograph of fabricated Schottky contacts.

The next fabrication step is first-level metallization (see Figure 3.5). One major purpose of first metallization is to increase conductivity. The thicknesses of the ohmic and the gate metal are less than one skin depth so it is desirable to overlay ohmic and gate metal to obtain higher conductivity. First-level metal is also used to form lower plates of MIM capacitors. Our gates are defined using e-beam lithography so we have to conserve e-beam writing time by defining only the gate fingers, not the related pad areas. These pad areas are fabricated at first metallization process step, overlapping pads on the ends of the gate fingers [61]. Thickness 50/300 nm of a Ti/Au metal stack is evaporated.

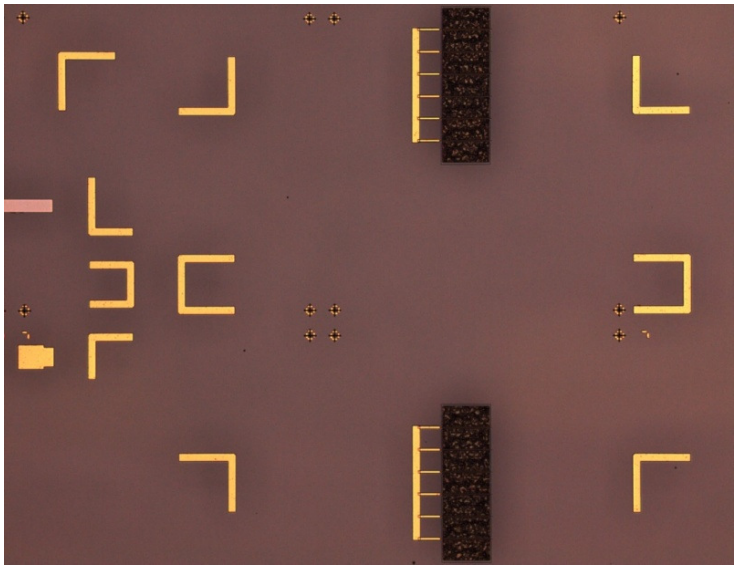


Figure 3.5 Photograph of fabricated first-level metallization.

The next process steps are considerably critical process steps which are SiN passivation and airbridge formation respectively. There are several effects of dielectric passivation layer. In particular, SiN passivation is an effective method to suppress negatively charged surface states [63]. This improves the DC and RF performance by increasing transconductance and decreasing resistance in the access region [64]. Theory behind negatively charged surface states comes from the enlargement of the gate depletion region. The gate depletion region becomes larger by contradicting the ionized positive donor density. This explains the existence of negative charges on the surface which is called as a virtual gate in literature [63]. A model of the AlGaN/GaN HEMT demonstrating the virtual gate formation and related band diagrams are provided in Figure 3.6.

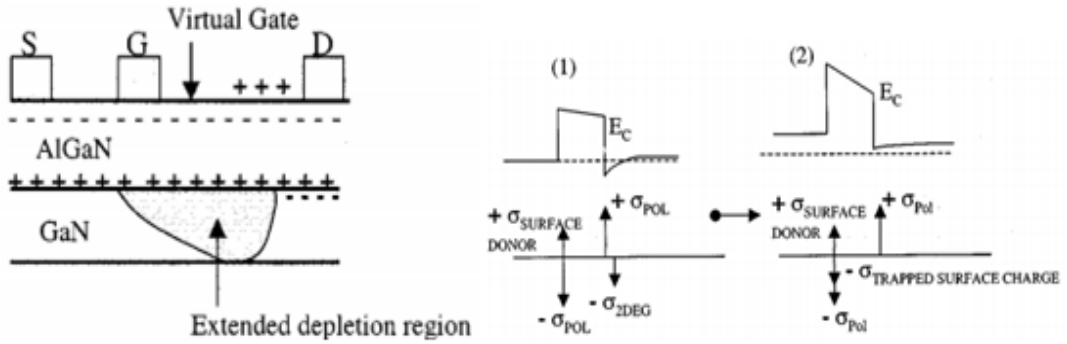


Figure 3.6 Virtual gate formation and the band diagrams (1) for a nonexistent virtual gate (2) for a negatively charged virtual gate [63].

The negative charges located on the surface extend the area of the depletion region but these charges are not able to respond fast enough at high frequencies [65], [66]. This can cause the dc-RF dispersion which means less RF current and lower output power especially at a higher drain bias voltage. In order to get lower dispersion, reducing ionization and charging of the surface is extremely important. Because of that, dc-RF dispersion also shows a significant dependence on the dielectric passivation. On the other hand, large relative dielectric constant causes a degrading effect by increasing the gate fringe capacitances and parasitic capacitances. Thus, the high dielectric constant of SiN leads to a decrease in the small signal gain dramatically by adding more gate fringing capacitances [49], [50]. In addition to this, there is another parameter that should be taken into consideration which is the thickness of the passivation layer. Power density and power added efficiency (PAE) decreases introducing a thinner passivation layer, however, a thick passivation layer lower the small gain and decrease the high frequency performance of the device [67].

Before passivation, our samples are carefully treated using ultrasonic acetone and isopropyl alcohol. A 300 nm thick SiN passivation layer is deposited with SiH_4:NH_3:Ar (300 sccm, 8 sccm, 50 sccm) by Plasma Enhanced Chemical Vapor Deposition (PECVD) at RF power of 20 W and at 300°C. This serves both for passivation and the insulator layer of the Metal-Insulator-Metal (MIM)

capacitance. Silicon Nitride is etched using CHF_3 at pressure of 0.4 Pa, flow rate of 60 sccm for 2.5 min in a RIE dry etch for dielectric opening (see Figure 3.7).

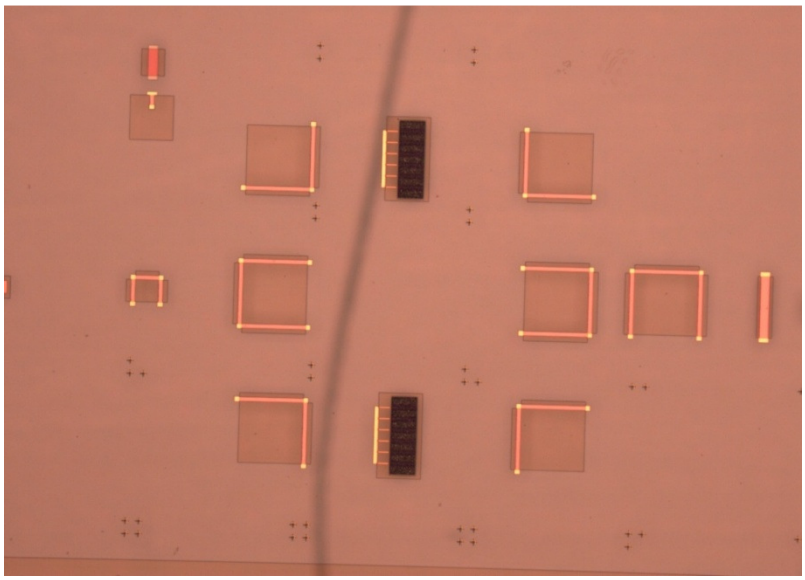


Figure 3.7 Photograph of fabricated MMIC after SiN passivation.

We have developed two alternative mask steps for passivation. The first one is that the dielectric opening is only realized in the active device and the Metal-Insulator-Metal (MIM) capacitance regions to fabricate the insulator layer. The second one and the last one is that the dielectric passivation exists everywhere except the intersection regions of interconnect metal and the first metal.

After the surface passivation of MMICs, the next step is the formation of air bridges. Airbridge post material lithography is applied and resist (S1828) is reflowed at 150 °C for 10 mins to strengthen the post material. The main purpose of the thermal reflow resist is to obtain ellipsoidal-shaped structures into the substrate to fabricate the airbridges. After metallization of the interconnect metals, AZ100 resist remover is used to remove the post material. Airbridges are used to connect isolated source pads in HEMTs. In addition, CPW ground lines are connected to each other via the first metal so that airbridge is needed to prevent contacts between the interconnect metal and the first metal. The illustrated photograph of airbridges is given in Figure 3.8.

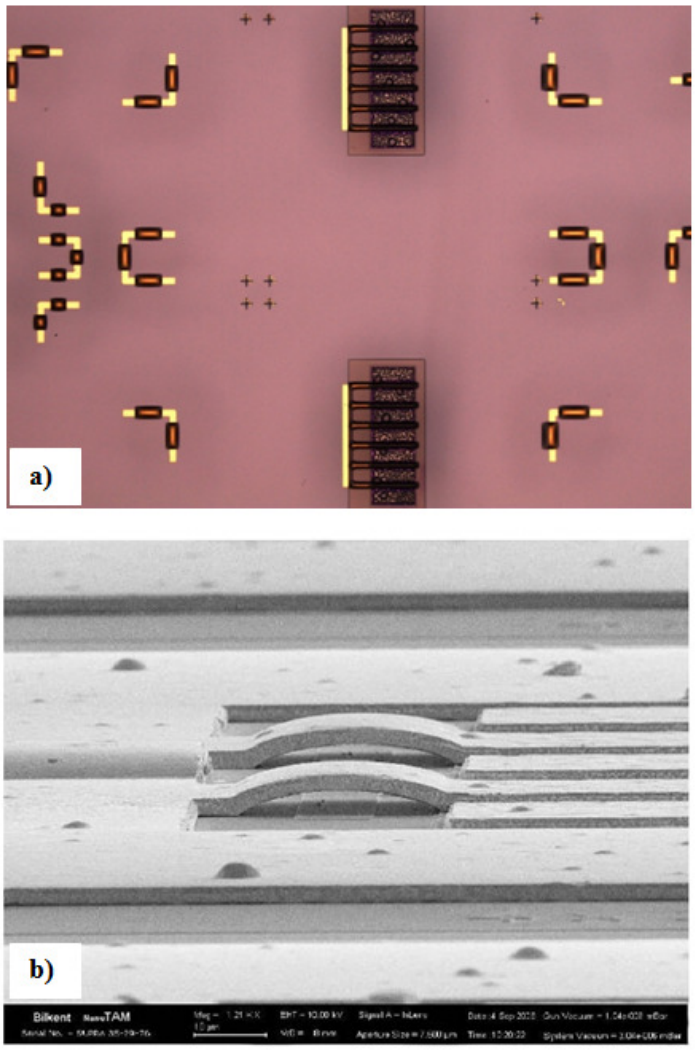


Figure 3.8 Photograph of the fabricated airbridges with a) a general view b) a zoomed view.

After the airbridge post material formation, the final process step is interconnect metallization or second level metal formation. This step is required to form interconnections on the integrated circuit. This metallization also serves for the upper metal layer of the MIM capacitors. Electroplating method was used for the second level metallization but removing seed layer was really hard stuff so e-beam evaporator is used to form the interconnect metals by using AZ nLOF 2070 photoresist. The metal thickness is around 2.2 µm. This thick metal layer takes some time so the photoresist is cooled down using wafer cooling mechanism of e-beam evaporator. Lift-off procedure is applied as a final step of

interconnect metal formation. A part of a fabricated MMIC with completed interconnect metallization is shown in Figure 3.9. As stated above, lift off process is followed by airbridge post material removal. Eventually MMICs are subjected to cleaning using ultrasonic acetone and isopropyl alcohol.

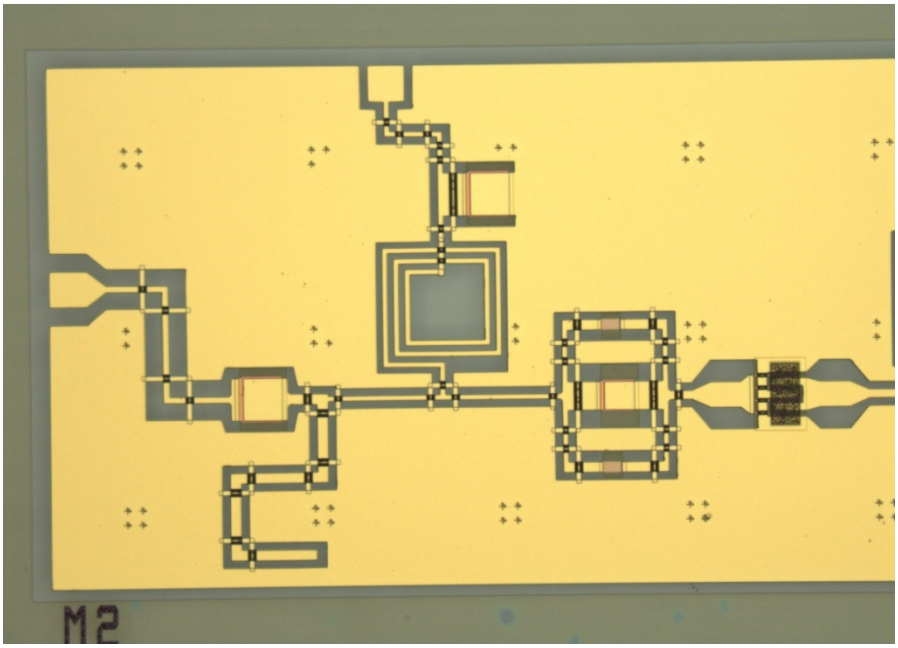


Figure 3.9 Photograph of the fabricated MMIC.

3.2 Electrical Characterization of GaN-based Active Devices

This section involves in major measurement methods for our GaN-based active devices. DC and RF characterization is required to evaluate process modifications by checking electrical parameters of transistors. During fabrication process electrical characterization is performed in order to ensure the quality of process. For instance we measure our contact resistances after ohmic contact metallization step by performing 4-point probe Transmission Line Method (TLM). The 2x100 µm control transistors that are on the mask are measured to control the goodness of the process. These inter-stage

measurements are typically repeated for each new fabrication processes. DC characterization also aims to observe the effect of passivation so DC characterization is performed on control transistors before and after passivation.

The maximum drain current, the peak DC transconductance are some of the parameters that we measured during the DC characterization of our devices. Additionally, several voltages are of interest in characterization of GaN HEMT devices. The knee voltage, the pinch-off voltage and the breakdown voltage are the characteristic voltage values that we need to check while performing DC characterization. The Knee voltage is the drain-source voltage when current saturation occurs. The breakdown voltage is one of the most important parameters in high power devices. Pinch-off voltage can be defined as the critical gate voltage where the drain current becomes almost zero. That is, if the gate voltage is negative enough, the depletion region will extend to the active channel and there will be no current flow between drain and source. The gate voltages higher than the pinch-off voltage shrink the depletion region by allowing current flow between drain and source. The maximum current that will flow under forward gate bias is also an important parameter in HEMTs since the larger maximum drain current the larger power. The change in drain-source current as a function of gate voltage is called transconductance, where drain voltage is constant (see equation (3.1)). A small change in gate voltage can lead a large change in drain current that makes the HEMTs works as an amplifier so DC transconductance parameter should be characterized.

$$g_m = \frac{\partial Ids}{\partial Vg} \tag{3.1}$$

DC characterization is performed by using a Semiconductor analyzer and a DC probe station. As previously stated, first measurement is to characterize the contact resistance values using four-point transmission line method (TLM). TLM is used to eliminate the parasitic resistances came by the probes and cables from the measurement setup. Rectangular shaped ohmic contact metal patterns are placed on the fabrication mask by leaving certain distances among them.

After ohmic contact metallization step, the resistance between each pair of ohmic contact patterns is measured. In this measurement method, a high impedance current source is used to drive current through the outer probes and a voltmeter measures the voltage difference between the inner probes so the contact resistance value are measured. TLM patterns pointing out the specific spacing between them and introducing four-point probe method are given in Figure 3.10.

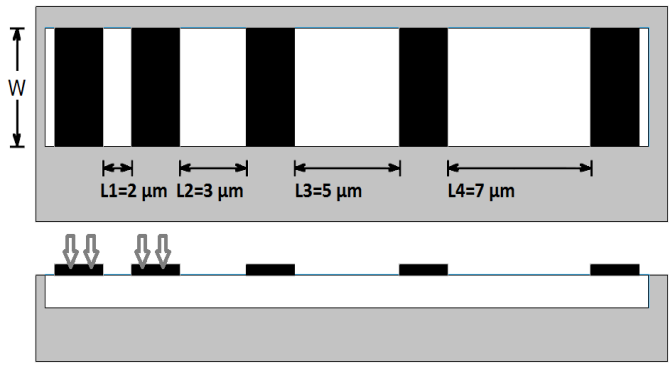


Figure 3.10 TLM pattern view.

Determination of contact resistance is significant to check the quality of Ohmic Contacts. Our contact resistance value changes between 0.2 and 0.6 Ω-mm as shown in Figure 3.11.

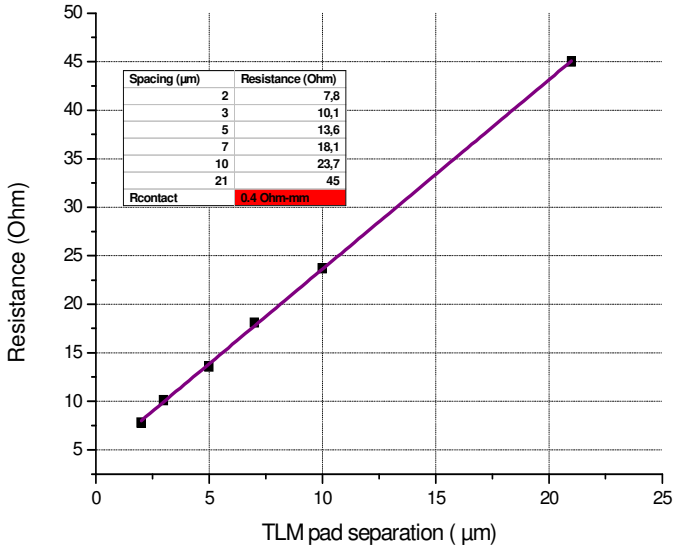


Figure 3.11 Graph of Resistance versus TLM pad seperation to calculate Contact Resistance.

Before passivation, characterization of the control transistors are made by looking at the I-V curve of a 2x100 µm HEMT to extract the maximum drain current and characterization voltages including breakdown voltage and peak transconductance parameters. DC-IV curve of the transistors is obtained by measuring drain current while sweeping gate and drain voltages in a specific voltage ranges. Gate bias voltage is swept between -6V to 0 V and drain voltage is swept till 15V starting from 0V. Maximum drain current per unit area is found around 700- 800 mA /mm for a typical unpassivated 0.25 µm gate length HEMT device. The corresponding DC-IV measurement results are provided in Figure 3.12. The total gate width is 0.2 mm so the measured maximum drain current and transconductance are required to divide by 0.2 mm (or multiply by 5 mm) to be normalized to a unit gate width. In Figure 3.12 the maximum drain current density of 750mA/mm and the peak trasconductance of 190 mS/mm are measured and the breakdown voltage is found to be larger than 40V before passivation.

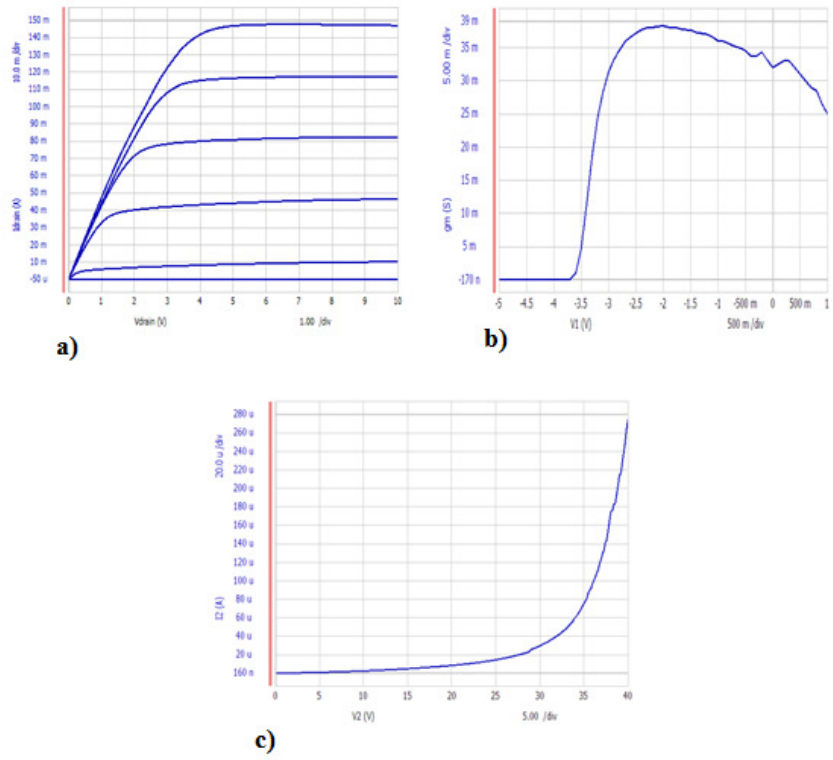


Figure 3.12 DC characterization Results for a 2x100µm HEMT.

An additional measurement is performed before going through SiN passivation process to identify the value of sheet resistance (*Rsheet*). Knowledge of sheet resistance is important for IC designers in order to make resistors. Sheet resistance is simply defined as the ratio of bulk resistivity (ρ) to film thickness (t). The related formula for sheet resistance is provided:

$$R_{sheet}\left(\frac{Ohm}{square}\right) = \frac{\rho}{t} \tag{3.2}$$

The sheet resistance value should remain same for all resistors when the resistor material was uniformly deposited across the circuit [68]. The sheet resistance is found to be around 15Ω/square. Sheet resistance measurements can be made applying four-point probe method but these measurements cannot be reliable because of change in the separation between TLM pads due to optical lithography tolerances [58]. In our MMIC mask, several resistors are placed to

obtain the sheet resistance value as shown in Figure 3.13. Slope of the graph of measured resistance versus Length/Width gives the value of sheet resistance. Corresponding sheet resistance measurement graph is given in Figure 3.13.

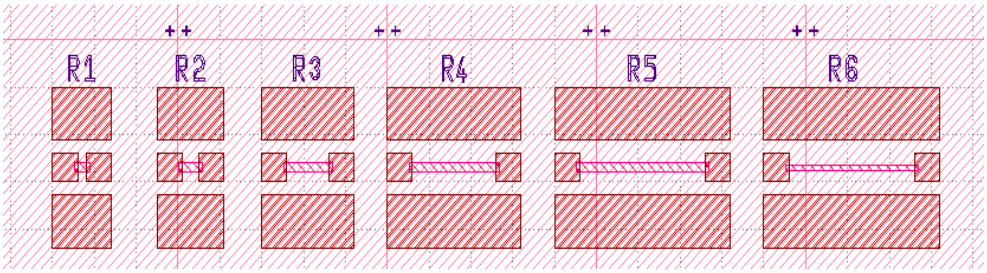


Figure 3.13 Schematic illustration of the sheet resistance measurements with various L and W.

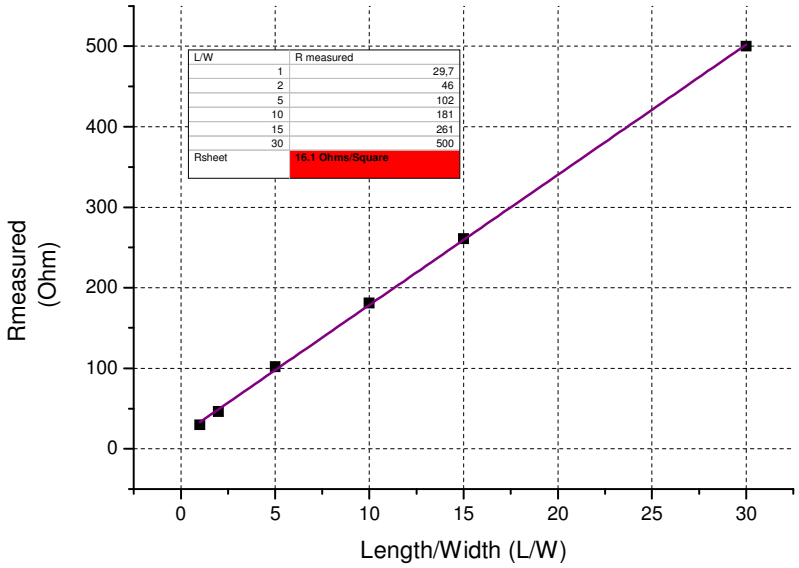


Figure 3.14 Sheet resistance measurement data and graph.

After passivation, this maximum current value is recorded around 1.1mA/mm. The definitions provided in the above are used to identify the parameters like the pinch-off voltage (V_{po}) and the knee voltage (V_{knee}). -5V and 6V are the typical values for the pinch-off voltage (V_{po}) and the knee voltage (V_{knee}), respectively. The related figures are shown in Figure 3.15.

The breakdown voltage is measured by increasing drain voltage to the point that allows current density of 10mA/mm while keeping the gate channel is off. The drain voltage at which current flow becomes around 10mA/mm equals the breakdown voltage. The total gate width of the control transistor is 0.2 mm so the drain current is limited around 2000µA (10mA/mm x 0.2 mm) which is a measure of the exact breakdown voltage value. The breakdown voltage, V_{br} is higher than 40V for a 2x100 µm HEMT.

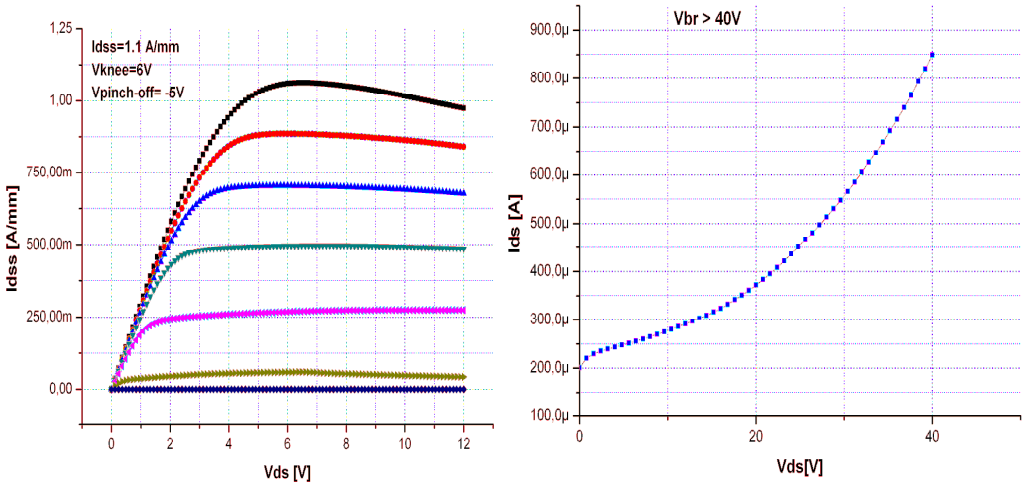
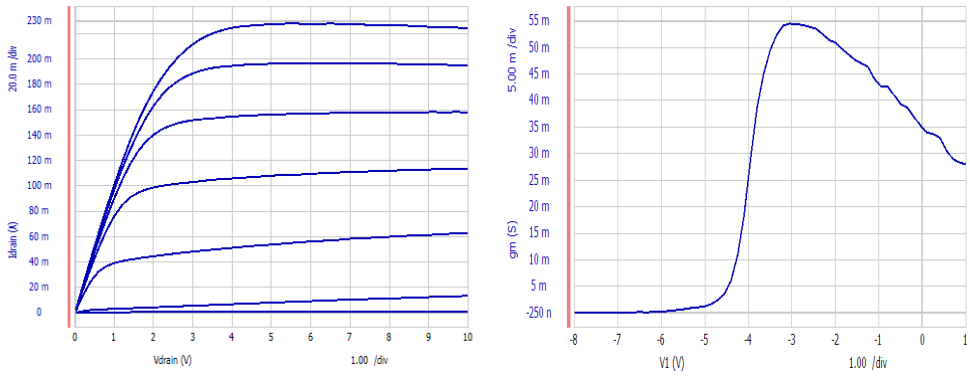
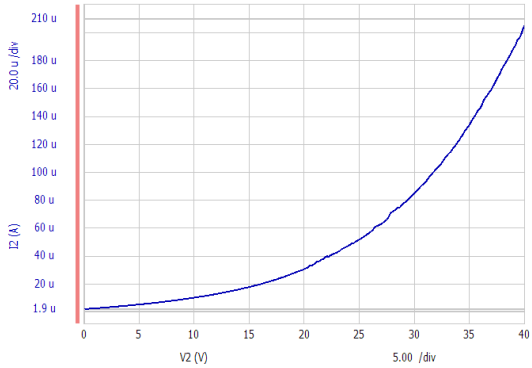


Figure 3.15 DC IV and breakdown voltage measurement results after passivation.

To characterize transconductance, drain voltage is kept constant around the knee voltage and the change in the drain current is observed while the gate voltage is swept. The peak DC transconductance, g_m is around 275mS /mm for a standard control device. The effect of the surface passivation can be seen here in Figure 3.16. Referring to the DC parameter measurements, we can say that passivation improves the DC performance, especially transconductance and drain current density of our AlGaN/GaN HEMT devices significantly.



(a) (b)



(c)

Figure 3.16 DC characterization results for a 2x100µm HEMT after passivation a) DC-IV graph b) gm versus Vgs c), Ids versus Vds.

After the DC characterization, the small-signal characterization of the transistors are made by measuring its scattering parameters (S-parameters) that represent the relationship between incident, transmitted and reflected voltage waves at the input and output of the HEMT. Knowledge of the S-parameter data is main building block in the design of the amplifiers. A small-signal gain graph of a 4x75µm HEMT device, which is actively used transistor in our amplifier designs, is given in Figure 3.17.

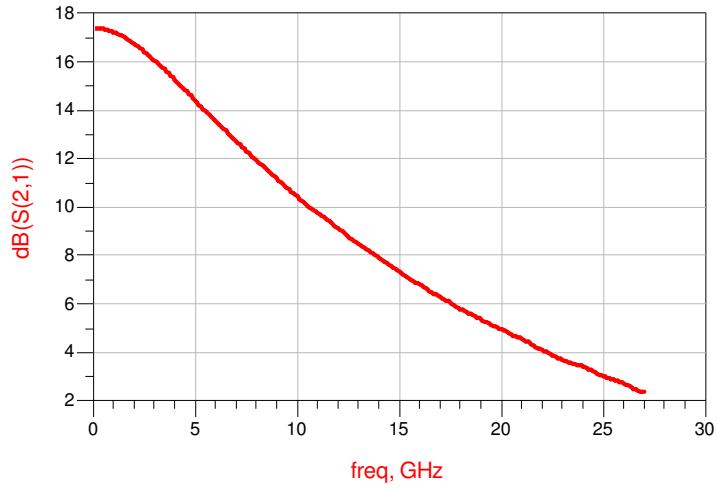


Figure 3.17 Small-signal gain of a 4x75µm HEMT device.

There are two essential frequency parameters that indicate device performance in terms of AC characterization which are the current-gain cutoff frequency, f_t and the maximum oscillation frequency, f_{max}. As it is pointed out in the name of current-gain cutoff frequency, the cutoff frequency is defined to be the frequency at which the current gain (H_{21}) of the transistor drops to zero. The ratio of the small-signal output current to the input current of a transistor with short-circuited output, parameter H_{21} can be calculated from the S-parameters by using equation (3.4) and (3.5) and we can deduce f_t by plotting H_{21} as a function of frequency. The related parameters can be stated by the following sets of formulas.

$$|H_{21}|\,(f = f_t) = 1 \tag{3.3}$$

$$H_{21} = -2S_{21}/((1 - S_{11}) \times (1 + S_{22}) + S_{12} \times S_{21}) \tag{3.4}$$

The maximum oscillation frequency (f_{max}) is the second important figure of merit (FoM) for the frequency characteristic of HEMTs. The maximum frequency is defined to be the frequency at which the transistor still presents a power gain. The maximum oscillation frequency can be calculated at which

unilateral power gain becomes 1. By using Mason's Rule we can calculate unilateral power gain employing the following formulas:

$$|G_U|\ (f = f_{max}) = 1 \tag{3.5}$$

$$G_U(f) = \frac{\left|\frac{S_{21}-S_{12}}{S_{12}}\right|^2}{2\times k\left|\frac{S_{21}}{S_{12}}\right| - 2Re\left(\frac{S_{21}}{S_{12}}\right)} \tag{3.6}$$

Kurokawa′s stability factor,

$$k(f) = \frac{(1-|S_{11}|^2-|S_{22}|^2+|S_{11}\times S_{22}-S_{12}\times S_{21}|^2)}{(2\times|S_{12}|\times|S_{21}|)} \tag{3.7}$$

The setup given in Figure 3.18 is used for small-signal measurements and f_t and f_{max} are obtained using measurement results and using the equations (3.4) and (3.6).

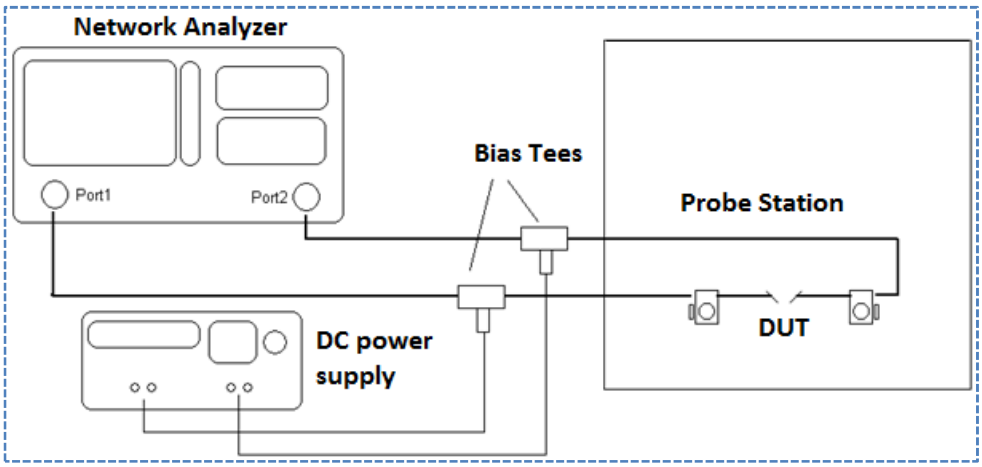


Figure 3.18 Measurement setup for scattering parameters.

Current gain and unilateral power gain graphs of a 4x50µm transistor is provided in Figure 3.19 and Figure 3.20, respectively. The corresponding graphs are fitted linearly and extrapolated to get the frequency values in dB

scale as it is shown in graphs. The current gain cutoff frequency of 85 GHz and the maximum oscillation frequency of 90 GHz are obtained for the 2x37.5 µm HEMT.

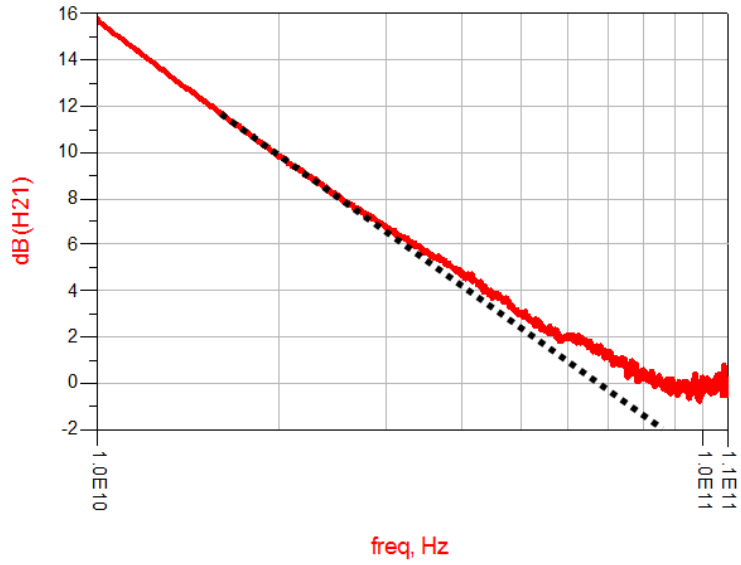


Figure 3.19 Current gain graph of a 4x50µm GaN HEMT.

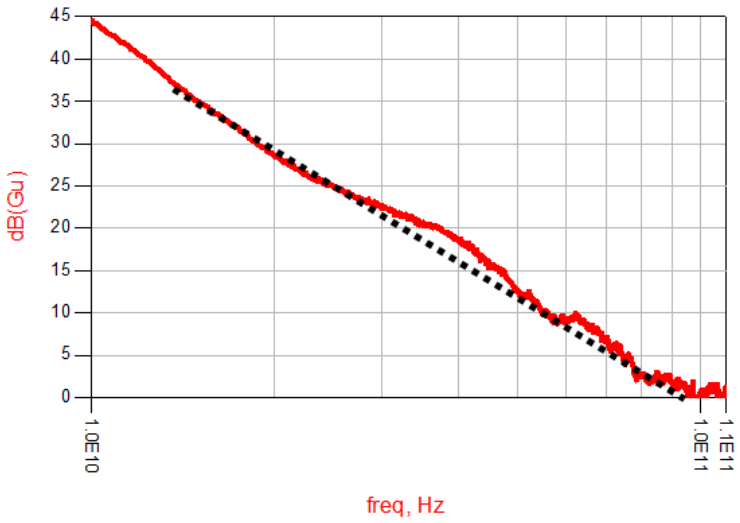


Figure 3.20 Unilateral gain graph of a 4x50µm GaN HEMT.

Chapter 4

AlGaN/GaN High Electron Mobility Transitor Modeling

4.1 Small-Signal HEMT Modeling Considerations

In this part, the extraction of small-signal parameters of the GaN based HEMTs with gate length of 0.25μm is reviewed before telling the whole story of the modeling in the next subsection. The small signal equivalent circuit used in our HEMT modeling, which is developed by IMST, is shown in Figure 4.1. The pad capacitances (C_{PD} and C_{PG}), the pad inductances (L_g, L_d, and L_s) and the gate and access resistances (R_g, R_d, and R_s) are given in the equivalent small signal circuit as extrinsic circuit elements and the other circuit elements symbolizes bias dependent intrinsic parameters.

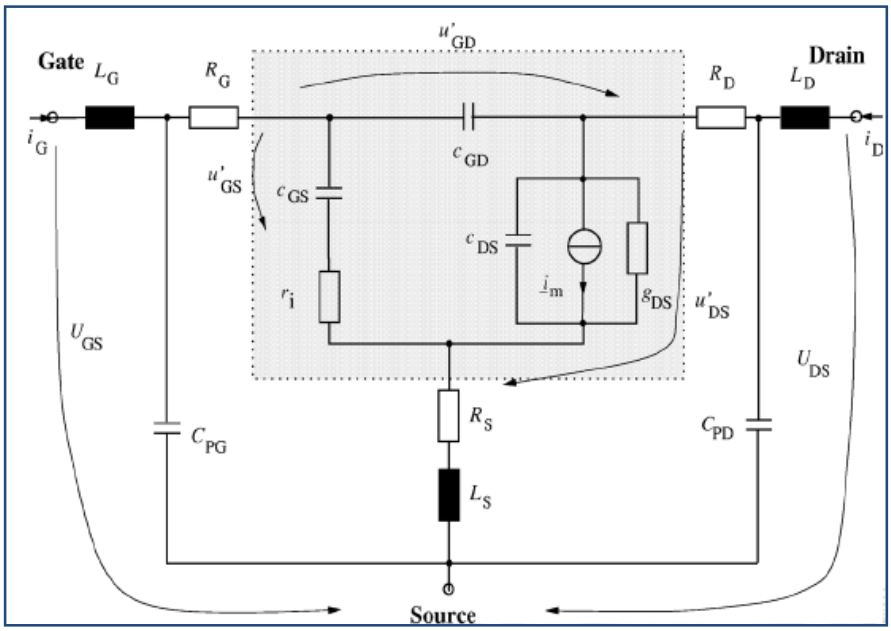


Figure 4.1 HEMT small signal equivalent circuit.

The small-signal model extraction can be also called as linear model extraction. The primary step in linear modeling is to perform S- parameter measurements and then it is followed by determination of the HEMT's extrinsic parasitic elements. The extrinsic elements are de-embedded from S-parameter measurement data before begining the determination of the intrinsic elements. Under "cold" bias condition (V_{DS}=0V), pinched cold-scattering (V_{GS}< $V_{pinch-off}$, V_{DS}=0V) and gate-forward cold-scattering (V_{GS}>0V, V_{DS}=0V) parameter measurements are performed for the determination of the extrinsic capacitances and the determination of the extrinsic inductances and resistances, respectively (see Figure 4.2). Due to "Π" shape equivalent circuit configuration under pinched cold bias conditions, the imaginary part of the simulated Y-parameters of the open circuited equivalent circuit shows a capacitive behavior and pad capacitances can be extracted. Due to "T" shape equivalent circuit configuration under gate-forward cold bias conditions, the imaginary part of the simulated Z-parameters of the short circuited equivalent circuit shows an inductive behavior and parasitic inductances can be estimated. The remaining parasitic resistances are extracted from the real part of the Z- parameters.

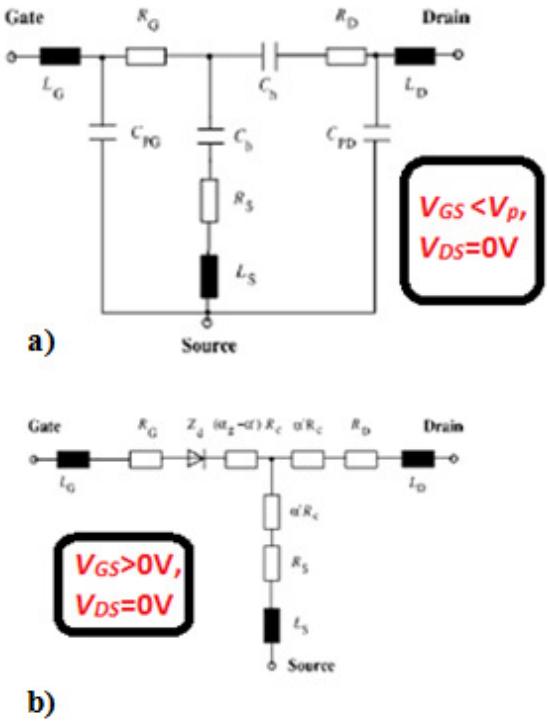


Figure 4.2 Circuit Schematics for the extraction of the extrinsic capacitances and inductances under (a)"Pinched cold" (V_{GS}<Vpinch-off, V_{DS}=0V) and (b) "gate-forward cold" (V_{GS}>0V, V_{DS}=0V) bias conditions.

When the extraction of the extrinsic parameters is completed, these calculated data is required to be de-embedded form the measured scattering parameters. To achieve these, S-parameters are converted to Z-parameters and series inductances (except source pad inductance) are omitted. Afterwards, the obtained Z- parameters are converted to Y-parameters and parallel capacitances are de-embedded and Y-parameters are converted back to Z- parameters and series parasitic resistors and source pad inductance. The related conversion matrices are given step by step in Figure 4.3.

$$\text{I.}\quad \begin{bmatrix} \overline{z_{11}} - jwL_D & \overline{z_{12}} \\ \overline{z_{21}} & \overline{z_{22}} - jwL_G \end{bmatrix} ([S]\rightarrow[Z])$$

$$\text{II.}\quad \begin{bmatrix} \overline{y_{11}} - jwC_{PG} & \overline{y_{12}} \\ \overline{y_{21}} & \overline{y_{22}} - jwC_{PD} \end{bmatrix} ([Z]\rightarrow[Y])$$

$$\text{III.}\quad \begin{bmatrix} \overline{z_{11}} - R_s - R_G - jwL_S & \overline{z_{12}} - R_s - jwL_S \\ \overline{z_{21}} - R_s - jwL_S & \overline{z_{22}} - R_s - R_G - jwL_S \end{bmatrix} ([Y]\rightarrow[Z])$$

Figure 4.3 Conversion matrices for extrinsic parameter calculation step by step.

Now all extrinsic parasitic elements are known and intrinsic elements in the small-signal equivalent circuit can be estimated using parameter fitting. As stated before, intrinsic elements are bias dependent parasitic elements so parameter fitting is required to be implemented for all measured bias points.

To sum up, starting from scattering parameter measurements at different operating points, the parasitic elements of the small-signal equivalent circuit are first determined. For the extraction of the extrinsic parameters, cold- scattering parameter measurements are performed. De-embedding of the extrinsic elements is implemented to receive the measured scattering parameters of the internal (intrinsic) transistor. Examples of an extracted intrinsic parameter according to the method described above, gate-source and gate-drain capacitances with TOPAS software are provided in the following Figure 4.4.

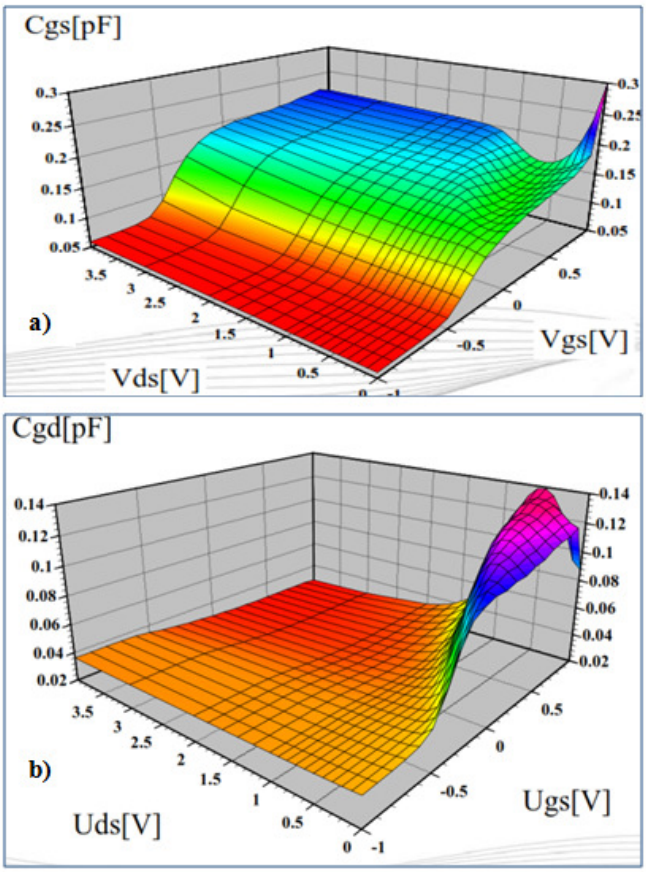


Figure 4.4 Extraction of a) gate-source and b) gate-drain capacitances with TOPAS software.

4.2 Large-Signal HEMT Modeling Considerations

Active device modeling is performed according to the application type that will be used: noise modeling for low noise amplifiers (LNAs), small-signal modeling for switch applications, nonlinear (large-signal) modeling for power amplifiers and LNAs, electro-thermal and trapping effect modeling for some power amplifiers. In this thesis, power amplifier design is the main consideration. Complete and accurate models allow a large percentage of integrated circuit designs to work the first time. Therefore, good large-signal models are needed to model our active devices used in our MMIC power amplifiers. Besides, a good

large signal model should be in good agreement for small-signal operation so small-signal performance of the device should be evaluated for validation of the extracted model. In this section, the complete modeling process is described including the parameters extraction of the small signal model and a table based modeling approach for nonlinear GaN based HEMTs.

In this section, before going through details of the modeling technique that we used for our GaN HEMT devices, three main types of large-signal transistor modeling are explained briefly. Since each modeling techniques have some unique advantages and disadvantages, the modeling technique should be chosen according to the needs of the design. Model convergence, operating range, easiness of modeling process, physical insight, model accuracy and model usability are the essential parameters which should be considered during modeling processes. The common large-signal modeling techniques used for GaN HEMT devices are: physical models, behavioral models and analytical models.

Devices fabricated on top of a semiconductor material can be modeled two or three dimensionally using physical modeling technique. Physics-Based models consist of thermal effects and optical behavior of the transistor in addition to electrical characteristic of the device. The main disadvantage of using physical modeling technique is that very time consuming simulations are required to solve complex semiconductor equations provided in the model. That is, Physics-Based models are not fast enough for circuit simulations. However, physical modeling methods can be used for larger operating range in comparison to behavioral and compact modeling techniques and can be used for optimization of transistor physical parameters such as gate length, gate width, gate finger spacing, etc. To sum up, this type of modeling is not a preferable method for circuit design, compared to the alternate modeling techniques.

Behavioral models are purely measurement-based models. Behavioral models, which are also called as black-box models, are based on frequency

domain measurement data. There are no parameters to extract and each device, even if they have the same geometry, needs a new model since a black box model cannot be customized by users. An average of measurement data for many devices can be used to construct the model. Nonlinear vector network analyzer models and X parameter models are included in this type of modeling. Recently, large-signal modeling using X-parameter technique has been improved. X parameters can be defined as the extended S- parameters depending on the input power and output power obtained at 2^{nd} and 3^{rd} order harmonics [69].This type of modeling is much more suitable for the system level, inter-modulation distortion (IMD), error vector magnitude (EVM) simulations. Scaling of the black box models is not feasible for a measurement based modeling type. Self- heating effects cannot be included models in a black box model. Nevertheless, a black box model is not flexible which means it requires multiple device measurements at each bias points and each input power. Transistor level designs needs a much more practical modeling technique rather than behavioral modeling.

Analytical or compact transistor modeling is the other modeling technique that is used to determine the large-signal performance of the transistor by extracting device parameters. These models are used for circuit design with a simplified approximation of the physics of the device [70], [71]. Extrinsic and intrinsic device parameters are extracted by permitting user's customization. The main advantage of this modeling technique is that any model can be developed upon. Extrinsic, bias independent, device parameters are obtained using small-signal S-parameter measurements and then intrinsic, bias dependent, model parameters are extracted by performing only pulsed I-V measurements or by performing both pulsed I-V measurements and pulsed RF measurements. After completing typical characterization process, validation of the model with load-pull measurements is required to ensure the accuracy of the model. Thermal and trapping effects are not included in conventional analytical models. However, thermal effects are included some of the analytical models. In recent years

several analytical models have been published by providing trapping effects. As a result, a typical advanced analytical modeling procedure can be summed up with the device model extraction flow indicated in Figure 4.5 [72]. Small signal model extraction through S- parameters and large signal model extraction through pulsed IV characterization are performed and then it continues with nonlinear capacitance modeling, thermal modeling and trapping effect modeling. This is a well developed compact modeling approach containing thermal and trapping effects [73]. As a final step, model validation with load pull characterization is needed.

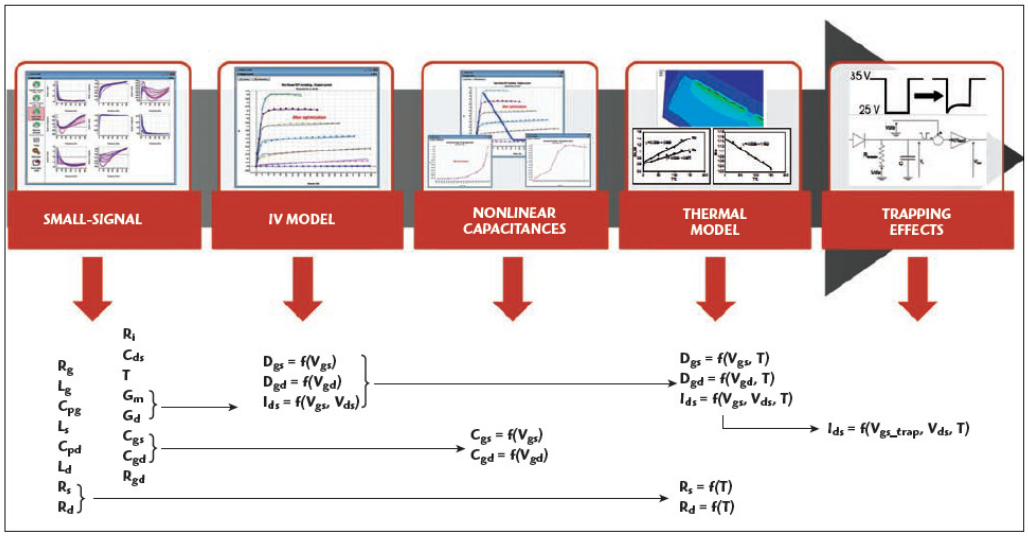


Figure 4.5 Compact Model Extraction flow of an active Device [72].

To obtain the nonlinear model of our GaN HEMT devices, table based modeling approach, which is a process- independent and measurement- based modeling technique based on discrete measured data points, is applied. TransistOrPArameterScaleable (TOPAS) software, which is upgraded by IMST GmbH, is used to obtain the nonlinear model of 4x50 µm, 4x75 µm, 6x75 µm GaN HEMTs. Non-linear transistor model is developed after completing the small signal equivalent circuit elements extraction. Due to its special large signal equivalent circuit (see Figure 4.6), small signal elements can be optimized without causing a large discrepancy between the static simulations and measurements. In our circuit simulations, ADS™ software developed by Agilent

is used and the TOPAS model can be implemented using this circuit simulator. TOPAS table-based model is valid for all bias points, which means nonlinear simulation switches to a linear simulation even if the bias dependent circuit elements are driven by the gate-source and the drain-source voltage for low input power [74].

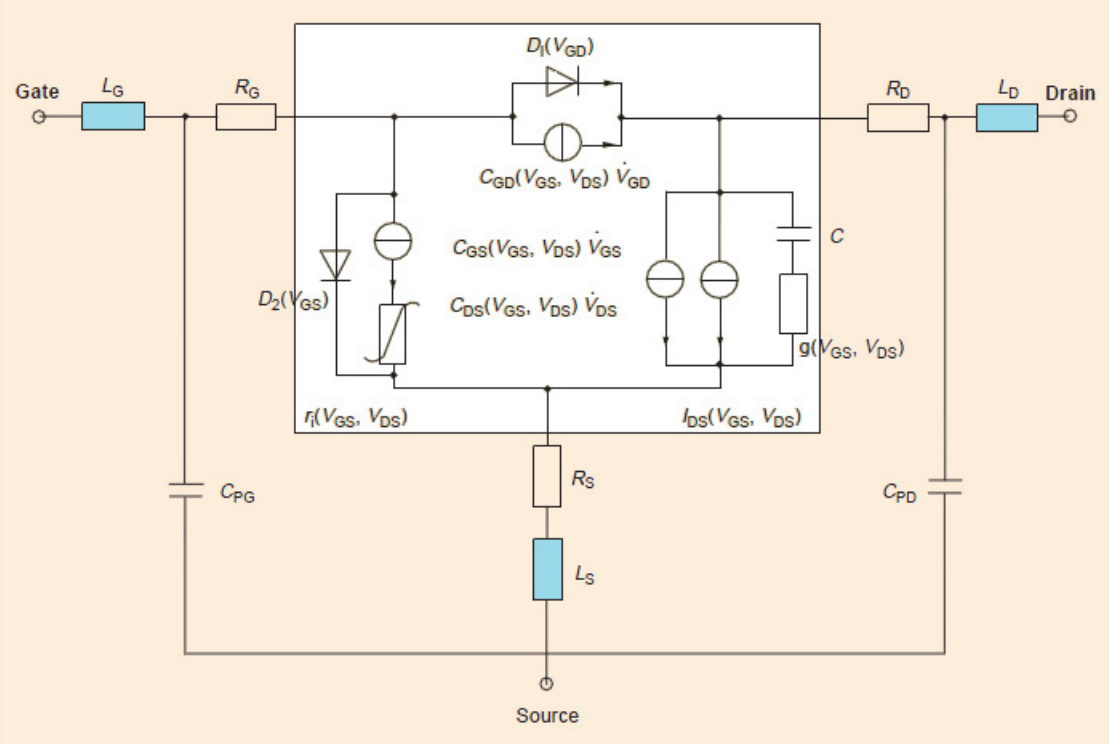


Figure 4.6 Large Signal equivalent circuit of the GaN HEMT.

Table based modeling is straightforward and fast technique compared to other modeling methods and also bias points and derivatives can be used for TOPAS extraction and bias dependent S- parameters are saved in a table without dealing with the physical insight of the device. Linear models describe the DC behavior while large signal amplitudes and change of bias points describe nonlinear behavior of our GaN HEMTs.

As outlined above, table based models are based on S-parameter and IV measurements, so accurate measurements should be performed to determine device characteristics confidently. Initial step in the characterization procedure is to perform the Continuous Wave (CW) measurements with a similar setup

given in Figure 3.18. Additionally, these measurements are carried out a computer controlled setup through a Labview project developed for the modeling purpose. Using this software tool, controlling and saving the measured S parameters are possible at each bias point defined by the users. The GPIB addresses, which are also introduced in Labview project, are used to make connections with DC power supply and PNA. User interface of this Labview project is provided in Figure 4.7.

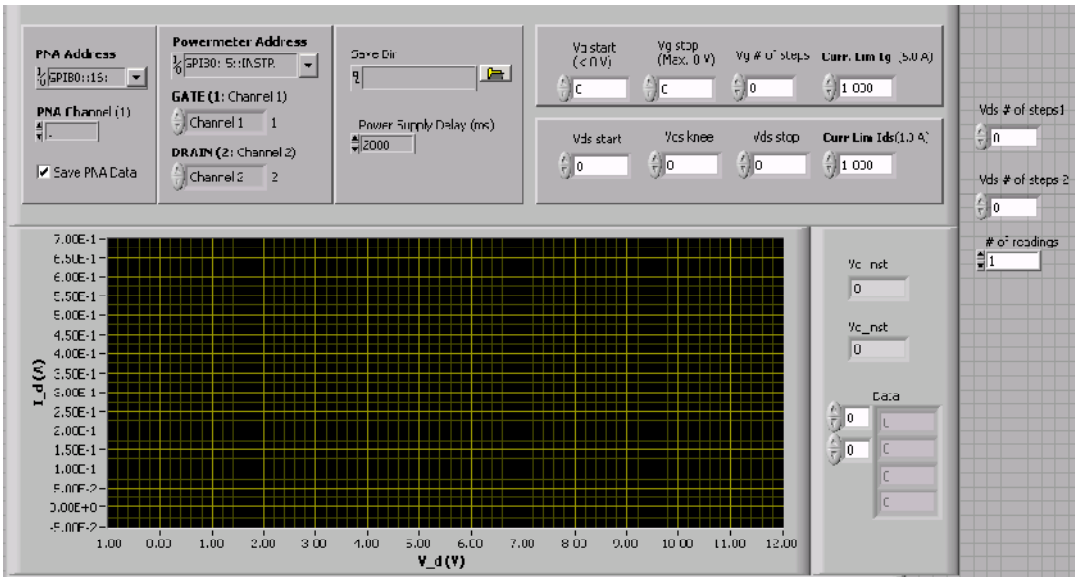


Figure 4.7 User interface for measurement based modeling.

Typical characterization process consists of Pulsed I-V characterization which eliminates the self-heating effects. Pulsed measurements are much more preferable to model high power devices due to degradation of the thermal effects since self-heating effects is very critical for large periphery transistors. However, accurate GaN HEMT models can also be obtained by making CW I-V measurements with a tolerable error. The gate bias is swept starting from the pinch-off voltage point to 0V. The first region of the drain bias sweeping is defined up to the knee voltage point of the HEMT starting from 0V drain voltage with a relatively small step size like 100 or 200 mV. The second sweeping range is specified from the knee voltage to drain bias of 20 V with a 1V step size. After determination of the model range, S parameters are measured at each bias point of the user-defined bias range. There are some measurement

considerations for our active device model: nonlinear device modeling of our GaN HEMTs is implemented over a wide drain voltage range to produce more accurate models and also relatively larger step sizes are defined within the saturation regime not to suffer from the thermal effects. The following viewgraph taken by Labview indicates the continuous IV plot for a 4x50 µm HEMT (see Figure 4.8).

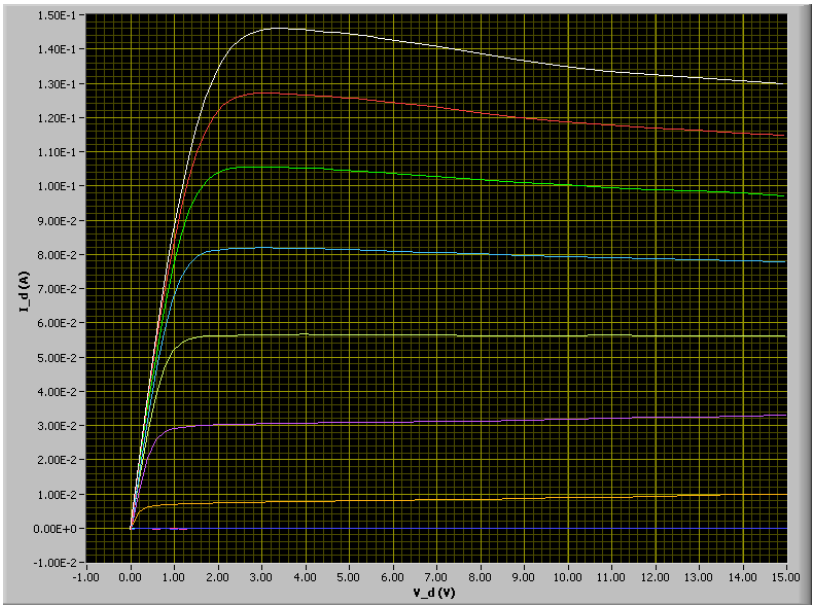


Figure 4.8 Continuous IV graph of a 4x50 µm HEMT obtained by modeling measurements.

After finalizing bias-dependent S-parameter measurements, small signal parameter extraction is the following step in table based modeling methodology. Small-signal equivalent circuit with extrinsic bias independent parameters like pad capacitances, port metallization inductances, port ohmic resistances are identified by linear model extraction as explained in section 4.1 (see Figure 4.9). S-parameter data obtained from the linear regime with a drain bias of 0V and a gate bias voltage smaller than pinch-off voltage refers to pinched cold-scattering parameter measurements [75]. The extraction and optimization of the extrinsic elements based on cold-scattering measurement data are performed using linear optimization tool provided by TOPAS software. The next two screenshots given

in Figure 4.9 indicates the extrinsic element calculation and optimization windows in TOPAS software.

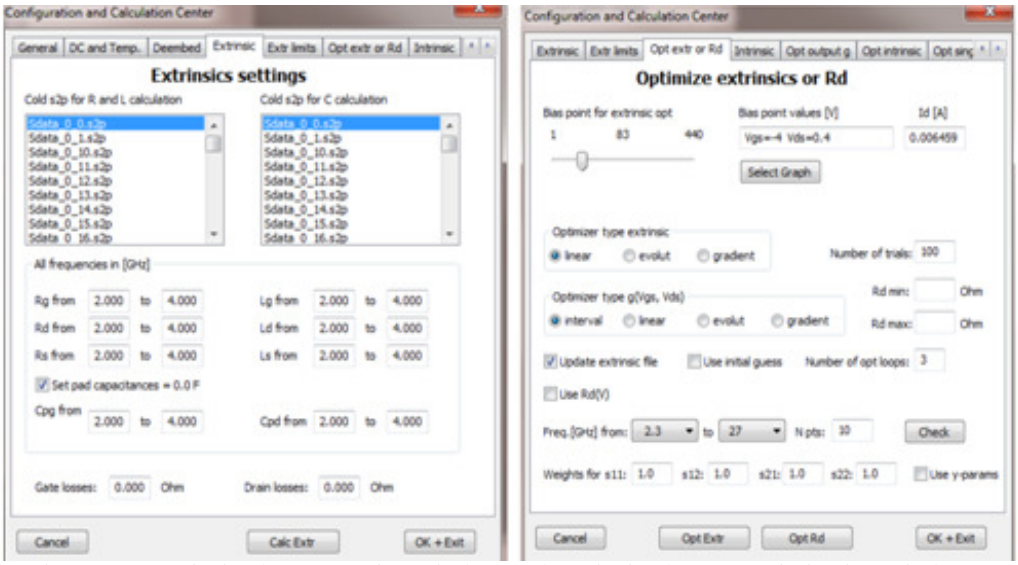


Figure 4.9 Extrinsic element setting window and extrinsic element optimization window.

Before going through the extraction of the nonlinear HEMT model, extrinsic parameters are de-embedded from the measured S parameter data by using the "Deembed "option suggested by TOPAS software. Afterwards, a set of intrinsic parameters are calculated by solving multi dimensional spline functions and again optimized by large signal optimization tool for intrinsic parameters. The related intrinsic parameter calculation and optimization windows are shown in Figure 4.10. Frequency ranges are adjusted and updated according to the extracted results to get a better model fit to measured data before going into full optimization process.

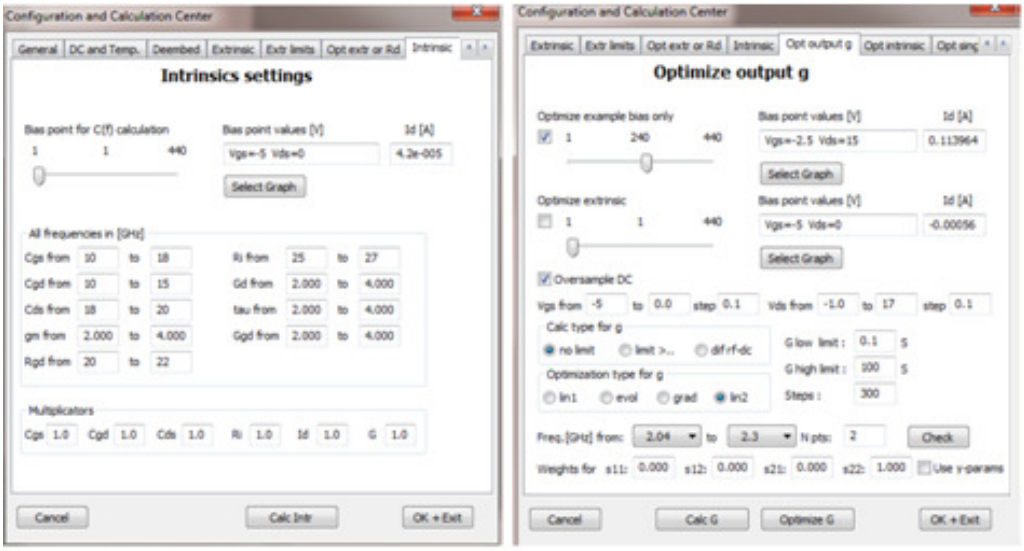


Figure 4.10 Intrinsic element setting window and intrinsic element optimization window.

In order to get a good fitting between measurement data and model, optimization should be simultaneously done by adapting frequency ranges. Intrinsic elements and S-parameters agreement should always be checked and if necessary, optimization should be repeated for different intrinsic frequency settings to improve the model.

To relate intrinsic parameters with inner voltages, voltage de-embedding process is performed. This is the last step before passing the nonlinear elements calculation. Through the conversion of outer to inner control voltages, the inner voltages can be found with the extracted external resistors. Below equations (4.1) and (4.2) are used to calculate the inner voltages in terms of outer voltages and drain-source current regardless of the gate current. Continuous nonlinear function of all intrinsic parameters, which are bias-dependent, is formed using TOPAS interpolation.

$$V_{GS}' = V_{GS} - I_{DS} \cdot R_S \tag{4.1}$$

$$V_{DS}' = V_{DS} - I_{DS} \cdot (R_D + R_S) \tag{4.2}$$

When implementing a non-linear model in a simulator, the charges of the capacitors for the large-signal case must be determined. This can be done by simple integration in TOPAS. A capacitor only depends on a control voltage so this integral is always uniquely determined from control voltage. However, the charge is not uniquely determined for example by two control voltages, since the integral itself is path dependent. One possibility is to impose a fixed charging cycle for the capacitor to solve this problem. Other routes require the use of so-called trans-elements like transcapacitances that influence the behavior of the small-signal. In TOPAS, nonlinear model parameter calculations are made by converting the charge sources into the current sources using the basic relationship $I = \dot{q} = C.\dot{V}$ (see equations (4.3), (4.4), (4.5)).

$$I_{GS} = c_{GS}(V_{GS}, V_{DS}) \cdot \dot{V}_{GS} \tag{4.3}$$

$$I_{GD} = c_{GD}(V_{GS}, V_{DS}) \cdot \dot{V}_{GD} \tag{4.4}$$

$$I_{DS} = c_{DS}(V_{GS}, V_{DS}) \cdot \dot{V}_{DS} \tag{4.5}$$

Modeling process is completed after the calculation of the nonlinear circuit elements and model validation should be done before simulating the extracted model in ADS. The next part shows the way how the HEMT models are validated.

4.3 GaN HEMT Model Validation

The extracted models should be checked to observe whether the model is consistent with the measurement data, or not. Controlling the agreement between the simulated (small-signal simulations) and measured S-parameter data is essential for the model validation process. For various bias points, we have to question the model consistency by looking at the percentage of error between the measured and simulated S-parameters. The load-pull characterization should be done to verify the nonlinear characteristic of the

extracted model (Harmonic Balance simulations). Besides a good enough nonlinear model is required to be valid under small-signal operation conditions and this must be true for all operating points. During transistor modeling with TOPAS, crosscheck of the optimized models with measurement results is simultaneously made. In Figure 4.11, comparison of the measurement data and modeling results of a 4x75 µm HEMT is made with S-parameters and there is an error of around 10 percent between them.

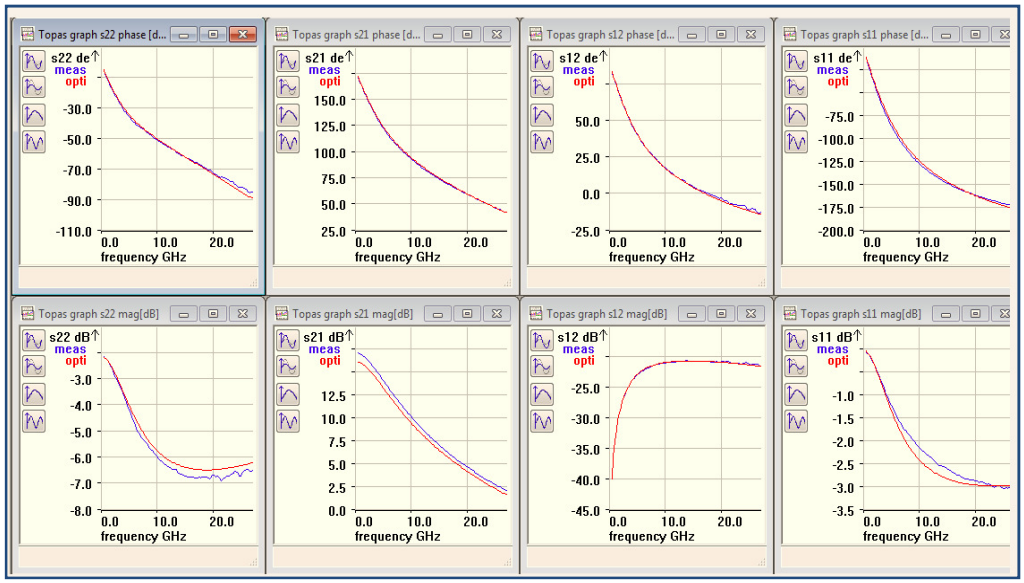


Figure 4.11 Measurement and Modeling Comparison for a 4x75 µm HEMT.

The following two graphs are provided to indicate the good agreement between the measured and the simulated S- parameter data at two different bias points for a 4x75 µm HEMT (see Figure 4.12 and Figure 4.13). These comparisons made to reveal the small-signal accurateness of the model.

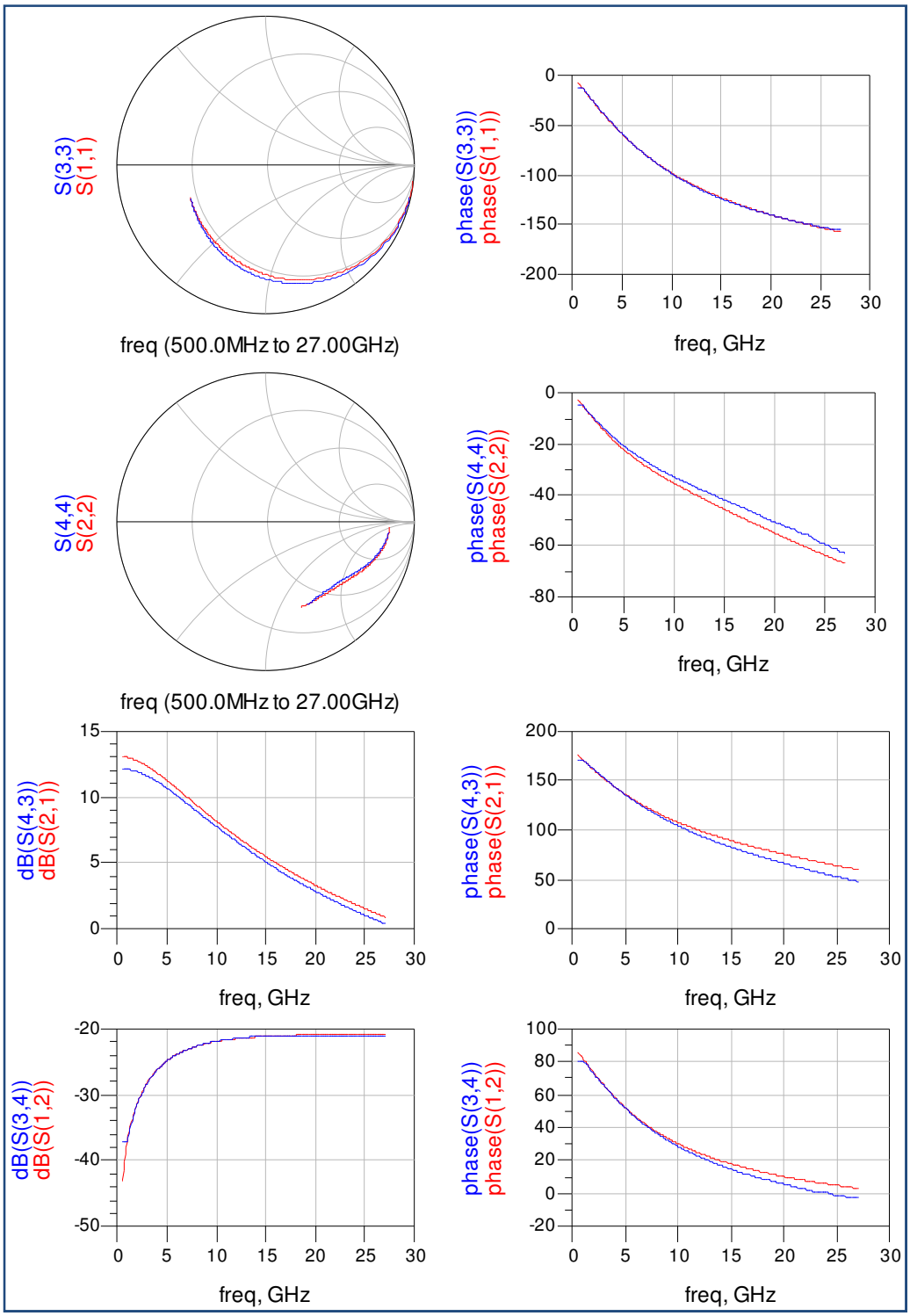


Figure 4.12 Measured (blue curves) and simulated (red curves) S-parameter data comparison at operating point of VGS=-2V and VDS=2V.

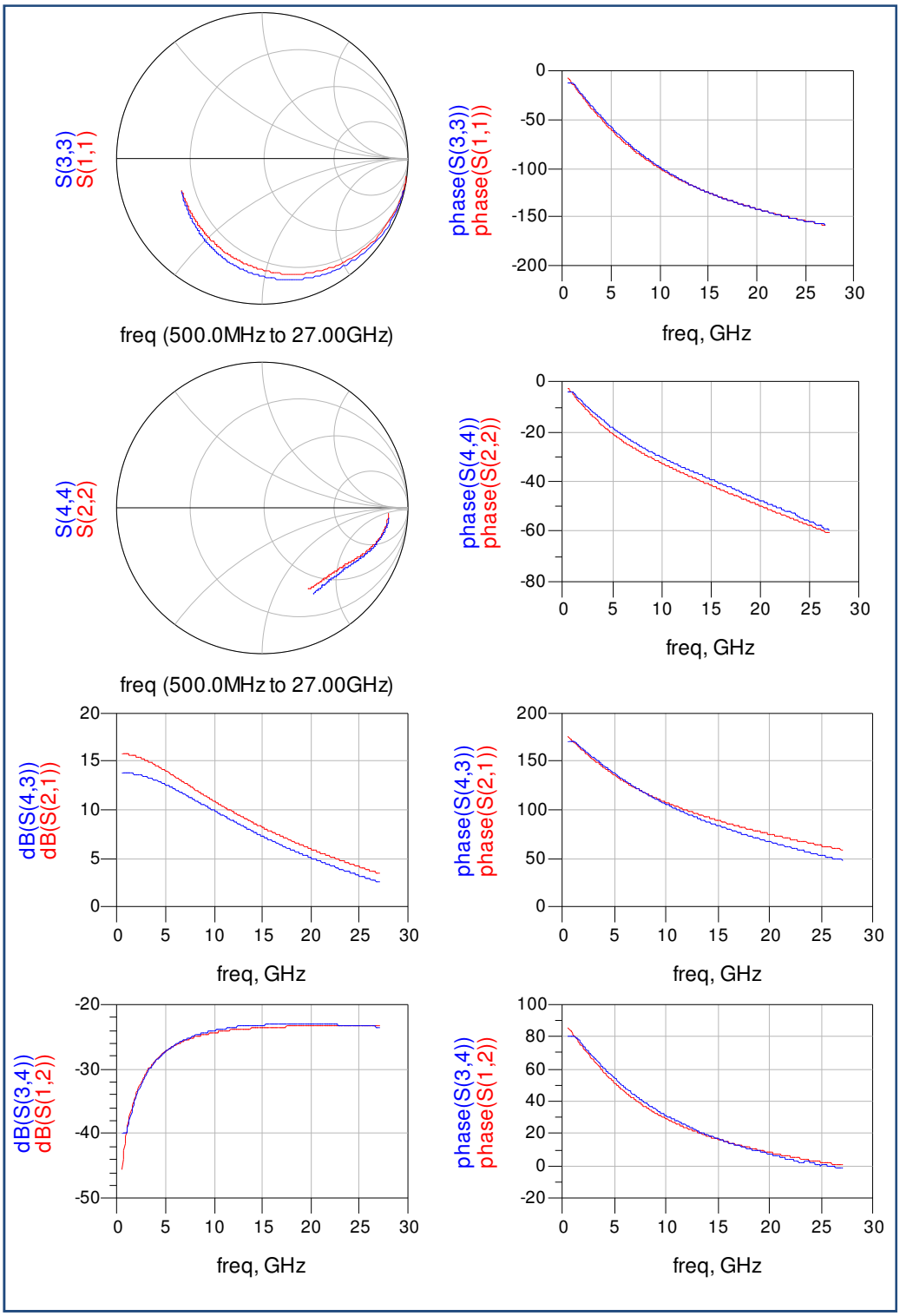


Figure 4.13 Measured (blue curves) and simulated (red curves) S-parameter data comparison at operating point of VGS=-3.5V and VDS=15V.

One last step is needed to complete the confirmation of model accuracy which is load pull characterization. Under CW 12 dBm input power signal, load pull measurements are performed. A gate voltage of -2.7 V and a drain voltage of 15V are the selected DC bias points. The Optimum load and source impedances were measured. The harmonic balance simulations give the similar results with the measured data. Power gain and output power graphs for measured and simulated data are observed that the large signal accuracy of the model is fairly consistent with the harmonic balance simulations for a 4x75 μm HEMT. The measured power gain is 1.5 dB less than the simulated one but it still works for the large signal simulations since the complete CW large signal behavior cannot be estimated due to self-heating effect. Since the impedances for the maximum output power in the model are close to the ones in the load pull measurements the model can be used in power amplifier design.

Chapter 5

6-18 GHz GaN-based Coplanar MMIC Amplifier Designs

In this chapter design of the microwave amplifiers with multi-octave performance is discussed. The design goal of required MMIC is to achieve a small signal gain of 7±1 dB for 6 GHz-18 GHz frequency band and minimum output power of 27 dBm at 3 dB compression. The chosen transistor's small-signal and large-signal models extracted from S-parameters and the CW DC- IV characteristics, as described in Chapter 3, were used for the design of the broadband amplifier. The amplifier's small-signal and large signal performance was analyzed using Agilent's ADS simulation tool. The small-signal gain and return losses at the input and output are optimized by the small-signal simulations, whereas the output power and power-added efficiency are optimized by the large-signal simulations. To achieve our design goals, the first design effort was made to reach the small-signal gain requirement with a gain flatness of $\pm$1 dB and then various circuit topologies are applied to satisfy the large-signal and small-signal design requirements. To satisfy the output power requirement, two paralleled transistors with the common-source configuration are used by employing negative feedback circuit topology and designing complex matching networks. Design progress is given step by step starting from the first design to the last design.

Designing the amplifiers with a feedback topology is useful to decrease the dependence on HEMT S-parameter variations, to increase the potential for wide bandwidths, i.e. 0.1-20 GHz with one design [76], to enable smaller device size and to increase power handling. In this thesis, three different designs, first with Chebyshev matching network without negative feedback (CMwoFB), the second with negative feedback (CMwFB) and third with two parallel transistors with negative feedback (PT) are realized, fabricated and measured. Evaluating the measurement results of these implemented designs, the second iteration of two transistors in parallel with negative feedback (PT) structure is realized and design goals achieved with this second iteration. Details of the design will be explained in the following subsections.

In section 5.1, general design considerations for wideband MMIC amplifier are overviewed and then in section 5.2, the design, realization and measurement results for the first wideband amplifier topology without negative feedback (CMwoFB) is given in details, after that, in section 5.3 design and realization of an amplifier by using Chebyshev matching network with negative feedback (CMwFB) is explained in detail including the simulations and measurements, following that design, realization and measurements of two parallel transistors with negative feedback topology (PT) is presented. In section 5.4, comparison of these three topologies is made including concluding remarks, finally, in section 5.5, second and final iteration of the topology with two parallel transistors using negative feedback, which satisfies all the design requirements, are given.

5.1 General Design Considerations for Wideband MMIC Amplifier

Broadband amplification has several difficulties like changes in transistor's small signal parameters, small signal gain, S_{21} and reverse voltage gain, S_{12} with frequency. It is well known that the small-signal gain (S_{21}) decreases with

frequency at 6 dB per octave and the reverse voltage gain (S_{12}) increases at the same rate with frequency. The other difficulty is that the input and output return losses fluctuate over the wide frequency range. Amplification over the multi-octave bandwidth with a flat small-signal gain is fairly challenging design question. Compensated matching design, balanced amplifier design, and wideband matching negative feedback design and network synthesis design are some techniques used in broadband amplifier design [77], [78].

Compensated matching is based on mismatching the input and/or output to obtain a flat gain response but it is hard to implement in several octave bands and also gives a poor input and output return loss at lower frequency. These types of amplifiers are not suitable to cascade due to their high power being reflected to the source which means high voltage standing wave ratio (VSWR).There is a large mismatch at the input and output so power gain is sacrificed for the sake of broadband operation.

Wideband matching network synthesis method is the other technique that can be used for broadband amplification purpose. Broadband bandpass Chebyshev or Butterworth filters can be realized with lumped components to synthesize the input and output networks. This method improves the gain characteristic by compensating the gain drop at higher frequencies but it suffers from the high VSWR again. This method is one of the methods used in our designs and design and realization details are given in the following section.

Negative feedback technique is another commonly used technique in amplifier design since it presents many important benefits. This method is the other method used in our broadband amplifier designs. Negative feedback can be employed to stabilize the gain of the amplifier against the transistor parameter fluctuations due to bias changes, to extend the bandwidth of the amplifier, to develop the gain linearity and to change impedances at the input and output of the amplifier in any desired fashion [79]. In addition to the listed advantages of the feedback topology, introducing a negative feedback results in

a gain reduction and it might decrease the tendency of standard oscillation, however due to feedback, feedback-induced oscillation may occur [80]. The shunt and series feedbacks can be employed separately or together to enhance the bandwidth of the amplifier (see Figure 5.1).

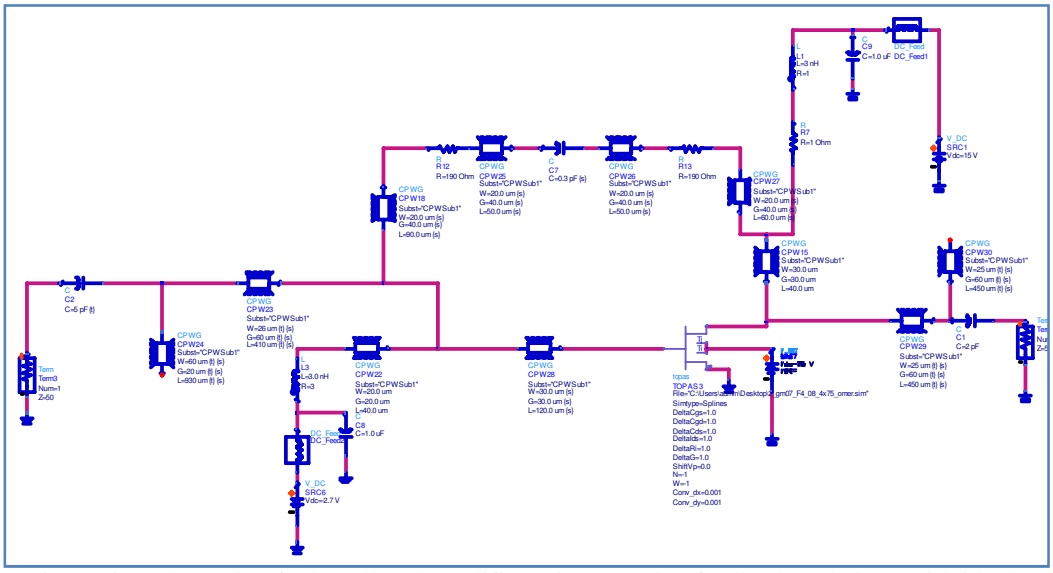


Figure 5.1 Schematic of a broadband amplifier using negative feedback technique with ideal lumped and coplanar elements.

All the wideband amplifier topologies can be used in balanced configuration. Balanced amplifiers are composed of two identical parallel amplifiers using 3 dB hybrid couplers at the input and the output for splitting and combining, respectively. Using this configuration, the output power can be increased by a factor of two with good input and output VSWRs. Input and output reflections are absorbed in the coupler terminations due to the phasing properties of the coupler by causing an enhancement on stability of the amplifiers and improvement on impedance matching. On the other hand there are frequency band limitations in these configurations since the bandwidth of the final amplifier is primarily limited by the bandwidth of the hybrid couplers used in design and the large bandwidth hybrid couplers that are suitable for MMIC design are typically up to one octave. However, our specified bandwidth is

higher than one octave bandwidth, improvement of hybrid coupler up to very wide bandwidth can be a topic of future work.

Design considerations of a multi-octave band MMIC amplifier are described in this section. Impedance matching at the output side of the transistor, maximum power capability and efficiency are the main design constraints in large-signal performance of a power amplifier while amplification, gain and linearity are important factors in terms of small-signal performance of the device. Design of a power amplifier is different from design of a small-signal amplifier. Large signal S parameters, which are defined at a specific signal level, are needed to design power amplifiers since small-signal approximation is not viable in power amplifiers. However, small signal approach might be used on the input side of the amplifier. In small-signal amplifiers, the active device is firstly stabilized and then using complex conjugate matching technique, which is also known as gain matching , the impedance seen from the load side is matched to the output of the transistor by showing the conjugate of the transistor's output impedance in order to maximize the small-signal gain of the amplifier. In large-signal amplifiers (power amplifiers), matching regarding of Load-pull data is required to get maximum output power since the optimum load impedance at high driving signal levels can be different from the small signal optimum load impedances. The optimum load impedance is determined from the large-signal IV characteristics of the active device under the specified bias conditions so load pull data is needed to obtain optimum load impedance (see equation (5.1)). During the design of our input matching circuit, using small signal conjugate match is still the best way to match the input side to maximize the linear gain of the device under small signal conditions.

5.2 Design, Realization and Results of a Multi-octave Band Amplifier Using the Wideband Matching Network

In this part, design of a wideband amplifier using Chebyshev matching network, which is called Chebyshev matching network without negative feedback (CMwoFB), is presented. Due to the wideband results and ease of implementation, it is decided to use this topology as an initial trial in required amplifier. The first step in the design is to choose a suitable transistor for the design. The transistor size of 4x75 µm was found to be the most appropriate to use in this design among the other options like 4x50 µm and 6x75 µm. The larger transistor means the larger output power capability but using a large transistor increases the matching network complexity by decreasing the impedances of the active device and also its maximum available small-signal gain is smaller than a device with a relatively small size and it will be very difficult to obtain the gain requirement with 6x75 µm transistor. After the choice of the transistor as 4x75 µm, HEMT model extraction is completed and, the bias points are determined from the drawn HEMT I-V curves (see Figure 5.3). The design goal puts the Q-point right in the middle of the saturation region where $V_{ds}>V_{gs}-V_{knee}$. In addition maximum available gain is checked for the chosen bias points. The amplifier was biased as Class-A. Class-A amplifier has higher gain and higher output power than Class B or Class C but the drain efficiency theoretical limit is 50% (in Class-B this theoretical limit is as high as 78%). Since for this design we want to obtain 7 dB gain with one stage and 27 dBm output power, the best choice is Class-A amplifier. To employ the Class-A, the quiescent current is selected at the half of the maximum drain current swing which is about 80 mA. The drain-source voltage is chosen as 15 V and gate bias voltage is chosen as -2.7 V. Hereby, the determination of operating points are completed.

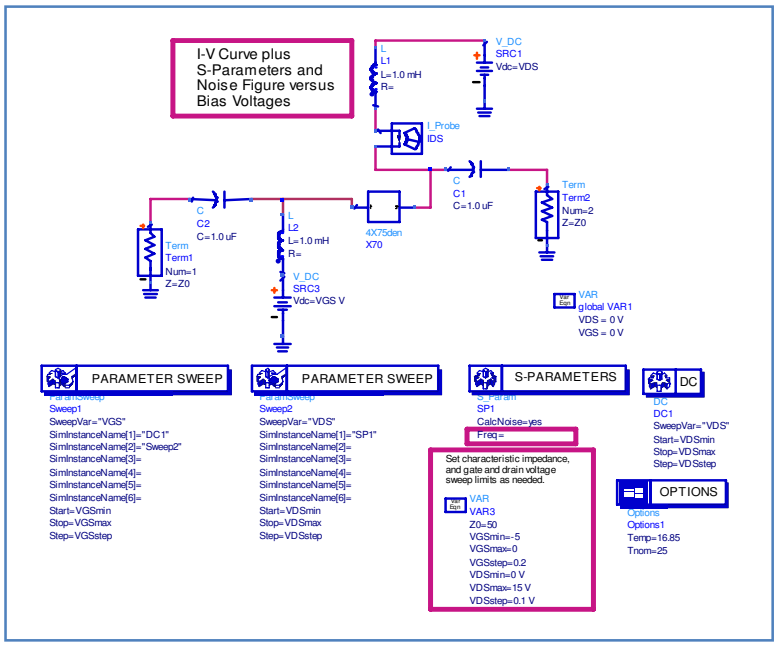


Figure 5.2 Circuit schematic that is used to draw I-V traces.

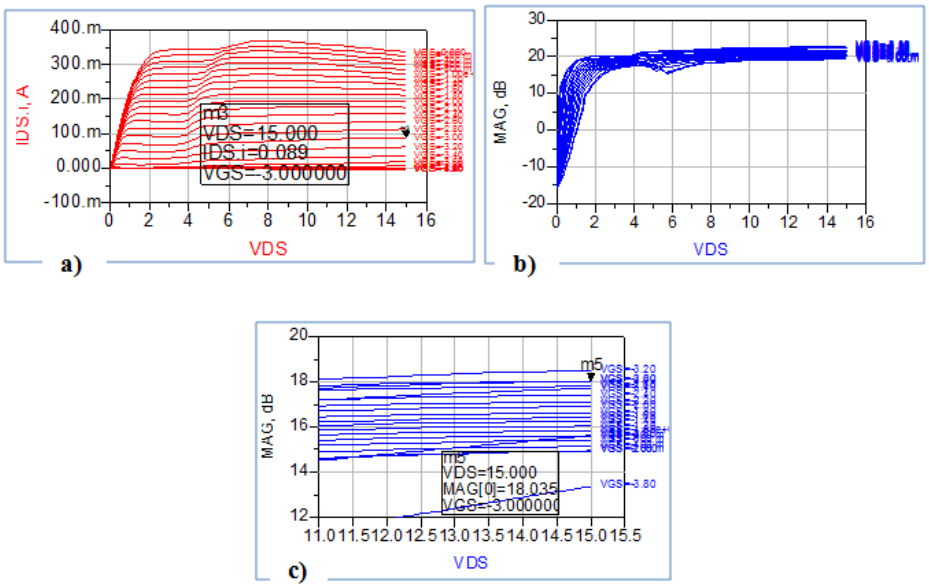


Figure 5.3 a) Drain current versus gate voltage and drain voltage b) Maximum available gain versus gate voltage and drain voltage c) The zoomed version of the plot.

After determining the bias point, the next step in the design is to make the device unconditionally stable for the whole frequency range to avoid unexpected oscillations. If the input (or output) reflection coefficient is larger than 1 in magnitude, the possibility of getting an instable device increases since a

reflection coefficient larger than 1 implies the existence of a negative resistance. To achieve unconditional stability, stability factor, K must be analyzed not only at the interested frequency range but also at other frequencies where the amplifier is potentially unstable. The stability factor (K), the stability circles for source and load is investigated to satisfy the unconditional device stabilization by adding a parallel capacitor to series resistor at the input. Since the unstable region of our transistor is at low impedance side and for power amplifiers, it is not preferable to add resistors at the output since it degrades the power performance; we prefer to add a series resistor in parallel with a capacitor at the input side. By selecting the value of the capacitor such that it shorts the resistor at high frequencies and it is negligible at low frequencies, loss due to resistor at high frequencies are minimized. The resistance value is selected by considering loss at high frequencies and the stability condition. Actually, the small-signal gain of our 4x75 μm transistor is 13.5 dB at 6 GHz while it is around 6 dB at 18 GHz so this stabilization network can be used for the gain equalization by preserving the gain at high frequencies by the help of the capacitance. The stabilization network are designed with ideal circuit components and then they are realized with Coplanar waveguide elements (CPW) and simulated by using the ADS's Momentum simulation tool (see Figure 5.4). All the matching networks, stabilization networks and bias networks designed are simulated and optimized using Momentum but the design process starts with ideal elements initially.

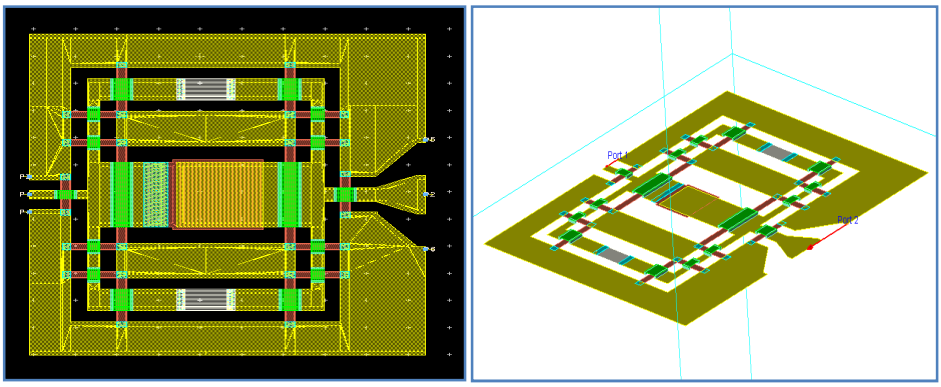


Figure 5.4 Stabilization network layout in Momentum and stabilization network view using 3D-EM viewer.

Biasing is required to operate the transistors in their active regions with the necessary quiescent current so designing the bias networks assigning the selected transistor with the selected bias voltages is the next step in the MMIC design. Bias circuits must not be sensitive to transistor parameter variations since the operation point may change due to transistor parameter fluctuations. To decrease sensitivity to the parameter variations in transistors, using a resistor at the source can be a method but in our case, our transistor's source is already grounded and it is not suitable to add resistor to the source. In order to isolate the bias lines from the matching circuits, short circuited hi-impedance (100-120Ω) λ/4 transmission lines can be used since a shorted transmission line with a λ/4 length behaves like an open circuit at the operating frequency but it does not work for our design due to the wide frequency band. Inductors can be used as radio frequency chokes (RFC's) with bypass capacitors (2 pF). By using inductors wide bandwidths can be obtained. The drain and gate bias circuitries were designed using large rectangular coplanar waveguide inductors with a self-resonant frequency (SRF) that is greater than the frequency of operation. Using an inductor as a bias feed is much more preferable technique to get high gain and linearity [79]. Since no gate current will flow in FET's, unlike BJT's, it is possible to add a large resistor (around 500 Ohm) between gate and the coupling capacitor to ground, this resistor can serve as gate bias feed. Using a rectangular

inductor as RFC or using a large resistor at the gate bias line is possible. Additionally, adding a small series resistance (10-15Ω in our designs) to the gate bias line, between bypass capacitor and gate bias point enhances the stability at low frequencies so generally we added a small resistance to the gate bias line to be far from the instability at low frequencies. Since passive devices are used in bias lines, passive device characterization is important to design the bias circuits with well-characterized inductors. In order to characterize bias circuit, ADS momentum is used as in the case of the other passive circuitry. In this realization, the bias lines with RFC and bypass capacitor are chosen, since this topology fits best when overall response is considered. Layout of the gate bias network and drain bias network are given in Figure 5.5 and Figure 5.6, respectively. As seen from the simulation results, the loss due to bias lines are less than 0.3 dB at 18 GHz, since gain at 18 GHz limits our performance, the bias lines are optimized according to 18 GHz performance not according to 6 GHz performance.

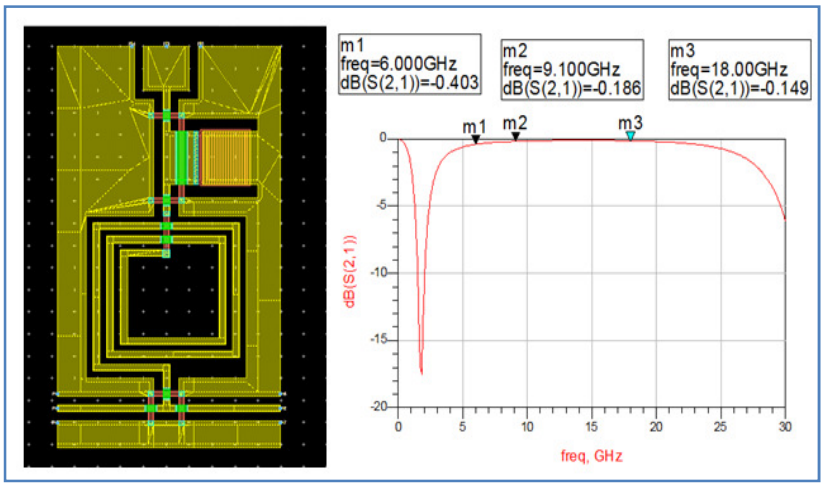


Figure 5.5 Layout of the gate bias network and forward gain voltage.

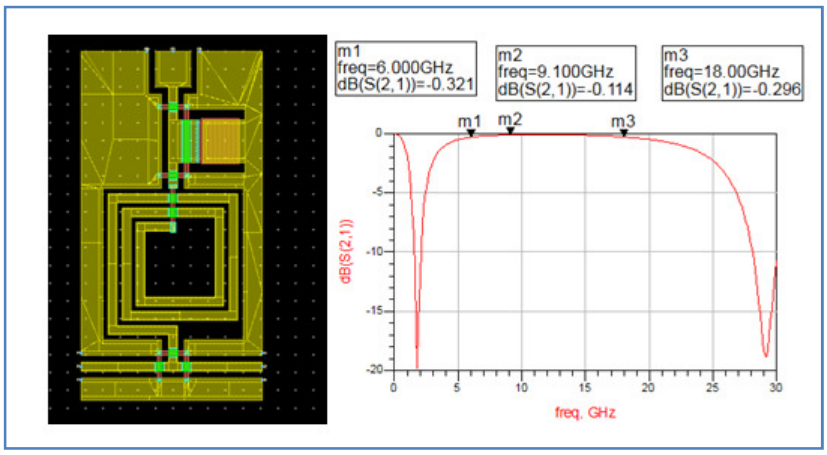


Figure 5.6 Layout of the drain bias network and forward gain voltage.

The next step is the most challenging step in the amplifier design which is the design of the matching circuits at the input and output. In power amplifier design, small signal approximation is not valid but as already outlined we can still use this approximation on the input side of a Class-A amplifier. Reactive matching topology was found to be the most appropriate topology for the first realized wideband MMIC. The stabilization is followed by load-pull and source-pull simulations. These simulations were performed with this iterative approach to get the optimum load and source impedances after the realization of the stabilization and bias networks. The basic idea behind the load-pull simulations

is to investigate the device large-signal performance by varying the load impedance seen by the transistor since the output impedances for maximum gain and maximum power are different. Similarly source-pull simulations are made by changing the source impedance seen by the device. Load-pull and source-pull simulation results at 12 GHz are given for a 4x75µm HEMT in Figure 5.7. The maximum power delivered 29.8 dBm with power added efficiency of 46.2% when the input power is 20 dBm for optimum load impedance termination of (70.13+j59.03Ω).

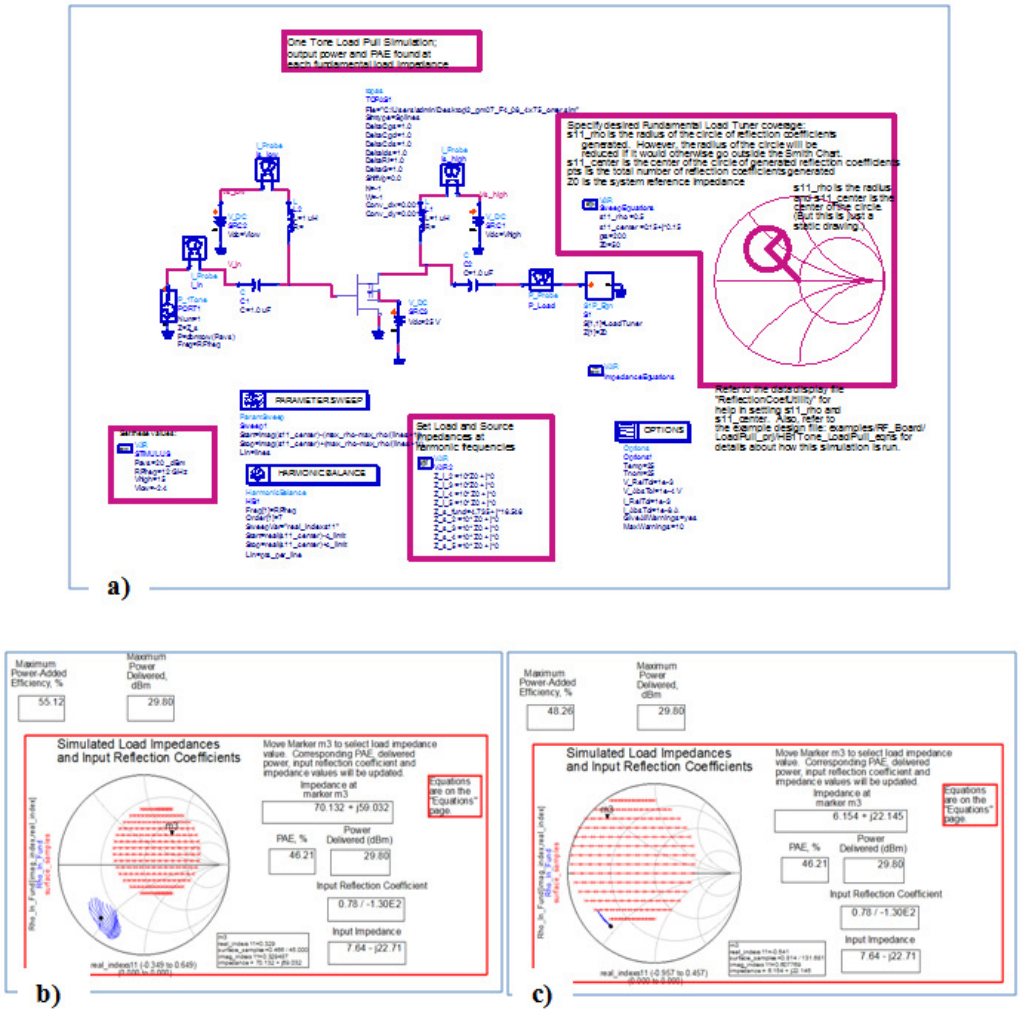


Figure 5.7 (a) The circuit schematic that is used for load-pull simulations (b) Load-pull simulations performed at 12 GHz (c) Source-pull simulations performed at 12 GHz.

Table 5.1 shows the simulation values of source and load impedances at drain bias of 15V, and drain current 72 mA. Due to the choice of GaN technology, source and load impedances are not so far from the 50 Ω system impedance and realization broadband matching would not require high impedance transformation ratio so the complexity of the wideband matching topology decreases compared to MMICs realized with GaAs technology [81].

Frequency (GHz)	Zsource	Zload
6 GHz	45+j35.5	83+j65
8 GHz	45+j35.5	67+j75.3
10 GHz	46.4+j27.8	67+j75.3
12 GHz	47.8+j20.5	59+j60.4
14 GHz	47.9+20.5	42+j55.6
16 GHz	47.9+j20.5	42+j55.6
18 GHz	49+j13.5	35.3+j58.4

Table 5.1 Source and load impedances obtained from load-pull and source-pull simulations.

Obtaining a flat gain response in our specifications is extremely important so in addition to gain equalization network, input and output matching topologies were optimized for this purpose. The aim for this amplifier is to achieve small signal gain of 7±1 dB for 6 GHz-18 GHz frequency band. As stated before, while designing an amplifier covering a broadband frequency range, wideband network synthesis method can be implemented with multi-section co-planar matching elements. The output matching network is designed by taking consideration into load-pull simulation data at certain discrete frequency points

(6, 8, 10, 12, 14, 16, 18 GHz) over the entire bandwidth using five section band-pass Chebyshev-type matching circuitry. The output matching network utilizes from multi-section components like rectangular inductors and open stub CPW lines. Open circuit CPW lines are used instead of MIM capacitors due to better matching performance at frequency of 18 GHz. Although it is possible to use short circuited stubs instead of coplanar rectangular inductors in output matching circuitry, it was not preferred since it affects the broadband response negatively. The input matching circuit was realized by supplying a simpler and minimized matching topology using reactive matching circuit with gain equalization network. Similar to the output matching network, shunt capacitances are realized as open stub CPW line instead of MIM capacitors. The MIM capacitances are used as DC block capacitances (see Figure 5.8).

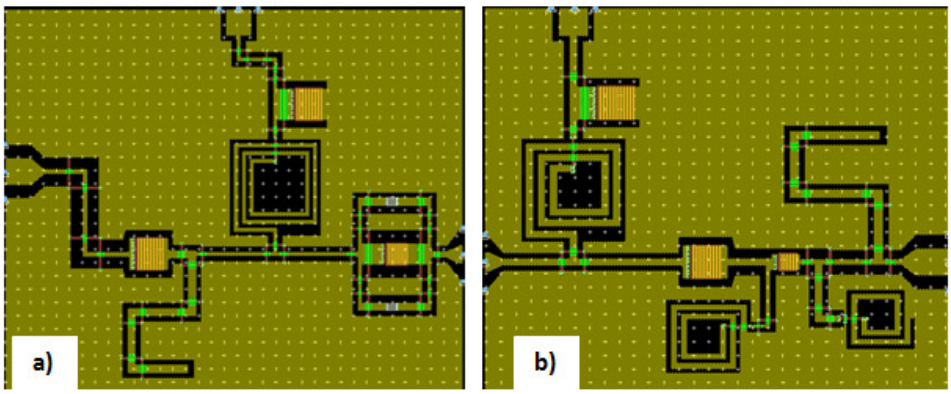


Figure 5.8 The realized coplanar a) input and b) output matching networks with bias networks using network synthesis method.

After designing the input and output matching circuits, harmonic balance (HB) simulations are performed to observe the large-signal performance of the device and to optimize the design. The schematic used in these simulations are given in the following Figure 5.9.

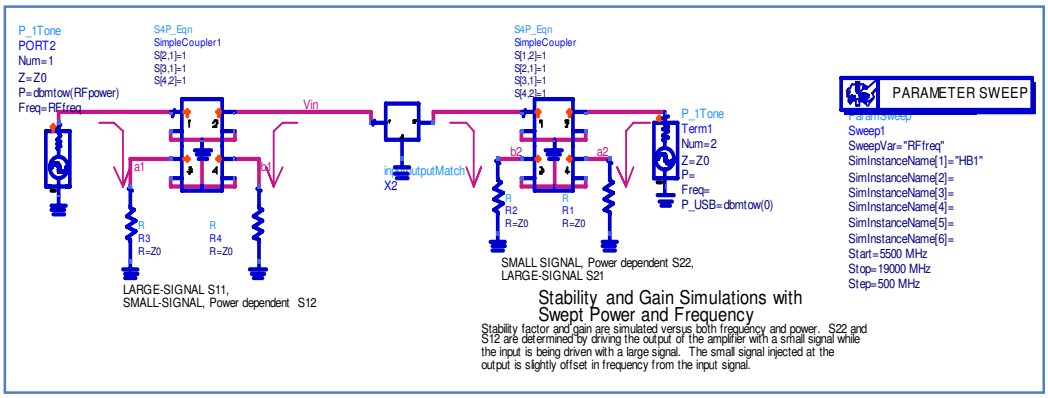


Figure 5.9 Circuit Schematic provided by ADS design guide to implement HB simulations.

The large signal gain of the amplifier is drawn while sweeping the input power level for different frequency levels. ADS harmonic balance simulation results of the amplifier under different input power conditions for 6GHz, 8GHz, 10GHz, 12GHz, 14GHz, 16GHz and 18GHz are given (see Figure 5.10).

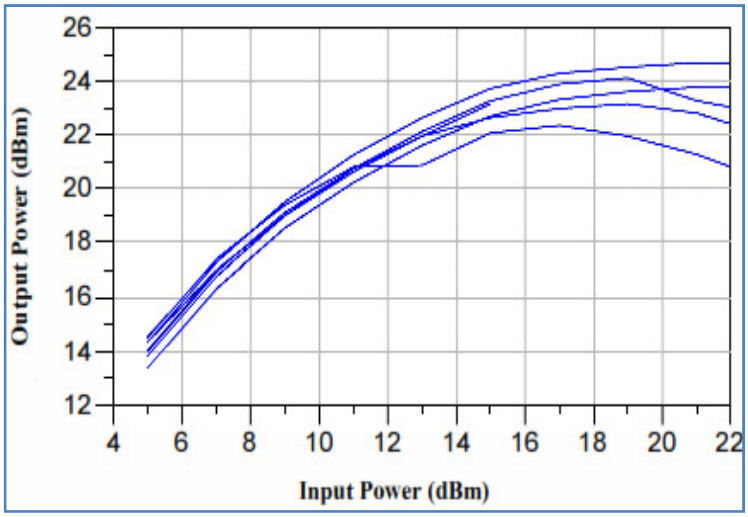


Figure 5.10 Simulated CW power versus input power at different frequencies.

Under high input RF power, the large signal gain of the amplifier stays within 2 dB which means that gain ripple level at high power levels is tolerable over the entire bandwidth. The performance of the MMIC amplifier is simulated accurately using Momentum simulation tool of Agilent's Advanced Design System (ADS). Figure 5.11 is the photograph of our fabricated GaN MMIC

amplifier in NANOTAM's clean room. The chip size of the device is 3.5 mm x 1.5 mm.

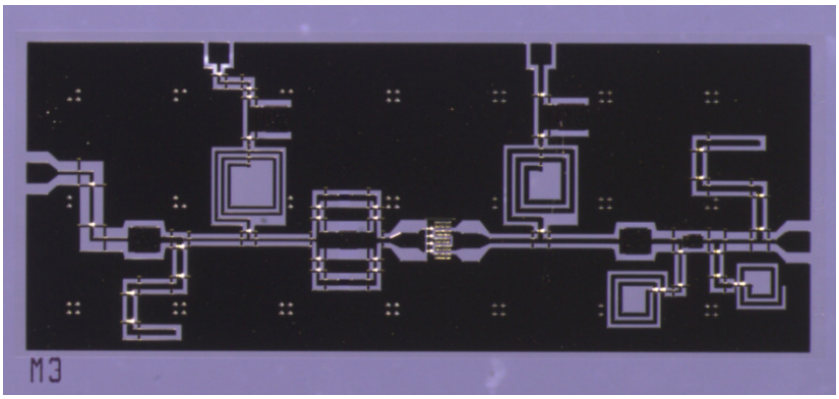


Figure 5.11 Photograph of the first fabricated GaN MMIC amplifier using network synthesis method.

The small-signal response of the Chebyshev Impedance matching without feedback (CMwoFB) amplifier is compared with the simulated small-signal response including the small-signal gain (S_{21}) (see Figure 5.12). In both simulation and measurement drain voltage of the amplifier is taken as 15V. The design goal for the small signal gain was 7±1 dB. The measured small signal gain varies between 6.3 dB and 7.5 dB within the entire frequency band. We have demonstrated that the resulting device with five section Chebyshev matching at the output and 3 section Chebyshev matching at the input satisfies the gain ripple specifications, also the results showed that fabrication gives compatible outcomes with the simulated small signal gain, input and output return losses.

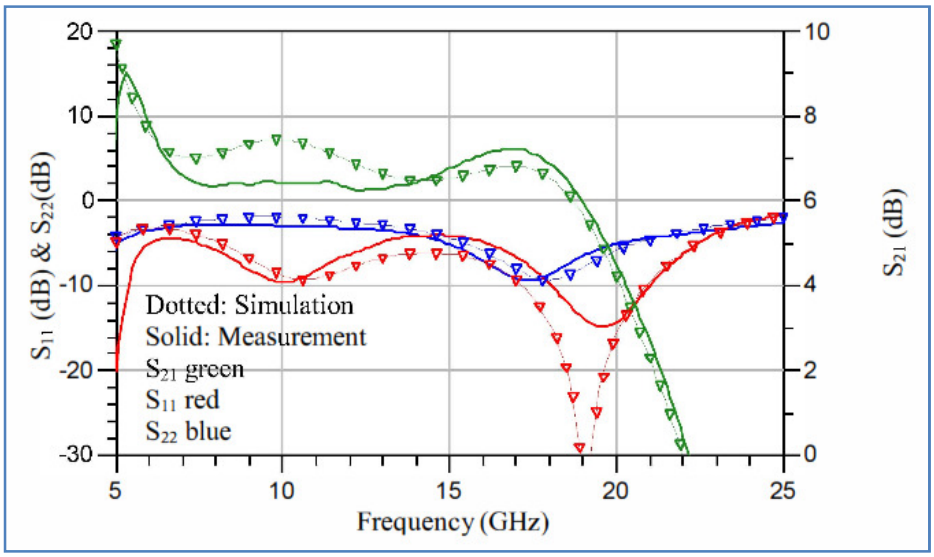


Figure 5.12 S- parameters (S21 (green), S11 (red) and S22 (blue) of the first realized MMIC from the simulation (dotted line) and the measurement (solid line).

Figure 5.13 demonstrates the output power and the drain efficiency of the MMIC for the swept CW input power for different frequencies. Drain efficiency, which is determined by the ratio of output RF power to input DC power, is a measure of how much DC power converted to RF power. In order to examine the point where the gain of the amplifier deviates from the small-signal gain by 3 dB which is called 3 dB compression point since the gain starts to fall off as the input signal level increases. That is, the gain compression at 3 dB compression point as a figure of merit is investigated to characterize the power handling capability. Output power of 24.5 dBm at 3 dB compression point is achieved over the desired frequency band.

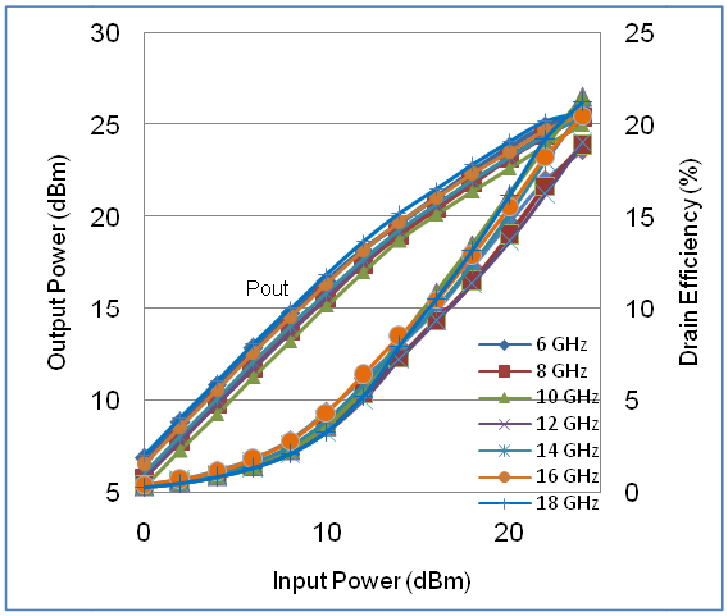


Figure 5.13 Measured CW output power and drain efficiency versus input power at different frequencies.

As a result, a multi-octave band GaN-HEMT MMIC amplifier has been presented with reactively matching topology. For the bandwidth of 6-18 GHz, a small signal gain of 7 ± 0.75 dB and output power (at 3 dB compression point) of around 316 mW in CW mode are obtained. The primary goal of this preliminary amplifier design was to observe the amplifier performance realized with a single transistor using wideband Chebyshev matching network and also observe the consistency between the simulation and measurement results.

5.3 Design and Realization of Multi-octave Band Amplifiers Using the Chebyshev Impedance Matching with Negative Feedback

In this part, design of 6 GHz–18 GHz MMIC amplifiers with negative feedback (CMwFB, PT) topology is proposed. Chebyshev matching technique with

feedback is proposed in the following two designs in order to increase the bandwidth. In addition to the amplifier designed with a single HEMT (CMwFB), Chebyshev matching technique with feedback is also applied for the amplifier designed with two transistors in parallel (PT) to increase the output power. The wideband MMIC with two paralleled transistors (PT), which is introduced in this section, is our first trial that is supposed to achieve our design goals. In section 5.4, a comparison of the measurement results of the designs mentioned in section 5.2 and this section (section 5.3) is made. After getting a reasonable feedback from the measurement results of these designs and gaining more practical insight about the process variations, the first trial with two paralleled transistors has modified. As a result, all of the design specifications are satisfied with this final design run, which is mentioned in section 5.5.

The shunt feedback was implemented in our MMIC design because the active device topology is not suitable to add a resistor to the source. Therefore, we used only shunt feedback circuitry in our MMIC designs to widen the frequency bandwidth. When the resistive shunt feedback is introduced, phase difference between the drain and gate voltages will be less than 180^o at high frequencies. This can cause to positive feedback in the amplifier resulting in oscillation. To prevent possibility of instability, the combination of a resistor and an inductor can be recognized in the feedback line. Since inductor introduces 90^o phase, the phase difference between the drain and gate will be less than 90^o. In addition capacitive degeneration can be used to increase the frequency bandwidth of the amplifier with a constant gain-bandwidth product [82], [83]. The shunt feedback must have a high-pass characteristic since DC potential at the gate and drain of a HEMT are not equal. Our MMIC amplifiers, which are designed using negative feedback approach, are realized employing a shunt RLC path as shown in Figure 5.1.

HEMT used in all the amplifiers has the gate dimension of 4x75 µm with gate length of 0.25 µm. All of the mentioned designs includes parallel connected RC network in series, this network both equalizes the gain in the band of interest

(6 GHz – 18 GHz) and increases the stability. The input and output matching of all the amplifiers are band-pass Chebyshev type matching in order to increase the bandwidth. Rectangular coplanar inductors were used in the bias lines with a chosen line width considering the current carrying capacity. The bias circuitry is the same as the previous amplifier topology and since design details of the bias circuitry is given in the previous section, it is not repeated.

The first MMIC design (CMwFB) is realized with the degenerative feedback stabilization that includes series RC network, in order to increase the bandwidth of the MMIC. By this technique, input and output impedances of the transistor are closer to 50 Ω system impedance and ultra wideband matching by employing less complex matching circuits is possible. Parallel RC circuit is used both for gain equalization and stability enhancement purposes. With this network, input return loss is relatively better and gain is flatter (±1 dB) over the whole bandwidth. Also, in this topology, the sections of the output matching circuit is considerably decreased because of the effect of negative feedback topology and the chip area is decreased compared to the one without parallel feedback.

In the third design higher output power is aimed and to achieve this goal, two paralleled 4x75 µm HEMTs is used with shunt RC feedback topology. Symmetrical shunt RC feedback is introduced in order to stabilize the gain of the amplifier against parameter changes in the HEMTs due to the variation of biasing condition. The photographs of the fabricated MMICs are shown in Figure 5.14.

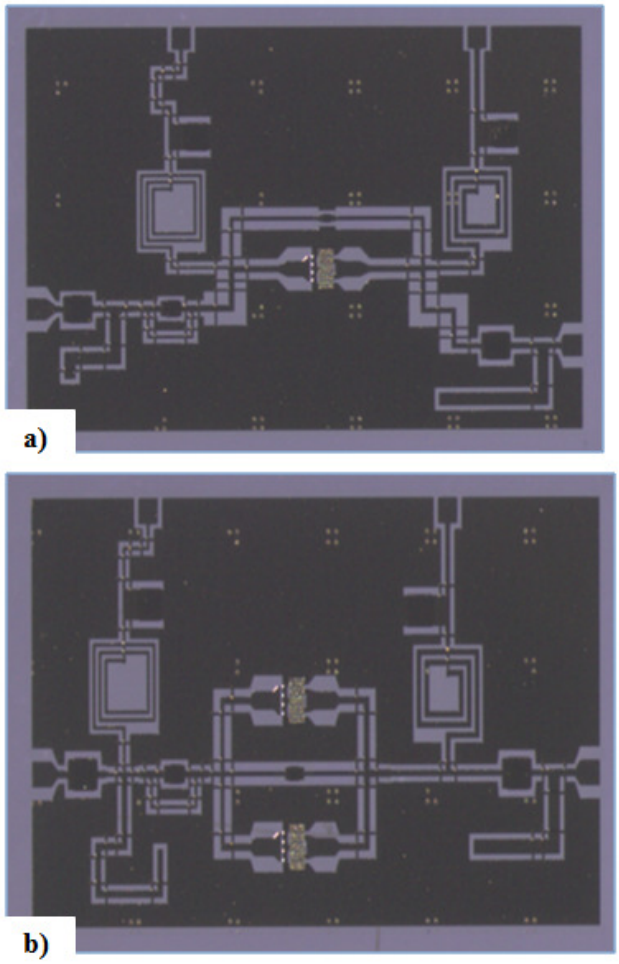


Figure 5.14 Photograph of (a) the GaN MMIC CMwFB and (b) the GaN MMIC PT.

The measurement results for the amplifiers discussed in this section are given in the following section. Since the next section is devoted for comparisons of the designs by means of the small-signal and the large-signal performances of the amplifiers. Not to repeat the measurement results, it is preferred to give the measurement results of the amplifiers, which are mentioned in this section, in section 5.4.

5.4 Comparison of the realized Multi-octave Band Amplifiers

Performance evaluation of the designs with Chebyshev impedance matching without feedback (CMwoFB), Chebyshev type matching introducing shunt feedback circuitry (CMwFB) and Chebyshev type matching using two paralleled transistors with shunt RCL feedback (PT) is given in this section. These designs are implemented before the final design trial to observe the effect of the negative feedback and the effects of variations that come from fabrication. The small-signal gain of the amplifier (using a single 4x75 μm HEMT) with feedback (CMwFB) is measured as 7.5 ± 2 dB while the small-signal gain of the amplifier (using a single 4X75 μm HEMT) without feedback (CMwoFB) is measured as 7.9 ± 0.4 dB for the band of interest (6 GHz - 18 GHz). The small signal gain of the amplifier (PT) designed with two parallel HEMT is 6.7 ± 1.3 dB. The measured and simulated small-signal responses (S_{21}) of the MMIC amplifiers CMwoFB, CMwFB and PT are depicted in Figure 5.15. The drain voltages of the amplifiers are adjusted to 15V in both simulations and measurements.

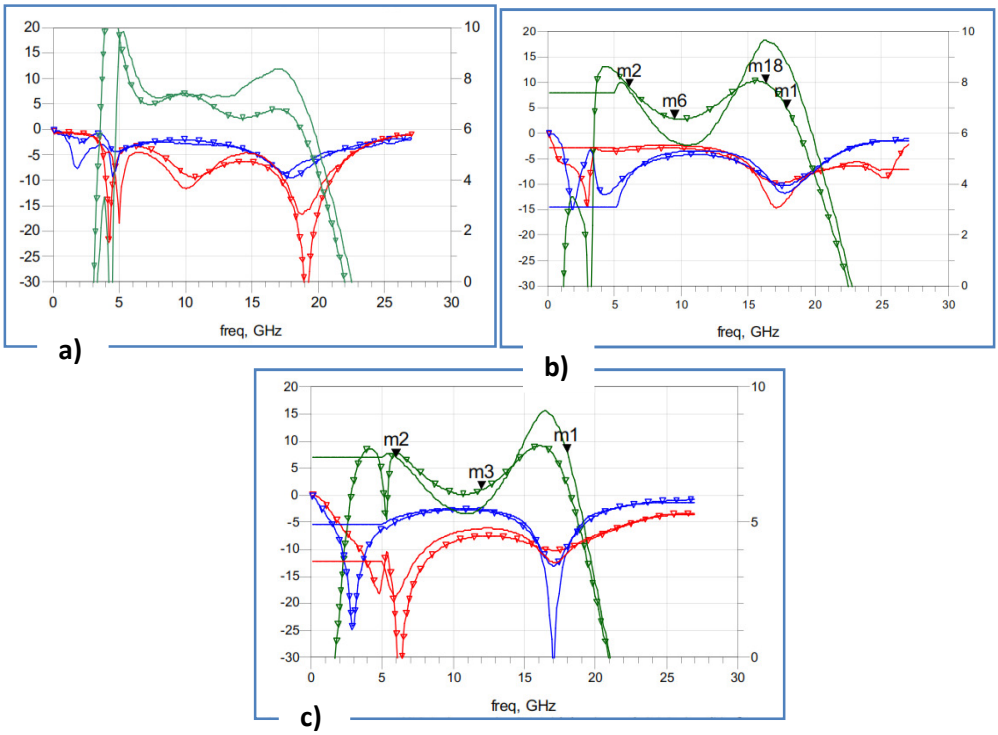


Figure 5.15 S- parameters a) S21(green),S11(blue) and S22(red) of the MMIC CMwoFB b) S21 (green),S11 (red) and S22 (blue) of the MMIC CMwFB c) S21 (green),S11 (blue) and S22 (red) of the MMIC PT (simulations (dotted line) and measurements (solid line)).

The response of the MMIC CMwoFB is better than MMIC CMwFB and PT designs in terms of gain flatness, however in CMwoFB the output matching circuit includes more sections since wideband matching without feedback is much more difficult. The designs with feedback stabilization are lack of flatness specification due to the fact that, the fabricated gain equalization and feedback RC network differs from the simulated RC network especially, the impedances of resistors show capacitive property. Ordinarily, feedback technique is widely used to have high practical input and output impedances at wide frequency range, however, the feedback network that we practiced consists of small capacitance and large resistors thereby the feedback is not as effective as we expected to improve the impedances and band ripple performance. The small signal gain performance comparison of MMIC CMwoFB, MMIC CMwFB and MMIC PT amplifiers are provided in Table 5.2.

Amplifier type	Small signal gain	Gain ripple	Chip area
CMwoFB	7.5dB-8.3dB	±0.4 dB	3.6mmx1.4mm
CMwFB	5.5dB-9.5dB	±2 dB	2.8mmx1.8mm
PT	5.4dB-9.0dB	±1.8 dB	2.8mmx1.6mm

Table 5.2 Comparison of the small-signal performances of the amplifiers realized so far.

Figure 5.16 shows output power and efficiency of the MMIC PT under CW input power at different frequencies. Output power of 27.3 dBm at 3 dB compression point was achieved over the intended frequency band. The output power at 6 GHz and 18 GHz are even better than the middle of the frequency band with an output power of around 1W at 3dB compression.

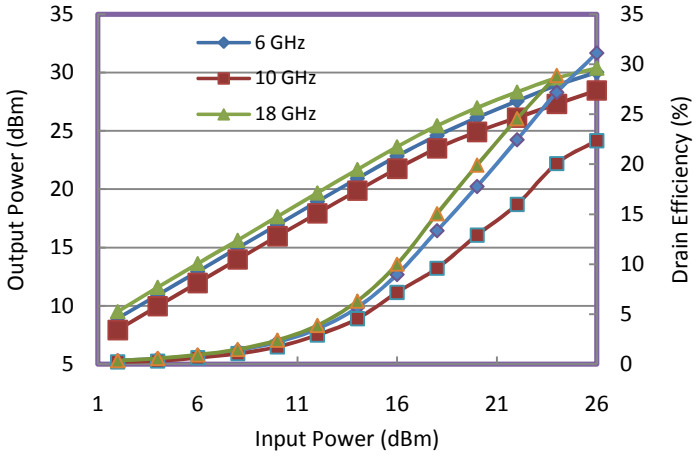


Figure 5.16 Measured CW output power and drain efficiency vs. input power at 6 GHz, 10 GHz, 18 GHz.

The power performances of the amplifiers are given in Table 5.3. As seen from this table, MMIC amplifier PT has the highest output power as expected since it has two transistors in parallel. The saturated power of MMIC PT should be 3 dB higher than the amplifier CMwFB but due to the combination losses this increase is around 2.7dB. Also the amplifier CMwoFB and CMwFB are

expected to have the same saturated output power but the first one has 0.3 to 0.5 dB less saturated output power, this is because of the complexity of the output matching, since the output matching of the former one has more elements, the total loss at the output matching circuit is higher in CMwoFB amplifier, CMwFB topology makes it possible to obtain the required matching with less elements and with less loss. So, as due to this, final topology is chosen to be CMwFB with parallel transistors.

Input power (dBm)	Output power of CMwoFB@6GHz (dBm)	Output power of CMwoFB @18GHz (dBm)	Output power of CMwFB @6GHz (dBm)	Output power of CMwFB @18GHz (dBm)	Output power of PT @6GHz (dBm)	Output power of PT @18GHz (dBm)
10	17.55	17.9	17.8	18.1	16.94	17.65
16	22.08	22.5	22.32	22.75	22.83	23.62
20	24.79	25.05	25.05	25.3	26.1	26.96
24	26.7	26.70	26.9	27.1	28.9	29.52
26	27.04	27.1	27.30	27.5	30.03	30.37

Table 5.3 Comparison of the large-signal performances of the amplifiers realized so far.

At 3 dB gain compression, minimum of 320 mW output power for single transistor designs and minimum of 600 mW output power for parallel transistor design is obtained for the band of interest. At 18 GHz higher than 1 W output power is obtained with power added efficiency above 30%.

With these results it can be concluded that, in order to achieve the output power goal, it is necessary to use parallel transistors, however when parallel transistors are used, wideband matching and gain flatness goals are more difficult to obtain. Since, for CMwFB topology, matching is easier and it can be

obtained using relatively less elements, it is decided to use CMwFB with parallel transistors to satisfy the design requirement. It is seen that one more design effort should be carried to obtain the final MMIC considering the results of these topologies and including the process variation effects.

5.5 Design, Realization and Results of the Final Wideband Amplifier Using the Negative Feedback

In this section, the final wideband amplifier design, which satisfies all the specifications of the project, is given. This amplifier was revised regarding the previous design results and variations which may come from fabrication. To ensure the output power criteria, two 4x75 μm HEMTs in parallel were used in this design and drain current is adjusted around 160 mA (80 mA for each transistor). In order to obtain a flat response with two parallel transistors, using negative feedback is thought to be necessary, however the layout and the element values of the feedback topology is optimized to minimize the gain ripple in the frequency band.. In Figure 5.17, stabilization network layout used in this design is shown. Green, red and grey colored fragments in the layout symbolizes airbridge, under-pass metal and resistor, respectively. This negative feedback network was composed of two capacitors, which have the same dimensions, and a resistor of 60 Ω as being fully symmetrical. It was simulated in Momentum just as a block.

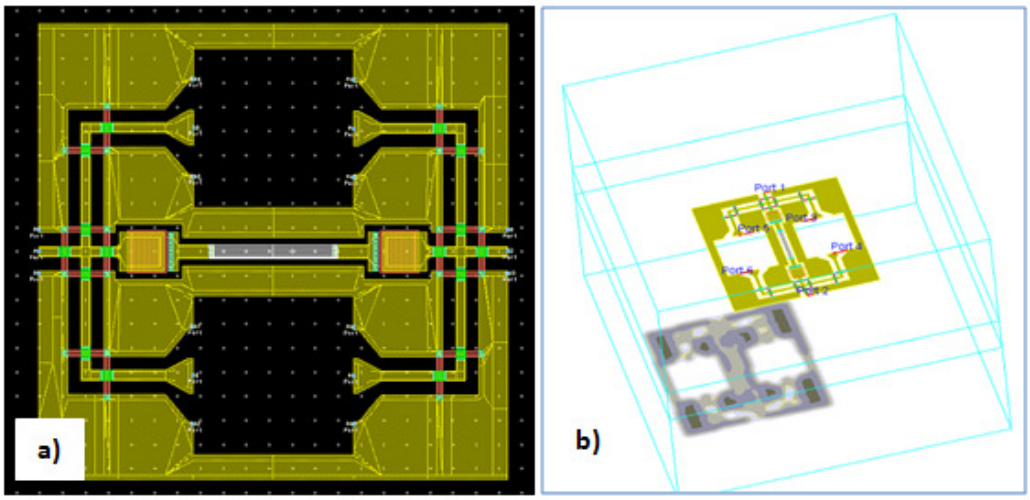


Figure 5.17 The negative feedback network layout a) in Momentum b) in 3D EM viewer.

After paralleling two transistors and introducing a negative feedback, the next step is to design the bias lines. Bias lines were not embedded to the matching circuit. The previously mentioned drain bias lines were also used in this design but at this time the gate bias was given through a resistor which also serves for stabilization and gives better simulation results in terms of gain flatness, since the frequency response of the resistor is flat where as the frequency response of an inductor is not (see Figure 5.18).

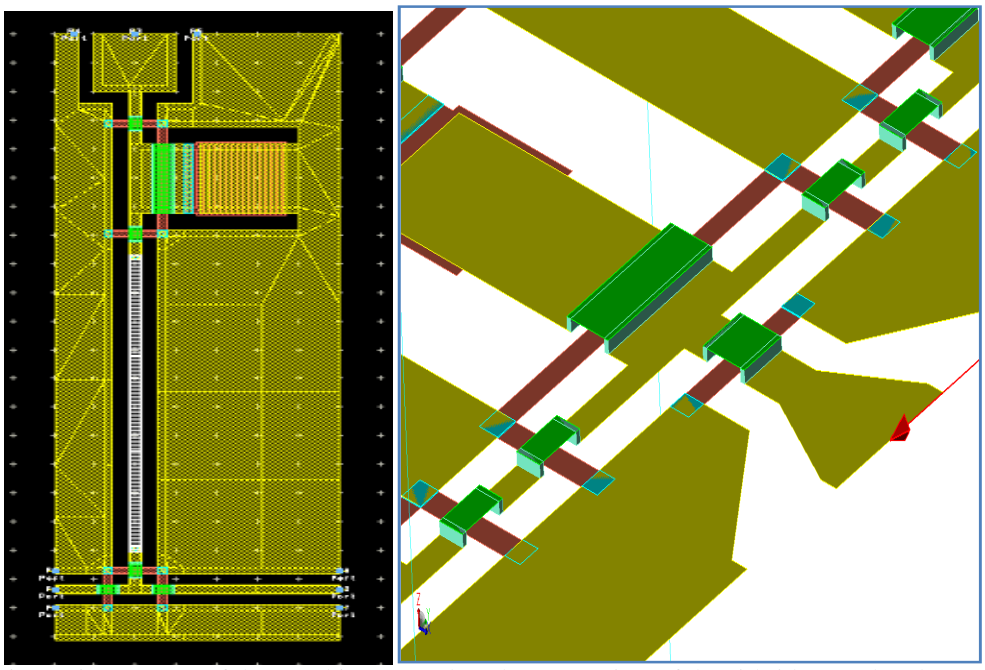


Figure 5.18 Layout of the gate bias network and 3D EM view of the airbridges and underpass metals for visualization.

To get a better idea about the optimum impedances, we prefer to renew the load-pull and source-pull simulations by replacing ideally paralleled transistors with the Momentum results of the given feedback network. Optimum load impedances of two parallel transistors are like in the following Figure 5.19.

As frequency increases, the real physical circuits describe traces that follow clockwise direction on the Smith Chart but our optimum load impedance trace follows counter clockwise frequency direction. This is one of the biggest challenges in this design since as we are trying to match the impedances at high frequencies, matching the lower frequency impedances is becoming much more difficult due to this reverse motion of the load impedance trace.

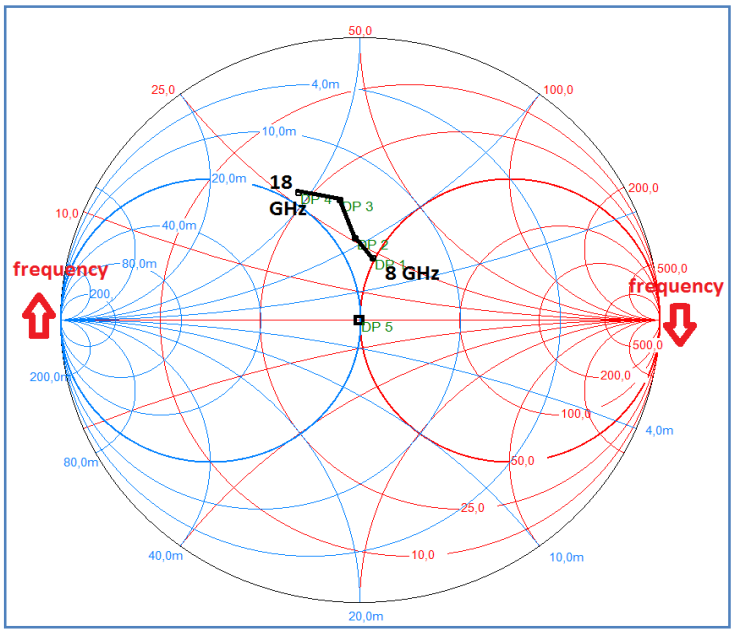


Figure 5.19 Optimum load impedances of two parallel transistors from 8 to 18 GHz.

The input and output matching networks are designed with ideal elements and then realized and tuned in Momentum with coplanar elements as separate segments. The input matching layout in Momentum is given as two separate segments as you can see from Figure 5.20.

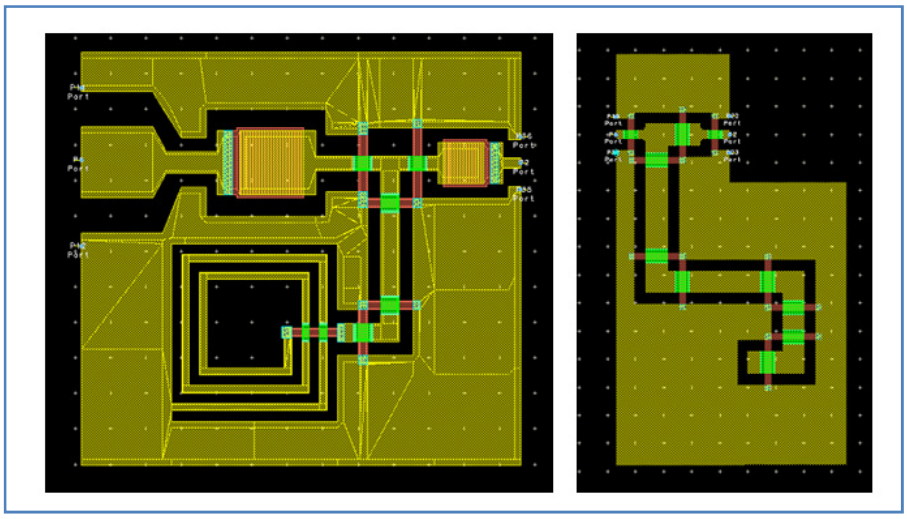


Figure 5.20 Input matching network for the final design as two segments.

The output matching impedances are determined using load-pull analysis like previous designs. For various input power levels, load-pull impedances are investigated but the convergence of our models are limited so we just swept our input power level up to 20 dBm. While designing the output matching circuit, the open stub line was preferred instead of shunt MIM capacitor. The fully simulated design with the output matching network is provided in Figure 5.21.

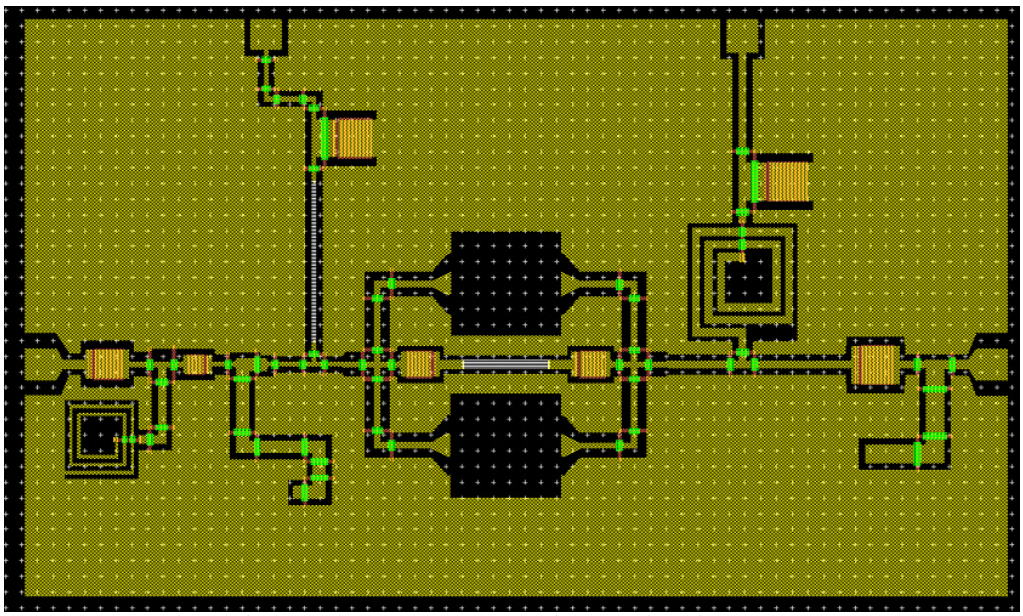


Figure 5.21 Coplanar MMIC layout fully realized in Momentum.

The small-signal simulation results are given in Figure 5.22. The small signal gain of the design is 7.1 dB, 8.1 dB and 5.5 dB at 6 GHz, 12GHz and 18GHz, respectively.

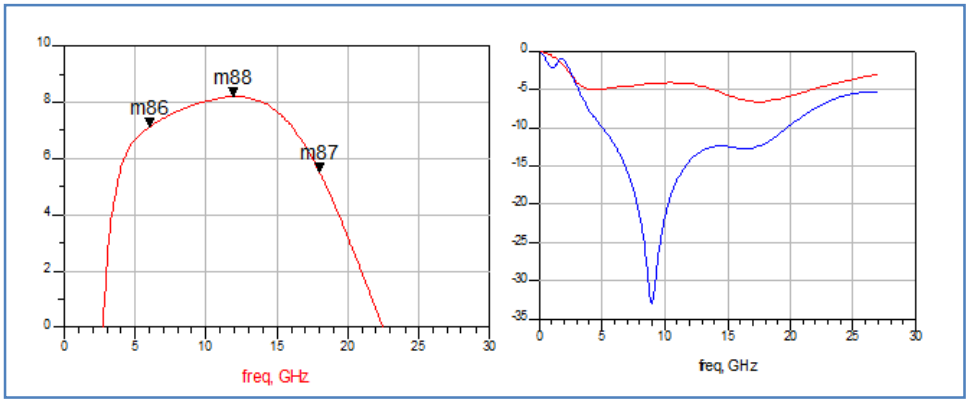


Figure 5.22 The small-signal simulation results of the overall design.

The output power of 27 dBm is obtained under the input power of 22 dBm at 18 GHz from the harmonic balance (HB) simulations. From our previous measurement results, we have an insight about the differences between the measurement and simulation results and a gain increase of 1.5 dB was observed in our measurements when compared with simulation at 18 GHz. Therefore, it is expected that the simulation results of the small-signal gain around 5.5 dB will result in 7 dB small signal gain and the design is finalized with this assumption. The results of the final realized MMIC is given in the next subsection.

MMICs realized and fabricated with two 4x75 μm HEMTs coplanar elements using the negative feedback technique gives the best results in terms of small-signal and large-signal performance of the amplifier. All of the design specifications are satisfied with this final wideband MMIC design (see Figure 5.23). In Figure 5.24, a photograph of the MMIC chip under test is shown.

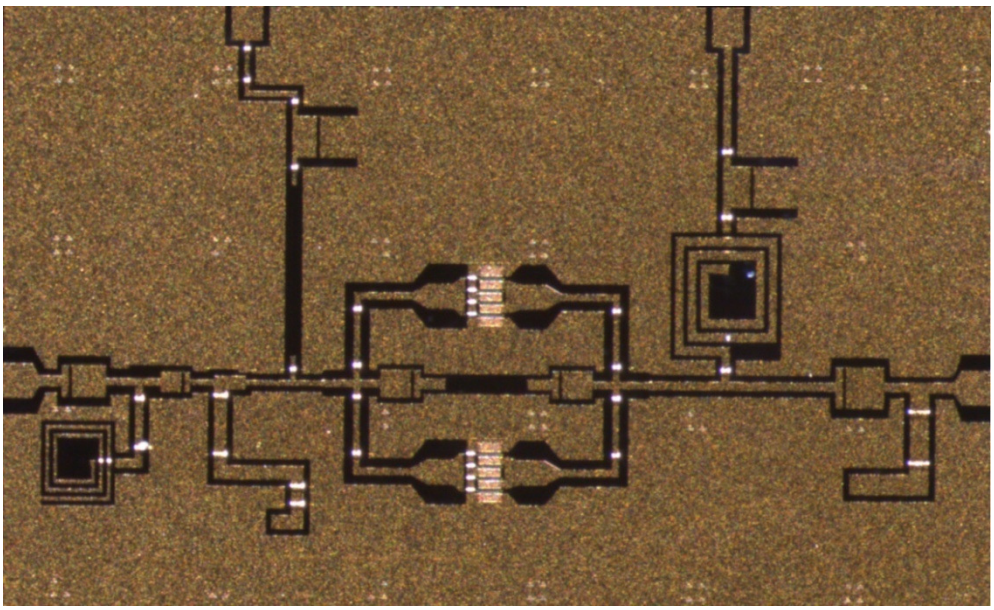


Figure 5.23 Photograph of the final wideband MMIC amplifier after the fabrication.

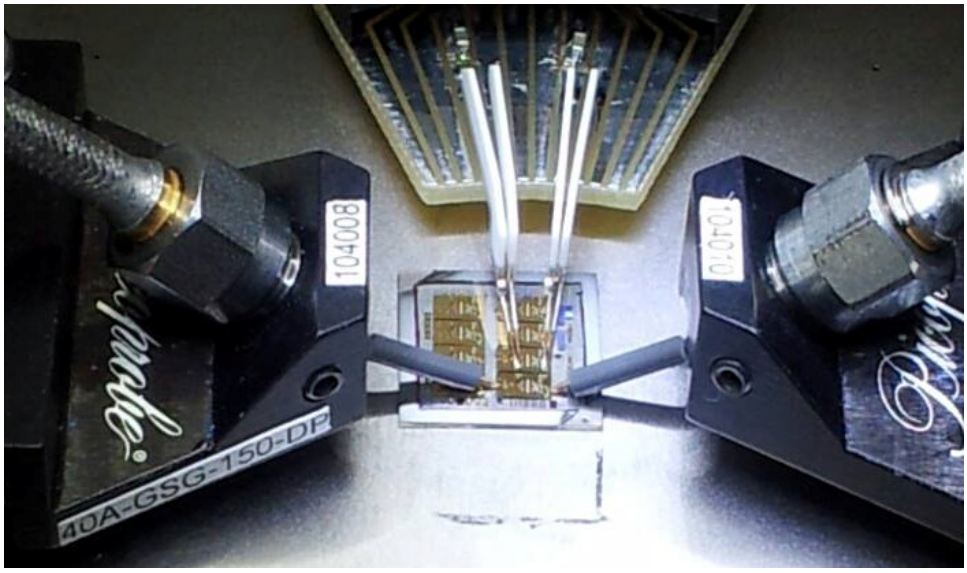


Figure 5.24 Photograph of the MMIC chip under test.

The small-signal measurement results are shown in Figure 5.25. The minimum small-signal gain at 18GHz is required to be higher than 7 dB and the maximum gain ripple should not exceed 2 dB. As a result, 7.2 dB of small-signal gain is achieved at 18 GHz and the associated gain ripple for this amplifier is 1.8 dB. These measurement results show the fulfillment of the small-signal design goals successfully.

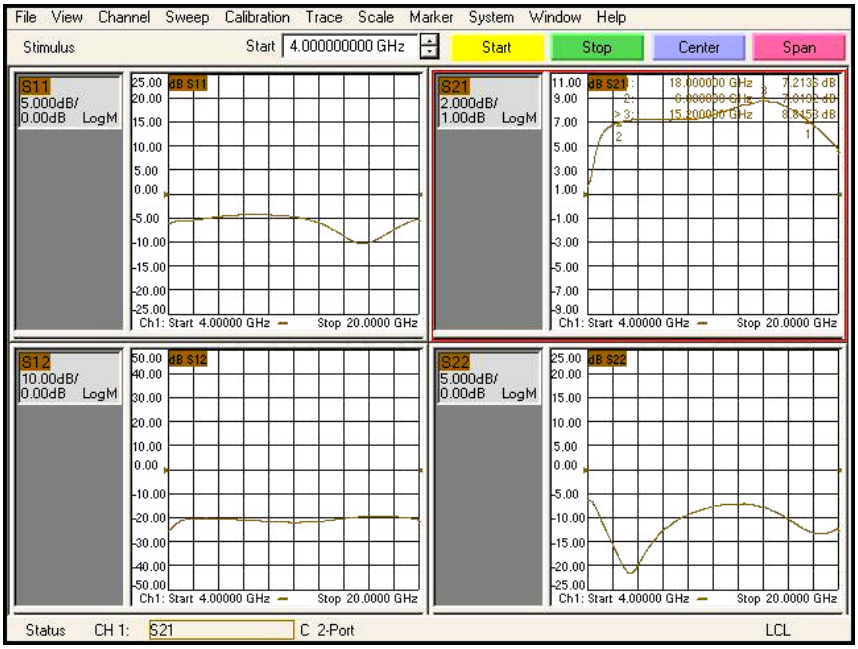


Figure 5.25 Small-signal measurement result for the final design which was designed by using the negative feedback technique.

The output power measurement results of the amplifier are given in the below graph for the various frequencies ranging from 6 to 18 GHz (see Figure 5.26). Minimum output power of 27 dBm at 3 dB compression point was achieved over the whole design frequency band. Power measurements are performed for the same design by choosing different fabricated sets of MMIC chips to investigate the design dependence on the variations came from the fabrication. Therefore, large-signal measurement results which are obtained from the different chips are shown in Table 5.4.

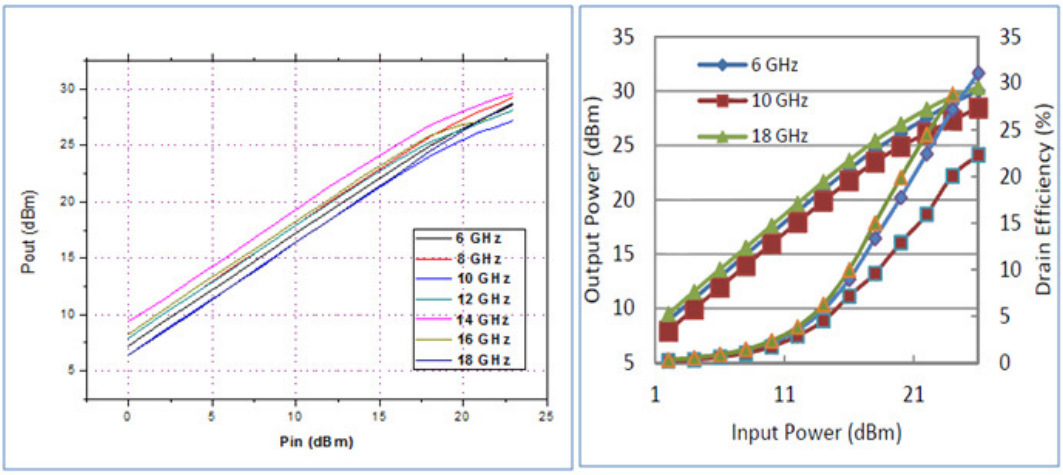


Figure 5.26 a) Output power measurement and b) Drain efficiency results for the final design which was designed by using the negative feedback technique.

	Measured Output Power (dBm)						
Frequency	6 GHz	8 GHz	10 GHz	12 GHz	14 GHz	16 GHz	18 GHz
Chip 1	27.2 dBm @ 1.0 dB komp.	29.2 dBm @ 2.7 dB komp.	27.2 dBm @ 2.2 dB komp.	28 dBm @ 2.8 dB komp.	29.1 dBm @ 2.2 dB komp.	27.1dBm @ 2.1 dB komp.	28 dBm @ 0.3 dB komp.
Chip2	28.4 dBm @ 1.8 dB komp.	29 dBm @ 1.7 dB komp.	27.1 dBm @ 2.3 dB komp.	27.9 dBm @ 3.0 dB komp.	29.6 dBm @ 2.7 dB komp.	28.5 dBm @ 2.7 dB komp.	28.6 dBm @ 0.7 dB komp.
Chip 3	28.7 dBm @ 2.3 dB komp.	29.2 dBm @ 2.1 dB komp.	27.1 dBm @ 2.9 dB komp.	27.9 dBm @ 3.0 dB komp.	29.4 dBm @ 3.0 dB komp.	29.2 dBm @ 2.6 dB komp.	29.0 dBm @ 1.1 dB komp.
Chip 4	28.6 dBm @ 2.0 dB komp.	28.7 dBm @ 2.1 dB komp.	27.3 dBm @ 2.8 dB komp.	27.4 dBm @ 3.0 dB komp.	27.0 dBm @ 3.0 dB komp.	27.2 dBm @ 3.0 dB komp.	27.0 dBm @ 2.9 dB komp.
Chip 5	28.9 dBm @ 1.9 dB komp.	29.3 dBm @ 1.6 dB komp.	27.1 dBm @ 2.2dB komp.	27.9 dBm @ 2.9 dB komp.	29.4 dBm @ 3.0 dB komp.	28.9 dBm @ 2.8 dB komp.	28.8 dBm @ 0.8 dB komp.

Figure 5.27 Output power measurement results for 5 different sets of fabrication.

Chapter 6

Conclusion & Future Work

In this work, the goal was to design, fabricate and characterize a wideband (6 GHz-18 GHz) medium power monolithic microwave integrated circuit (MMIC) amplifier using a 0.25 μm gate Gallium-Nitride (GaN) HEMT technology for radar applications. We used our own fabricated transistors in our designs without using any foundry services.

Firstly, physical and electrical properties of GaN based HEMT devices are examined, the hetero- epitaxial structure is investigated and then the characterization process of the grown epitaxial layers is given. Later the microfabrication process, characterization and large signal modeling of the HEMT devices are performed to employ the model in the simulation environment. The next step is to design a CPW GaN MMIC wideband amplifier as already outlined. For this purpose, wideband design considerations are investigated in detail since the intended frequency range, which is larger than an octave band, is the biggest design challenge in this design problem. In addition, it is critical to note that device modeling since it plays a quite important role to achieve the first-pass success for the amplifier design. In power amplifier design, large signal model is the main concern to get reliable results from the measurements since the more reliable large signal model means the more predictable optimum load impedance for maximum output power. Thus the large signal model consistency of the HEMTs was checked by performing load pull measurements and harmonic balance simulations in ADS at discrete frequency points (6GHz, 8GHz, 10GHz, 12GHz, 14GHz, 16GHz, 18GHz) within the entire frequency range of the amplifier. Several design iterations are

implemented during the design phase to obtain a flatter small-signal gain response and to achieve power requirement specified in the requirements for the entire frequency range from 6 to 18 GHz step by step. However, before going through the design phase of the amplifier, the transistor widths are selected according to our power and gain specifications. The available output power can be maximized by paralleling many transistors or using transistors that are larger in size. When transistor size increases, the gain can decrease due to the parasitic effects and grounding problems, so paralleling two 4x75um transistors are preferred. Paralleling the transistors makes the design of matching circuitries harder due to lower device impedances. Since one of the main goal of our design is 0.5W output power for the whole frequency band, the output matching is optimized to maximize the output power of the amplifier. We proposed a multi-octave MMIC realized with feedback circuitry by using wideband Chebyshev matching topology. The chip size of the device is 3.5 mm x 1.5 mm. After the design phase was finished, the MMICs have been fabricated and measured in NANOTAM at Bilkent University. A small signal gain of 7.8 ± 0.7 dB and minimum output power of 27 dBm at 3 dB compression point are obtained in CW mode for the whole 6 GHz-18 GHz frequency band and the associated drain efficiency (PAE) is above 22%.We have demonstrated that the resulting device gives compatible outcomes with the simulated small signal gain, input and output return losses but still there is a small difference between the measurement and simulation results can be related to the model accuracy. The RMS error of the models can be around 10%.

As future work, trapping and thermal effects have a great impact on the device electrical characteristics so our GaN HEMT models can be improved by using Agilent'sW8533 Angelov-GaN extraction package which is part of the Integrated Circuit Characterization and Analysis Platform (IC-CAP) Device Modeling Software. Angelov-GaN model, which is developed by Prof. Angelov at Chalmers University, provides a basis for more accurate modeling of GaN HEMT's for nonlinear applications including self-heating and dispersion [84].

Appendix-A

MOCVD Growth Steps of Bilkent NANOTAM AlGaN/GaN HEMTs

Epitaxial Layers	B-2323
GaN Capping Layer	**Reactor temperature:** 1100°C, **Reactor pressure:** 50 mbar **Gases:** 5 sccm TMGa, 500 sccm NH_3 **Thickness:** 3-5 nm
Undoped AlGaN Barrier Layer	**Reactor temperature:** 1100°C, **Reactor pressure:** 50 mbar **Gases:** 5 sccm TMGa, 10 sccm TMAl, 500 sccm NH_3 **Thickness:** 20-25 nm
AlN Spacer Layer	**Reactor temperature:** 1100°C, **Reactor pressure:** 50 mbar **Gases:** 10 sccm TMAl, 200 sccm NH_3 **Thickness:** 1 nm
GaN Buffer Layer	GaN **Reactor temperature:** 1050-1075°C **Reactor pressure:** 200 mbar **Gases:** 10-17 sccm TMGa, 1300-1800 sccm NH_3 **Thickness:** 2600 nm (in total)
HT AlN Buffer Layer	HT-GaN **Reactor temperature:** 1130 ºC **Reactor pressure:** 25 mbar **Gases:** 20 sccm TMAl, 50 sccm NH_3 **Duration:** 10 min, Thickness: 100 nm
AlN Nucleation Layer	LT-GaN **Reactor temperature:** 500ºC-750 ºC **Reactor pressure:** 50 mbar **Gases:** 15 sccm TMAl, 200 sccm NH_3 **Duration:** 180 sec, Thickness: 10 nm

Appendix-B

Fabrication Process Summary of Bilkent NANOTAM GaN HEMTs

1. **MESA**
   Lithography: AZ5214E
   ICP- RIE: Freon-20sccm-200W-8 µbar- 90-100 sec.

2. **Ohmic Contacts:**
   Lithography: TI35ES
   Metalization: Ti/Al/Ni/Au (150Å/1500Å/400Å/700Å)
   RTP annealing: 850C-30sec.

3. **Gate lithography - RIE O_2 descum etching - Metalization:**
   Lithography: PMMA-A6-950K
   RIE dry etch: O_2-40sccm-50W-33µbar-10sec.
   Metalization: Ni/Au (500Å/3000Å)

4. **Gate Pad Metalization:**
   Lithography: TI35ES
   Metalization: Ti/Au (500Å/2500Å)

5. **SiN deposition - Etching:**
   PECVD: 30min.
   RIE dry etch: CHF_3-O_2-27sccm-8sccm-200W-33µbar-4min.

6. **Bridge post & Reflow:**
   Lithography: Su1828
   Reflow: 150C-10min.

7. **Interconnect metalization:**
   Lithography: TI35ES
   Metalization: Electroplated Au (2um)

8. **Bridge post removing:**
   Ultrasonic Cleaner - Aceton

BIBLIOGRAPHY

[1] C. G. Xie and A. Pavio, "Development of GaNHEMT based high power high efficiency distributed power amplifier for military applications," *2007 Ieee Military Communications Conference, Vols 1-8,* pp. 3909-3912, 2007.

[2] U. K. Mishra*, et al.*, "AlGaN/GaN HEMTs - An overview of device operation and applications," *Proceedings of the Ieee,* vol. 90, pp. 1022-1031, Jun 2002.

[3] O. Ambacher*, et al.*, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures," *Journal of Applied Physics,* vol. 87, pp. 334-344, Jan 1 2000.

[4] U. K. Mishra, "Status of AlGaN/GaN HEMT Technology - A UCSB perspective," *GAAS 2005: 13th European Gallium Arsenide and Other Compound Semiconductors Application Symposium, Conference Proceedings,* pp. 21-27, 2005.

[5] O. Ambacher*, et al.*, "High performance polarization induced AlGaN/GaN HEMTs," Compound Semiconductors 1999, 2000.

[6] P. Waltereit*, et al.*, "GaN HEMT and MMIC development at Fraunhofer IAF: performance and reliability," *Physica Status Solidi a-Applications and Materials Science,* vol. 206, pp. 1215-1220, Jun 2009.

[7] U. K. Mishra*, et al.*, "AlGaN/GaN HEMTs-an overview of device operation and applications," *Proceedings of the Ieee,* vol. 90, pp. 1022-1031, 2002.

[8] Y. F. Wu*, et al.*, "High power AlGaN/GaN HEMTs for microwave applications," *Solid-State Electronics,* vol. 41, pp. 1569-1574, Oct 1997.

[9] L. F. Eastman*, et al.*, "Undoped AlGaN/GaN HEMTs for microwave power amplification," *Ieee Transactions on Electron Devices,* vol. 48, pp. 479-485, Mar 2001.

[10] T. P. Chow and R. Tyagi, "Wide Bandgap Compound Semiconductors for Superior High-Voltage Unipolar Power Devices," *Ieee Transactions on Electron Devices,* vol. 41, pp. 1481-1483, Aug 1994.

[11] M. Trivedi and K. Shenai, "Performance evaluation of high-power wide band-gap semiconductor rectifiers," *Journal of Applied Physics,* vol. 85, pp. 6889-6897, May 1 1999.

[12] O. Ambacher*, et al.*, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *Journal of Applied Physics,* vol. 85, pp. 3222-3233, 1999.

[13] http://www.itp.phys.ethz.ch/research/condmat/strong/events/ncsc.
[14] O. Ambacher, "Polarization induced effects in AlGaN/GaN heterostructures," *Acta Physica Polonica A,* vol. 98, pp. 195-201, Sep 2000.
[15] E. T. Yu, *et al.*, "Spontaneous and piezoelectric polarization effects in III-V nitride heterostructures," *Journal of Vacuum Science & Technology B,* vol. 17, pp. 1742-1749, Jul-Aug 1999.
[16] R. Vetury, *et al.*, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *Electron Devices, IEEE Transactions on,* vol. 48, pp. 560-566, 2001.
[17] R. Vetury, "Polarization Induced 2DEG in AlGaN/GaN HEMTs: On the origin, DC and transient characterization," University of California, Santa Barbara, 2000.
[18] S. J. Heikman, "MOCVD growth technologies for applications in AlGaN/GaN high electron mobility transistors," UNIVERSITY of CALIFORNIA, 2002.
[19] A. Chini, *et al.*, "12 W/mm power density AlGaN/GaN HEMTs on sapphire substrate," *Electronics Letters,* vol. 40, pp. 73-74, 2004.
[20] J. Johnson, *et al.*, "12 W/mm AlGaN-GaN HFETs on silicon substrates," *Electron Device Letters, IEEE,* vol. 25, pp. 459-461, 2004.
[21] U. K. Mishra, *et al.*, "GaN-based RF power devices and amplifiers," *Proceedings of the Ieee,* vol. 96, pp. 287-305, 2008.
[22] A. Ping, *et al.*, "DC and microwave performance of high-current AlGaN/GaN heterostructure field effect transistors grown on p-type SiC substrates," *Electron Device Letters, IEEE,* vol. 19, pp. 54-56, 1998.
[23] A. P. Grzegorczyk, "GaN grown on sapphire by MOCVD: material for HEMT structures," 2006.
[24] S. C. Binari, *et al.*, "Trapping effects in GaN and SiC microwave FETs," *Proceedings of the Ieee,* vol. 90, pp. 1048-1058, 2002.
[25] S. L. Selvaraj, *et al.*, "Breakdown enhancement of AlGaN/GaN HEMTs on 4-in silicon by improving the GaN quality on thick buffer layers," *Electron Device Letters, IEEE,* vol. 30, pp. 587-589, 2009.
[26] R. Lahiji, "GaAs High Electron Mobility Transistor."
[27] J. Ibbetson, *et al.*, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors," *Applied Physics Letters,* vol. 77, pp. 250-252, 2000.
[28] M. A. Khan, *et al.*, "Observation of a two-dimensional electron gas in low pressure metalorganic chemical vapor deposited GaN-Al x Ga 1-x N heterojunctions," *Applied Physics Letters,* vol. 60, pp. 3027-3029, 1992.
[29] J. Derluyn, *et al.*, "Improvement of AlGaN/ GaN high electron mobility transistor structures by in situ deposition of a SiN surface layer," *Journal of Applied Physics,* vol. 98, p. 054501, 2005.
[30] L. McCarthy, *et al.*, "AlGaN/GaN heterojunction bipolar transistor," *Electron Device Letters, IEEE,* vol. 20, pp. 277-279, 1999.
[31] A. Asgari, *et al.*, "The effects of GaN capping layer thickness on two-dimensional electron mobility in GaN/AlGaN/GaN heterostructures,"

Physica E: Low-dimensional Systems and Nanostructures, vol. 25, pp. 431-437, 2005.

[32] C. Özgen, "THE GROWTH AND CHARACTERIZATION OF INDIUM RICH INDIUM-GALLIUM-NITRIDE (INGAN) SOLAR CELL EPITAXIAL STRUCTURESBY METAL ORGANĐC CHEMICAL VAPOR DEPOSITION (MOCVD)," MIDDLE EAST TECHNICAL UNIVERSITY, 2012.

[33] C. Elsass*, et al.*, "High mobility two-dimensional electron gas in AlGaN/GaN heterostructures grown by plasma-assisted molecular beam epitaxy," *Applied Physics Letters,* vol. 74, pp. 3528-3530, 1999.

[34] P. Asbeck*, et al.*, "Piezoelectric charge densities in AlGaN/GaN HFETs," *Electronics Letters,* vol. 33, pp. 1230-1231, 1997.

[35] T. Palacios*, et al.*, "High-power AlGaN/GaN HEMTs for Ka-band applications," *Electron Device Letters, IEEE,* vol. 26, pp. 781-783, 2005.

[36] M. HL*, et al.*, "MOCVD-grown high-mobility Al0. 3Ga0. 7N/AlN/GaN HEMT structure on sapphire substrate," 2007.

[37] X. Wang*, et al.*, "Room temperature mobility above 2100 cm2/Vs in Al0. 3Ga0. 7N/AlN/GaN heterostructures grown on sapphire substrates by MOCVD," *physica status solidi (c),* vol. 3, pp. 607-610, 2006.

[38] A. Saxler*, et al.*, "Characterization of an AlGaN/GaN two-dimensional electron gas structure," *Journal of Applied Physics,* vol. 87, pp. 369-374, 2000.

[39] H. Jiang*, et al.*, "Determination of exciton transition energy and bowing parameter of AlGaN alloys in AlGaN/GaN heterostructure by means of reflectance measurement," *Journal of Applied Physics,* vol. 89, pp. 1046-1052, 2001.

[40] S. Lee*, et al.*, "In situ measurements of the critical thickness for strain relaxation in AlGaN⁄ GaN heterostructures," *Applied Physics Letters,* vol. 85, p. 6164, 2004.

[41] S. Boeykens*, et al.*, "Investigation of AlN nucleation layers for AlGaN/GaN heterostructures on 4H-SiC," *physica status solidi (c),* vol. 3, pp. 1579-1582, 2006.

[42] H. Amano*, et al.*, "Metalorganic vapor phase epitaxial growth of a high quality GaN film using an AlN buffer layer," *Applied Physics Letters,* vol. 48, p. 353, 1986.

[43] S. Corekci*, et al.*, "Structural, morphological, and optical properties of AlGaN/GaN heterostructures with AlN buffer and interlayer," *Journal of Applied Physics,* vol. 101, pp. 123502-123502-6, 2007.

[44] A. Grzegorczyk*, et al.*, "Resistivity control of unintentionally doped GaN films," *physica status solidi (c),* vol. 2, pp. 2113-2116, 2005.

[45] M. A. Khan*, et al.*, "Photoluminescence characteristics of AlGaN-GaN-AlGaN quantum wells," *Applied Physics Letters,* vol. 56, pp. 1257-1259, 1990.

[46] J. Bergman*, et al.*, "Photoluminescence related to the two-dimensional electron gas at a GaN/AlGaN heterointerface," *Applied Physics Letters,* vol. 69, pp. 3456-3458, 1996.

[47] S. M. Sze, *Semiconductor devices: physics and technology*: John Wiley & Sons, 2008.
[48] X. Zhang*, et al.*, "title: AlNGaN HEMT T-gate Optimal Design."
[49] G. H. Jessen*, et al.*, "Short-channel effect limitations on high-frequency operation of AlGaN/GaN HEMTs for T-gate devices," *Electron Devices, IEEE Transactions on,* vol. 54, pp. 2589-2597, 2007.
[50] D. Guerra*, et al.*, "Aspect ratio impact on RF and DC performance of state-of-the-art short-channel GaN and InGaAs HEMTs," *Electron Device Letters, IEEE,* vol. 31, pp. 1217-1219, 2010.
[51] U. K. Mishra*, et al.*, "AlGaN/GaN HEMTs-an overview of device operation and applications," *Proceedings of the Ieee,* vol. 90, pp. 1022-1031, 2002.
[52] A. Vertiatchikh and L. Eastman, "Effect of drain-to-source spacing of AlGaN/GaN transistor on frequency response and breakdown characteristics," *Electronics Letters,* vol. 39, pp. 876-877, 2003.
[53] Y. Yamashita*, et al.*, "Effect of source-drain spacing on DC and RF characteristics of 45 nm-gate AlGaN/GaN MIS-HEMTs," *Electronics Letters,* vol. 47, pp. 211-212, 2011.
[54] S. Taking, "AlN/GaN MOS-HEMTs Technology," University of Glasgow, 2012.
[55] S. Taking*, et al.*, "New process for low sheet and ohmic contact resistance of AIN/GaN MOS-HEMTs," in *Microwave Integrated Circuits Conference (EuMIC), 2010 European*, 2010, pp. 306-309.
[56] D. Deen*, et al.*, "Dependence of ohmic contact resistance on barrier thickness of AlN/GaN HEMT structures," *Solid-State Electronics,* vol. 54, pp. 613-615, 2010.
[57] P. Parikh*, et al.*, "High power density and/or linearity transistors," ed: Google Patents, 2007.
[58] V. K. Paidi, "MMIC Power Amplifiers in GaN HEMT and InP HBT Technologies," UNIVERSITY of CALIFORNIA, 2004.
[59] F. M. Mohammed*, et al.*, "The role of barrier layer on Ohmic performance of Ti⁄ Al-based contact metallizations on AlGaN⁄ GaN heterostructures," *Journal of Applied Physics,* vol. 100, p. 023708, 2006.
[60] F. M. Mohammed*, et al.*, "Anatomy-performance correlation in Ti-based contact metallizations on AlGaN⁄ GaN heterostructures," *Journal of Applied Physics,* vol. 101, p. 033708, 2007.
[61] R. E. Williams and R. Williams, *Gallium arsenide processing techniques*: Artech House Dedham, MA, 1984.
[62] P. Coane, "Introduction to Electron Beam Lithography," *Louisiana Tech University, Institute for Micromanufacturing*.
[63] B. M. Green*, et al.*, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMTs," *Electron Device Letters, IEEE,* vol. 21, pp. 268-270, 2000.
[64] D. Guerra*, et al.*, "Carrier dynamics investigation on passivation dielectric constant and RF performance of Millimeter-Wave power GaN

HEMTs," *Electron Devices, IEEE Transactions on,* vol. 58, pp. 3876-3884, 2011.
[65] Z. H. Liu, *et al.*, "Comprehensive Study on the Bias-Dependent Equivalent-Circuit Elements Affected by PECVD SiN Passivation in AlGaN/GaN HEMTs," *Electron Devices, IEEE Transactions on,* vol. 58, pp. 473-479, 2011.
[66] Y. Pei, *et al.*, "Effect of dielectric thickness on power performance of AlGaN/GaN HEMTs," *Ieee Electron Device Letters,* vol. 30, pp. 313-315, 2009.
[67] T. Palacios, *et al.*, "AlGaN/GaN high electron mobility transistors with InGaN back-barriers," *Electron Device Letters, IEEE,* vol. 27, pp. 13-15, 2006.
[68] D. K. Schroder, *Semiconductor material and device characterization*: John Wiley & Sons, 2006.
[69] D. E. Root, *et al.*, "Broad-band poly-harmonic distortion (PHD) behavioral models from fast automated simulations and large-signal vectorial network measurements," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 53, pp. 3656-3664, 2005.
[70] W. R. Curtice and M. Ettenberg, "A nonlinear GaAs FET model for use in the design of output circuits for power amplifiers," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 33, pp. 1383-1394, 1985.
[71] W. R. Curtice and W. C. Consulting, "The Importance of Using Pulsed Current and RF data for Compact Modeling of RF Power Devices."
[72] T. Gasseling, "Compact Transistor Models: The Roadmap to First-Pass Amplifier Design Success," *Microwave Journal,* vol. 55, pp. 74-86, 2012.
[73] L. Dunleavy, *et al.*, "Modeling GaN: Powerful but Challenging," *Microwave Magazine, IEEE,* vol. 11, pp. 82-96, 2010.
[74] A. Alabadelah, *et al.*, "Nonlinear Models of Microwave Power Devices and Circuits," in *IEEE 12th GAAS Symposium*, 2004.
[75] R. Follmann, *et al.*, "Extraction and Modeling Methods for FET devices," *Microwave Magazine, IEEE,* vol. 1, pp. 49-55, 2000.
[76] D. J. Maclean, *Broadband feedback amplifiers*: Research Studies Press, 1982.
[77] A. J. Bichler, "An Introduction to Broadband Impedance Transformation for RF Power Amplifiers," *High Frequency design,* 2009.
[78] D.-T. Wu, *et al.*, "Design of a broadband and highly efficient 45W GaN power amplifier via simplified real frequency technique," in *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International*, 2010, pp. 1090-1093.
[79] P. R. Gray and R. G. Meyer, *Analysis and design of integrated circuits*: John Wiley & Sons, Inc., 1992.
[80] Available: http://www.microwaves101.com/encyclopedia/feedbackamp.cfm

[81] D. E. Meharry, *et al.*, "Multi-Watt Wideband MMICs in GaN and GaAs," in *Microwave Symposium, 2007. IEEE/MTT-S International*, 2007, pp. 631-634.
[82] Y. Ayasli, *et al.*, "Capacitively coupled traveling-wave power amplifier," *Electron Devices, IEEE Transactions on,* vol. 31, pp. 1937-1942, 1984.
[83] K. Krishnamurthy, *et al.*, "Broadband GaAs MESFET and GaN HEMT resistive feedback power amplifiers," *Solid-State Circuits, IEEE Journal of,* vol. 35, pp. 1285-1292, 2000.
[84] I. Angelov, *et al.*, "A new empirical nonlinear model for HEMT and MESFET devices," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 40, pp. 2258-2266, 1992.