A TRANSIMPEDANCE AMPLIFIER DESIGN FOR CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCERS OPERATING AT 7.5MHZ

A THESIS SUBMITTED TO

THE GRADUATE SCHOOL OF ENGINEERING AND SCIENCE

OF BILKENT UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR

THE DEGREE OF

MASTER OF SCIENCE

IN

ELECTRICAL AND ELECTRONICS ENGINEERING

By

Giray İlhan

January 2021

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We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

A TRANSIMPEDANCE AMPLIFIER DESIGN FOR CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCERS OPERATING AT 7.5MHZ

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M.S. in Electrical and Electronics Engineering
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January 2021

Capacitive Micromachined Ultrasonic Transducers (CMUTs) are MEMS devices used in ultrasound imaging, e.g. ultrasound mammography. CMUT proved to be a viable transducer solution in ultrasound mammography without the hazardous effects of conventional X-ray mammography. The CMUTs have a very high electrical impedance, where a transimpedance amplifier (TIA) is most appropriate for preamplification during reception.

A TIA with 25MHz bandwidth and 120kΩ transimpedance gain is designed on Cadence Virtuoso using XFAB XC06M3 process. The CMUT small signal model is used for 50μm radius and 7.5MHz operating frequency. This model is incorporated into TIA circuit simulations.

Two design options are proposed for the TIA, one with the passive feedback resistor and the other with a MOSFET feedback resistor. The latter enabled us to save space in layout design compare to the former. Transient and noise simulations are conducted and compared for schematic and layout views. The input referred current noise of the TIA is simulated to be 0.5pA/√Hz and the power consumption is simulated to be approximately 3.3mW for both designs.

Keywords: CMUT, Transimpedance Amplifier, TIA, Small Signal Equivalent Model, Transducer.

ÖZET

7.5MHZ'TE ÇALIŞAN KAPASİTİF MİKROİŞLENMİŞ ULTRASONİK DÖNÜŞTÜRÜCÜLER İÇİN TRANSEMPEDANS AMPLİFİKATÖR TASARIMI

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Tez Danışmanı: Prof. Dr. Hayrettin Köymen
Ocak 2021

Kapasitif Mikro İşlenmiş Ultrasonik Dönüştürücüler (CMUT'lar), ultrason görüntülemede kullanılan MEMS cihazlarıdır, ör. ultrason mamografisi. CMUT, geleneksel X-ışını mamografisinin zararlı etkileri olmadan ultrason mamografisinde uygulanabilir bir dönüştürücü çözümü olduğunu kanıtlamıştır. CMUT'lar çok yüksek elektriksel empedansa sahiptir, bu sebeple bir transempedans amplifikatörü (TIA) alış sırasında ön amplifikasyon için en uygun olan amplifikatör türüdür.

25MHz bant genişliğine ve 120kΩ transempedans kazancına sahip bir TIA, XFAB XC06M3 prosesi kullanılarak Cadence Virtuoso'da tasarlanmıştır. CMUT küçük sinyal modeli, 50µm yarıçap ve 7.5MHz çalışma frekansı için kullanılmıştır. Bu model, TIA devre simülasyonlarına dahil edilmiştir.

TIA için biri pasif geri besleme direncine ve diğeri MOSFET geri besleme direncine sahip iki tasarım seçeneği önerilmiştir. İkincisi, yerleşim tasarımında öncekine kıyasla alandan tasarruf etmemizi sağlamıştır. Geçici hal ve gürültü simülasyonları şematik ve yerleşim görünümleri için yapılmış ve karşılaştırılmıştır. TIA'nın giriş referanslı akım gürültüsü 0.5pA/√Hz olarak simüle edilmiş ve güç tüketimi her iki tasarım için yaklaşık 3.3mW olarak simüle edilmiştir.

Anahtar Kelimeler: CMUT, Transempedans Amplifikatötü, TIA, Küçük Sinyal Devre Modeli, Dönüştürücü.

Acknowledgements

I would like to start by expressing my deepest gratitude and respect to, one and only, Professor Hayrettin Köymen. His guidance did not just shine my way through academic studies, but also led me to become a better person. His comments, underlaid with great wisdom, helped me to understand the matters at hand in an intuitive manner. For all the things I have learnt and all the experience I have gained, I am forever in his debt.

I would like to extend my gratitude to Prof. Yusuf Ziya İder and Asst. Prof. Itır Köymen for reviewing my thesis and for their contributions. A

I would like to thank my colleagues whom I have shared countless hours studying. Firstly, to Murat Alp Güngen for helping me with every stage of this thesis, his help on my studies can only be surpassed by his friendship off campus. Also, I would like to thank Yusuph Abhoo, Talha Khan, Yasin Kumru and Kerem Enhoş for their help and inspiration.

This task would have not been completed without the love and support of my dear friends. I would like to thank my, not in blood but in bond brother Ahmet Can Varan for his constant support throughout the years. Also, to my dear friends Ercan Coşkun, Ömer Gözüaçık, Ramazan Kağan Erbay, Çetin and Pınar Taştekin, Serkan İslamoğlu, Burak Özbek, Berkay Oymak, Emir Ceyani, Berk Küçükoğlu, Zülal Bingöl and Ezgi Cebeci for their unprecedented love and support.

Without music, life would be joyless, hence I would like to thank Texan music groups Khruangbin and Black Pumas for their inspiring songs, which helped me excessively throughout my M.S. studies.

Finally, I would like to thank my dear mother Nurşen İşman, my father Recep Tufan İlhan, and Erkan Erdal for their constant belief in me, which I hope I did not disappoint.

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In loving memory of
Feride Gizem İlhan

Chapter 1

Introduction

Capacitive Micromachined Ultrasonic Transducers (CMUTs) are MEMS devices which are widely used in ultrasound imaging. CMUTs converts acoustic signals to electrical signals and vice versa. CMUTs provide a range of advantages compare to its counterparts. Offering a wide bandwidth, ease of fabricating large arrays and integration with electronics are a few of them [1]. In ultrasound imaging, CMUTs are used both as transmitters and receivers.

A CMUT cell can be thought as a parallel plate capacitor with an elastic membrane as one of the plates [2]. When excited with ultrasound the membrane vibrates, causing a change in capacitance, hence producing a current, which is the general idea behind the reception mode CMUTs. In reception mode, CMUTs yield a very high electrical impedance. This high impedance limits the bandwidth in voltage amplification. Hence, a current amplification system is required.

A transimpedance amplifier (TIA) is chosen for this task. TIA produces voltage output signals with respect to current input signals. TIA yields very low input impedance which makes it favorable in preamplification processes of high electrical impedance yielding sensors such as MEMS accelerometers [3] and CMUTs [4] [5].

Since designing and analyzing arrays containing large number of CMUTs using finite element method (FEM) is computationally intensive and practically impossible, lumped element nonlinear circuit model is adopted [6] [7]. This approach enables us to simulate CMUT cells in conventional SPICE programs, incorporated with the proposed TIA as well.

Since most reception mode devices analyzed as small signal operations and since we need to propose a TIA for receiving mode CMUTs, we must deal with CMUT small signal equivalent model [2]. In Chapter 2, CMUT equivalent circuit model is presented. Necessary parameters are calculated for CMUTs having $50\mu m$ radius and $7.5MHz$ operating frequency. Calculated parameters are then used to incorporate the CMUT's electrical properties into the TIA simulation environment.

Resistive feedback TIA design is presented with the circuit analysis and noise simulations. Prosed design yields a $120k\Omega$ transimpedance gain, $25MHz$ bandwidth, $0.48pA/\sqrt{Hz}$ input referred noise and $56.09nV/\sqrt{Hz}$ output noise at $7.5MHz$ with less than $3.3mW$ power consumption. An alternate design is proposed as well, having a voltage controlled MOSFET transistor feedback instead of a passive resistor. The goal with the alternate design is to save up space in layout design without compromising the already achieved resistive feedback TIA features.

Both TIA versions are designed and simulated on Cadence Virtuoso Analog Design Environment [8] with XFAB XC06M3 process. Post-layout simulations and schematic simulation comparisons are provided.

Chapter 2

CMUT Equivalent Circuit Model

2.1 Lumped Element Model and Small Signal Equivalent Circuit

A capacitive micromachined ultrasonic transducer (CMUT) is an electroacoustic transducer, which transforms electrical energy to mechanical energy and vice versa. Since the main goal of this thesis is to design and implement a Transimpedance Amplifier for CMUTs operating at 7.5Mhz, we firstly need to model the CMUT with respect to design criteria. The related work of equivalent circuit modelling has been heavily carried out by [2] [6] [7] [9]. Equations and assumptions of their work will be carefully followed throughout this chapter.

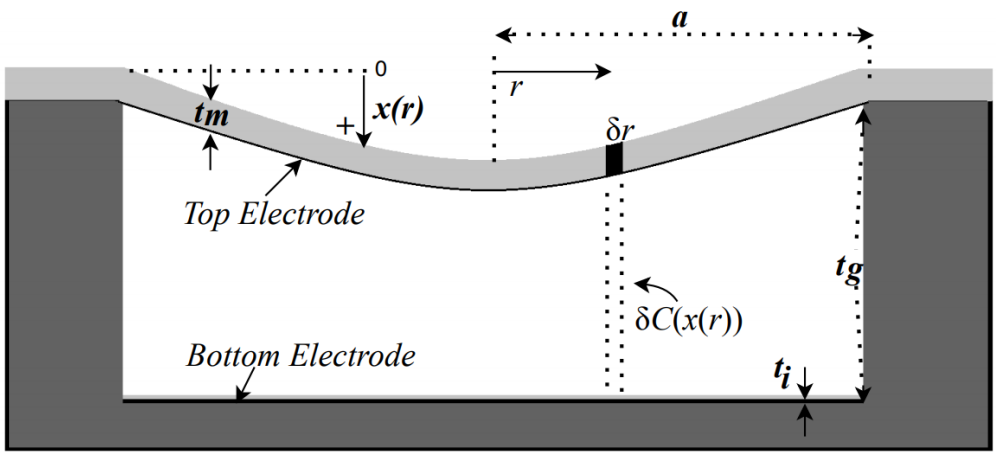

Figure 2.1: 2D view of the circular CMUT geometry

Both large and small signal equivalent circuit model is presented in 2012 [2]. With the help of this lumped element model, we can simulate CMUT cells with generic circuit analysis software. In our work, the required Transimpedance

Amplifier is for receiving mode CMUT arrays, hence we are interested in small signal equivalent circuit model. However, we firstly need to discuss the large signal equivalent model and work our way to small signal equivalent circuit model which is derived from the large signal equivalent model. Below is the figure of large signal equivalent circuit and table of circuit variables.

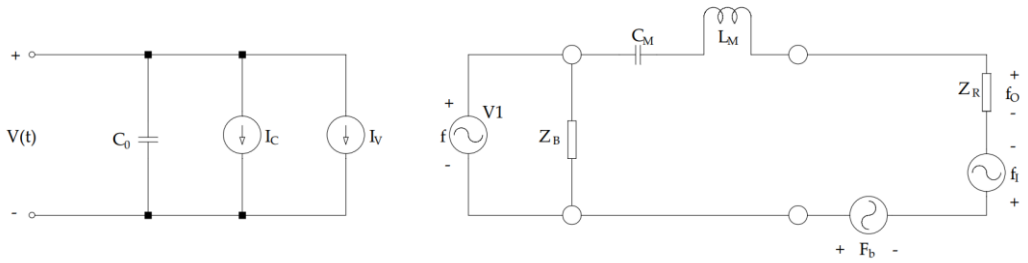

Figure 2.2: CMUT Large Signal Model

Model	RMS $\{f_R, v_R\}$	Average $\{f_A, v_A\}$	Peak $\{f_P, v_{RP}\}$
f	f_R	$(3/\sqrt{5})\, f_R$	$(1/\sqrt{5})\, f_R$
v	v_R	$(\sqrt{5}/3)\, v_R$	$\sqrt{5} v_R$
C_M	$C_{Rm} = \frac{9}{5}\frac{(1-\sigma^2)a^2}{16\pi Y_0 t_m^3}$	$C_{Am} = 5/9\ C_{Rm}$	$C_{Pm} = 5\ C_{Rm}$
L_M	$L_{Rm} = \pi a^2$	$L_{Am} = 9/5\ L_{Rm}$	$L_{Pm} = 1/5\ L_{Rm}$
Z_R	Z_{RR}	$Z_{AR} = Z_{RR}$	$Z_{PR} = Z_{RR}$
F_b	$F_{Rb} = (\sqrt{5}/3)\pi a^2 P_0$	$F_{Ab} = \pi a^2 P_0$	$F_{Pb} = 1/3\ \pi a^2 P_0$
f_I	$f_{RI} = 2\pi a^2 p_i$	$f_{AI} = (3/\sqrt{5}) 2\pi a^2 p_i$	$f_{PI} = (1/\sqrt{5})\ 2\pi a^2 p_i$
f_O	$f_{RO} = \pi a^2 p_o$	$f_{AO} = (3/\sqrt{5})\ \pi a^2 p_o$	$f_{PO} = (1/\sqrt{5})\pi a^2 p_o$
n	n_R	$n_A = (3/\sqrt{5})\ n_R$	$n_P = (1/\sqrt{5})\ n_R$
C_S	C_{RS}	$C_{AS} = 5/9\ C_{RS}$	$C_{PS} = 5 C_{RS}$

Table 1. The variables and parameters of large signal equivalent circuit. P_O is the ambient static pressure, p_i and p_0 are incedent free field pressure and transmitted pressure, respectively.

The small signal equivalent model is acquired from the large signal model with certain assumptions. Since many elements are carried out from the large signal model, we will heavily utilize the above table for our small signal equivalent model. Below is the small signal equivalent circuit model.

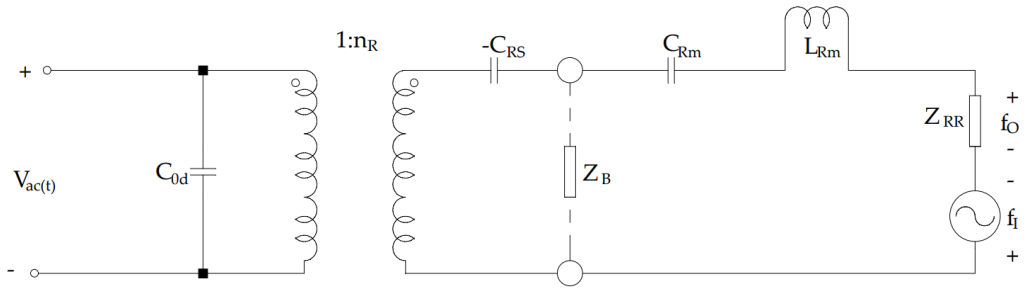

Figure 2.3: Small signal equivalent circuit

C_{Rm} and L_{Rm} elements can be calculated via table 1. The only small signal component of the electrical side C_{0d}, which is the capacitance of the deflected membrane can be found as:

$$C_{0d} = C_0 g\left(\frac{X_P}{t_{ge}}\right) \tag{1}$$

The electromechanical turns ratio at the operating point can be found using:

$$n_R = \frac{2F_R}{V_{DC}} = \sqrt{5}\frac{C_0 V_{DC}}{t_{ge}} g'\left(\frac{X_P}{t_{ge}}\right) \tag{2}$$

The spring softening capacitor C_{RS} can be found using:

$$C_{RS} = \frac{2t_{ge}^2}{5C_0 V_{DC}^2 g''\left(\frac{X_P}{t_{ge}}\right)} = C_{RM}\left[\frac{2}{3}\frac{V_{DC}^2}{V_r^2}\ g''\left(\frac{X_P}{t_{ge}}\right)\right]^{-1} \tag{3}$$

The last parameter to be discussed is the radiation impedance Z_{RR}, which has been fairly discussed in [10] [11]. Z_{RR} can be found using:

$$Z_{11}(ka) = \pi a^2 \rho_0 c_0 \{R_1(ka) + jX_1(ka)\} \tag{4}$$

where a is the radius of the piston, ρ_0 is the density of water ($1000 kg/m^3$) and c_0 is the velocity of sound in water ($1500 m/s$).

$$R_1(ka) = 1 - \frac{2J_1(2ka)}{2ka}; \quad X_1(ka) = \frac{2H_1(2ka)}{2ka}$$

Where J_1 and H_1 are Bessel function of first kind of order 1 and Struve function of order 1, respectively.

2.2 CMUT Design Parameters

In order to successfully simulate the transimpedance amplifier and include CMUT in the circuit simulation, we must calculate the electrical side of the CMUT small signal model. We will start with the given variables and determine the rest accordingly. The radius of the CMUT is taken to be 50μm, the reference voltage V_r is taken to be 100V, t_i is taken to be 300nm of Alumina, and the resonance frequency is taken as 7.5MHz. As a design choice, the CMUTs will be biased at 70% of the collapse voltage. Silicon is chosen as the base material and Alumina as insulating material. In the following equations the resonance frequency is taken 15MHz since we are dealing with waterborne CMUTs. All the calculations are carried with MATLAB.

The mechanical and electrical properties of silicon and alumina are given as follows.

Membrane and Insulator Parameters		
Y_0	Young's Modulus	149 GPa
σ	Poisson ratio	0.17
ρ	Density	2370 kg/m^3
ϵ	Dielectric Constant of Al_2O_3	9

Table 2: Membrane and Insulator Parameters

The membrane thickness t_m is calculated using:

$$\omega_m = \frac{1}{\sqrt{L_{Am}C_{Am}}} = \frac{t_m}{a^2}\sqrt{\frac{80}{9}\frac{Y_0}{\rho(1-\sigma^2)}} \tag{5}$$

Since the resonance frequency is decided earlier, L_{am} and C_{am} product is known as well. The equation yields t_m = 7.7173 μm. Then t_{ge} is calculated using:

$$\mathrm{V_r} = 8\frac{\mathrm{t_m}}{\mathrm{a^2}}\mathrm{t_{ge}}^{3/2}\mathrm{t_m}^{1/2}\sqrt{\frac{\mathrm{Y_0}}{27\varepsilon_0(1-\sigma^2)}} \tag{6}$$

where ε_0 is vacuum permittivity and equals to $8.85 \cdot 10^{-12} C/Vm$. The equation yields t_{ge} = 129.5nm, and t_g is calculated using:

$$t_{ge} = t_g + \frac{t_i}{\varepsilon} \tag{7}$$

The equation yields t_g = ~96nm, which is taken as 100nm for convenience and carried as such for further calculations.

F_{pb}/F_{pg} is calculated as 0.0085 using:

$$\frac{F_{pb}}{F_{pg}} = \left(\frac{t_m}{t_{ge}}\right)\left(\frac{a}{t_m}\right)^4 \frac{3}{16}\frac{P_0(1-\sigma^2)}{Y_0} \tag{8}$$

After calculating $\frac{F_{pb}}{F_{pg}}$, collapse voltage is approximately found as 103.6V using:

$$\frac{V_c}{V_r} \approx 0.9961 - 1.0468\frac{F_{pb}}{F_{pg}} + 0.06972\left(\frac{F_{pb}}{F_{pg}} - 0.25\right)^2 + 0.01148\left(\frac{F_{pb}}{F_{pg}}\right)^6 \tag{9}$$

To find C_{0d} we need to calculate C_0 and X_P, which are given as:

$$C_0 = \frac{\epsilon_0 \pi a^2}{t_{ge}} \tag{10}$$

$$for \quad \frac{V_{DC}}{V_C} = 0.70: \quad \frac{X_P}{t_{ge}} \approx 0.128 + 0.8738\frac{F_{pb}}{F_{pg}} \tag{11}$$

Using Equation (1), (10) and (11), and considering we are driving the CMUT at the 70% of the collapse voltage, we find $C_{0d} = 0.18pF$. Using Equation (2), the electromechanical turns ratio at the operating point n_R is calculated as $2.19 \cdot 10^{-4}$, and using Equation (3) the spring softening capacitor C_{RS} is calculated as $31.4nF$. The radiation impedance Z_{RR} is calculated using Equation (4).

Finally we have to calculate Z_{in} at resonance frequency, to find the CMUT resistance R_{CMUT} and the short circuit current i_{sc} with respect to incident pressure p_i.

$$Z_{in} = \frac{Z_{RR}}{n_R^2} + \frac{1}{j\omega_{res}C_{0d}} \tag{12}$$

Real part Z_{in} yields the R_{CMUT}, which is calculated as $223.46k\Omega$. Short circuit current is calculated with respect to incident pressure p_i as follows.

$$i_{sc} = \pi a^2 p_i \left[\left(-\frac{1}{n_R Z_{in}} \right) \left(\frac{1}{1 + \frac{C_{0d}}{n_R^2} \left(\frac{1}{C_{Rm}} - \frac{1}{C_{RS}} \right)} \right) \right] \tag{13}$$

For an incident pressure of $1000Pa$, short circuit current i_{sc} is calculated as $1.1nA$.

Found parameters are used to simulate the electrical port of the small signal circuit model. CMUT capacitance and the current produced by the CMUT with respect to incident pressure is calculated. Using different current values, the operating range of Transimpedance Amplifier is found. Further calculations and combination of CMUT small signal model and the TIA circuitry is presented in Chapter 3.

Chapter 3

Transimpedance Amplifier

CMUT cells produce current signals with respect to incident pressure waves. In receiver mode, generated currents are small in value and needs to be amplified. For the following stage of signal processing, the produced analog signals must be converted to digital signals via Analog to Digital converters. Most ADCs convert analog voltages to digital signals, hence the current signal of CMUTs must be converted to voltage signals as well. Transimpedance Amplifier (TIA) amplifies the current signals and converts them to voltage signals, acting as a preamplifier.

TIA is a widely used topology in preamplification processes in ultrasound imaging [12] and also for receiving mode CMUT cells [13] [14]. TIAs have important parameters to be considered, such as the transimpedance gain, bandwidth and input-referred current noise [15]. The transimpedance gain is the ratio of the output voltage to the input current.

Receiver mode CMUT produces very small current values, hence the input referred current noise of the TIA is an important factor to be considered. Input refereed current noise limits the minimum current that can be detected by the TIA. Design of TIA requires the lowest possible noise for the given bandwidth to achieve high SNR of the transducer system [16].

Bandwidth of the TIA circuit, which is the operating frequency range of the TIA, is determined by the CMUT design. Bandwidth should be wide enough to ensure that the received analog information is amplified without a loss. Since the designed CMUT has an operating frequency of 7.5MHz, the TIA should be designed accordingly.

3.1 Resistive Feedback Transimpedance Amplifier

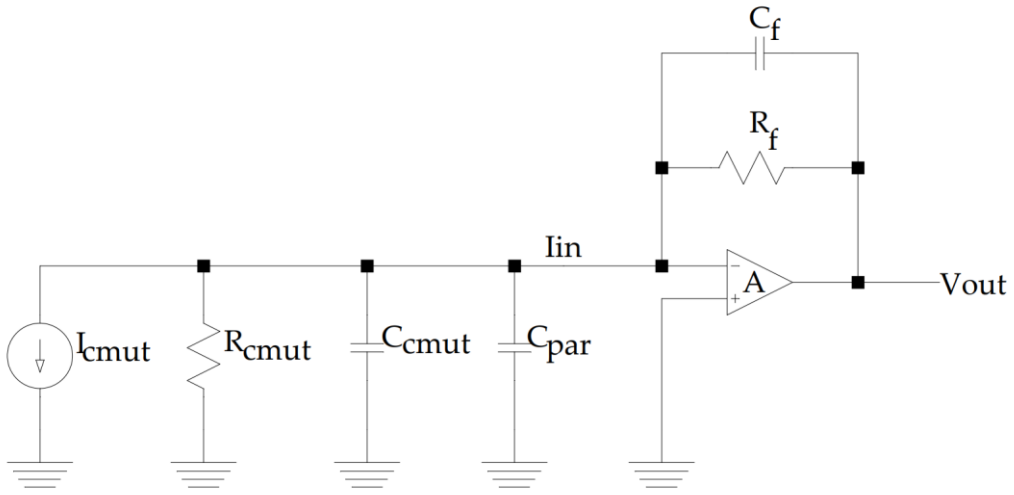

Figure 3.1: Resistive Feedback Transimpedance Amplifier

Resistive Feedback Transimpedance Amplifier senses the input and generates a proportional current that is fed back to the input via feedback resistor. This type of an amplifier is widely used in optoelectronic applications. This topology provides us a low input impedance. Due to the Miller effect the input impedance of the amplifier is equal to $\frac{R_f}{A_0}$, where A_0 is the open loop gain of the amplifier.

The resistive feedback transimpedance amplifier can be treated as a second order system as described by B. Razavi [17]. Transfer function of the amplifier is given as follows for $C_f = 0$:

$$\frac{V_{out}}{I_{cmut}} = -\frac{\frac{A_0\omega_0}{C_{tot}}}{s^2 + \frac{R_f C_{tot} + \frac{1}{\omega_0}}{R_f C_{tot}} s + \frac{(A_0+1)\omega_0}{R_f C_{tot}}}, \tag{14}$$

where C_{tot} it the total capacitance at the input of the resistive feedback amplifier and ω_0 is the open loop voltage gain corner frequency. When $s = 0$ and $A_0 \gg 1$,

transimpedance gain of the amplifier approaches the feedback resistor R_f. When $C_f \neq 0$, the TIA bandwidth becomes as follows:

$$\omega_n = \frac{1}{R_f C_f} \tag{15}$$

In order to achieve sufficient bandwidth and gain for CMUTs operating at 7.5MHz, the TIA bandwidth is set to 25MHz. To provide this BW, C_f is set to $53fF$ and R_f is set to 120kΩ.

One of the most important criteria in designing a TIA for small signal applications with current signal inputs, is the input referred current noise. The noise calculations related to resistive feedback TIA is provided in Section 3.1.4.

3.1.1 The Cascode Common Source Amplifier

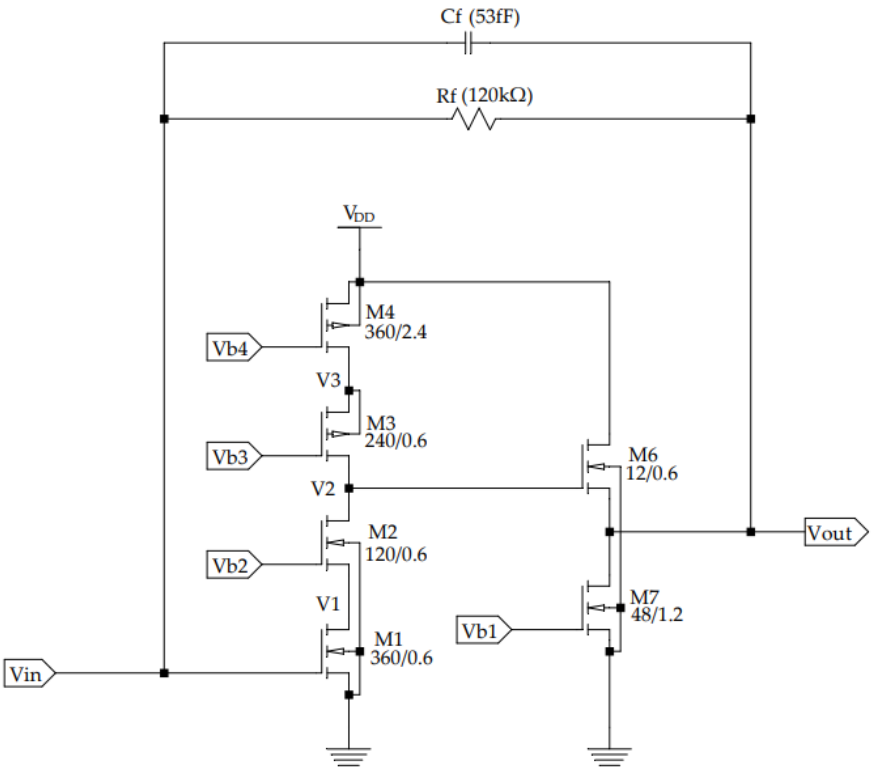

Figure 3.2: Cascode Common Source Amplifier

Above is the topology of the Cascode Common Source Amplifier, which acts as the core amplifier, which contains four NMOS and two PMOS transistors. Transistor couple M_1 and M_2 are cascode transistors and provides the main gain of the amplifier. M_3 and M_4 transistors are cascode connected as well where M_4 act as a constant current source and M_3 boosts the output impedance of M_4. A source follower amplifier is added to the output of the cascode common source stage to lower the stage impedance. Transistor M_6 act as the source follower, which is connected to current mirror transistor M_7. R_f and C_f are feedback resistor and capacitor respectively.

Since CMUT receiver arrays contain large number of elements generating current signals to be processed in the latter stages, the outputs must be multiplexed.

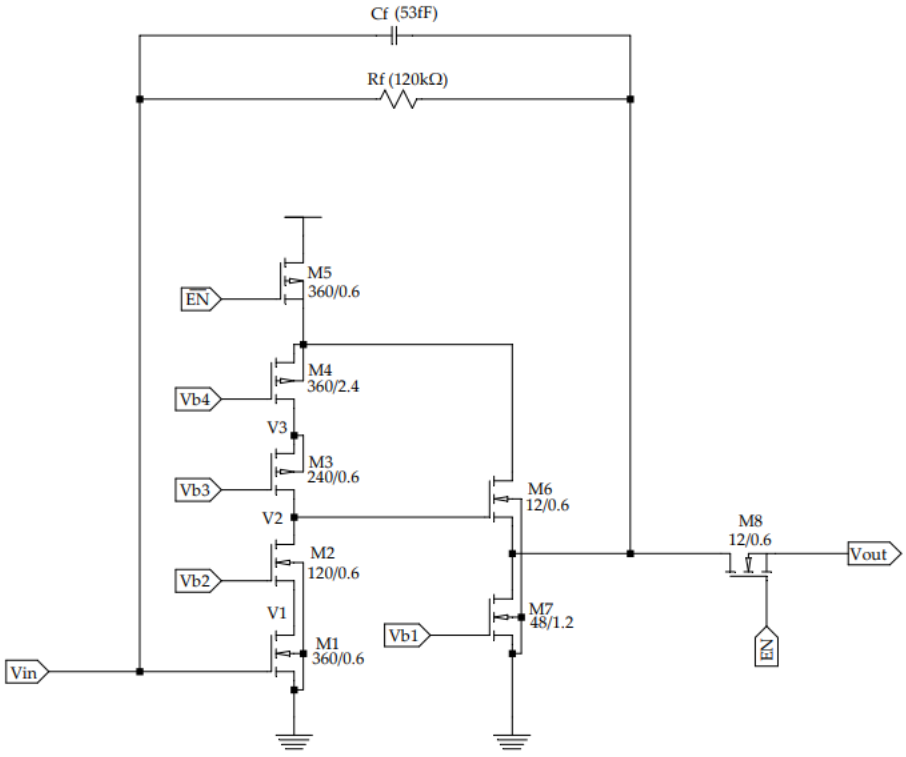

Figure 3.3: Cascode Common Source Amplifier Multiplexer Topology

Transistor M_5 is the power shutdown switch and transistor M_8 is the output switch. Multiple M_8 transistors form a multiplexer as shown below.

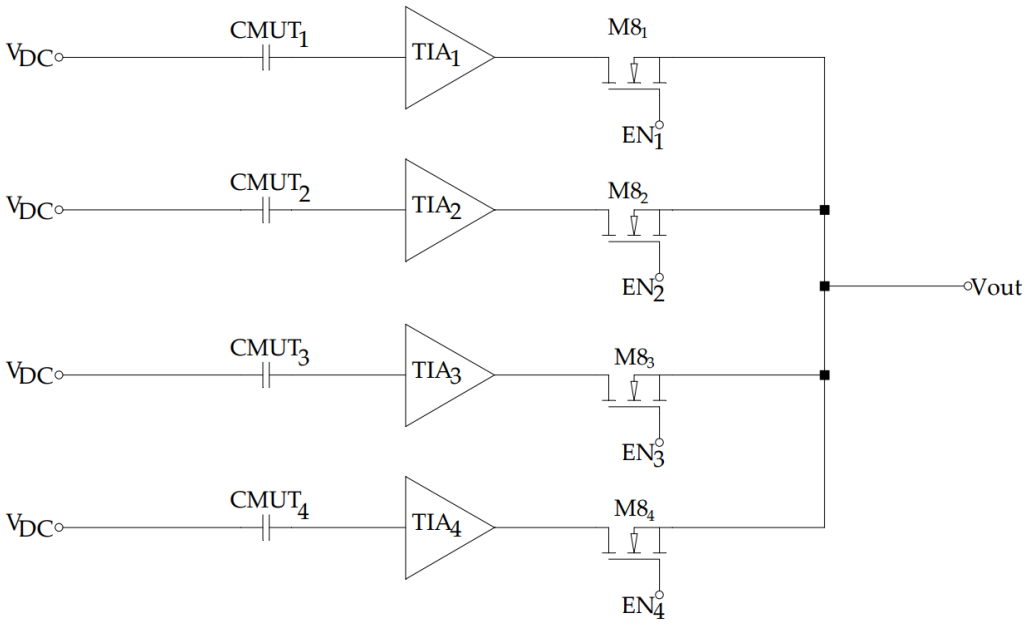

Figure 3.4: Multiplexing of Multiple TIAs

3.1.2 The Circuit Analysis

The circuit analysis is carried out and the effects of M_5 and M_8 are neglected since both transistors act only as switches. M_3 and M_4 act as PMOS cascode current source load together with NMOS cascode amplifier transistors M_1 and M_2. The PMOS transistors yields close-to-ideal current source due to the high output impedance, however causing a cost of voltage headroom. The following circuit calculations are also successfully carried out by Yavuz Kansu, in his thesis [18].

Related output impedance of the PMOS cascode current source load is provided as follows:

$$R_{l3} = r_{o3}(1 + g_{m3}r_{o4}) + r_{o4} \approx g_{m3}r_{o3}r_{o4} \tag{16}$$

It can be seen R_{l3} is intrinsic gain of M_3, which is $A_{i3} = g_{m3}r_{o3}$, multiplied by the output impedance of transistor M_4, which is r_{o4}. A long channel length is chosen for M_4 to increase the output impedance r_{o4}. Smallest possible process

length of $0.6\mu m$ is chosen for L_3 and a wide length of $240\mu m$ is chosen for W_3 of transistor M_3 and to increase the intrinsic gain A_{i3}. Now we need to find the gain of M_2, which is the gain from V_1 to V_2, to be able to find the open-loop gain of the cascode amplifier.

$$A_{v2} = \frac{V_2}{V_1} = \frac{1 + (g_{m2} + g_{mb2})r_{o2}}{r_{o2}}(r_{o2} \,||\, R_{l3}) \approx (g_{m2} + g_{mb2})r_{o2} \tag{17}$$

R_{l2}, the resistance seen from the drain of M_1 can be written as follows.

$$R_{l2} = \frac{r_{o2} + R_{l3}}{1 + (g_{m2} + g_{mb2})r_{o2}} \approx \frac{g_{m3}r_{o3}r_{o4}}{(g_{m2} + g_{mb2})r_{o2}} \tag{18}$$

Since M_1 is a common source amplifier, the gain from V_{in} to V_1 can be written as follows:

$$\begin{aligned} A_{v1} = \frac{V_1}{V_{in}} &= -g_{m1}(r_{o1} \,||R_{l2}) \\ &= -g_{m1}r_{o1}\frac{g_{m3}r_{o3}r_{o4}}{g_{m3}r_{o3}r_{o4} + (g_{m2} + g_{mb2})r_{o2}r_{o1}} \end{aligned} \tag{19}$$

The source follower stage gain is written as follows to find the gain from V_{in} to V_{out}.

$$A_{v3} = \frac{V_{out}}{V_2} \approx \frac{g_{m6}}{g_{m6} + g_{mb6}} \approx 0.85 \tag{20}$$

Open loop gain of the cascode common source amplifier becomes as follows.

$$A_v = A_{v1}A_{v2}A_{v3} \approx -0.85g_{m1}\frac{g_{m2}g_{m3}r_{o1}r_{o2}r_{o3}r_{o4}}{g_{m2}r_{o1}r_{o2} + g_{m3}r_{o3}r_{o4}} \tag{21}$$

The most dominant pole of the cascode common source amplifier system is created due the node with the highest impedance. The node in question is V_2 for two casdoded transistors are connected. Related impedance and capacitance at node V_2 is written as follows.

$$R_{out1} = [r_{o1} + r_{o2}(1 + (g_{m2} + g_{mb2})r_{o1})] \;||\; [r_{o4} + r_{o3}(1 + g_{m3}r_{o4})] \approx \frac{g_{m2}g_{m3}r_{o1}r_{o2}r_{o3}r_{o4}}{g_{m2}r_{o1}r_{o2} + g_{m3}r_{o3}r_{o4}} \tag{22}$$

$$C_{out1} = C_{DG2} + C_{DB2} + C_{DG3} + C_{DB3} + C_{GD6} \tag{23}$$

The dominant pole at the node V_2 is written as follows.

$$\omega_0 = \frac{1}{2\pi R_{out1}C_{out1}} \approx \frac{g_{m2}r_{o1}r_{o2} + g_{m3}r_{o3}r_{o4}}{2\pi(C_{DG2} + C_{DB2} + C_{DG3} + C_{DB3} + C_{GD6})(g_{m2}g_{m3}r_{o1}r_{o2}r_{o3}r_{o4})} \tag{24}$$

The unity gain bandwidth of the cascode common source amplifier is written as follows.

$$GBW = \frac{g_{m1}}{2\pi C_{out1}} \approx \frac{\sqrt{2I_{D1}K_n(W/L)_1}}{2\pi C_{out1}} \tag{25}$$

where I_{D1} is the bias current of transistor M_1, K_n is transconductance parameter for NMOS transistors. From GBW equation we can observe, to achieve a higher unity gain bandwidth C_{out1} must be smaller. Hence a small width transistor is used in the source follower stage. A wide transistor is used for the input transistor M_1 to further enhance the unity gain bandwidth.

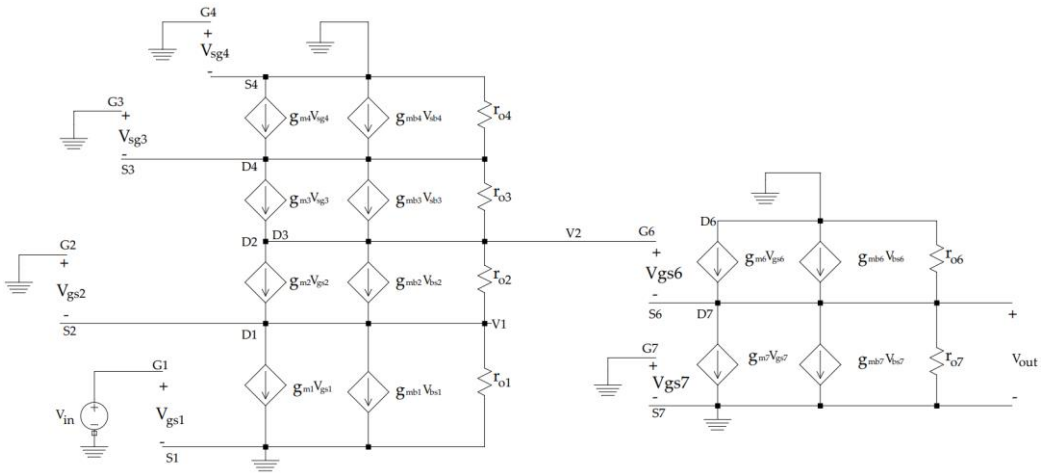

Figure 3.5. Core Amplifier Small Signal Equivalent Circuit

Above calculations for circuit analysis are completed using the small signal equivalent circuit. Fig. 3.5 shows the small signal equivalent circuit of the cascode common source amplifier with cascode current source topology. For convenience, transistors M5 and M8 are omitted in the equivalent circuit since they act only as switches. The equivalent circuit model also includes the body effect. Drain current of the transistors depends on the threshold voltage, which depends on V_{SB}, voltage difference between the base and the source of a four terminal MOSFET. In the small signal circuit model, the body effect is presented for all transistors, however for the ones who have $V_{SB} = 0$, the body effect is neglected in the circuit analysis.

3.1.3 Bias Circuit

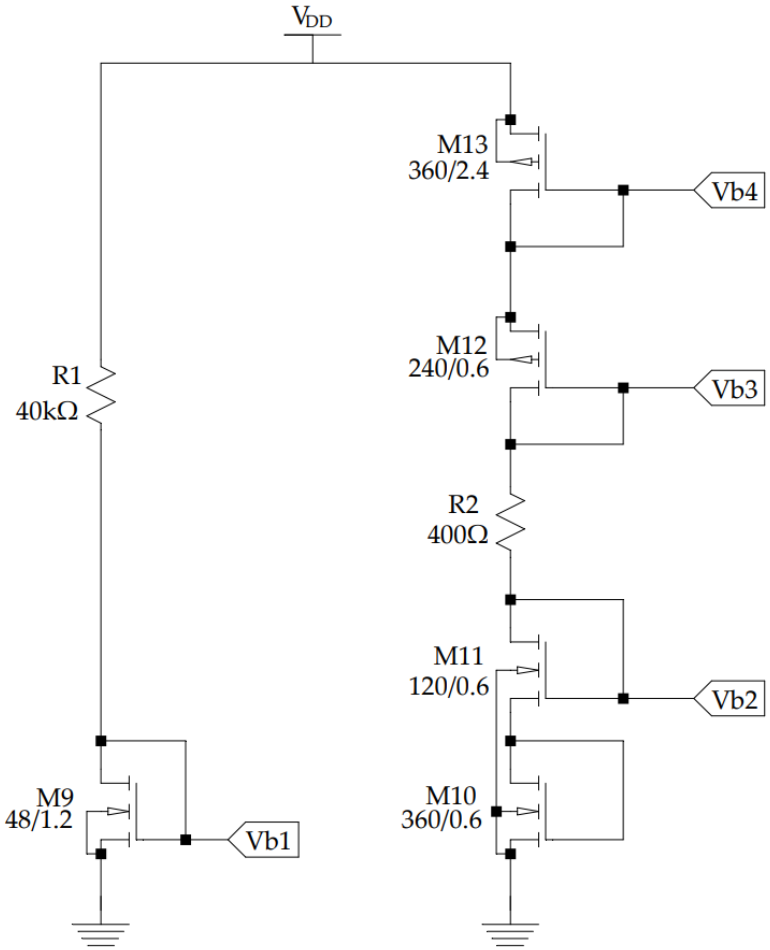

Figure 3.6: Bias Circuit Schematic

The amplifier design requires a certain biasing voltage in order to keep all amplifier MOSFETs in saturation region. For this approach a simple current mirror topology is followed. Widths and lengths of the biasing transistors corresponding to the biased transistors are kept the same to equate the reference current with the actual amplifier transistor current. The resistor R_1signifies the on-resistance of the M_5 transistor in the core amplifier.

3.1.4 Noise Analysis

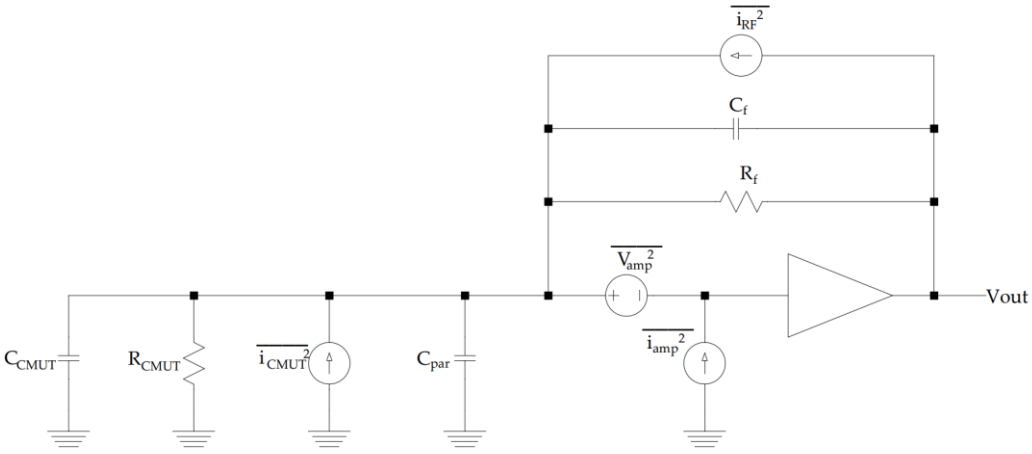

Figure 3.7: Resistive Feedback Transimpedance Amplifier Noise Sources

Since the CMUT cells produce current as output signals the input-referred current noise of the Transimpedance amplifier will be the main subject to be studied, which is discussed in detail in [15]. Above figure shows the noise sources with the circuit schematic. The total input-referred current noise is given as follows.

$$\overline{i_{in}^2} = \frac{\overline{v_{amp}^2}}{(R_{CMUT}//R_F//C_{IN,EXT})^2} + \overline{i_{amp}^2} + \overline{i_{RF}^2} + \overline{i_{CMUT}^2} \tag{26}$$

where $C_{IN,EXT}$ is the sum of external capacitances of the core amplifier which are C_{CMUT}, C_{PAR} and C_F, the CMUT capacitance, the parasitic capacitance at the amplifier input and the feedback capacitance, respectively. The thermal noise introduced by the feedback resistor R_F is shown as $\overline{i_{RF}^2}$. $\overline{i_{amp}^2}$ and $\overline{v_{amp}^2}$ indicates the input equivalent current noise source and voltage noise source, respectively. $\overline{i_{amp}^2}$ and $\overline{v_{amp}^2}$ can be expressed as follows.

$$\overline{i_{amp}^2} = \omega^2 C_{IN,AMP}^2 \frac{\overline{i_d^2}}{g_m^2} \tag{27}$$

$$\overline{v_{amp}^2} = \frac{\overline{i_d^2}}{g_m^2} \tag{28}$$

where $C_{IN,AMP}$ is the input capacitance, $\overline{i_d^2}$ is the current noise and g_m is the transconductance of the input transistor, which predominantly designates the core amplifier noise. The sum of the all input-referred current noise sources can be written as follows:

$$\overline{i_{in}^2} = \omega^2\left(C_{IN,AMP} \,//\, C_{PAR} \,//\, C_F \,//\, C_{CMUT}\right)^2 \frac{\overline{i_d^2}}{g_m^2} + \frac{1}{(R_{CMUT} \,//\, R_F)^2}\frac{\overline{i_d^2}}{g_m^2} + \frac{4kT}{R_F} + \frac{4kT}{R_{CMUT}} \tag{29}$$

$C_{IN,AMP}$ can be calculated with the equation given in Yavuz Kansu's thesis [18]:

$$C_{IN,AMP} = W_1\{(2 - g_m r_o)C_{ov} + \frac{2L_1 C_{ox}}{3}\} \tag{30}$$

where W_1 is the width, $L_1$is the length, C_{ov} is the overlap capacitance and C_{ox} is the gate capacitance of the input transistor M_1. Below is the table for parameters already calculated in previous sections, to be used to solve the total input-referred current noise equation.

R_F	$120k\Omega$
C_F	$53fF$
R_{CMUT}	$223.46k\Omega$
C_{CMUT}	$0.184pF$
C_{PAR}	$1p$
W_1/L_1	$360\mu/0.6\mu$
C_{ov}	$134.6fF$
C_{ox}	$498fF$
g_m	$7.729m$
r_o	$1.709k\Omega$

Table 3: Noise Figure Parameters

From the above calculated and measured parameters, we calculate and plot the total input referred current noise as follows. At $7.5MHz$, the calculated input referred noise is approximately $0.46pA/\sqrt{Hz}$.

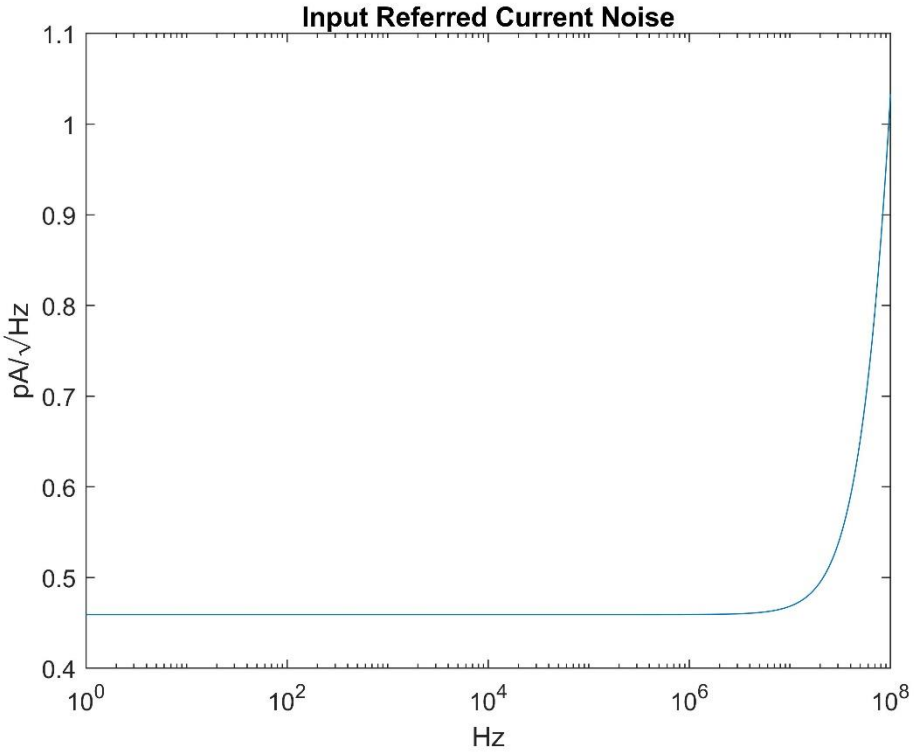

Figure 3.8: Calculated Input Referred Current Noise

3.1.5 MOSFET Feedback Resistor Version

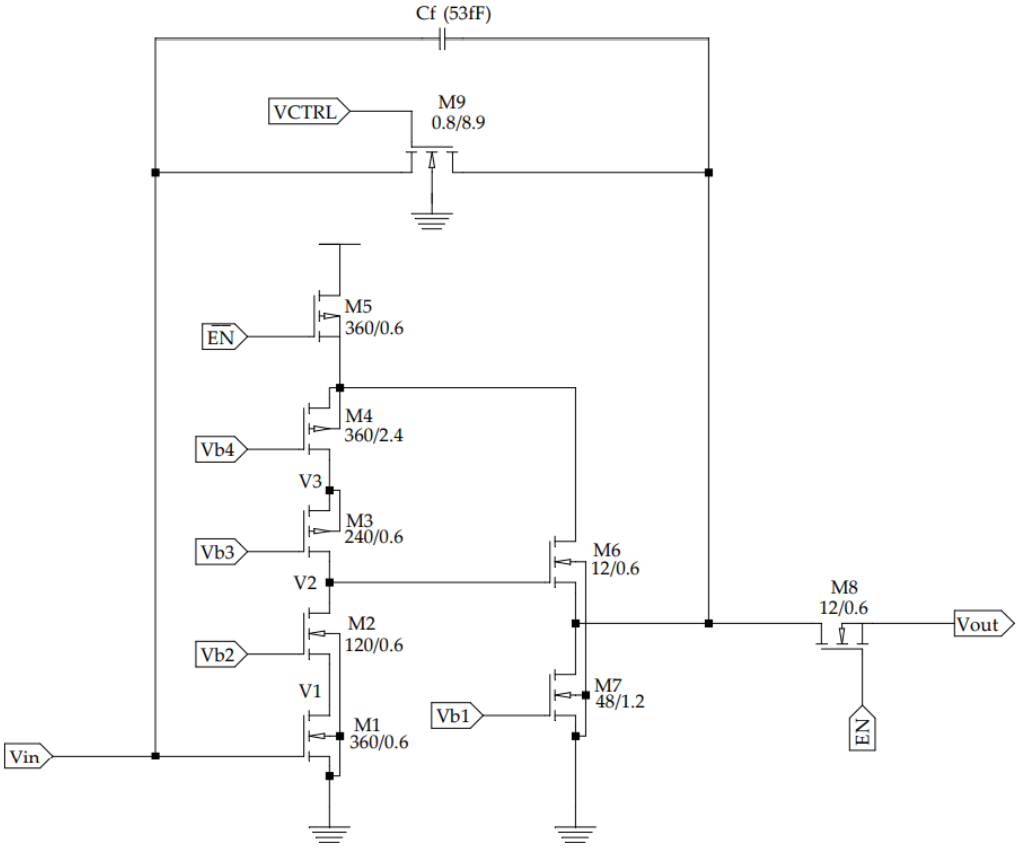

Figure 3.9: Cascode Common Source Amplifier with NMOS Transistor Feedback Resistance

As an optional choice for the feedback resistance, an NMOS transistor with long channel in linear region is introduced instead of the passive resistor. As stated in [15], the choice if active resistor further stabilizes the circuit for higher feedback capacitance values and ideally enables us to increase the feedback resistance for higher bandwidth applications.

Additional advantage provided with the use of active feedback resistance as a long channel MOSFET device is to dynamically change the resistance with a single control voltage, resulting in changing the transimpedance gain on-demand. Even though the TIA is designed for particular CMUT devices which are carefully designed and microfabricated for specified feature size, the dynamic transimpedance gain enables us to cancel unwanted noise introduced in higher or lower frequencies of the bandwidth.

In layout design of the circuit, polysilicon layer is used for passive resistance values. However, these passive polysilicon resistors cover too much space, even larger than or equal to the area needed for the core amplifier transistors. Hence, using a single long channel NMOS transistor device enables us to reduce the layout design size to almost half compare to layout design with passive polysilicon resistance. Comparison of passive polysilicon resistance and single NMOS transistor as active resistance is conducted in Layout Design chapter.

The size of the long channel NMOS resistance must be calculated according to the passive polysilicon resistance, which yielded $120k\Omega$. The equation to be used is as follows.

$$R_f = \frac{1}{\mu_N C_{OX} \frac{W}{L} (V_{CTRL} - V_{OUT} - V_T)} \tag{31}$$

where μ_N is the carrier mobility, C_{OX} is the gate capacitance per unit area, W and L are the channel width and length of the NMOS transistor, respectively, V_T is the threshold voltage of the NMOS transistor. V_{CTRL} is the related control voltage to dynamically alter the closed loop gain of the TIA.

For $120k\Omega$, aspect ratio of the NMOS transistor is set to be $W/L = 0.8\mu/8.9\mu$ and V_{CTRL} is set to $3.6V$.

3.2 Schematic Simulations

The circuit simulations to find the bandwidth, transimpedance gain and noise of the amplifier are completed using Cadence Virtuoso Analog Design Environment. For this section, simulations are completed for the ideal state of the both amplifier designs, which means the parasitic capacitances and resistances introduced in layout design process is omitted. Post-layout simulations and their comparison with the schematic simulations will be presented in the Layout Design chapter.

The power consumption is simulated to be $3.39mW$ for the resistive feedback transimpedance amplifier, $3.33mW$ for MOSFET feedback resistor transimpedance amplifier and $3.44mW$ for the bias circuit.

3.2.1 Resistive Feedback TIA Simulations

3.2.1.1 Transimpedance Gain Simulation

To successfully simulate the circuit for CMUT receiver mode applications, the CMUT cell must be modeled for spice programs. In CMUT Equivalent Circuit Model chapter, the needed variables to enter the simulation program are calculated.

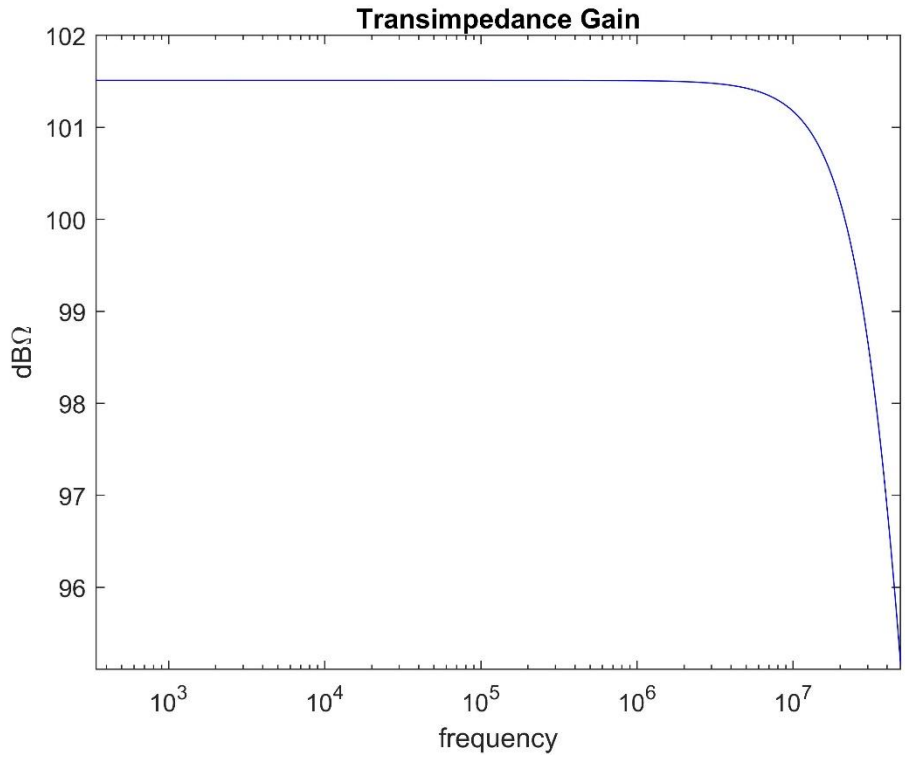

Figure 3.10: TIA Transimpedance Gain

Fig. 3.9 shows the transimpedance gain of the amplifier. Feedback resistance and capacitance values are calculated to provide a $25MHz$ bandwidth and simulation results shows that we have succeeded in achieving the desired value.

3.2.1.2 Transient Simulations

As a trial, an input of $3\mu A$ amplitude sinusoidal input current at 7.5MHz is given to the designed resistive feedback transimpedance amplifier as input.

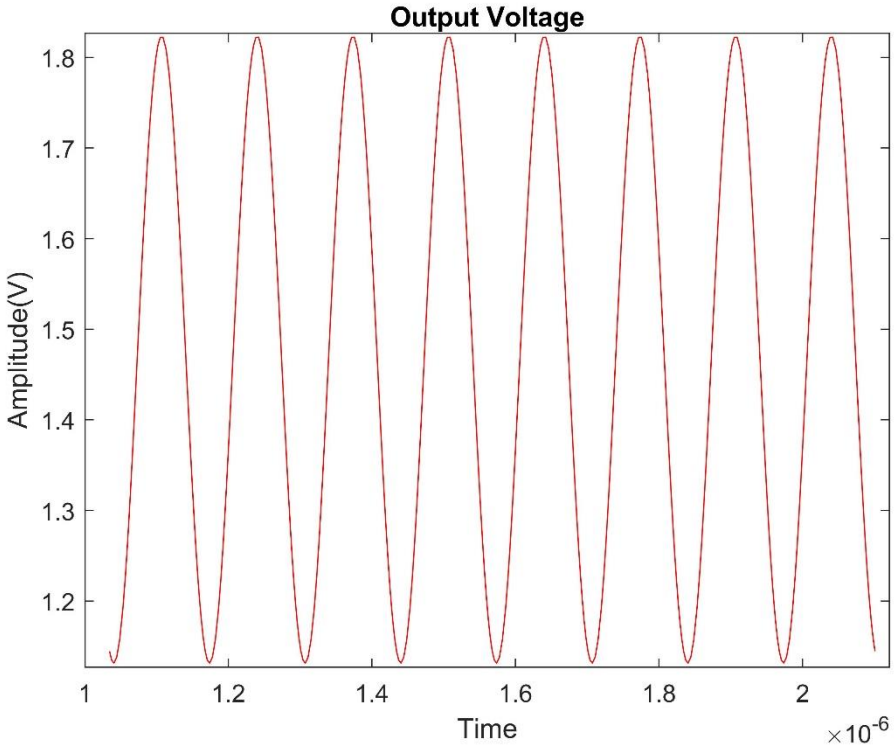

Figure 3.11: TIA output voltage to 3µA input

The output yields a sinusoidal wave at 7.5MHz with $0.7V$ peak-to-peak amplitude. If we calculate the transimpedance gain for this set of input and output, we find:

$$TIA_{gain} = 20log\left(\frac{0.7V}{6\mu A}\right) \tag{32}$$

$$TIA_{gain} = 101.3dB\Omega \tag{33}$$

For a more realistic input-output relation, calculated CMUT short circuit current i_{sc} of $1.1nA$ peak input is fed to the TIA.

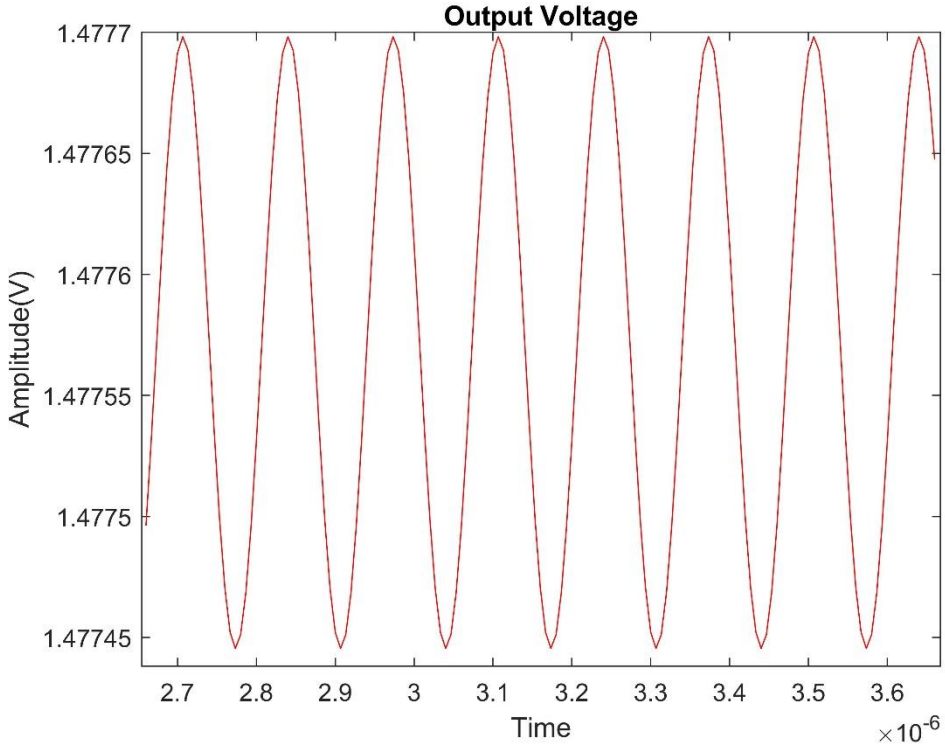

Figure 3.12: TIA output voltage to 1.1nA input

The output yields a sinusoidal wave at 7.5MHz with $0.253mV$ amplitude. If we calculate the transimpedance gain for this set of input and output, we find:

$$TIA_{gain} = 20log\left(\frac{0.253mV}{2.2nA}\right) \tag{34}$$

$$TIA_{gain} = 101.2dB\Omega \tag{35}$$

3.2.1.3 Noise Simulations

In this section the noise simulations are completed for schematic view of the circuit. Simulated input referred current noise is compared with the calculated input referred current noise.

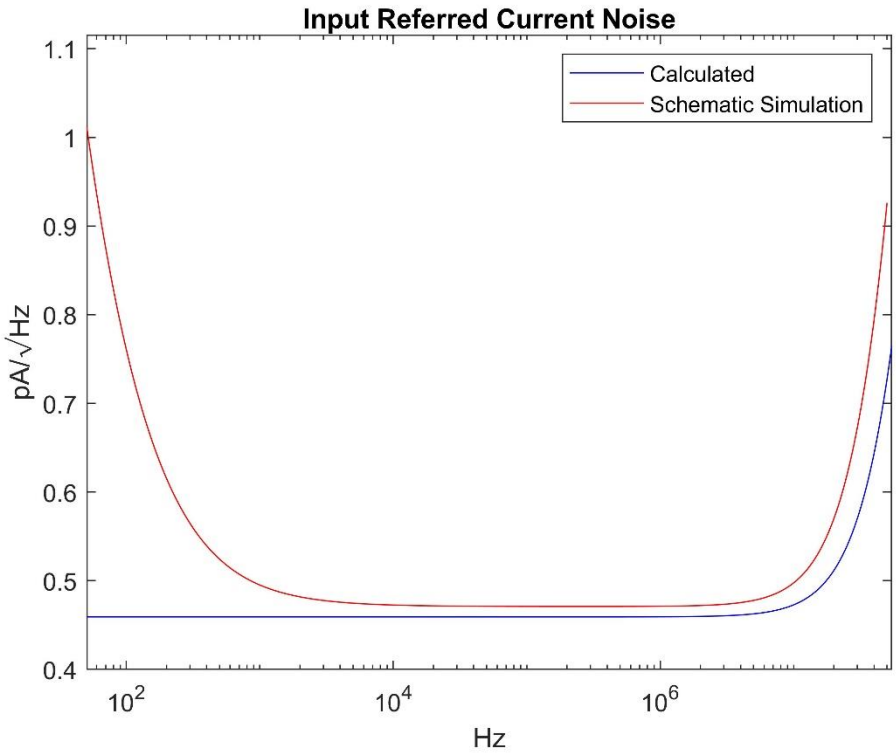

Figure 3.13: Simulated vs. Calculated Input Referred Current Noise Comparison

As can be seen from the plot, there occurs a difference in lower frequency regions. This is due to the flicker noise of the transistors, which is omitted in Matlab calculations. At $7.5MHz$, the simulated input referred noise is approximately $0.48pA/\sqrt{Hz}$.

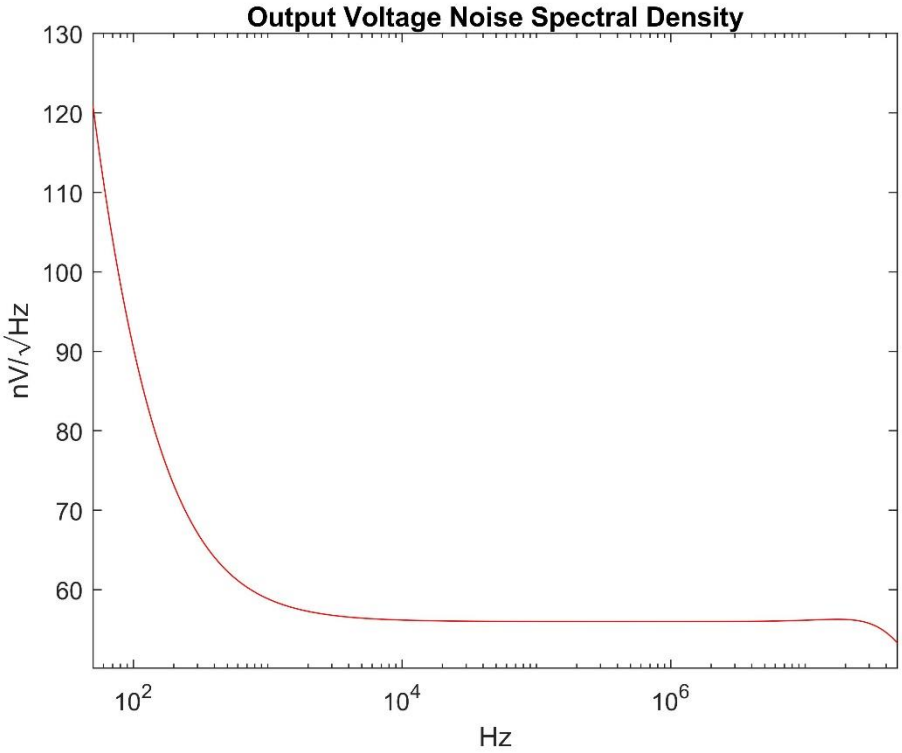

Figure 3.14: Output Voltage Noise Spectral Density

At 7.5MHz, the output voltage noise is simulated to be approximately $56.09nV/\sqrt{Hz}$. The comparison with the post layout noise simulation is provided in the Layout Design chapter.

3.2.2 MOSFET Feedback TIA Simulations

3.2.2.1 Transimpedance Gain Simulation

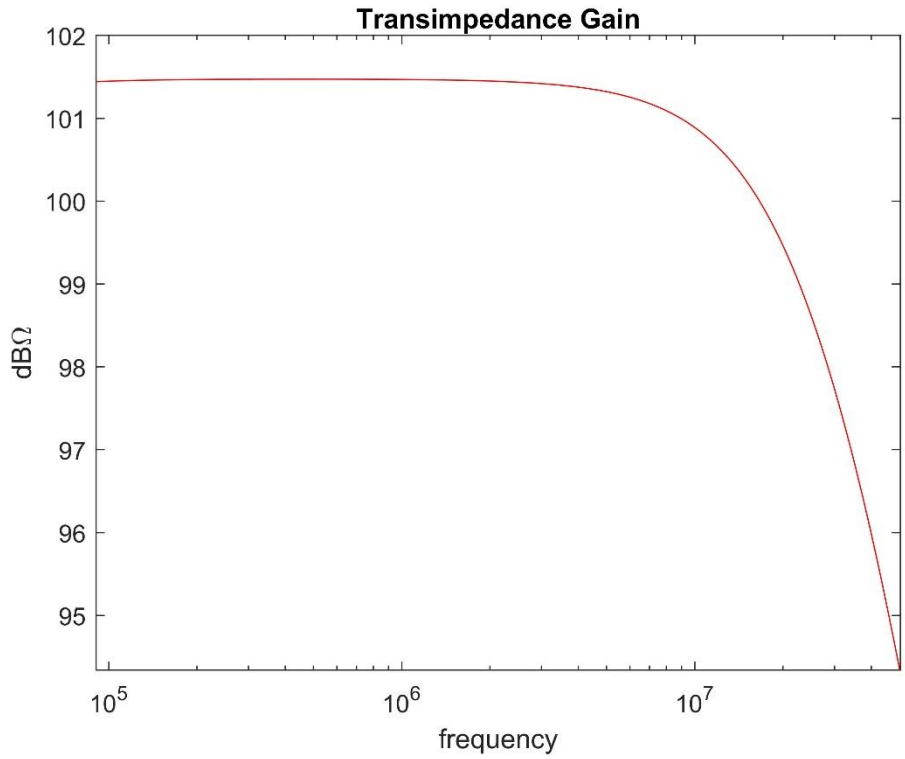

Figure 3.15: TIA Transimpedance Gain

Fig. 3.17 shows the transimpedance gain of the MOSFET feedback resistance transimpedance amplifier. Feedback resistance and capacitance values are calculated to provide a $25MHz$ bandwidth and simulation results shows that we have succeeded in achieving the desired value.

3.2.2.2 Transient Simulations

As a trial, an input of $3\mu A$ peak-to-peak sinusoidal input current at 7.5MHz is given to the designed transimpedance amplifier as input.

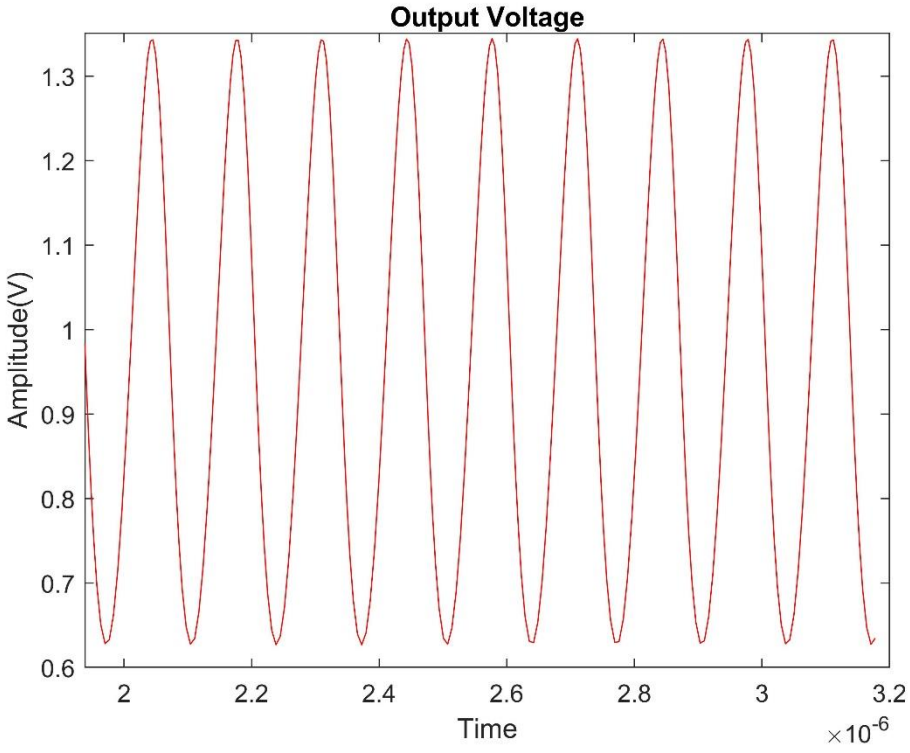

Figure 3.16: TIA output voltage to 3µA input current

The output yields a sinusoidal wave at 7.5MHz with $0.7V$ amplitude. If we calculate the transimpedance gain for this set of input and output, we find:

$$TIA_{gain} = 20log\left(\frac{0.719V}{6\mu A}\right) \tag{36}$$

$$TIA_{gain} = 101.6dB\Omega \tag{37}$$

For a more realistic input-output relation, $1.1nA$ peak input is fed to the TIA since short circuit current i_{sc} of the designed CMUT is calculated to be $1.1nA$.

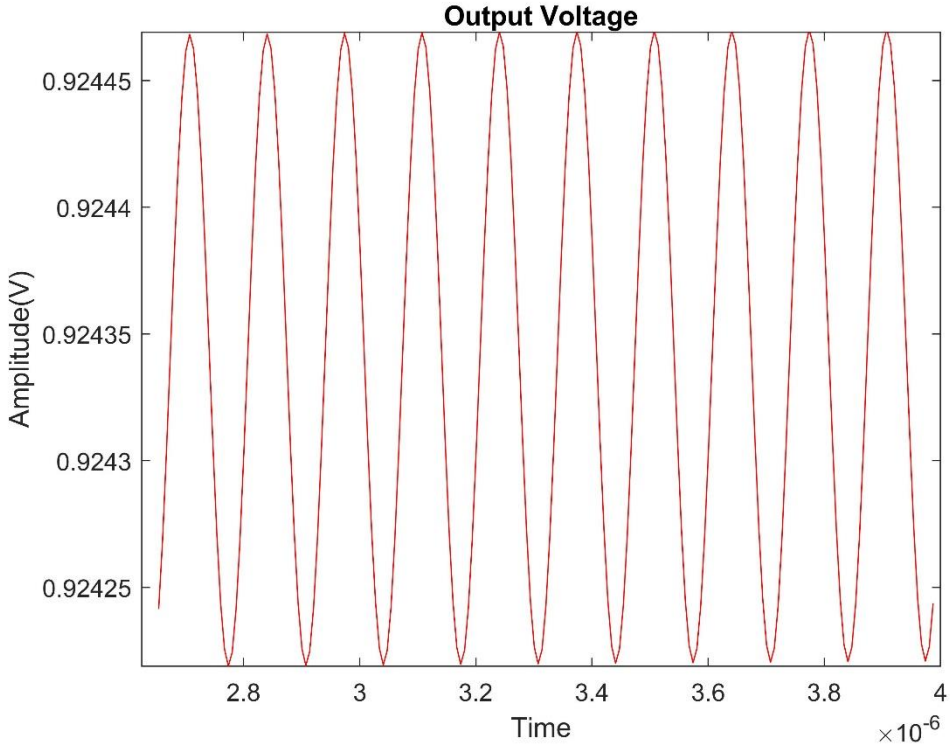

Figure 3.17: TIA output voltage to 1.1nA input current

The output yields a sinusoidal wave at 7.5MHz with $0.249mV$ amplitude. If we calculate the transimpedance gain for this set of input and output, we find:

$$TIA_{gain} = 20log\left(\frac{0.249mV}{2.2nA}\right) \tag{38}$$

$$TIA_{gain} = 101.1dB\Omega \tag{39}$$

3.2.2.3 Noise Simulations

In this section the noise simulations are completed for schematic view of the MOSFET feedback resistance transimpedance amplifier circuit. Simulated input referred current noise is compared with the calculated input referred current noise.

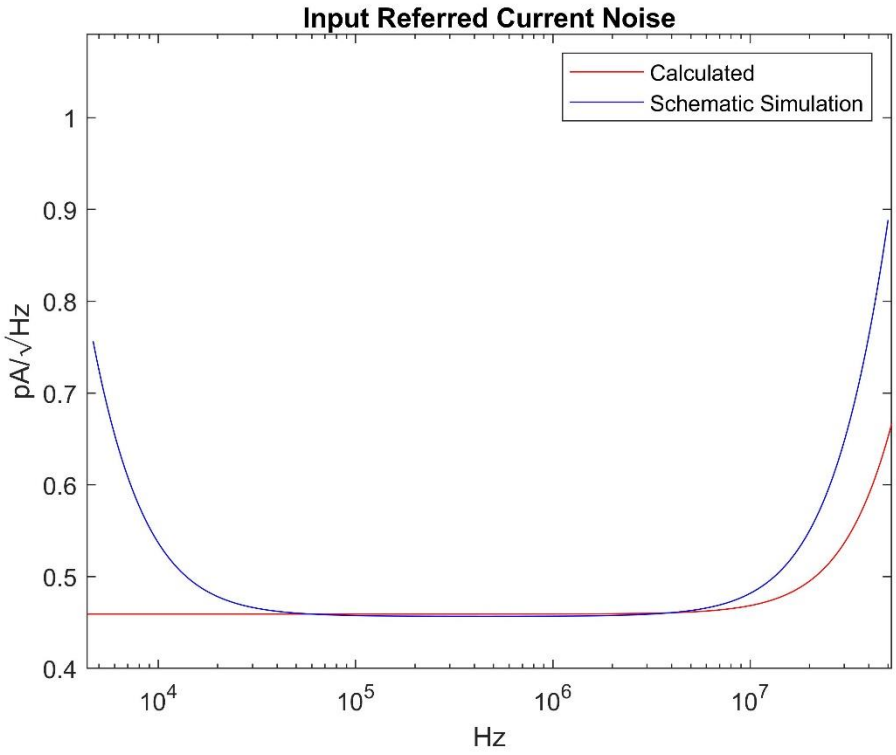

Figure 3.18: Simulated vs. Calculated Input Referred Current Noise Comparison

As can be seen from Fig. 3.17, there occurs a difference in lower frequency regions. This is due to the flicker noise of the transistors, which is omitted in Matlab calculations. At $7.5MHz$, the simulated input referred noise is approximately $0.47pA/\sqrt{Hz}$.

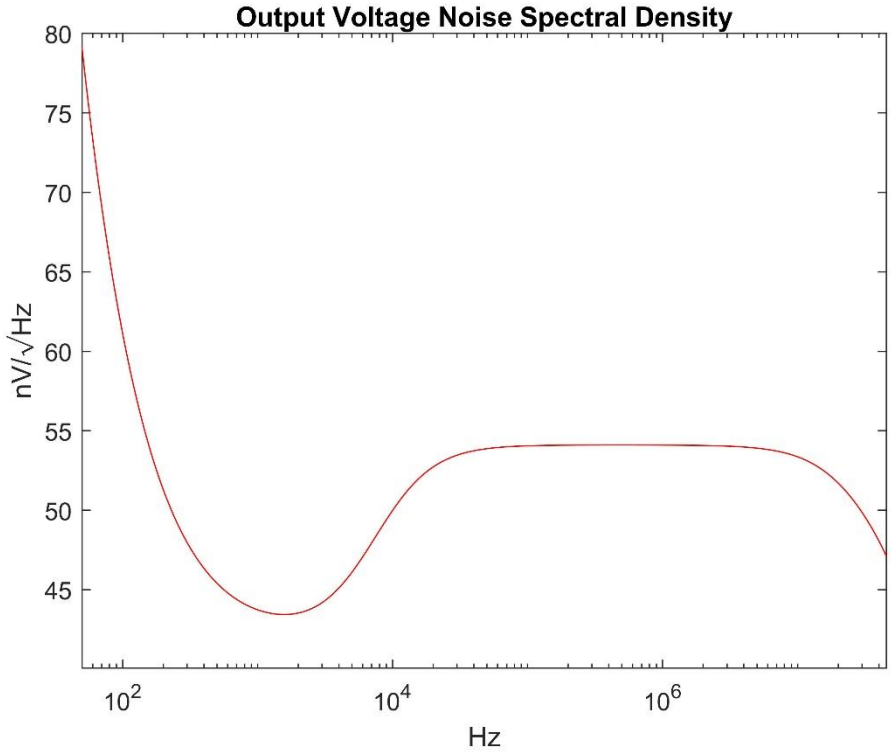

Figure 3.19: Output Voltage Noise Spectral Density

At 7.5MHz, the output voltage noise is simulated to be approximately $53.6nV/\sqrt{Hz}$. The comparison with the post-layout noise simulation is provided in the Layout Design chapter.

Chapter 4

Layout Design

4.1 XFAB Foundry Layout Specifications

The resistive feedback transimpedance amplifier is designed on Cadence Virtuoso Analog Design Environment [8] using the XFAB "0.6 Micron Modular Mixed Signal Technology with Embedded Non-Volatile Memory and High Voltage Option" $0.6\mu m$ – XC06M3 process. The circuit is simulated using Virtuoso Schematic Editor L and following the successful simulations the Virtuoso Layout Suite L is used for designing the layout.

Before proceeding with the post-layout simulations, the layout designs are passed through generic tests, such as Design Rule Check (DRC) and Layout Versus Schematic (LVS). All designs included perfect schematic match and no DRC errors.

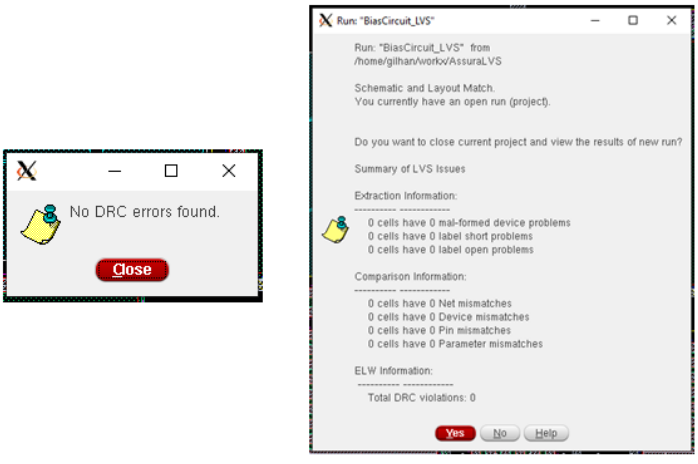

Figure 4.1: DRC and LVS

After DRC and LVS match, we proceeded with the parasitic extraction using Quantus QRC. All post-layout simulations incorporated the parasitic extracted versions of the circuits to thoroughly simulate the fabricated versions.

4.2 TIA Layout

4.2.1 Resistive Feedback Transimpedance Amplifier Layout

The resistive feedback transimpedance amplifier design consists of a feedback resistor, a feedback capacitor and 8 MOSFET devices, being 5 NMOS transistors and 3 PMOS transistors. The resistor at hand is $120k\Omega$ and "High Resistive Poly" *rpolyh* is used for layout drawing of the resistance. To avoid the feedback resistor taking up space in linear shape placing, meander90 shape is used instead. In order save as much space as possible in layout and since we have large width transistors, multi-finger gate is used in layout version of the circuit.

The layout size of the resistive feedback transimpedance amplifier design is measured to be $146.4\mu m$ by $108.8\mu m$. The circuit input signal and the bias voltage inputs are set on the left side whereas the output signal and the enable signal voltages for power on-off switch transistor and multiplexer transistor are set on the right side of the layout.

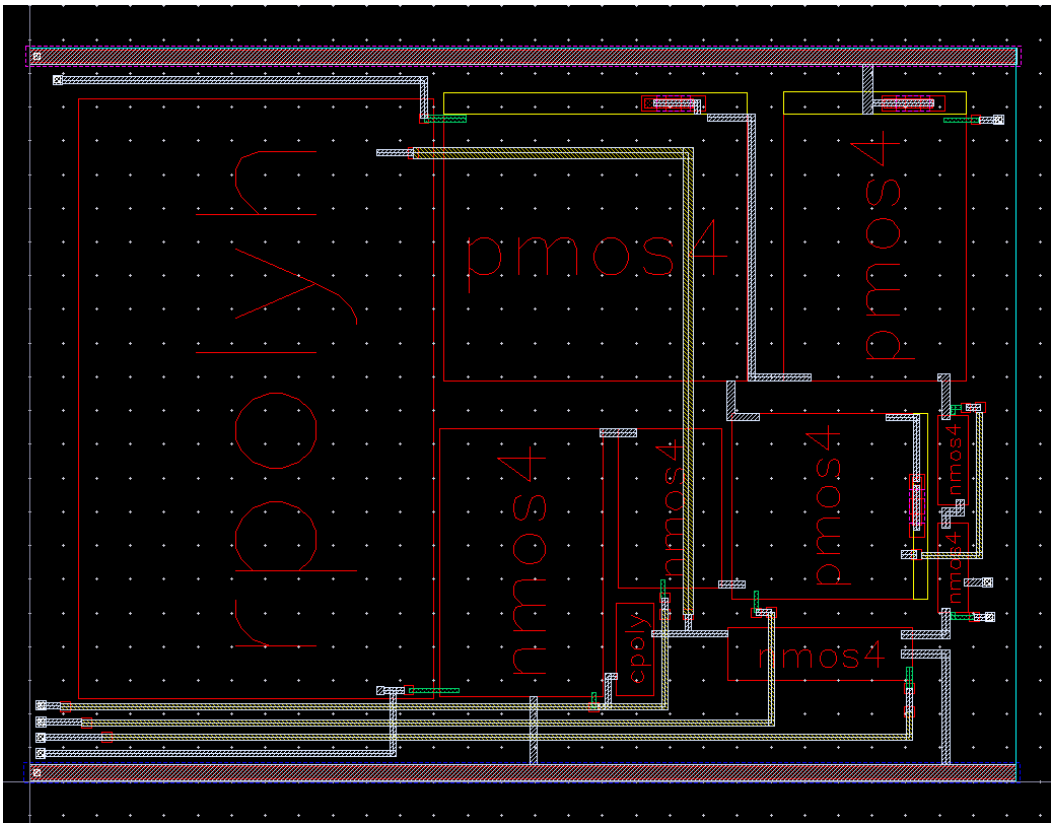

Figure 4.2: Resistive Feedback Transimpedance Amplifier Layout Outline

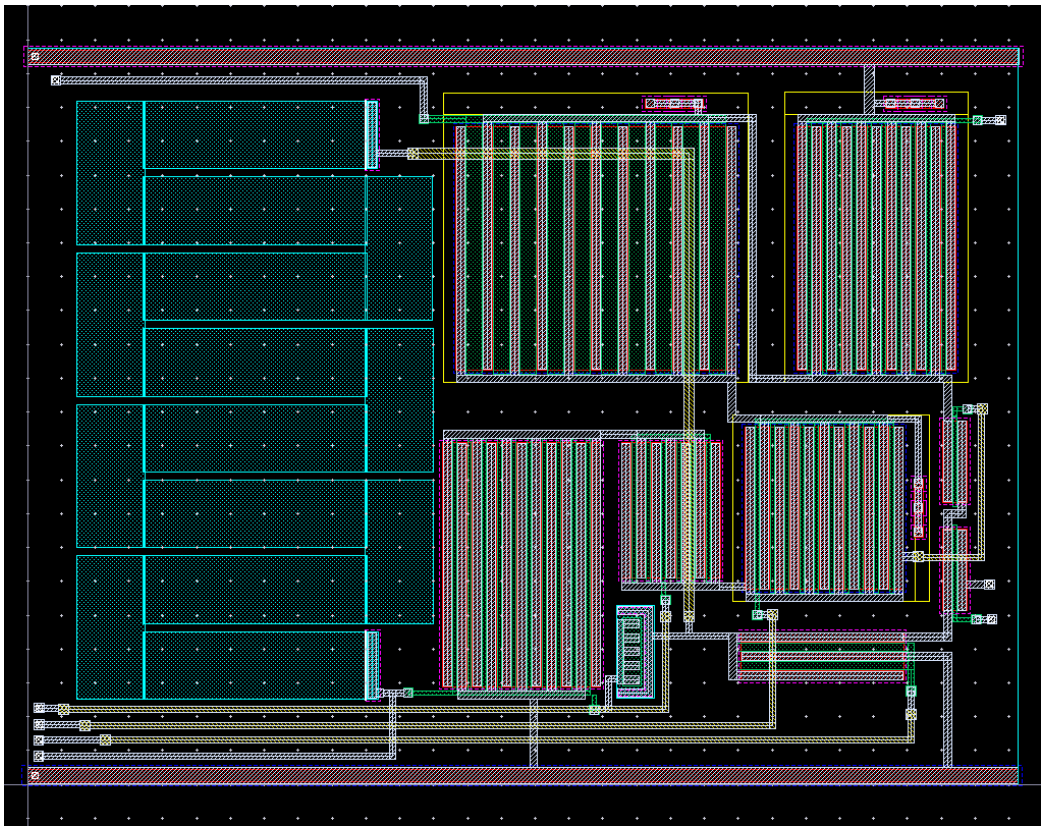

Figure 4.3: Resistive Feedback Transimpedance Amplifier Layout

4.2.2 MOSFET Feedback Resistor Transimpedance Amplifier Layout

The MOSFET feedback transimpedance amplifier design consists of a voltage controlled NMOS transistor as the feedback resistance, a feedback capacitor and 8 MOSFET devices, being 5 NMOS transistors and 3 PMOS transistors. Since passive high resistance polysilicon resistors of *rpolyh* covers much space, the use of voltage controlled MOSFET resistance is found suitable as a different option. In order to achieve the feedback resistance of $120k\Omega$, $W/L = 0.8\mu/8.9\mu$ is set for the feedback MOSFET and control voltage V_{CTRL} is set to $3.6V$. Again, in order save as much space as possible in layout and since we have large width transistors, multi-finger gate is used in layout version of the circuit.

The layout size of the MOSFET feedback resistor transimpedance amplifier design is measured to be $91.5\mu m$ by $107.6\mu m$. The circuit input signal, MOSFET feedback resistor control signal and the bias voltage inputs are set on the left side whereas the output signal and the enable signal voltages for power on-off switch transistor and multiplexer transistor are set on the right side of the layout.

By using a MOSFET feedback resistance instead of a high-density polysilicon resistor, we save up approximately 40% layout space, hence lowering the fabrication costs.

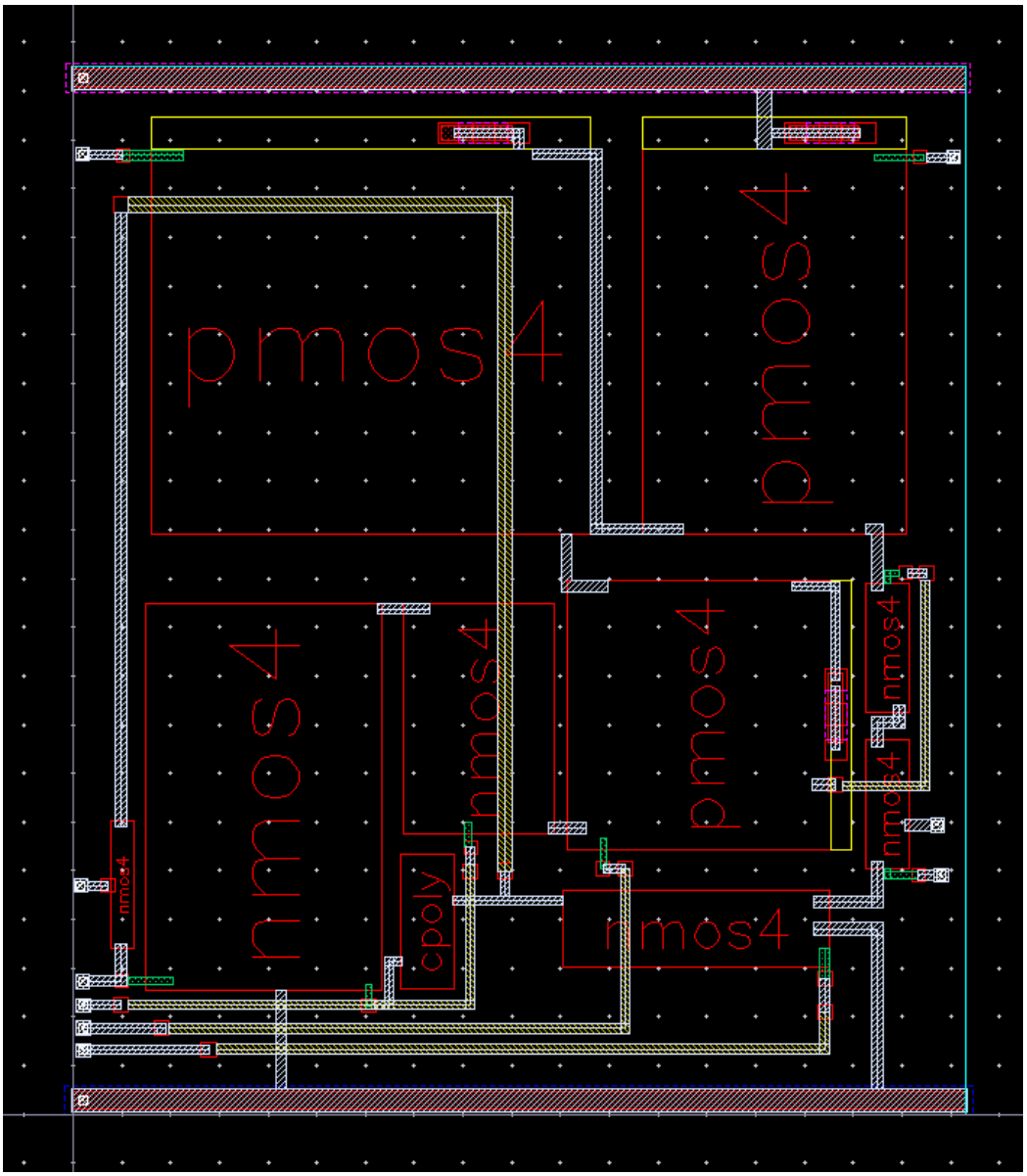

Figure 4.4: MOSFET Feedback Resistor Transimpedance Amplifier Layout Outline

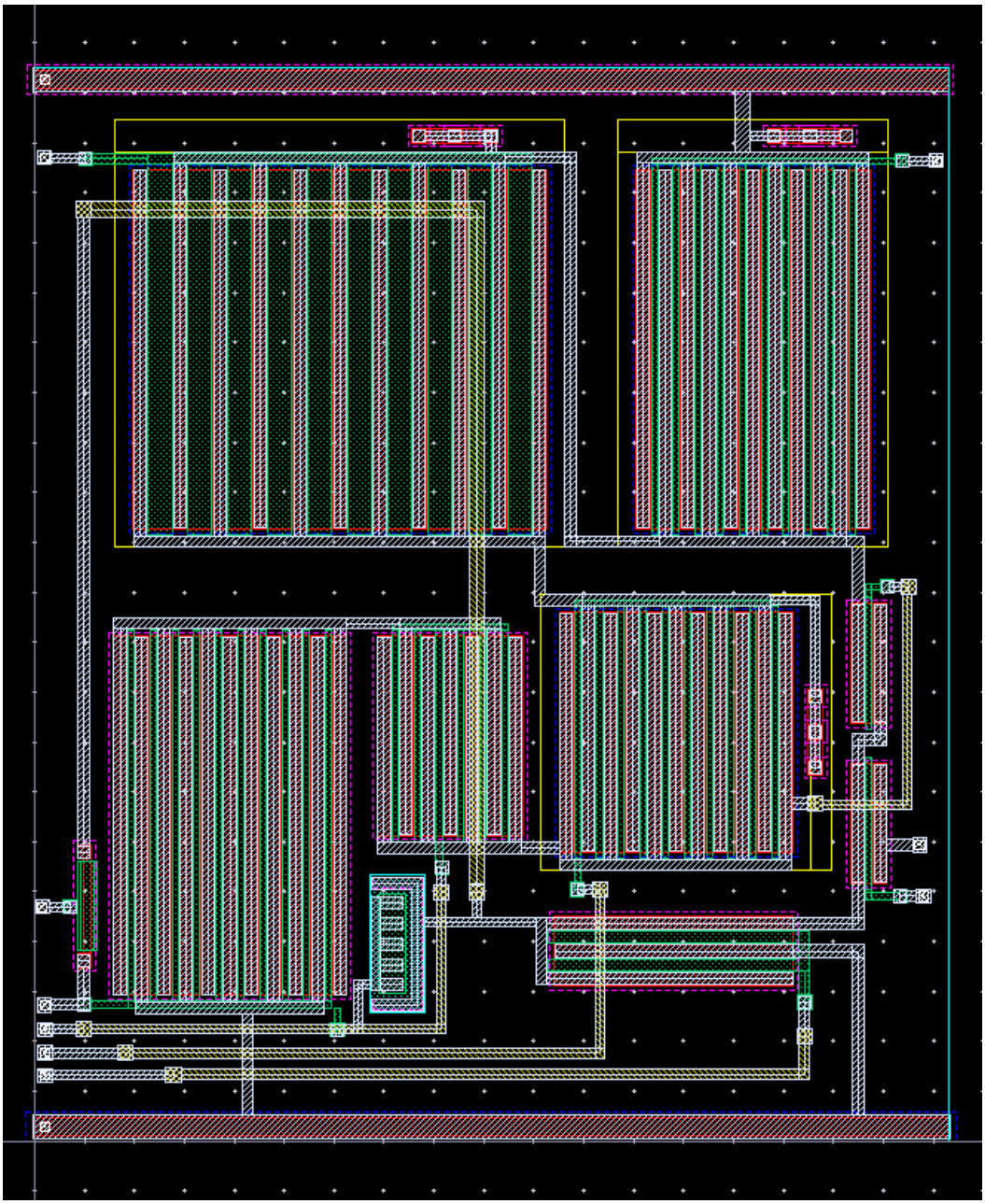

Figure 4.5: MOSFET Feedback Resistor Transimpedance Amplifier Layout

4.2.3 Bias Circuit Layout

Bias circuit for transimpedance amplifier consists of 2 resistors and 5 MOSFET devices, being 3 NMOS transistors and 2 PMOS transistors. The first resistor in use is $39k\Omega$ and "High Resistive Poly" *rpolyh* is used for layout drawing of the resistance. To avoid the high value resistor taking up space in linear shape placing, meander90 shape is used instead. Similar to the core amplifier layout design, in order save as much space as possible in layout and since we have large width transistors, multi-finger gate is used in layout version of the bias circuit as well.

The layout size of the bias circuit design is measured to be $110.9\mu m$ by $84.7\mu m$. The bias voltage outputs are set on the right side of the layout to match with the left-side input design of the core transimpedance amplifier.

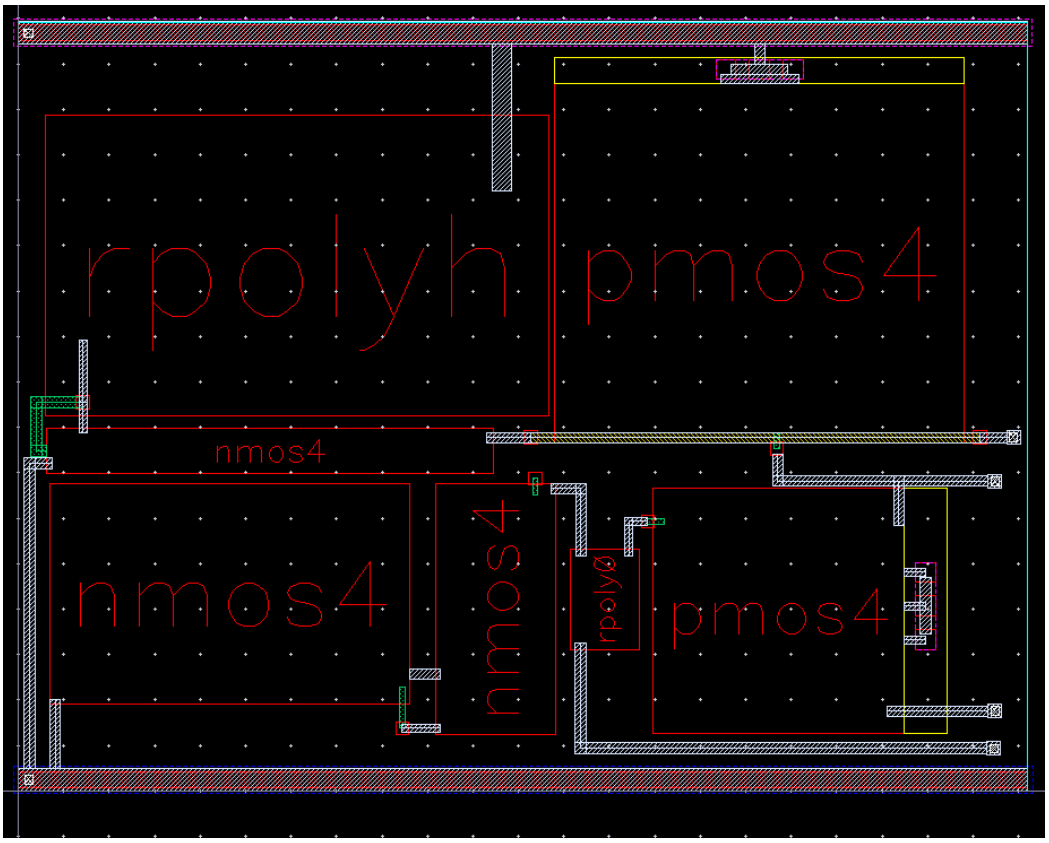

Figure 4.6: Bias Circuit Layout Outline

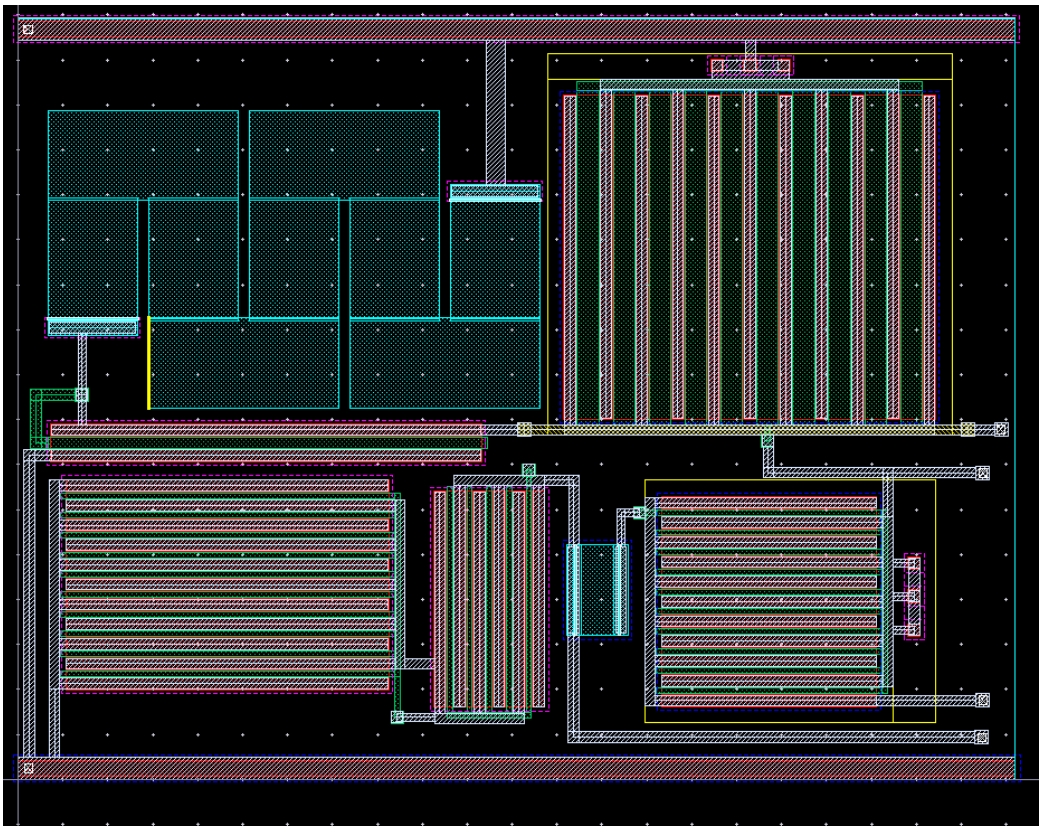

Figure 4.7: Bias Circuit Layout

4.3 Post-Layout Simulations

After completing the layout design and acquiring the parasitic extracted versions of the circuits, we proceed with the post-layout simulations and their comparison with the schematic simulations. The post-layout simulations to find the bandwidth and transimpedance gain, transient signals and the noise figures of the amplifier are completed using Cadence Virtuoso Analog Design Environment with a config file to incorporate the parasitic extracted versions into the test bench.

The post-layout power consumption is simulated to be $3.28mW$ for the resistive feedback transimpedance amplifier, $3.2mW$ for MOSFET feedback resistor transimpedance amplifier and $3.35mW$ for the bias circuit.

4.3.1 Resistive Feedback TIA Post-Layout Simulations

In this section the post-layout simulations of the resistive feedback transimpedance amplifier are provided. Comparisons with the schematic simulations and calculations are conducted.

4.3.1.1 Transimpedance Gain Simulation

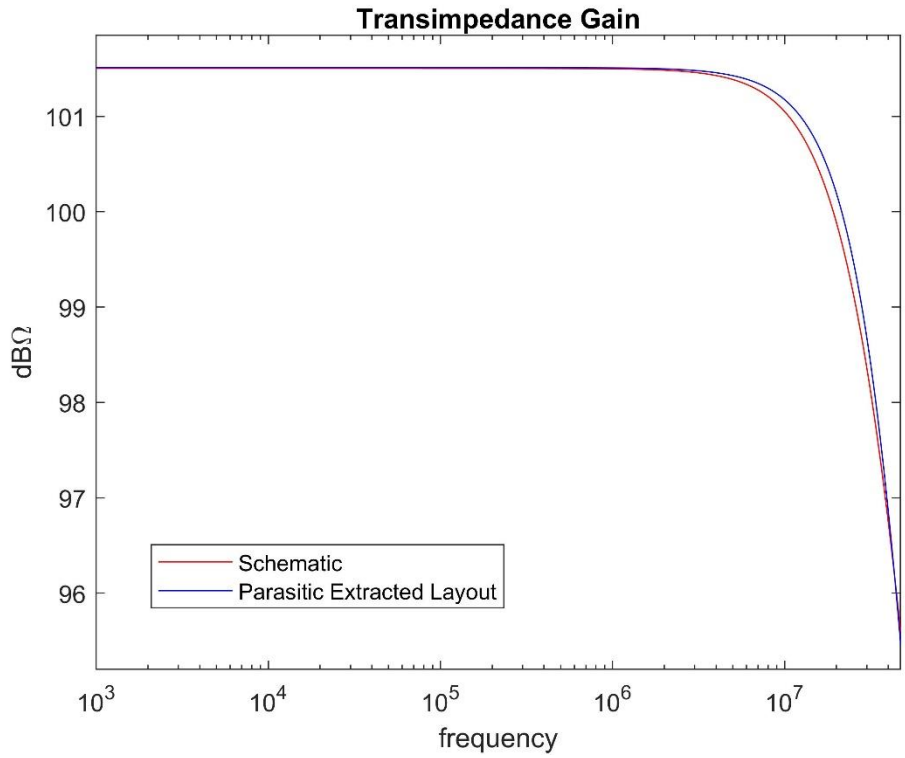

Figure 4.8: Schematic vs. Post-Layout Transimpedance Gain Comparison

As can be seen from the Fig. 4.8, the transimpedance gain changes slightly compare to the schematic simulations.

4.3.1.2 Transient Simulations

Similar to the schematic transient simulation, an input of $3\mu A$ peak-to-peak sinusoidal input current at 7.5MHz is given to the designed resistive feedback transimpedance amplifier as input.

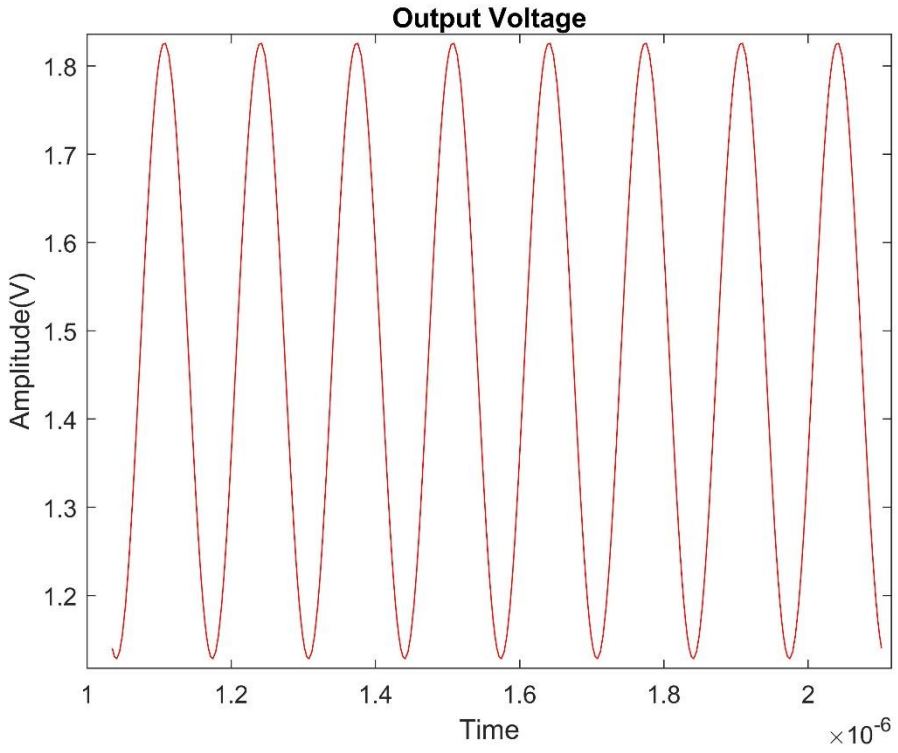

Figure 4.9: TIA output voltage to 3µA input current

The output yields a sinusoidal wave at 7.5MHz with $0.697V$ amplitude. If we calculate the transimpedance gain for this set of input and output, we find:

$$TIA_{gain} = 20log\left(\frac{0.697V}{6\mu A}\right) \tag{40}$$

$$TIA_{gain} = 101.3dB\Omega \tag{41}$$

For a more realistic input-output relation, calculated CMUT short circuit current i_{sc} of $1.1nA$ peak input is fed to the resistive feedback TIA.

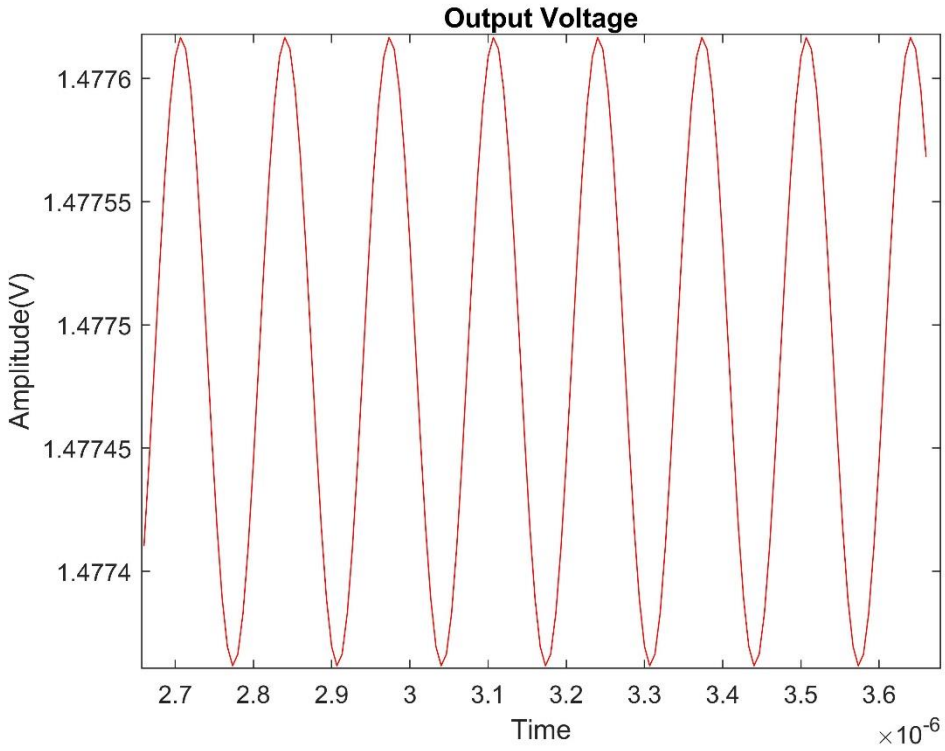

Figure 4.10: TIA output voltage to 1.1nA input current

The output yields a sinusoidal wave at 7.5MHz with $0.255mV$ amplitude. If we calculate the transimpedance gain for this set of input and output, we find:

$$TIA_{gain} = 20log\left(\frac{0.255mV}{2.2nA}\right) \tag{42}$$

$$TIA_{gain} = 101.3dB\Omega \tag{43}$$

4.3.1.3 Noise Simulations

In this section, post-layout noise simulations are conducted for input referred current noise and the output voltage noise spectral density of the resistive feedback transimpedance amplifier. Input referred current noise simulation is compared with the calculated and schematic simulated counterparts. The output voltage noise spectral density is compared with the schematic simulated version. Below are the related plots.

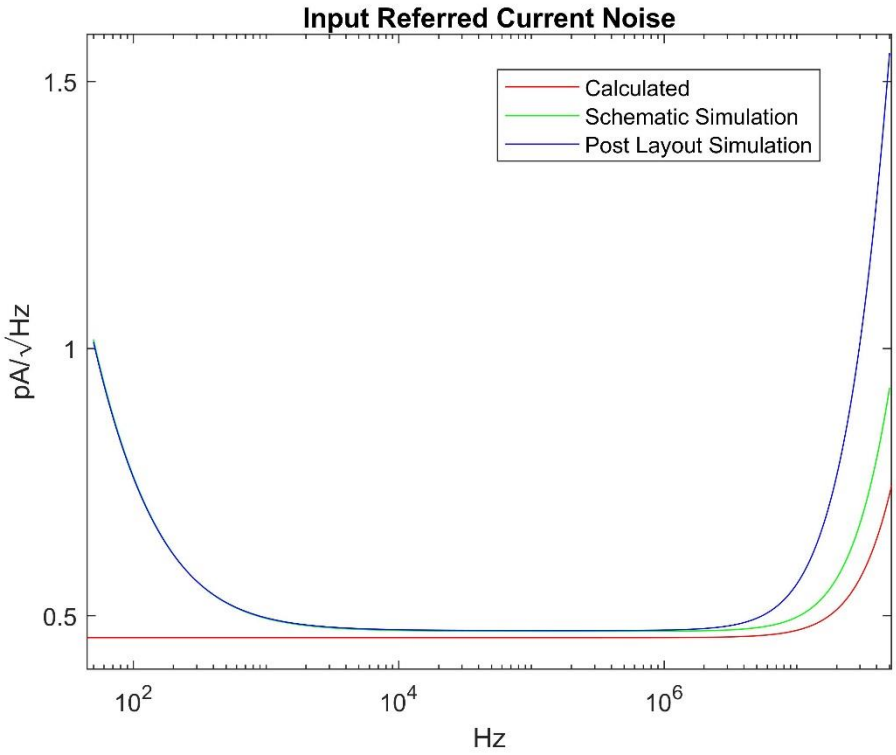

Figure 4.11: Input Referred Current Noise Comparison

At 7.5MHz, the input referred current noise is approximately $0.5pA/\sqrt{Hz}$ for post-layout, parasitic extracted resistive feedback transimpedance amplifier compare to $0.48pA/\sqrt{Hz}$ for schematic simulation and $0.46pA/\sqrt{Hz}$ for theoretical calculation.

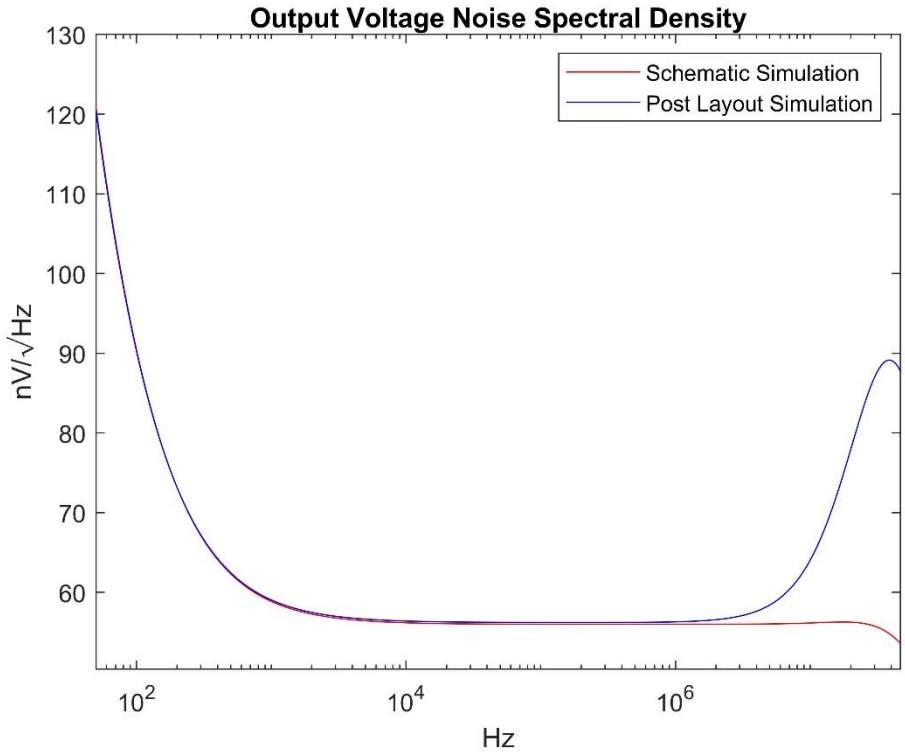

Figure 4.12: Output Voltage Noise Spectral Density Comparison

At 7.5MHz, the total output voltage noise density is approximately $60.95nV/\sqrt{Hz}$ for parasitic extracted resistive feedback transimpedance amplifier compare to $56.09nV/\sqrt{Hz}$ for schematic simulation.

4.3.2 MOSFET Feedback TIA Post-Layout Simulations

In this section the post-layout simulations of the MOSFET feedback transimpedance amplifier are provided. Comparisons with the schematic simulations and calculations are conducted.

4.3.2.1 Transimpedance Gain Simulation

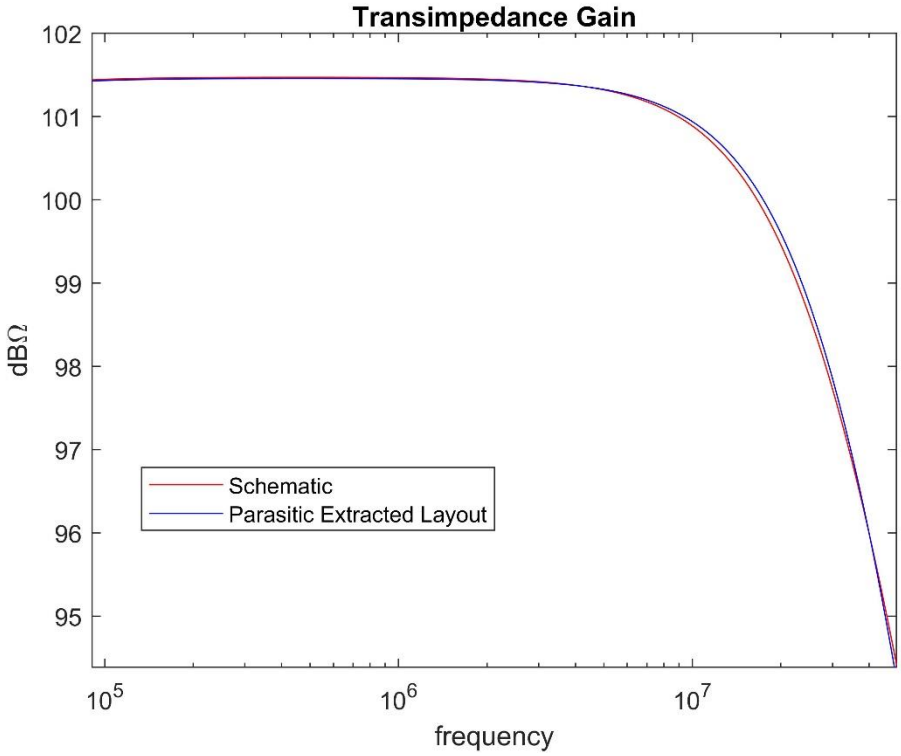

Figure 4.13: Transimpedance Gain Comparison

As can be seen from the Fig. 4.13, the transimpedance gain changes slightly compare to the schematic simulations.

4.3.2.2 Transient Simulations

Similar to the schematic transient simulation, an input of $3\mu A$ peak-to-peak sinusoidal input current at 7.5MHz is given to the designed MOSFET feedback transimpedance amplifier as input.

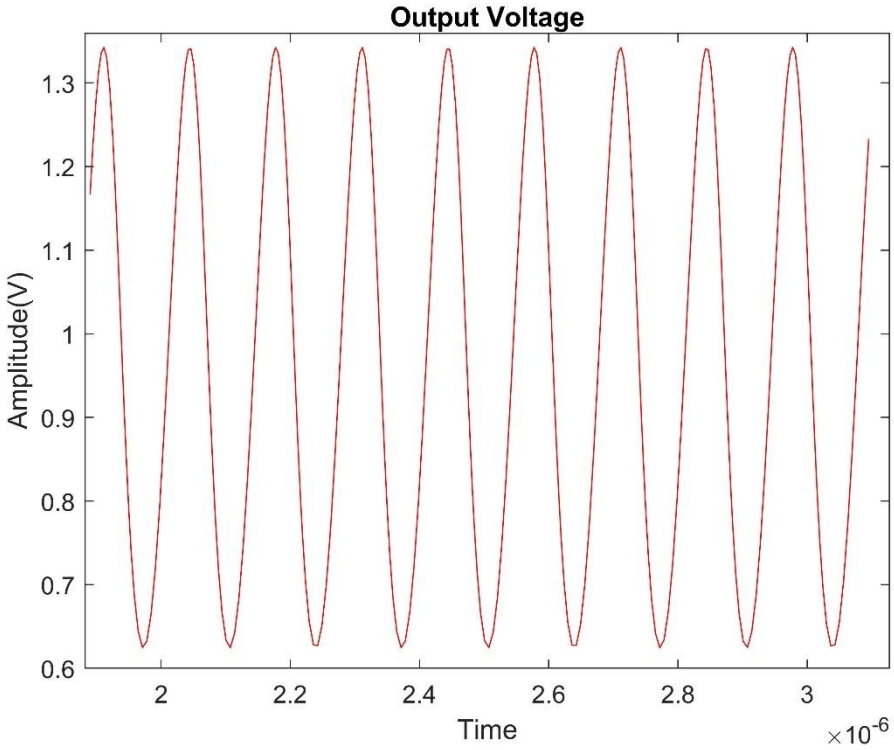

Figure 4.14: TIA output voltage to 3µA input current

The output yields a sinusoidal wave at 7.5MHz with $0.718V$ amplitude. If we calculate the transimpedance gain for this set of input and output, we find:

$$TIA_{gain} = 20log\left(\frac{0.718V}{6\mu A}\right) \tag{44}$$

$$TIA_{gain} = 101.5dB\Omega \tag{45}$$

For a more realistic input-output relation, $1.1nA$ peak input is fed to the MOSFET feedback TIA since short circuit current i_{sc} of the designed CMUT is calculated to be $1.1nA$.

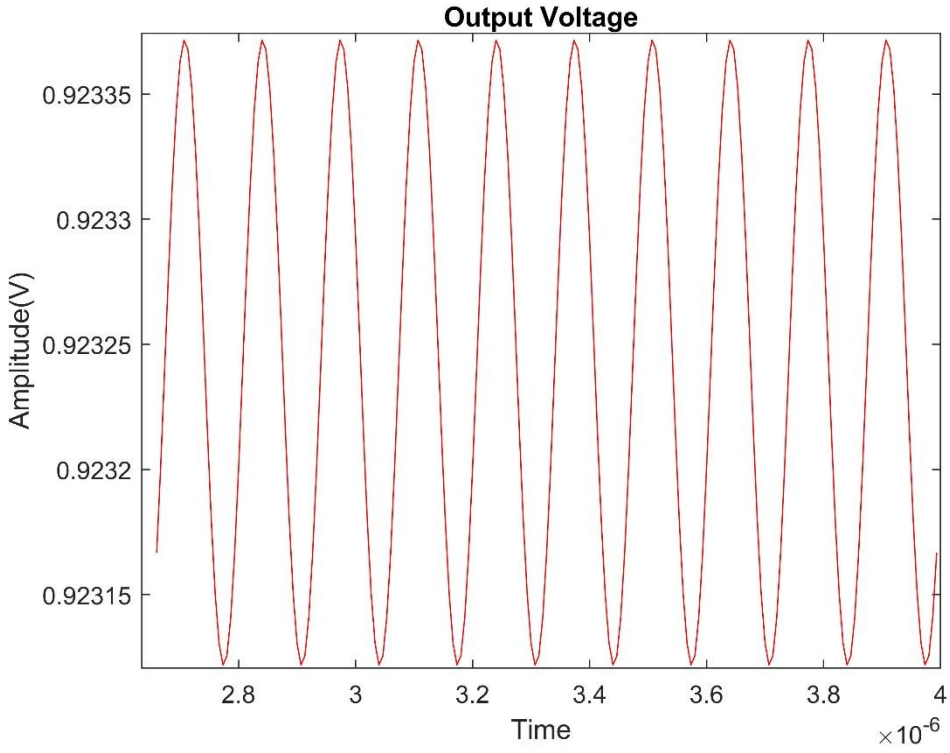

Figure 4.15: TIA output voltage to 1.1nA input current

The output yields a sinusoidal wave at 7.5MHz with $0.249mV$ amplitude. If we calculate the transimpedance gain for this set of input and output, we find:

$$TIA_{gain} = 20log\left(\frac{0.249mV}{2.2nA}\right) \tag{46}$$

$$TIA_{gain} = 101.1dB\Omega \tag{47}$$

4.3.2.3 Noise Simulations

In this section, post-layout noise simulations are conducted for input referred current noise and the output voltage noise spectral density of the MOSFET feedback transimpedance amplifier. Input referred current noise simulation is compared with the calculated and schematic simulated counterparts. The output voltage noise spectral density is compared with the schematic simulated version. Below are the related plots.

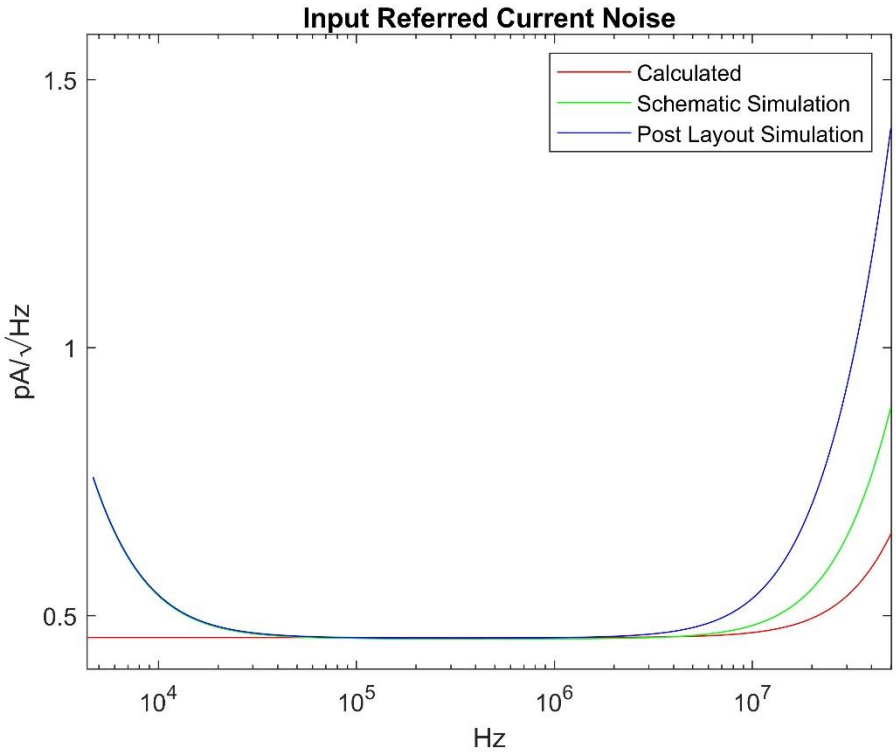

Figure 4.16: Input Referred Current Noise Comparison

At 7.5MHz, the input referred current noise is approximately $0.5pA/\sqrt{Hz}$ for post-layout, parasitic extracted MOSFET feedback transimpedance amplifier compare to $0.47pA/\sqrt{Hz}$ for schematic simulation and $0.46pA/\sqrt{Hz}$ for theoretical calculation.

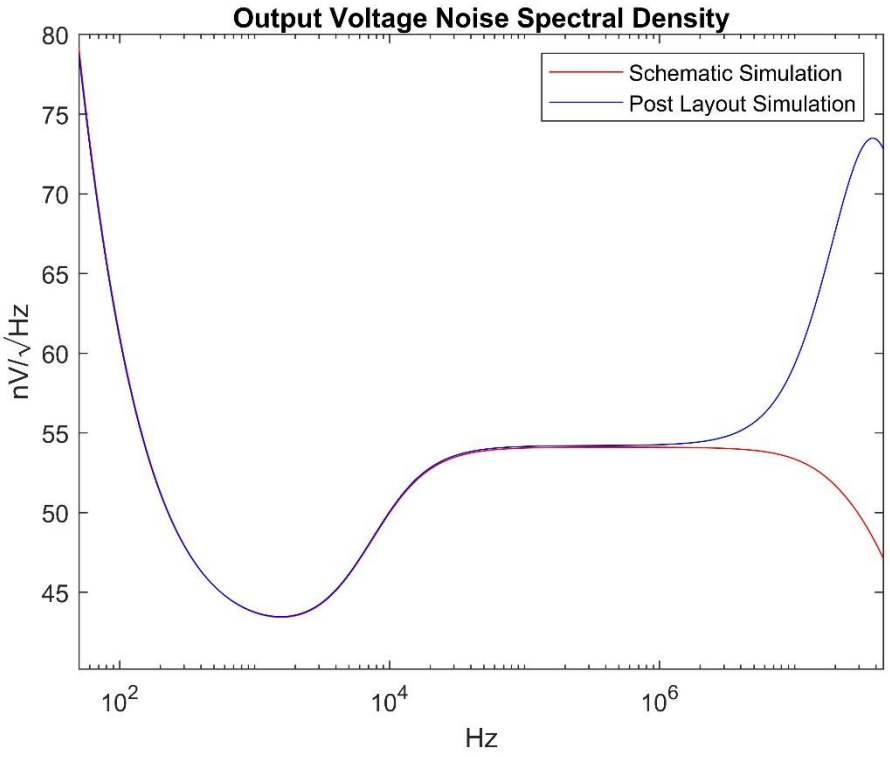

Figure 4.17: Output Voltage Noise Spectral Density Comparison

At 7.5MHz, the total output voltage noise density is approximately $57.3nV/\sqrt{Hz}$ for parasitic extracted MOSFET feedback transimpedance amplifier compare to $53.6nV/\sqrt{Hz}$ for schematic simulation.

Chapter 5

Conclusion

A transimpedance amplifier design is presented for $50\mu m$ radius, reception mode CMUTs operating at 7.5MHz. CMUT equivalent circuit model is presented and small signal model is utilized to incorporate the CMUTs electrical properties with the TIA design on the same SPICE program for coherent results. The CMUT capacitance C_{CMUT}, resistance R_{CMUT} and short circuit current i_{sc} for $1000Pa$ are calculated to be $0.18pF$, $223.46k\Omega$ and $1.1nA$, respectively.

A TIA design with $120k\Omega$ transimpedance gain and $25MHz$ bandwidth is presented. The design consists of 6 MOSFET transistors, a feedback resistance and a feedback capacitor, excluding power shutdown switch and output switch transistors. Fairly straightforward bias circuit for the TIA is presented as well to keep all the core amplifier transistors in saturated region. Related circuit and noise analysis carried out and TIA calculated input referred noise is found to be $0.46pA/\sqrt{Hz}$.

A voltage controlled MOSFET transistor feedback resistance version of the passive resistor feedback TIA is presented, with the goal of TIA covering less space in layout design and having a dynamic bandwidth. MOSFET and passive feedback resistor versions of the circuit have been passed through schematic simulations on Cadence Virtuoso, both yielding $120k\Omega$ transimpedance gain, $25MHz$ bandwidth and approximately $0.48pA/\sqrt{Hz}$ input referred current noise at $7.5MHz$. The passive resistor version of the TIA yielded $56.09nV/\sqrt{Hz}$ output voltage noise, compare to $53.6nV/\sqrt{Hz}$ of the MOSFET resistor version at $7.5MHz$.

After satisfying schematic simulations, layout design work is carried out on Cadence Virtuoso with XFAB XC06M3 process. Resistive feedback TIA size is measured to be $146.4\mu m$ by $108.8\mu m$ whereas MOSFET feedback TIA size is measured to be $91.5\mu m$ by $107.6\mu m$. Usage of a MOSFET transistor instead of a large passive resistor in layout design resulted in a 40% less layout space. Bias circuit layout size is measured to be $110.9\mu m$ by $84.7\mu m$.

After receiving zero DRC and LVS errors, Cadence Virtuoso's Quantus QRC Extraction Solution is used for parasitic extraction of both TIA designs and the bias circuit. Post-layout simulations incorporated the parasitic extracted versions of the circuits to thoroughly simulate the fabricated versions. Post-layout simulations are compared with schematic simulations and calculated counterparts.

At $7.5MHz$, resistive feedback TIA post-layout input referred noise is measured to be $0.5pA/\sqrt{Hz}$ compare to $0.48pA/\sqrt{Hz}$ schematic simulation and post-layout output voltage noise is measured to be $60.95nV/\sqrt{Hz}$ compare to $56.09nV/\sqrt{Hz}$ for schematic simulation. At $7.5MHz$, MOSFET feedback TIA post-layout input referred noise is measured to be $0.5pA/\sqrt{Hz}$ compare to $0.47pA/\sqrt{Hz}$ schematic simulation and post-layout output voltage noise is measured to be $57.3nV/\sqrt{Hz}$ compare to $53.6nV/\sqrt{Hz}$ for schematic simulation.

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