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DC and RF performance of lateral AlGaN/GaN FinFET with ultrathin gate dielectric

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Abstract

In this study, an enhancement-mode (E-mode) GaN high electron mobility transistor (HEMT) with lateral tri-gate structure field effect transistor (FinFET) is proposed. To passivate the fin width, while keeping the normally-off performance of the FinFET intact, an ultrathin aluminium-oxide/sapphire (Al_2O_3) gate dielectric is proposed (in a basic single-finger 0.125 mm device). Later, the DC and radio frequency (RF) performances of the proposed FinFET designs (with optimized fin width and Al_2O_3 thickness) are compared with that of conventional planar HEMT. DC and RF measurements are performed using power transistors in ten-fingers configuration, with a total gate periphery of 2.5 mm. The effect of Fin structure and Al_2O_3 thickness on the electrical performance of HEMTs, including threshold voltage (V_{th}) shift, transconductance (g_m) linearity, small-signal gain, cut off frequency (f_t), output power (P_{out}), and power-added efficiency (PAE) are investigated. Based on our findings, FinFET configuration imposes normally-off functionality with a $V_{th} = 0.2\ V$, while the planar architecture has a $V_{th} = -3.7\ V$. Originating from passivation property of the alumina layer, the FinFET design exhibits two orders of magnitude smaller drain and gate leakage currents compared to the planar case. Moreover, large signal RF measurements reveals an improved P_{out} density by over 50% compared to planar device, attributed to reduced thermal resistance in FinFETs stemming from additional lateral heat spreading of sidewall gates. Owing to its superior DC and RF performance, the proposed FinFET design with ultrathin gate dielectric could bear the potential of reliable operating for microwave power applications, by further scaling of the gate length.

Keywords: AlGaN/GaN Enhancement mode (E-mode), FinFET, gate dielectric, Al_2O_3 MOS, V_{th} shift, DC and RF performance

(Some figures may appear in colour only in the online journal)

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1. Introduction

In recent years, the demand for high-frequency/high-power operation in the wireless data communication and microwave technology market has highlighted the superiority of AlGaN/GaN high electron mobility transistors (HEMTs). Stemming from GaN's excellent material properties (compared to Si and GaAs), such as high bandgap, large thermal conductivity, high critical breakdown voltage, and high-power density, commercial GaN based devices have attracted intensive attention in consumer electronics, electric vehicles, and defense applications. Besides all these advantages, the performance limits of GaN have not been reached yet, and therefore, significant studies are still ongoing to optimize its operation. Essentially, the epitaxial growth for GaN HEMT transistors is performed in three main substrates, including SiC, Si, and sapphire, defined based on the requirements and applications [1–3]. Because of the polarization-induced charge formation at the GaN/AlGaN interface, traditional GaN-based HEMTs are inherently normally-on devices, or so called depletion-mode (D-mode) devices, with large two-dimensional electron gas (2DEG) density at zero gate bias. However, for the power electronic industry, especially for switching devices, enhancement-mode (E-mode) transistors are required for safe, simple and fail-free circuit operation conditions [4–6].

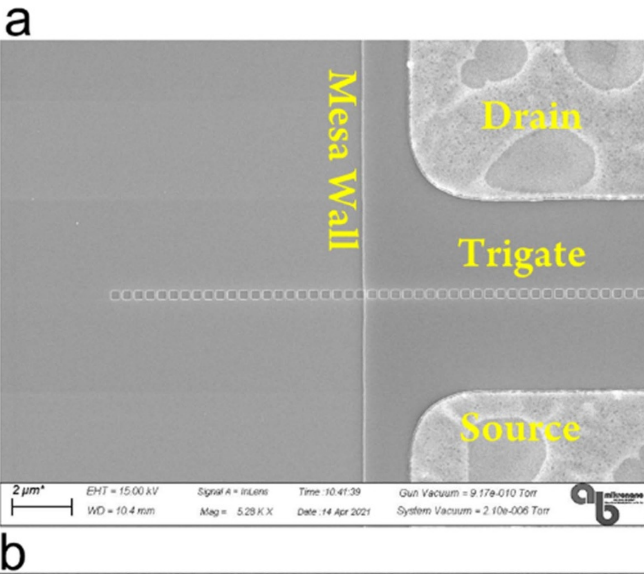
There are several approaches to achieve E-mode operations, including: (a) fluorine plasma treatment, (b) p-GaN gate, and (c) recess gate [7, 8]. However, all these methods have their own bottlenecks. In the plasma treatment approach, the negative F^- ions deplete electrons from the channel and shifts the threshold voltage towards positive values. This shift depends on the radio frequency (RF) power and exposure time to the plasma. Thus E-mode operations are obtained by charge storing, without reducing the channel conductance compare to other approaches [9–11]. However, the main drawback with this method is maintaining the V_{th} stable in the thermal steps during the fabrication process. This is caused by fluorine out-diffusion, upon exposing to high temperature cycles. Moreover, the fluorine plasma treated HEMT exhibits low drain current and small transconductance which is related to the impact of plasma on the carrier concentration, mobility, and sheet resistance (R_s) [12]. For p-GaN approach, the obtainable threshold voltages are relatively limited to small positive voltage values and the gate leakages are comparably larger [13]. Additionally, the V_{th} of p-GaN strongly depends on the doping concentration of p-GaN and the thickness of AlGaN. Hence, there is a trade-off between electron concentration and V_{th} [14]. Besides this, there are still reliability and trapping issues, as normally-off p-GaN HEMTs are often affected by gate leakage current, when the gate is stressed at forward voltage. Finally, in the gate recess method, the region beneath of the gate contact is etched by a plasma etch process. The depth of the recess etch can be used to control the gate threshold voltage. However, the plasma etching process damages the epitaxial layer crystallinity and generates a large density of the dangling bonds. The reduced AlGaN layer thickness, together with the formation of trapping states, significantly reduce the 2DEG density and DC performance of the device. Moreover, the nanometer scale uncertainty on the etching depth causes repeatability issues. It should be mentioned that these two techniques also increase the transistor On resistance (R_{ON}) [15]. Taking all into account, in an ideal platform, E-mode operation should be realized without sacrificing the device's DC and RF performance.

FinFET configuration could be a solution and in recent years, its usage started to dominate the GaN power device technology. FinFET has several advantages over the above-mentioned approaches like E-mode operation, small On resistance, less gate and drain leakage, more linear transconductance (g_m) and higher output power density [16–20]. In this design architecture, V_{th} could be shifted toward a positive direction by shrinking the channel lateral width. Owing to its three-dimensional (3D) configuration, both top and sidewalls simultaneously deplete the gate region and therefore, better controllability is achieved compare to the planar HEMT. Indeed, recent studies have successfully fabricated E-mode FinFETs with fin widths below 100 nm [21–24]. This method is also preferred in applications where both E- and D-mode devices are on the same chip, as this can be achieved by adding a few fabrication steps compared to other normally-off HEMT methods. Recent studies report the fact that FinFETs can improve the current density and linearity of the transconductance, which is an important factor for RF power amplifiers due to the large dynamic range in the highly variable modulation signals [25–31]. However, similar to gate recess method, in FinFET, the gate walls are formed using plasma etching process and this process generates large density of surface trap states. These trap states mediate the current conduction between the gate and buffer/barrier layers and consequently lead to high leakage currents. Moreover, the existence of interface trap states, in gate-barrier interface, significantly degrade the RF performance of the device. Passivation of these trap states could be achieved using a proper oxide and nitride based passivation layer. However, these dielectric layer can suppress the fringing effects in sidewalls and lack of lateral depletion mechanism could lead to loss of E-mode operation. Thus, a fine trade-off in the dielectric layer thickness is needed to acquire both E-mode functionality and passivation in the FinFET device configuration [32, 33].

In general, atomic layer deposition (ALD) is used to obtain high-quality and high-dielectric thin film because of the layer-by-layer nature of its deposition kinetics [34]. High-performance metal-oxide-semiconductor (MOS) diodes and MOS field effect transistors can also be realized by combining GaN with high-κ dielectric materials such as Ga_2O_3, HfO_2, ZrO_2, and Al_2O_3 instead of conventional low-κ SiO_2 as the gate dielectric [35–39]. Among these materials, sapphire is a very stable and robust material and also it has many favorable properties, including high-κ dielectric (∼9), high-bandgap (∼7 eV), high-breakdown electric-field (∼10^9 V m^{-1}), thermodynamic stability on the semiconductors up to high-temperatures [40].

In this study, a FinFET HEMT device, with ultrathin Al_2O_3 layer, is designed and fabricated. The proposed design shows E-mode operation with threshold voltage of $V_{th} = 0.2\,V$.

Besides its E-mode operation, the use of optimal alumina layer thickness (which is 3 nm in our case) provides excellent DC and RF characteristics, outweighing the planar design. For this aim, first, single-finger 0.125 mm gate HEMT devices were fabricated and the impact of fin width and Al_2O_3 thickness were investigated. The DC characterization are conducted to investigate the HEMTs DC characteristics, including V_{th} shift, drain current density, gate turn on and gate leakages. The pulsed I_d–V_d and I_d–V_g measurements are done to understand the passivation perform. Based on these findings, at the optimum alumina thickness of 3 nm, we have achieved normally-off operation with near two orders of magnitude smaller gate leakage currents. It was found that thicker gate dielectric does not significantly change the leakage current, while it diminishes the E-mode operation of the FinFET. Moreover, thinner dielectrics cannot effectively passivate the surface dangling bonds. In the second part of the manuscript, the optimized trigate AlGaN/GaN HEMTs were fabricated with 80 nm fin width and 3 nm Al_2O_3 thickness, in ten-fingers configuration, with a total gate periphery of 2.5 mm, drain-source distance of $L_{SD} = 5\ \mu$m, gate length of $L_G = 0.8\ \mu$m, and gate-source distance of $L_{SG} = 1.5\ \mu$m. DC and RF measurements are performed in these large-scale HEMT devices. According to our DC measurements, the FinFET design shows above two-fold enhancement in maximum drain current (I_d) and conductance (g_m), compared to that of D-mode planar HEMT reference. Moreover, similar to small scale device, the gate and drain leakages are reduced by above two orders of magnitude. Moreover, load-pull measurements are performed to scrutinize the RF performance of the device. The obtained characterization results prove a more stable operation of FinFET, under large RF signal condition. The P_{out} density is improved by 50% in FinFET HEMT.



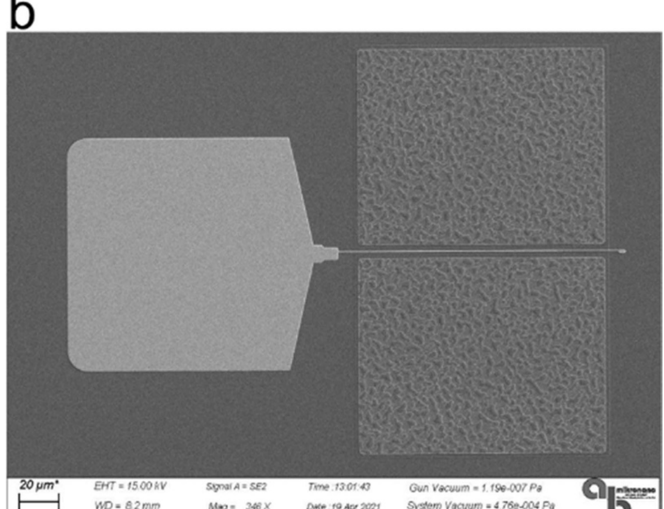


Figure 1. SEM images of (a) FinFET structure and (b) the single-gate HEMT device.

2. Experimental

2.1. Epitaxial structure

The AlGaN/GaN multilayer structure was grown by using metal organic chemical vapor deposition on a three-inch-diameter SiC substrate which includes 1.8 μm GaN Buffer, a 0.8 nm AlN spike layer, a 20 nm undoped AlGaN barrier layer with Al content of 25% capped with 3 nm GaN. The channel electron mobility (μ), sheet resistance (R_s), and the sheet carrier concentration (N_s) are measured as 1890 cm^2 (V s)$^{-1}$, 310 Ω sq^{-1}, and 1.06×10^{13} cm^{-2}, with the Lehighton contactless hall system, respectively.

2.2. Device fabrication

2.2.1. Single gate process. The fabrication of 0.125 mm HEMT starts with conventional Cl-based mesa isolation. The process continues with ohmic contact formation via deposition of a Ti/Al/Ni/Au multilayer metal stack. Before the ohmic annealing, e-beam alignment marks are defined as a negative etched marker. The etched mark is advantageous in the repeatability of electron beam (e-beam) lithography over annealed metal with a rough surface. After defining e-beam alignment marks, the ohmic contacts are annealed at 850 °C in an N_2 gas environment for 30 s. Later, TLM method is used to measure contact resistance values which was found to be 0.3 Ω mm. In the case of FinFET device, the Fin structure is patterned in various widths by 100 keV e-beam lithography. ZEP 520 A e-beam resist is used due to its both high etch selectivity and high resolution. After the Fin lithography is defined, 50 nm deep Fin etch is done with Cl_2 based plasma (see figure 1(a)). The Al_2O_3 thin films with different thicknesses of 1 nm, 3 nm and 5 nm were deposited by ALD. This Al_2O_3 thin film also is used for the surface passivation. As the reference, one sample is left with no Al_2O_3 gate dielectric. It means that there is no passivated access region for this sample. For this case only gate leakage is considered for a fair comparison. The gate is defined with copolymer/pmma bilayer by e-beam lithography again. Considering the S-band power transistor design, the thickness of gate metal and alignment accuracy, the gate footprint is optimized 0.8 μm which is the same as the multi-gate footprint. The 450 nm Ni/Au gate

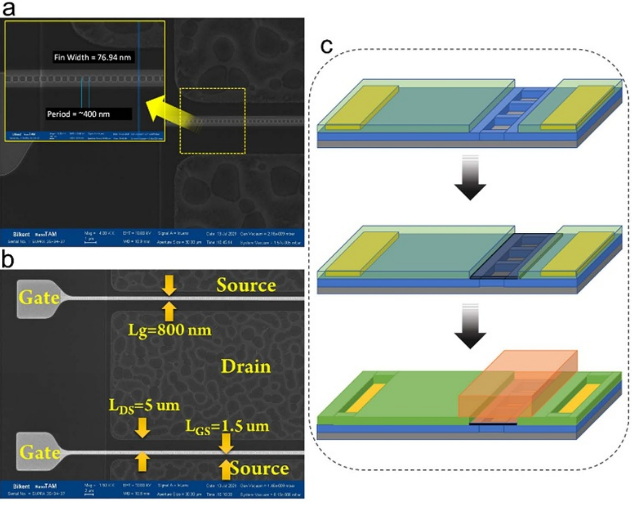
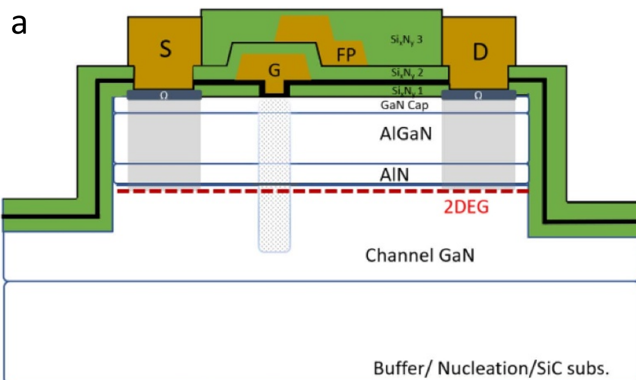


Figure 2. SEM images of (a) gate foot and Fin structures, and (b) fabricated multi-gate device with corresponding geometries. (c) 3D schematic of the fabrication route of FinFET including (i) Fin Etch, (ii) Al_2O_3 deposition, and (iii) gate metalization.



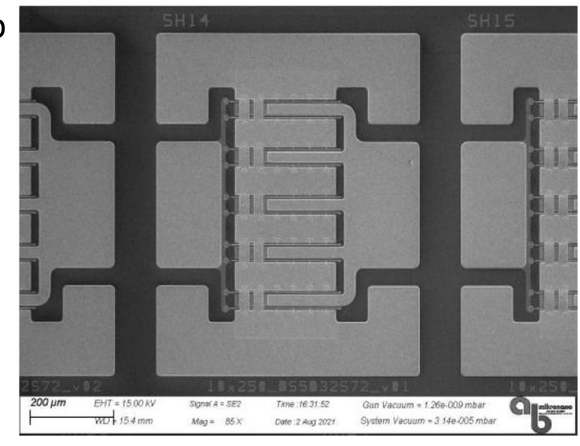


Figure 3. (a) The schematic illustration of device cross section, and (b) the SEM image of the final multi-gate HEMT device.

electrodes are patterned by the e-beam evaporation and lift-off technique. During the evaporation, samples are also rotated to avoid shadow effects. For the parametric study of trigate structure, the 250 nm designed trench area is fixed to have uniform coating of the metal in the tri-gate sidewalls, considering the nickel (Ni) and gold (Au) grain sizes. Fin width is changed from 60 to 250 nm. It should be noted that for all the e-beam lithography processes that are described, a conductive polymer was spin coated on top to avoid charging. The scanning electron microscopy (SEM) image of fabricated single-gate device is shown in figure 1(b). After successful fabrication of both FinFET and planar HEMTS, DC and pulsed measurements are carried out for all samples. The details will be provided in upcoming sections.

2.2.2. Multi-gate process. In the other part of the study, the conventional and tri-gate AlGaN/GaN HEMTs were fully fabricated with optimized geometries of 80 nm Fin width and approximately 3 nm Al_2O_3 gate dielectric. These HEMTs consisted of 250 μm ten-fingers transistors, drain-source distance of $L_{SD} = 5$ μm, gate length of $L_G = 0.8$ μm, gate-source distance of $L_{SG} = 1.5$ μm, $W_{fin} = 80$ nm and $W_{trench} = 320$ nm for 400 nm period, accumulating a total effective gate width of $W_{eff} = 500$ μm. (see figures 2(a) and (b)) For this multi-gate device, the same fabrication steps, as one followed in single-gate transistors, are applied until the end of the mesa step. After the mesa etching, the 75 nm 1st Si_3N_4 passivation is formed to passivate the access region and to create the foot width in the T-Gate structure. Before the deposition, surface-controlled wet treatment is applied with hot ammonia solution to remove the oxide layer formed on the epi surface. Typical F- based gases are used to completely etch the film, the Si_3N_4 layer has to be 30% over etched. One sample is continued after forming the gate foot with the optimized Fin width and Al_2O_3 thickness.

Ni (50 nm) /Au (400 nm) are deposition for the gate metal. The process flow is schematically illustrated in figure 2(c). Gate location, Fin, and trench width are checked with a SEM. The other one is the conventional planar HEMT which means there is no Fin and Al_2O_3 deposition.

A 210 nm 2nd Si_3N_4 layer is deposited between the gate and field-plate as passivation to suppress the formation of hot spot electric fields near the drain side of the gate and reduces gate-to-drain feedback capacitance. The first thick metal was formed by evaporation of Ti-Au. For protection, Si_3N_4 was deposited over the samples by plasma-enhanced chemical vapor deposition (PECVD). Fabrication is finished with an air bridge and a 4 μm thick metal deposition. A representative cross-sectional view of the device at the end fabrication is presented in figure 3(a). An SEM image of the fabricated device with a multi-gate periphery is shown in figure 3(b).

The focus of electron-beam lithography (EBL) is the main issue of the reliable and repeatable fabrication of sub100 nm periodic Fin pattern on the large size device. As is known, SiC samples are transparent semiconductors. that is, the focusing process of samples like this is quite challenging for systems that make height maps with laser. The issue can be ignored with no height, blind job, or reflective layer but all these techniques cause a resolution and focusing issue. In this process to expose the sub-100 multi-structure, the negative 20 μm square EBL markers are used for focusing. With this method, we

succeed the same resolution and Fin size for all gate fingers on the 10 × 250 μm FinFET and also from sample to sample. Pattering is done with 100 keV acceleration voltage to minimize the proximity effect.

3. Result and discussion

In the first step of the characterization part, DC measurements were performed for the single-finger HEMTs. The main purpose of this step is to analyze the impact of fin width and alumina thickness in device normally-off operation and gate leakage. Later, the optimal geometries are utilized to demonstrate multi-finger large-scale designs. For these devices, both DC and RF performances are evaluated. The upcoming section summarizes our findings. To understand the FinFET's performance, the effect of device geometry should be analyzed. For a fair comparison among devices, all device performance has to be normalized.

There are two factors that affect the electron concentration of the device, one is fin width (W_{fin}) and the other one is depletion of the electron because of the sidewall gate (W_{dep}). The real channel width is W_{fin}—$2W_{\mathrm{dep}}$ where W_{dep} is fixed and is formed by the Schottky gate metal or gate-insulator-semiconductor. Devices have trenches on the active area and there is no electron concentration at the near sidewall [20, 41].

Tri-gate lateral GaN HEMT performance is independent of the Fin height (H_{fin}) which is ignored because does not affect the sheet density. H_{fin} is important for a Silicon on Insulator FinFET device [42].

In the literature, the widely accepted normalization method for laterally GaN HEMTs is to calculate the effective channel width (W_{eff}) with total electron concentration which only change with the total active region. Therefore,

$$W_{\mathrm{eff}} = W_{\mathrm{fin}} \times n,$$
$$W_{\mathrm{channel}} = (W_{\mathrm{fin}} + W_{\mathrm{trench}}) \times n,$$

n is number of Fin. And filling factor (FF) is given by $W_{\mathrm{fin}}/(W_{\mathrm{fin}} + W_{\mathrm{trench}})$.

Based on this, W_{eff} is also calculated as (total L_g) × FF [43–47].

All measured values are normalized by effective gate width.

3.1. DC performance of single gate devices

As already stated above, the samples in the first set of experiments were evaluated for V_{th} shift and leakage current performance. For the FinFET design, the Fin width was spanned from 60 to 250 nm. Additionally, the Al_2O_3 thickness was chosen to be 1, 3 and 5 nm. Initially, the Fin width is fixed at 80 nm and three different Al_2O_3 gate dielectrics are fabricated and compared with the reference planar design. Table 1 summarizes the threshold voltage for all the studied cases. In the conventional planar HEMTs, the threshold voltage is negatively shifted from −3.48 to −4.11 V, as we move from bare device (with no gate dielectric) to 5 nm-thick alumina dielectric gate structure. These values are significantly shifted toward positive values, in the FinFET design, mainly due to sidewall-gate depletion effect. Among all four cases, the first three samples (annotated as sample 1, sample 2 and sample 3) shows E-mode operation, while the last sample (i.e. sample 4) has D-mode functionality with a threshold voltage of −0.55 V. As expected, as the gate dielectric gets thicker, the fringing effects from the sidewalls lose their impact and full depletion cannot be acquired. In this sense, a thinner alumina layer is preferred. However, another factor that should be considered is the passivation property of such an ultrathin dielectric layer. To verify this, I_g–V_g characteristics of FinFET designs with and without gate dielectrics are studied, as depicted in figure 4(a). As it can be clearly seen from this panel, 1 nm thick layer has similar gate leakage response with the unpassivated design. According to the leakage and lag measurements, 1 nm thick layer cannot effectively passivate the dangling bonds, formed on the surface. However, 3 nm thick gate dielectric has unprecedentedly mitigated the gate leakage by above two orders of magnitude (at a gate bias of −5 V). Further increase in the dielectric thickness has not pronounced impact in the gate leakage suppression. Therefore, a fine trade-off between normally-off operation and gate passivation is achieved using 3 nm ultrathin Al_2O_3 gate dielectric.

Further positive shift in V_{th}can be accomplished by reducing the fin width. As the width shrinks, the sidewall depletion becomes more dominant and therefore more positive bias is required to build up the 2DEG density [48]. This can be seen in the normalized I_d–V_g graph of FinFET designs with widths ranging from 250 nm to 60 nm, as shown in figure 4(b). It should be mentioned that all these results are obtained with 3 nm Al_2O_3 gate dielectric. As plotted in the inset, for fin widths below 100 nm the E-mode operation is realized. Although narrowing the fin structure can positively shift the V_{th}, from the fabrication perspective, the dimension below 80 nm had repeatability and reliability issues. That is why, we chose 80 nm fin width as the optimal geometry.

As the drain current density, FinFET structures are 54% to 95% higher than planar structures at $V_g = +2$ V. Performance on some Fin widths differed from theoretical expectations due to deviation in fabrication such as drain-source distance, the position of gate and gate width variation or mismatch between the fin and footprint.

The double pulsed I_d–V_d measurements are done to analyze drain and gate lag to see dynamic R_{on} change, and the results are shown in figure 5. *I*–*V* measurements are performed by sweeping the pulsed drain voltage from 0 to 10 V under three quiescent points in order: Q(0 V, 0 V), Q(−6 V, 0 V), and Q(−6 V, 10 V). The gate and drain lag values are 51% and 86%, respectively, for the unpassivated sample. It is seen that dynamic Ron is increased dramatically in the stress condition of Q(−6 V, 10 V). The Lag performance of 1 nm Al_2O_3 is between the unpassivated sample and 3 or 5 nm Al_2O_3 samples which ensure that the GaN surface is not effectively passivated [26].

Moreover, the threshold voltage stability test is performed under the same quiescent voltage values sweeping the gate voltage from −8 V to +2 V while the drain voltage is +10 V. The results are shown in figure 6. While the reference sample

Table 1. V_{th} of the single gate device.

	Sample 1	Sample 2	Sample 3	Sample 4
Type of device	Bare	1 nm Al_2O_3	3 nm Al_2O_3	5 nm Al_2O_3
Planar HEMT	−3.48 V	−3.66 V	−3.82 V	−4.11 V
80 nm FinFET	0.56 V	0.46 V	0.20 V	−0.55 V

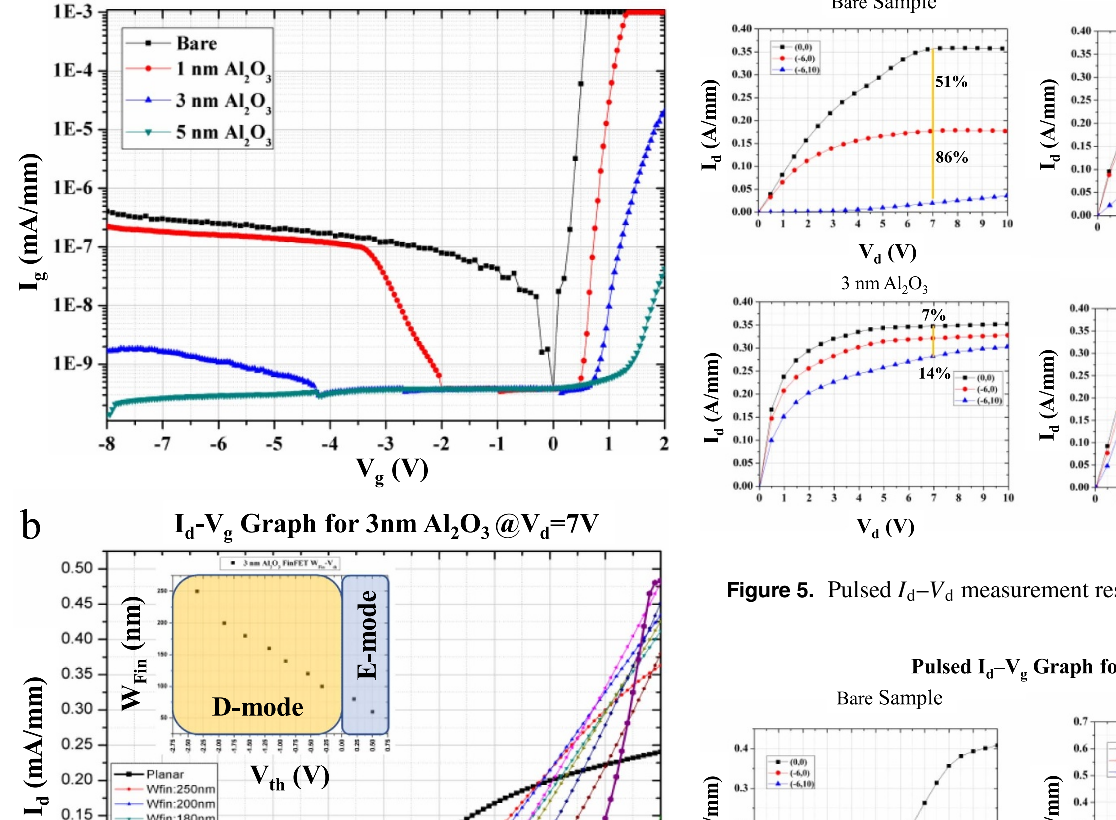


Figure 4. (a) I_g–V_g graph for Set1 samples, and (b) I_d–V_g graph for 3 nm Al_2O_3 sample which is number 3.

Figure 5. Pulsed I_d–V_d measurement results for Set1 samples.

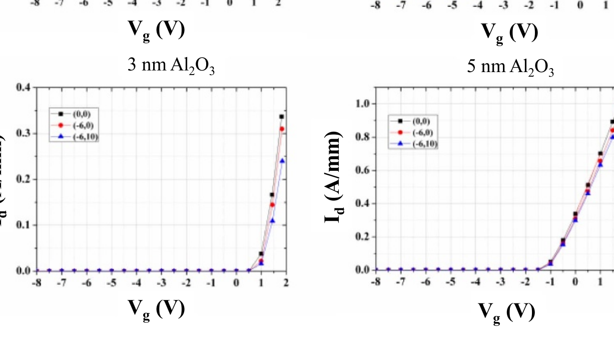


Figure 6. Pulsed I_d–V_d measurement results for Set1 samples.

showed the biggest V_{th} shift (more than 0.6 V) performance, 3 and 5 nm Al_2O_3 gate dielectric samples performed very stable V_{th}. The 1 nm Al_2O_3 sample's I_d–V_g behavior looks like a bare sample.

3.2. DC and RF performance of ten-fingers devices

After optimization of device performance in a single-gate configuration, the next step, the design is scaled up to ten-fingers multi-gate transistor, with a total gate periphery of 2.5 mm. In this set, again a reference planar HEMT is compared with the optimal FinFET structure with a fin width of 80 nm and alumina thickness of 3 nm. Figure 7(a) shows I_d–V_d characteristics of these two under different gate bias voltages between −8 V to +3 V. The FinFET design demonstrates a maximum drain current of 1.43 A mm^{-1} at 10 V drain and +3 V gate bias, while that for planar HEMT is found to be 0.74 A mm^{-1}. This means FinFET current density 95%

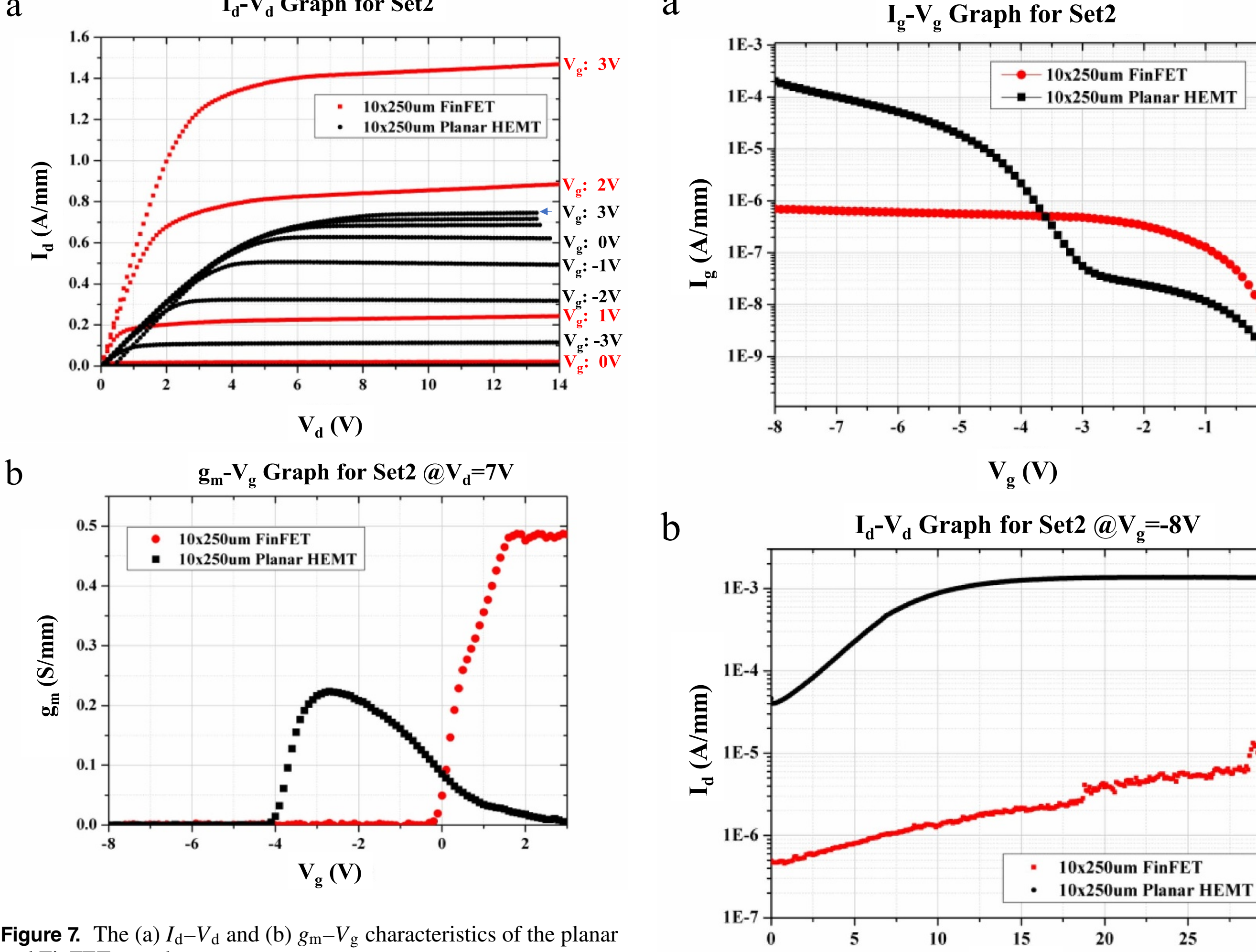


Figure 7. The (a) I_d–V_d and (b) g_m–V_g characteristics of the planar and FinFET samples.

Figure 8. The (a) I_g–V_g graph and (b) drain leakage current for gate bias of -8 V in both planar and FinFET configurations.

higher than planar device. It is worth noting that, to completely eliminate 2DEG in the multi mesa region, total gate width normalization is done for the FinFETs.

Additionally, the G_m–V_{gs} characteristics of these samples at $V_d = 10$ V have been extracted, illustrated in figure 7(b). The FinFET sample gives a maximum g_m of ∼490 mS mm^{-1}, while this value for reference planar design is found to be 230 mS mm^{-1}. Also, the linearity improvement has been achieved in the FinFET configuration. Compare to planar HEMT bell-shaped transconductance, FinFET's linearity refers to reducing the source resistance in the linear region and linear source and drain resistances. In the planar device, source resistance is increased with increasing the drain current [49–51]. As these graphs imply, the FinFET architecture has almost two-fold larger maximum drain current and conductance, in comparison with planar HEMT reference design. This remarkable improvement could be attributed to reduced thermal resistance in FinFETs stemming from additional lateral heat spreading of sidewall gates. The FinFET device also offers better electrostatic control of the gate. Moreover, the passivation property of the alumina layer reduces the density of trap states in vicinity of the 2DEG channel.

Another important factor, defining the overall performance of the transistor is its gate and drain leakages. As we can see from figure 8(a), the gate leakage in bias values below -4 V are significantly lower than that of planar design. The higher leakage values in lower voltage values could be attributed to lower Schottky barrier formed between gate and GaN, compared to the one formed between gate and AlGaN. Moreover, the drain leakage has been also significantly suppressed in the FinFET configuration, owing to a better gate control in this configuration, see figure 8(b).

After completing the DC measurements, RF and large-signal measurements were done on the wafer to see and compare the performance of the devices. Small-signal measurements are performed for Set2 samples, with a drain voltage of 45 V and 40 mA drain current. Maximum available gain (MAG) is measured as 15.8 and 19.3 dB at 3 GHz for the FinFET and planar devices and, respectively, shown in figure 9(a). The cut-off frequency of the devices is also calculated from S-parameters. For the same bias conditions, the planar-gate (f_t: 8 GHz) transistor over-performed FinFET devices (f_t: 3.5 GHz), as seen in figure 9(b). This performance can be explained by the higher parasitic capacitance of FinFET coming from the trench region and sidewall gates [52].

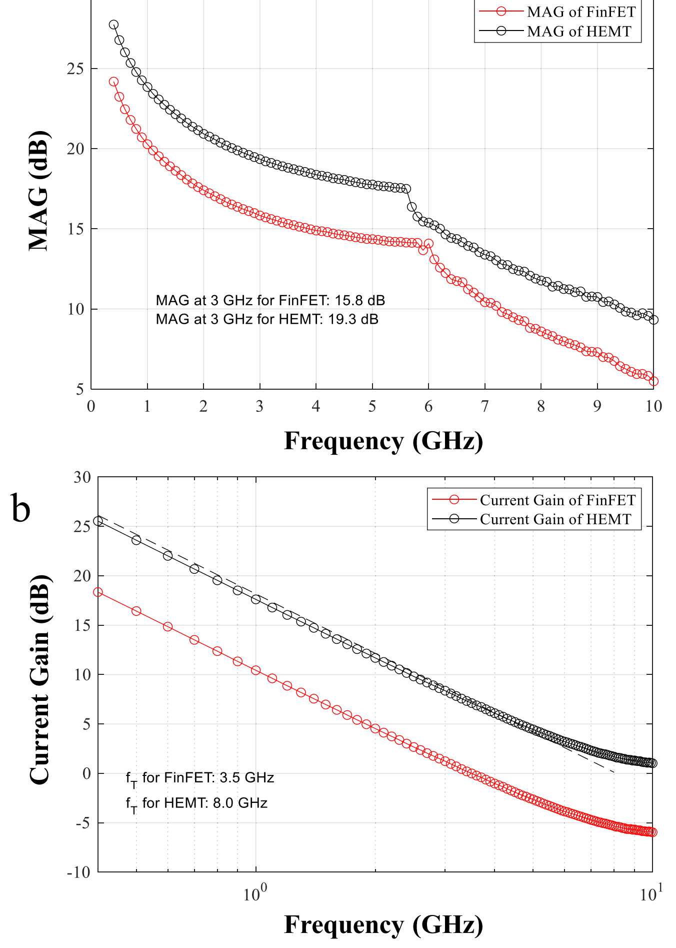


Figure 9. MAG and f_t characteristics of FinFET and planar HEMT.

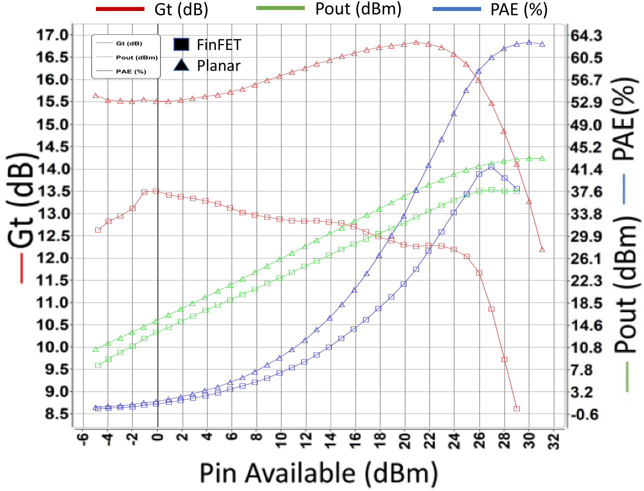


Figure 10. Power characteristics of FinFET and planar HEMT.

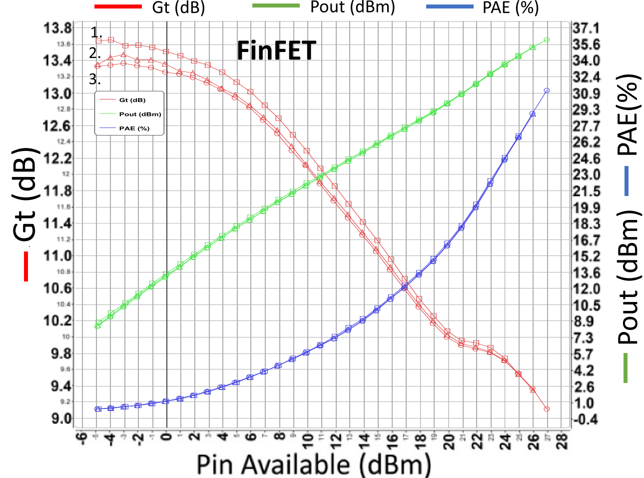


Figure 11. Three power sweep measurements for the sample with FinFET.

For the large-signal measurements, Class AB operation is selected for samples with a bias voltage of V_{ds}: 45 V and quiescent I_{DQ}: 16 mA mm^{-1} with 15% duty cycle at 3.1 GHz at room temperatures. The gain, P_{out}, and power-added efficiency results are given in figure 10 which presents the results for FinFET (square) and planar (triangle). Planar HEMT shows a small-signal gain of 15.5 dB, while HEMT with Fin has a gain of 10.8 dB. On the other hand, HEMT with Fin gives a saturated P_{out} of 37.85 dBm (6.1 W), while the planar sample gives a saturated P_{out} of 43.05 dBm (20.2 W) at 3.0 dB gain compression. Considering the total effective gate width as a $W_{fin} = 80$ nm and $W_{trench} = 320$ nm for 400 nm period, accumulating a total effective gate width of $W_{eff} = 500\ \mu$m, FinFET has a 12.2 W mm^{-1} output power density, and planar is almost 8 W mm^{-1}. FinFET results in 4.2 W mm^{-1} of more output power density. These measurements yield an increase in P_{out} performance at FinFET at the same level of gain compression compared to the planar device.

The threshold voltage stability is important for devices when it comes to high power applications, as the performance of the transistor should be stable with high input power levels. To see this performance, three power sweep measurements are taken back-to-back for both devices. The forward gate currents are observed during the measurements. For FinFET, the small-signal gain performance is stable after giving 27 dBm input power to the transistor, as no gain degradation is seen for the second and third measurements (figure 11). The gate current increases up to 70 mA (140 mA mm^{-1}) during this measurement, while the transistor is not saturated yet. For the planar device, after the first and second power sweep measurements up to 31 dBm, small-signal gain degraded by 0.8 dB and 0.5 dB. With 31 dBm input power, the forward gate current of planar HEMT increases to 17 mA (6.8 mA/mm). The degradation of the small-signal gain is due to the shift in V_{th} with high power levels, which is not desired in high power applications, as transistors need to endure very high input power levels. (figure 12).

Many papers have been reported on the GaN FinFET technology since 2009. A general review and perspective of Gan FinFETs were reported bu Zhang *et al* [18]. Lateral AlGaN/GaN power FinFET transistors are focused on the benchmark.

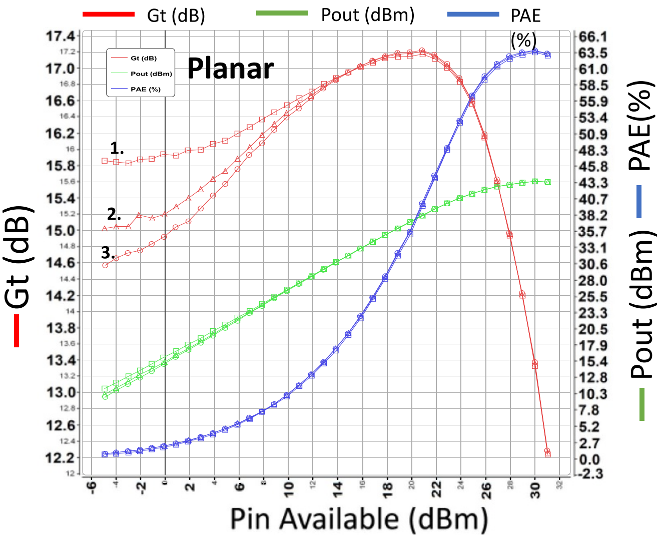


Figure 12. Three power sweep measurements for the sample with Planar HEMT.

Table 2. Comparison of Laterally AlGaN/GaN FinFETs.

Reference	Year	Mode	Device size (um)	DC performance	RF performance
[45]	2015	D	2 × 50	I_{ds}: 2200 mA mm^{-1} (+%69) G_m: 750 mS mm^{-1} (+%66) I_g: <10^{-6} A mm^{-1}	Pout: NR
[17]	2017	D	2 × 125	I_{ds}: 1640 mA mm^{-1} (+%145) G_m: NR I_g: <10^{-4} A mm^{-1}	Pout: 11.3 W mm^{-1} (+%66) @8 GHz
[53]	2019	E	25	I_{ds}: 896 mA mm^{-1} (−%48) G_m<200 mS mm^{-1} (−%10) I_g: <10^{-6} A mm^{-1}	Pout: NR
[54]	2022	E	50	I_{ds}: 1121 mA mm^{-1} (+%109) G_m: 185 mS mm^{-1} (+%125) I_g: <10^{-6} A mm^{-1}	Pout: NR
This Work	2022	E	10 × 250	I_{ds}: 1430 mA mm^{-1} (+%93) G_m: 490 mS mm^{-1} (+%115) I_g: <10^{-6} A mm^{-1}	Pout: 12.2 W mm^{-1} (+%52) @3.1 GHz

NR, not reported.

Table 2 summarizes the E/D mode, size and electrical characterization of AlGaN/GaN FinFETs. The DC and RF performance of the device is affected by the Fin structure and fabrication, as well as the %Al and thickness of AlGaN, drain-source length, gate type and footprint. Therefore, the comparison with the planar device and FinFET is more important for the same process. The difference with the planar device is also shown.

From the comparison, the largest E mode transistor was fabricated in the literature. As a result of the power performance and three-point reliability measurements of the device operating at the AB class S-band, promising results were obtained for power applications. By further reducing trench size, more power can be obtained in the same size device.

4. Conclusion

In this paper, the influences of the fin width and ultrathin Al_2O_3 gate dielectric on the DC and RF characteristics of FinFET and planar AlGaN/GaN HEMTs have been

investigated. Considerable threshold voltage shift was achieved with decreasing the channel width, moving the threshold voltage from −3.7 V (for planar design) to 0.2 V (for FinFET design). It was found that in a 2.5 mm device periphery, 80 nm Fin width, and 3 nm gate dielectric thickness, a reliable E-mode operation can be achieved in FinFET design. The optimized has superior DC performance with near two times larger drain current and conductance values. The obtained value of leakage current density is two orders lower than the conventional HEMTs for the gate voltage of −8 V and the drain voltage of 30 V. FinFET with these optimized geometries reveals 4.2 W mm^{-1} more P_{out} performance at the same level of gain compression compare to a planar device. The large signal measurements of the devices confirm that FinFET has an increase of P_{out} density by over 50% compared to planar device. As a gain degradation, FinFET shows perfect stable performance, compared to that of planar HEMT. With this advantage, FinFET could be seen at commercial device levels in high power applications in the coming years.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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