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Graphene Nanoplatelets Embedded in HfO_2 for MOS Memory

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In this work, a MOS memory with graphene nanoplatelets charge trapping layer and a double layer high-κ Al_2O_3/HfO_2 tunnel oxide is demonstrated. Using C-V_{gate} measurements, the memory showed a large memory window at low program/erase voltages. The analysis of the C-V characteristics shows that electrons are being stored in the graphene-nanoplatelets during the program operation. In addition, the retention characteristic of the memory is studied by plotting the hysteresis measurement vs. time. The measured excellent retention characteristic (28.8% charge loss in 10 years) is due to the large electron affinity of the graphene. The analysis of the plot of the energy band diagram of the MOS structure further proves its good retention characteristic. Finally, the results show that such graphene nanoplatelets are promising in future low-power non-volatile memory devices.

Introduction

Recently, two-dimensional graphene has attracted great efforts and research due to its unique characteristics such as large work-function, high carrier mobility, thermal conductivity, and optical transparency (1-3). These outstanding properties enabled promising graphene-based electronics, filtration, photovoltaics and energy storage devices (4-7). However, the use of graphene in non-volatile memory devices hasn't been studied extensively. In this work, the effect of using Quattro-layer graphene-nanoplatelets as a charge trapping layer in non-volatile MOS memory devices with double layer Al_2O_3/HfO_2 tunnel oxide is investigated. The memory performance is studied by conducting high frequency C-V measurements, charge retention measurement, and analysis of the energy band diagram of the memory structure.

Experimental

The fabrication of the memory cells is conducted as follows: first a 4-nm-thick tunnel oxide Al_2O_3 is deposited at 250°C in Cambridge Nanotech Savannah-100 atomic layer deposition (ALD) system on an n+-type (111) (Antimony doped, 15-20 mΩ-cm) Si wafer. Next, 1-nm-thick HfO_2 is deposited by Plasma Assisted ALD at 195°C in an Oxford FlexAL system. Then, the sample is placed on a hot plate at 110°C and 2-2.5 ml of

graphene nanoplatelets solution with 0.05 mg/ml concentration are drop casted slowly using pipettes. A 1-nm-thick HfO_2 is again deposited by plasma assisted ALD at 195°C followed by an 8-nm-thick Al_2O_3 blocking oxide deposited by ALD at 250°C. Finally, the gate contacts are created by e-beam evaporating a 400-nm-thick Al layer using a shadow mask with 10 µm feature size. An illustrative cross-section of the fabricated memory is shown in Figure 1.

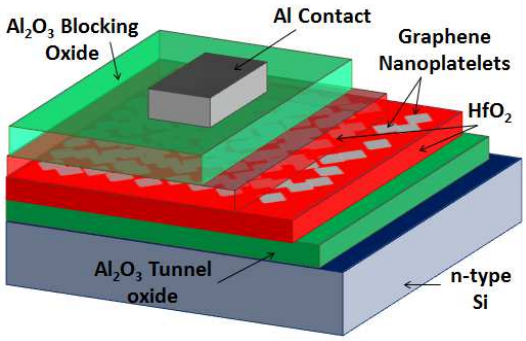

Figure 1: Schematic cross-section of the fabricated charge trapping memory cell with graphene nanoplatelets.

In order to analyze the effect of embedding graphene nanoplatelets in the MOS memory and to quantify the stored charge at different gate voltages, high frequency (1 MHz) C-Vgate measurements are conducted using an Agilent B1505A Semiconductor Device Parameter Analyzer to measure the programmed and erased C-V characteristics of the fabricated memory devices as depicted in Figure 2. The memory cells showed a 1.35 V threshold voltage (V_t) shift upon sweeping the gate voltage from -5 V forward to 5 V then backwards. At -7/7 V gate sweeping voltage, more charging is observed through the higher 3 V V_t shift as shown in Figure 3. The results show that the memory is being programmed by storing electrons in the graphene nanoplatelets as shown by the shift of the programmed state in the positive direction at higher gate sweeping voltages (8-10). The observed pure electrons storage is expected to increase the program/erase operations speeds with respect to memory devices where both electrons and holes are stored due to the larger mass of holes and larger valence band offsets.

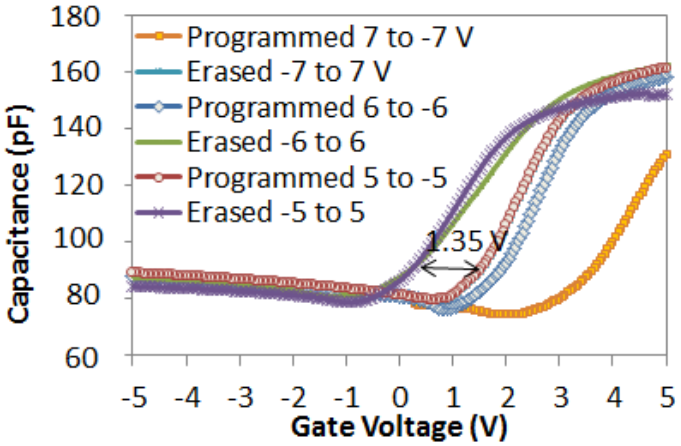

Figure 2: Measured hysteresis behavior using the C-V_{gate} characteristic showing a 3 V V_t shift at 7/-7 V gate sweeping voltage.

At 7/-7 V gate sweeping voltage and with a measured 3 V V_t shift, the charge trapping density in the graphene nanoplatelets is calculated (11-13) and found to be 1.54 $\times 10^{13}$ cm^{-3}.

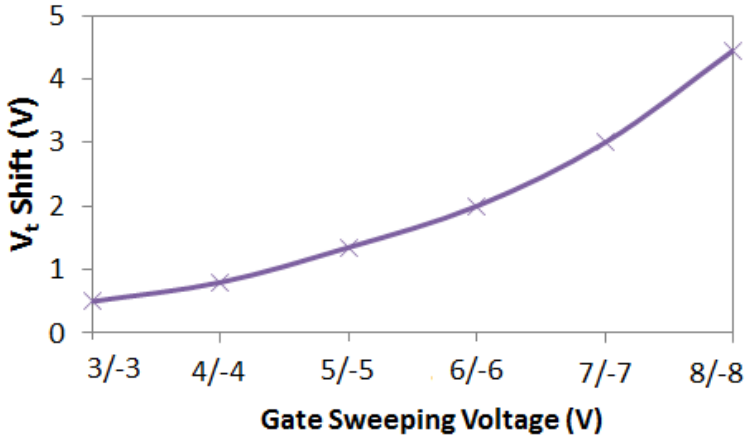

Figure 3: Measured threshold voltage shift using the *C-V*$_{gate}$ characteristic at different gate sweeping voltage.

Using the reported material properties of Al_2O_3, HfO_2, and graphene, the energy band diagram of the memory is constructed as shown in Figure 4 (14-31). The conduction band offset between Si and tunnel oxide is smaller than the valence band offset (ΔE_C = 2.44 eV < ΔE_V = 3.24 eV), thus the electrons tunneling probability is expected to be much higher than holes tunneling probability which confirms the observed electrons storage. In addition, due to the large work-function of graphene, a deep quantum well is formed where electrons can be stored. In fact, the conduction band offset between charge trapping layer and tunnel oxide is very large (ΔE_C = 2.99 eV) which exponentially reduces the leakage of stored electrons in the graphene nanoplatelets as expressed in Einstein's quantum tunneling equation (11-12). Moreover, the addition of the high-dielectric constant (κ=20) HfO_2 layer is expected to further reduce the leakage of stored charges.

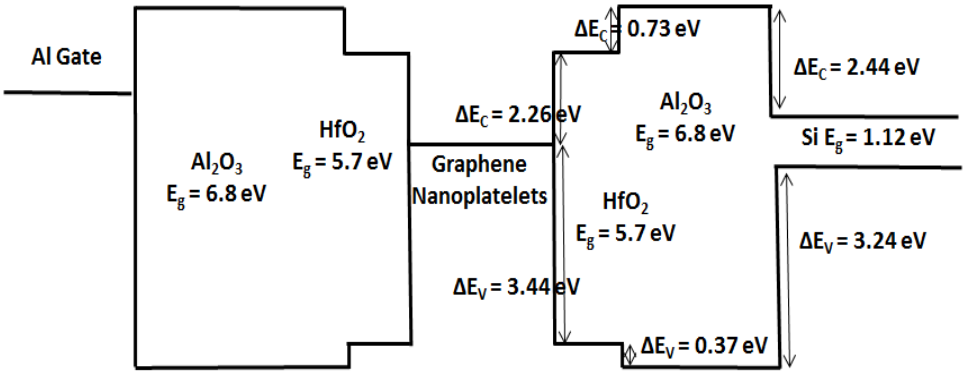

Figure 4: Energy band diagram of the fabricated MOS memory with graphene nanoplatelets.

Furthermore, the retention of the memory cells is characterized by first programming/erasing the memory at 8/-8 V and observing the change in V_t shift in time as shown in Figure 5. The figure shows that 28.8% of the initial charge is lost in 10 years and a memory hysteresis of ~3.3 V is shown at 10 years. This good retention

characteristic with graphene nanoplatelets is due to the large electron affinity of graphene (4.6 eV) which increases the conduction band offset between charge-storage layer and tunnel oxide, and therefore exponentially reduces the back tunneling of electrons.

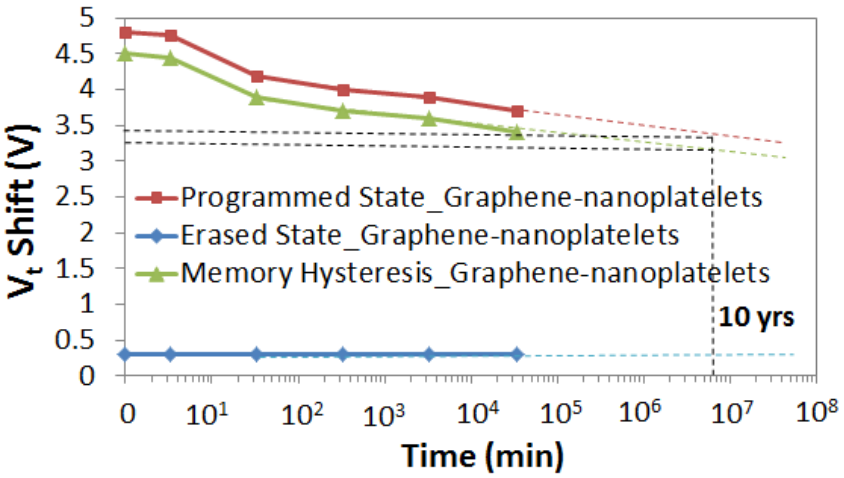

Figure 5: Retention characteristic of the MOS memory with graphene nanoplatelets

Conclusion

In conclusion, a MOS memory device with graphene nanoplatelets and double layer Al_2O_3/HfO_2 tunnel oxide is demonstrated. The results show that graphene nanoplatelets provide a large memory window at low operating voltages in addition to an excellent retention characteristic which is due to the large conduction band offset between charge storage layer and Al_2O_3. The results highlight that such memory structures have potential in next-generation low power non-volatile-memory devices.

Acknowledgments

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