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A Wired-AND Current-Mode Logic Circuit Technique in CMOS for Low-Voltage, High-Speed and Mixed-Signal VLSIC

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Abstract. A wired-AND current-mode logic (WCML) circuit technique in CMOS technology for low-voltage and high-speed VLSI circuits is proposed, and a WCML cell library is developed using standard 0.8 micron CMOS process. The proposed WCML technique applies the analog circuit design methodologies to the digital circuit design. The input and output logic signals are represented by current quantities. The supply current of the logic circuit is adjustable for the required logic speed and the switching noise level. The noise is reduced on the power supply lines and in the substrate by the current-steering technique and by the smooth swing of the reduced node potentials. Precise analog circuits and fast digital circuits can be integrated on the same silicon substrate by using the low noise property of the WCML. It is shown by the simulations that at low supply voltages, the WCML is faster and generates less switching noise when compared to the static-CMOS logic. At high speeds, the power dissipation of the WCML is less than that of the static-CMOS logic.

Key Words: Analog logic, current-mode, wired-logic, low-voltage, high-speed, low-power, mixed-signal.

1. Introduction

When both digital and analog circuits are integrated on a single chip, the switching noise of the digital part degrades the precision of the analog part by the noise coupling through the substrate and the power supply rails [1]. Although the layout design methods can reduce the effects of the digital switching noise, they are not sufficient for high-precision analog applications, and they require additional I/O pins and silicon area which increase the chip cost [2], [3].

As the CMOS IC technology scaled down to submicron range, the interconnection line parasitics became the major source of logic circuit delays. In an IC, the capacitive parasitics are more effective than the resistive and inductive parasitics on the line delay. The effect of the capacitive parasitics can be reduced by using a low impedance load, which motivates both the digital and the analog IC designers to develop the current-mode circuits [4], [5], [6].

Power dissipation of the circuits should be reduced for the VLSI, the device reliability, and the battery life in the portable equipment. As the supply voltage is decreased, the power dissipation reduces, however the low-voltage degrades the speed of the logic circuits.

A Wired-and Current-Mode Logic (WCML) circuit technique, proposed in this paper, reduces the digital switching noise and provides high speed at low supply voltage by combining the current-steering [7], [4], and the wired logic [8] properties. The WCML circuit resembles the Merged-Transistor Logic [9], Integrated Injection Logic [10], the voltage-mode Current-Steering Logic (CSL) [1] and the Multi-Drain Logic [11].

The new logic circuit technique is given in Section 2, followed by the design and characterization of the WCML cells in Section 3 and the library development for the cell based designs in Section 4.

2. Wired-AND Current-Mode Logic Circuit Technique

The WCML circuit, given in Figure 1, is composed of an NMOS current mirror analog circuit (M1 and M2) biased by a constant current source (I_b). The current source is implemented by a PMOS transistor (Mb) with adjustable V_G gate potential whose level keeps Mb in saturation for the lowest switching noise, and its level determines the speed of the logic gate. The input signal to the logic gate is current (I_{in}) and the output signal from the logic gate is also current (I_{out}). When a positive I_{in} is applied, ($I_b - I_{in}$) difference flows through

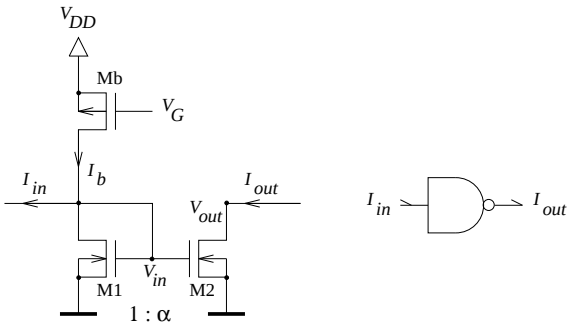


Fig. 1. The basic circuit schematic and symbol of the Wired-AND Current-Mode Logic (WCML).

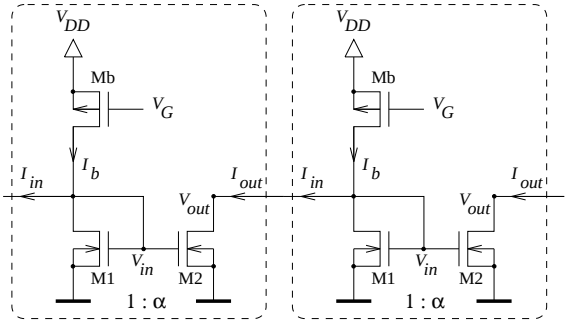


Fig. 2. Cascade connected WCML circuits.

M1, then it is amplified by a factor of $\alpha > 1$, and it is mirrored to the output. In terms of logical signals, when the gate input current is $I_{in} = 0$ (logic-high), the gate output current becomes $I_{out} = \alpha I_b$ (logic-low), and when $I_{in} = I_b$ (logic-low), the gate output current becomes $I_{out} = 0$ (logic-high). Hence, the gate functions as an inverting logic.

2.1. DC Characteristics

In the analysis of the WCML circuit, simple MOSFET Spice model (level 1), proposed by Shichman and Hodges is used. Assuming that both M1 and M2 transistors of the current mirror are in saturation without channel modulation ($\lambda = 0$), the output current is calculated by using the equations,

$$\begin{aligned} I_b - I_{in} &= K_{M1}(V_{in} - V_{tn})^2 \\ I_{out} &= K_{M2}(V_{in} - V_{tn})^2 \\ \alpha &\triangleq \frac{K_{M2}}{K_{M1}} \end{aligned}$$

where,

$$K_{Mi} = \frac{KP_i}{2}\frac{W_i}{L_i}$$

and KP_i is the unit transconductance (Spice model parameter), V_{tn} is N-MOSFET threshold voltage, W_i and L_i are the effective channel width and length of the MOSFET, M_i. Then, the output current is given as,

$$I_{out} = \alpha(I_b - I_{in}) \tag{1}$$

which is valid for the saturation condition,

$$V_{out} \geq V_{in} - V_{tn} > 0.$$

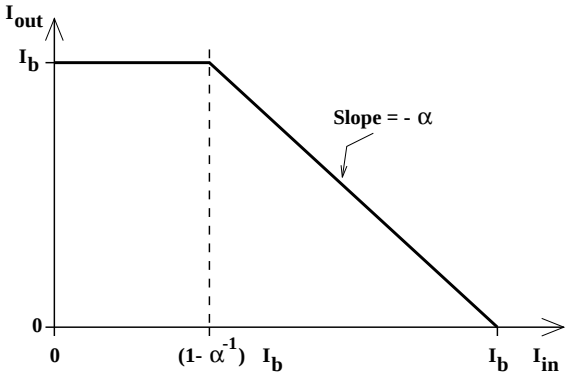


Fig. 3. The WCML inverting gate I_{out} versus I_{in} characteristic in cascade connection.

A chain of gates is constructed by simply cascading the WCML gate circuits, as shown in Figure 2. As the current mirror tries to sink more current (αI_b) than the supplied current (I_b), the transistor M2 enters into linear operating region. So, equation (1) is no longer valid and the output current (I_{out}) is limited to the bias current (I_b) of the succeeding gate. Therefore, input and output relation of an inverting gate is given by,

$$I_{out} = \begin{cases} I_b & \text{for } 0 \leq I_{in} \leq I_b(1-\alpha^{-1}) \\ \alpha(I_b - I_{in}) & \text{for } I_b(1-\alpha^{-1}) \leq I_{in} \leq I_b \\ 0 & \text{for } I_{in} = I_b. \end{cases}$$

In cascade connection, the inverting gate output versus input DC characteristic curve is plotted in Figure 3.

When multiple logic current signals are wired-AND and fed into an inverting gate, the gate becomes a multi-input NAND gate. Also, multiple fan-out WCML gate is implemented by repeating the mirrored current by multiple transistors at the output of the current mirror. A generalized WCML NAND gate, with fan-in of *m*

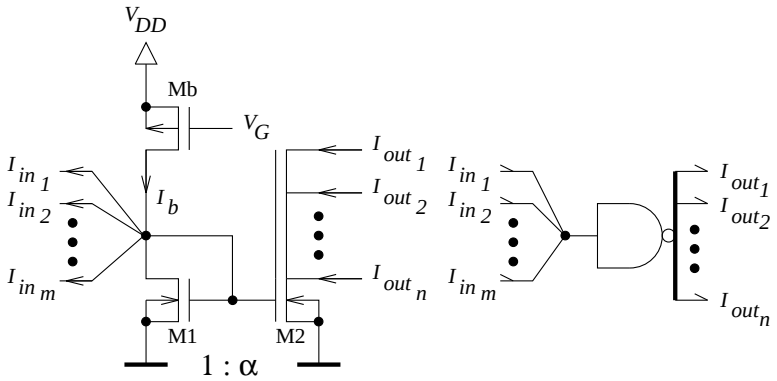


Fig. 4. Multi-input (fan-in=m), multi-output (fan-out=n) WCML NAND gate circuit and its symbol.

and fan-out of n, is implemented by $(n+2)$ transistors, which is independent of m, as shown in Figure 4.

2.2. Noise Margins

In the WCML circuit, valid logic signals are represented by ranges of currents. Let logic-low and logic-high current signals for the output and the input signals be defined as I_{OL}, I_{OH}, I_{IL}, and I_{IH}, respectively. We have,

$$\begin{aligned} I_{OL} &= \alpha I_b, \\ I_{IL} &= I_b, \\ I_{IH} &= (1-\alpha^{-1})I_b, \\ I_{OH} &= 0, \end{aligned}$$

and

$$\begin{aligned} I_{OH} &\leq I_{IH} - NM_H, \\ I_{OL} &\geq I_{IL} + NM_L. \end{aligned}$$

The low and the high noise margins, NM_L and NM_H are found as,

$$NM_L = (\alpha - 1)I_b, \tag{2}$$

$$NM_H = (1-\alpha^{-1})I_b \tag{3}$$

in which $\alpha > 1$ inequality should hold in order to restore the logic signal levels.

2.3. Switching Noise

The low switching noise of the WCML circuit on the power supply lines is maintained when Mb transistor is kept in saturation region as a constant current source. Ideally, there will be no variation neither in the bias current, nor in the supply current. If Mb transistor leaves the saturation region then the bias current through Mb starts to vary as I_{in} changes, and this causes noise. In order to determine the conditions for saturation of Mb transistor in the succeeding gate, the gate output voltage (V_{out}) needs to be computed, see Figure 2. While the output current swings, V_{out} also swings within a certain range. V_{out} has its minimum value when $I_{out} = I_b$ and M2 is in the linear region. This implies that $V_{in} > V_{tn}$ and M1 is in saturation. Neglecting the channel modulation ($\lambda = 0$), for M2 in linear region,

$$I_{out} = 2K_{M2}\left(V_{in} - V_{tn} - \frac{V_{out}}{2}\right)V_{out}$$

and solving for V_{out} yields,

$$\begin{aligned} V_{out} &= (V_{in} - V_{tn}) \\ &\quad - \sqrt{(V_{in} - V_{tn})^2 - \frac{I_{out}}{K_{M2}}}. \end{aligned} \tag{4}$$

For M1 in saturation,

$$V_{in} - V_{tn} = \sqrt{\frac{I_b - I_{in}}{K_{M1}}} \tag{5}$$

and substitution of equation (5) into (4) with $I_{out} = I_b$

and $I_{in} = 0$ results in,

$$V_{out_{MIN}} = (1 - \sqrt{1 - \alpha^{-1}})\sqrt{\frac{I_b}{K_{M1}}}.$$

V_{out} has the maximum value when $I_{in} = I_b$ and hence $I_{out} = 0$. Therefore, input current of the succeeding gate is zero, and M1 transistor of the succeeding gate is in saturation that satisfies equation (5). After substituting $I_{in} = 0$ into equation (5), the maximum value of V_{out} is calculated as,

$$V_{out_{MAX}} = V_{tn} + \sqrt{\frac{I_b}{K_{M1}}}. \quad (6)$$

The saturation condition of Mb transistor is given by,

$$(V_{out} - V_{DD}) \leq (V_G - V_{DD} - V_{tp}) < 0$$

where V_{tp} is P-MOSFET threshold voltage. The calculated maximum value of V_{out} in equation (6) should still keep Mb in saturation. Therefore,

$$V_{tn} + \sqrt{\frac{I_b}{K_{M1}}} - V_{DD} \leq (V_G - V_{DD} - V_{tp}) < 0 \quad (7)$$

should hold. The I_b current supplied by Mb in saturation ($\lambda = 0$) is given by,

$$I_b = K_{Mb}(V_G - V_{DD} - V_{tp})^2. \quad (8)$$

Substitution of equation (8) into the inequality (7) results in,

$$\sqrt{\frac{K_{Mb}}{K_{M1}}} \leq \frac{V_{DD} - V_{tn}}{V_{DD} - V_G + V_{tp}} - 1. \quad (9)$$

So, inequality (9) gives the relationship among the sizes of Mb and M1, and the values of V_G and V_{DD}. If the inequality is satisfied then Mb remains in saturation, and the logic circuit has its low noise property.

Inequality (9) is evaluated for 0.8μm CMOS process parameters,[1] and plotted in Figure 5 for the supply voltages of 1.2V, 1.5V and 3.0V. The solid lines are drawn by using the inequality (9) for the case of equality. The small circles indicate the PSpice simulation results for different transistor sizes, and the bias current (I_b) through Mb transistor is recorded next to the circles. The Mb transistor operates in saturation in the region bounded by the solid curve for a given supply voltage and the threshold voltage (V_{tp}) of Mb.

In the case of multiple fan-in of m and fan-out of n, again inequality (9) is used in the design because the maximum node voltage, given by equation (6), does not change. On the other hand, parallel connection of linear transistors divides the I_b current, and this causes $V_{out_{MIN}}$ to decrease. Its value is calculated by the substitution of equation (5) into (4) with $I_{out} = I_b/m$ and $I_{in} = 0$, which gives,

$$V_{out_{MIN}} = (1 - \sqrt{1 - (m\alpha)^{-1}})\sqrt{\frac{I_b}{K_{M1}}}.$$

The difference between $V_{out_{MAX}}$ and $V_{out_{MIN}}$, and the slew rate of the node potentials, affect the noise coupling amount into the substrate. The current-mode operation leads to smooth voltage variations at the nodes. The node potential variation is reduced to less than $(V_G - V_{tp})$ by a proper choice of the effective size ratio of M1 to Mb.

3. WCML Cell Design and Characteristics

The current mirror ratio, α, is selected as 1.5 for each WCML cell. With this α value, and using the equations (2) and (3), the noise margins of a single input inverting gate are evaluated as

$$NM_L = 0.50 I_b,$$
$$NM_H = 0.33 I_b.$$

The size ratio of Mb to M1 is determined from the maximum bias current versus the ratio characteristic curves plotted in Figure 6. The curves are obtained from the data in Figure 5. It can be observed that the bias current does not increase considerably beyond the ratio of about 3.5 for each supply voltage. At this ratio, the maximum possible bias currents for a WCML gate are approximately 2.9μA, 8.5μA and 76μA for supply voltages of 1.2V, 1.5V and 3.0V, respectively. Beyond these bias currents, Mb transistor is no longer in saturation and it starts to generate noise on the supply line. When more bias current is required, Mb and M1 transistors are equally scaled up, so that their size ratio is kept the same. Although the scaling can be implemented by the parallel connection of the WCML gate

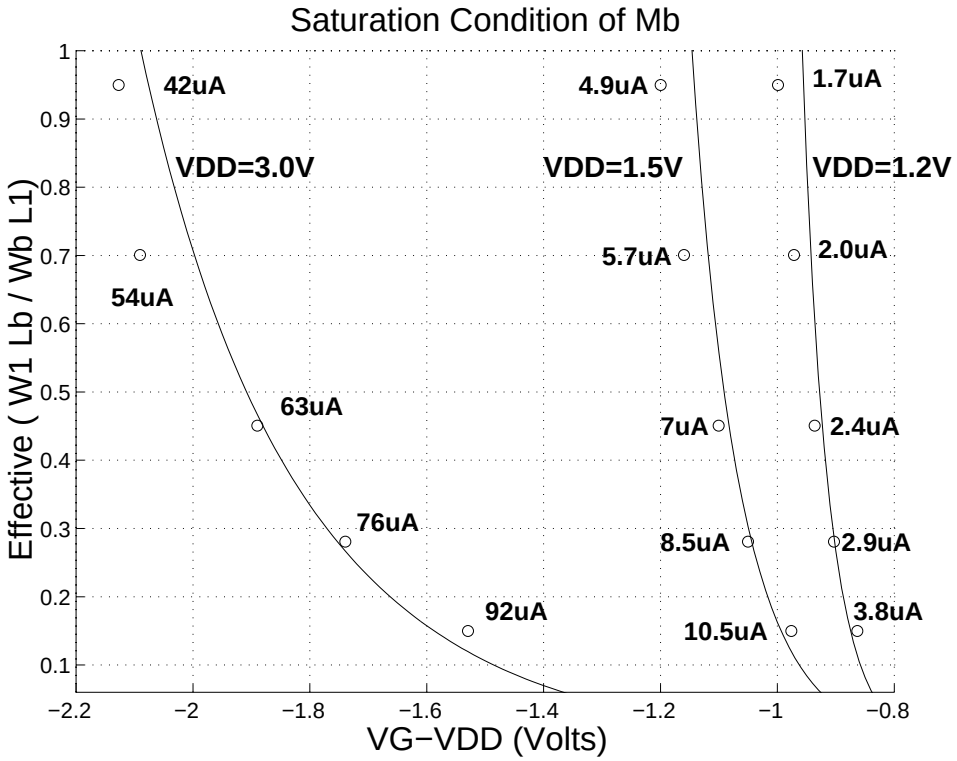


Fig. 5. The saturation condition curves of Mb transistor for the supply voltages of 1.2V, 1.5V and 3.0V. The bias current (I_b) value is recorded at the measured points.

circuits, it would be better to implement it in another WCML cell circuitry. This way, not only the MOSFET parasitics and the wiring parasitics are minimized, but more compact cell layout is obtained.

The scaling effect on the WCML gate characteristics is studied on a 2-input NAND gate with fan-out of 3. In order to simulate the inter-block cell to cell connection line parasitics, a 50fF wiring load capacitance is added to the gate input. The load capacitance corresponds to about 400μm long metal-1 layer parasitic capacitance. The test circuit is shown in Figure 7(a). Either output-(i) or output-(ii) is connected to the wired-AND node for the measurement of the worst case average current propagation delay through the NAND gate. The delay is measured between the output current of the active inverter and the output current of the NAND gate.

The maximum delay for low to high current transition at the NAND gate output occurs when the inputs of the 2-input wired-AND node makes a current transition from high to low at the same time. This is implemented by the connection of output-(i) while output-(ii) is not used. The maximum delay for high to low current transition at the NAND gate output occurs when a single input of the wired-AND node makes a current transition from low to high. In this case, output-(ii) is connected and output-(i) is not used.

For a comparison between the WCML and the standard static-CMOS logic, the 2-input NAND gate with fan-out of 3 and loading of 50fF is designed in the static-CMOS logic, and the test circuit is given in Figure 7(b). A scale factor is defined as the multiplier of the transistor effective sizes in the test circuits. The transistor sizes of the WCML NAND gate and the static-CMOS logic NAND gate for each scale factor are given in Table 1.

Simulations are done at various supply voltages, supply currents, scale factors, and load capacitances. A range of supply current is applied to the WCML circuit for each scale factor, and the average supply current of the static-CMOS logic is measured at the maximum output frequency. The MOSFET drain/source layout parasitics are included in the simulations. In order to observe the effect of the bias transistor Mb on the switching noise generation, the supply current is not

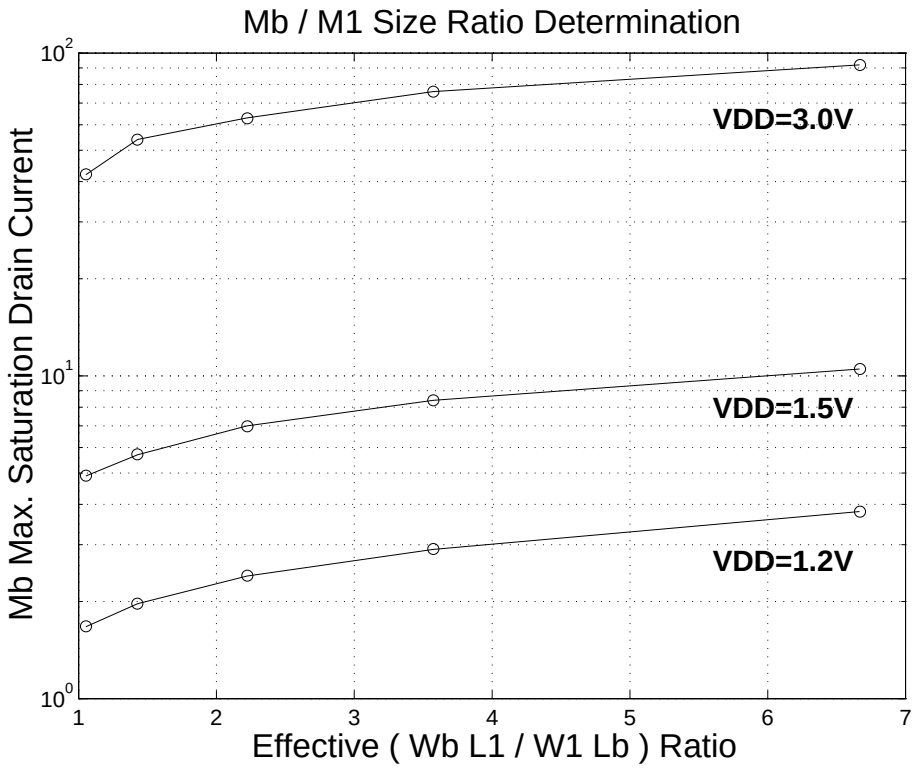


Fig. 6. The Mb/M1 size ratio determination for supply voltages of 1.2V, 1.5V and 3.0V.

Table 1. The NAND gate test circuit transistor drawn widths for the WCML and the static-CMOS logic. The effective lengths and widths of the transistors are multiplied by the scale factor. The drawn channel length of each transistor is 0.8μm.

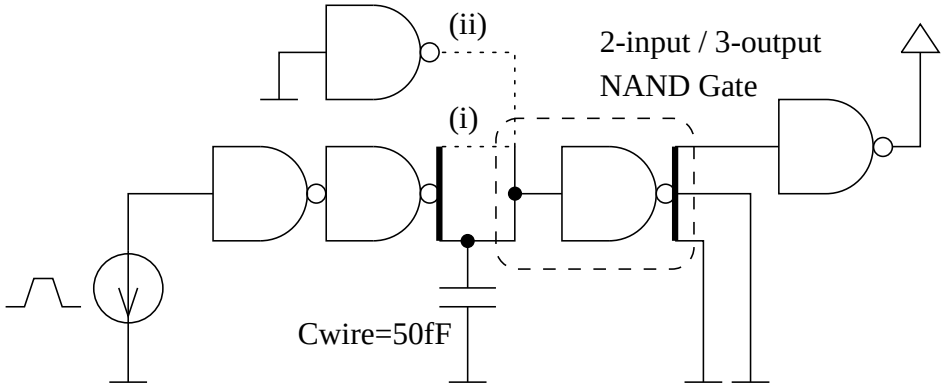
Scale Factor	W_{Mb} (μm)	W_{M1} (μm)	W_{M2} (μm)	W_p (μm)	W_n (μm)
1	5.0	2.2	2.7	1.9	2.2
2	9.3	3.2	4.3	3.1	3.2
3	13.7	4.3	5.8	4.4	4.3
5	22.3	6.4	9.0	6.8	6.4
10	44.0	11.6	16.8	13.1	11.6
20	n.a.	n.a	n.a	25.2	22.0

limited to the non-saturation point of Mb, but it is limited to the point at which low noise margin limit is approximately reached ($I_{in} \approx I_b \Rightarrow I_{out} \approx 0$). The simulation results of the NAND gate test circuits are given in Figure 8.

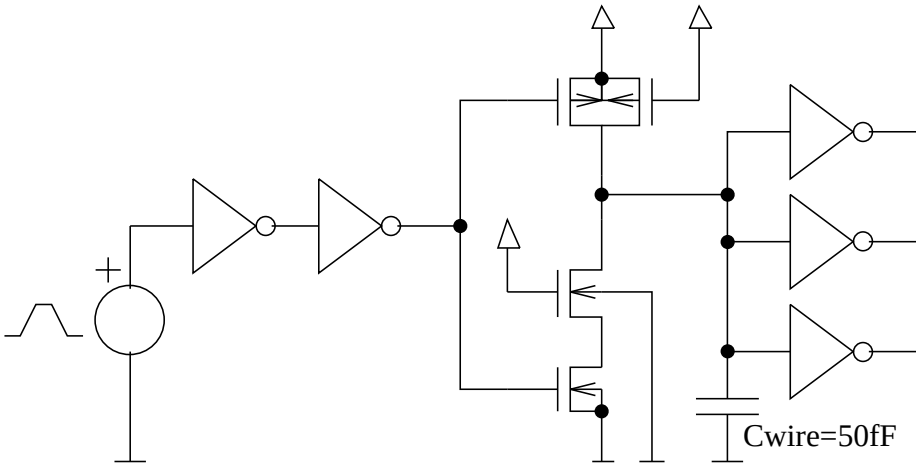
3.1. Basic Observations

The observations and the comparisons between the WCML and the static-CMOS logic are itemized below:

1. For the WCML, at a given scale factor, the gate delay is controllable by the supply current. Without any modification on the transistor sizes, the delay can be reduced by increasing the supply current via the gate bias voltage (V_G).
   For the static-CMOS logic, the gate delay can be controlled by the scale factor. So, the delay can be reduced by increasing the transistor sizes by the scale factor.
2. For the WCML, at a given scale factor, the supply current can be reduced as much as desired, at the expense of delay.
   For the static-CMOS logic, at a given scale factor, the supply current can be reduced by lowering the gate output frequency.
3. For the WCML, the peak-to-peak current noise on



(a) WCML



(b) Static CMOS Logic

Fig. 7. The 2-input NAND gate (fan-out=3) test circuits for (a) the WCML, and (b) the static-CMOS logic.

the supply current can be reduced by decreasing the supply current.

For the static-CMOS logic, the peak-to-peak current noise can be reduced by decreasing the scale factor.

4. For both WCML and static-CMOS logic, there exist break points for the scale factors at which no more significant delay improvement is obtained as the scale factor is increased. The scale factor breakpoints are listed in the following table.

VDD	WCML Scale Factor	Static-CMOS Scale Factor
1.2V	10	10
1.5V	5	10
3.0V	2	5

3.2. Performance Comparison

1. The minimum gate delay and the average supply current (Iavg) of the WCML at the scale factor

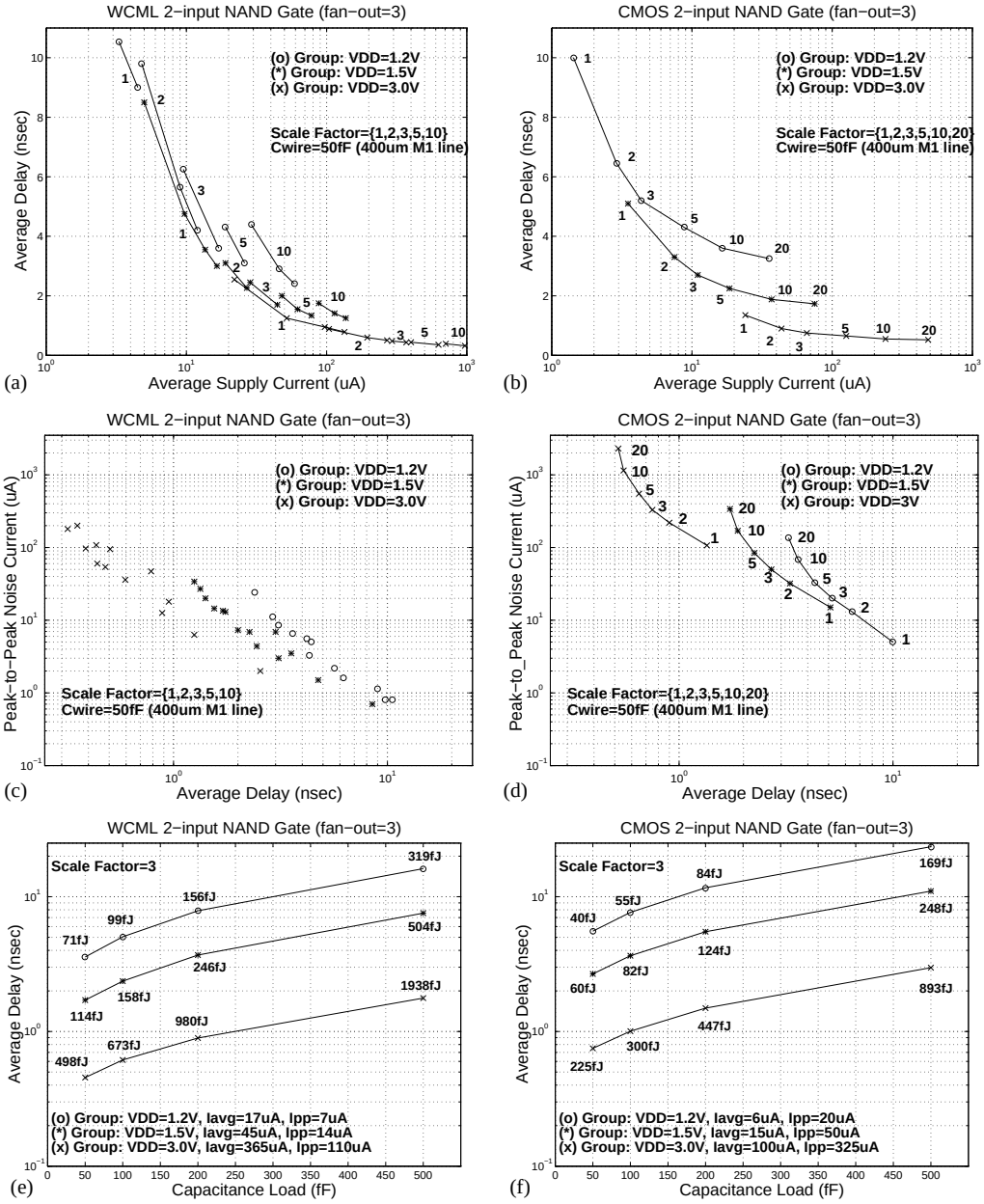


Fig. 8. The 2-input (fan-out=3) NAND logic gate characteristics for the WCML implementation and the static-CMOS logic implementation at the supply voltages of 1.2V, 1.5V and 3.0V. Average delay versus average supply current plots for (a) WCML using scale factors of 1, 2, 3, 5, 10, and (b) static-CMOS logic using scale factors of 1, 2, 3, 5, 10, 20. Peak-to-peak noise on the supply current versus average delay plots for (c) WCML using scale factors of 1, 2, 3, 5, 10, and (d) static-CMOS logic using scale factors of 1, 2, 3, 5, 10, 20. Average delay versus wiring load capacitance plots with the power-delay products for (e) WCML using a scale factor of 3, and (f) static-CMOS logic using a scale factor of 3.

breakpoints are compared with those of the static-CMOS logic in the table below.

VDD	WCML Delay	CMOS Delay	WCML Iavg	CMOS Iavg
1.2V	2.4 ns	3.6 ns	60μA	20μA
1.5V	1.4 ns	1.9 ns	80μA	40μA
3.0V	0.44ns	0.65ns	270μA	130μA

2. The average supply currents of the WCML and the static-CMOS logic for the same delays are compared in the table below.

VDD	Delay	WCML Iavg	CMOS Iavg
1.2V	9.0ns	4.5μA	1.7μA
1.2V	3.5ns	17 μA	17 μA
1.2V	3.3ns	26 μA	34 μA
1.5V	5.0ns	9.2μA	3.5μA
1.5V	1.8ns	40 μA	40 μA
1.5V	1.7ns	44 μA	75 μA
3.0V	1.0ns	90 μA	40 μA
3.0V	0.6ns	200 μA	190 μA
3.0V	0.4ns	270 μA	500 μA

3. The peak-to-peak supply currents (Ipp) of the WCML and the static-CMOS logic for the same delays are compared in the table below.

VDD	Delay	WCML Ipp	CMOS Ipp
1.2V	10.0ns	0.9μA	5μA
1.2V	3.3ns	8μA	135μA
1.5V	5.0ns	1.5μA	15μA
1.5V	1.7ns	10 μA	340μA
3.0V	1.4ns	5 μA	107μA
3.0V	0.5ns	40 μA	2300μA

4. At a scale factor of 3, and in a wiring load capacitance range of 50fF to 500fF, the performance ratios of the WCML to the static-CMOS logic in terms of average delay, average supply current and peak-to-peak noise on the supply current are given in the table below.

	(WCML)/(CMOS)		
VDD	Delay	Iavg	Ipp
1.2V	0.66	2.83	0.35
1.5V	0.65	3.0	0.28
3.0V	0.60	3.65	0.34

4. WCML Cell Library Development

A WCML cell library is developed using standard 0.8μm CMOS technology in Cadence design environment. Although any Boolean function can be implemented by using the elementary WCML NAND gate cell, complex gates are hand-craft laid out in order to have compact layouts. Small sized transistors (scale factor of 1) are used in the logic cells, and for large wiring loads, the scale factors of 3 and 5 are used in the buffer circuits.

Various logic function schematics are shown in Figure 9. In general, a WCML gate is composed of an m-input/1-output AND gate, and an n-output inverter gate. The cascade connection of the AND gate and the inverter gate results in an m-input/n-output NAND gate. The AND gate is a simple wired-AND connection of m wires. The number of transistors required for an n-input inverter gate is the same as an m-input/n-output NAND gate, which is $(n+2)$. On the other hand, the number of transistors required for an m-input/n-output NOR gate or for an OR gate is dependent on the number of gate inputs as well as the number of gate outputs, which are $(3m+n+5)$ and $(3m+n+2)$, respectively. The layout areas of the various WCML library cells are compared with the areas of the static-CMOS logic cells from $0.8\mu m$ CMOS standard cell library. The comparison in Table 2 indicates that the WCML cell layout area is comparable with the area of the static-CMOS logic cell from a standard cell library. It is expected that at the register-transfer design level, the WCML design occupies less area than the static-CMOS logic design, because a WCML AND gate, with any number of inputs, is simply implemented by wiring which does not require any transistor. Consequently, the routing channels of an IC can be efficiently utilized by the logical AND operations without an increase in the channel area. Layouts of the 4-input/4-output OR gate and the D-type flip-flop from the WCML cell library are drawn as examples in Figure 10.

The performance of each WCML cell can be optimized in terms of the delay, the power, and the switching noise for a given supply voltage. This is achieved by the adjustment of the gate supply current via the V_G potential. Therefore, a number of biasing circuits are included in the WCML library in order to control the supply current of a group of logic cells in a design. A toggling D-type flip-flop and a one bit full adder from the WCML library are simulated at 1.5V supply volt-

Table 2. Cell area comparison between WCML with scale factor=1 and CMOS logic with scale factor=5, except D-FF for which scale factor=1.

Function	fan-out	WCML Area(μm^2)	CMOS Area(μm^2)
2 input NAND	2	338.4	414.0
4 input NAND	2	338.4	828.0
4 input OR	4	1296.0	1242.0
2 input EXOR	3	1065.6	966.0
D-FF	2	1886.4	1518.0
1-bit FADD	2	2980.8	3174.0

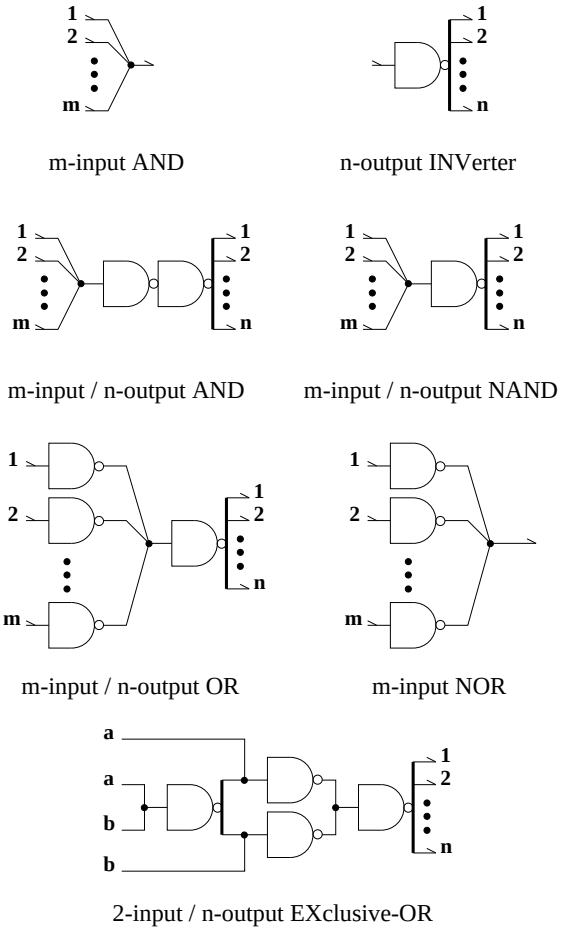


Fig. 9. Various logic functions implemented by the WCML circuit technique.

age at two supply current levels. The performance of each cell is given in Table 3.

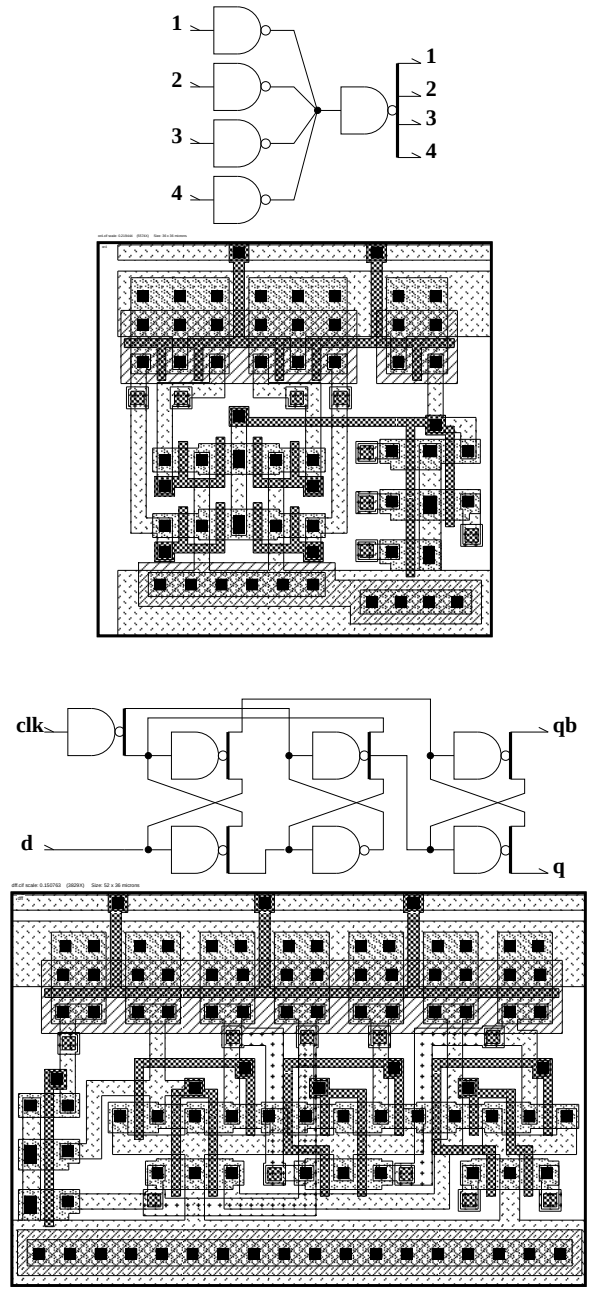


Fig. 10. The WCML 4-input OR gate (fan-out=4) and WCML D-type Flip-Flop (fan-out=1) circuits and layouts from WCML library.

5. Conclusion

By using the new Wired-AND Current-Mode Logic (WCML) circuit technique in CMOS technology, low-noise digital circuits can be designed, and they can be mixed with the high precision analog circuits in a single

Table 3. The performances of Toggle D-type Flip Flop and Full Adder from WCML cell library at 1.5V supply voltage.

	Toggle D-FF		Full Adder	
Fclk/Delay	90MHz	160MHz	10.5ns	2.8ns
Iavg	67μA	122μA	50μA	240μA
Ipp	10μA	13μA	12μA	30μA

IC and on the same silicon substrate.

The WCML circuits can operate at lower supply voltages and they have lower gate delays than the static-CMOS logic circuits. The supply current of a WCML gate is independent of the operating frequency, therefore, the WCML circuits have static power dissipation. However, at high frequencies, the WCML circuits dissipate less power than the static-CMOS logic circuits. The layout areas of the low fan-in WCML gates are comparable with the static-CMOS logic. For high fan-in AND and NAND gates, the WCML occupies much less area compared to the static-CMOS. In the cell based IC designs, the channel utilization of the WCML is expected to be better than that of the static-CMOS logic, because the logical AND operation in the WCML is achieved by the wiring only.

Moreover, the supply currents of the WCML cells in an IC are controllable, hence it is possible to optimize the performance of the IC dynamically.

Notes

1. The circuit simulations throughout the study in this paper are done by using the PSpice analog circuit simulator. In the simulations, MOSFET parameters of a standard 0.8μm CMOS technology are used. Some of the MOSFET Spice model parameters are given in the table below:

Parameter	N-MOSFET	P-MOSFET	Unit
TOX	15.5	15.5	nm
LD	0.0	$-.075$	μm
WD	0.58	0.33	μm
VTO	0.84	$-.73$	V
KP	103	37	uA/V^2

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