DESIGN, FABRICATION AND OPERATION OF A VERY HIGH INTENSITY CMUT TRANSMIT ARRAY FOR BEAM STEERING APPLICATIONS

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IN

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By

Talha Masood Khan

December 2020

Design, Fabrication and Operation of a Very High Intensity CMUT Transmit Array for Beam Steering Applications
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We certify that we have read this dissertation and that in our opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Doctor of Philosophy.

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ABSTRACT

DESIGN, FABRICATION AND OPERATION OF A VERY HIGH INTENSITY CMUT TRANSMIT ARRAY FOR BEAM STEERING APPLICATIONS

Talha Masood Khan
Ph.D. in Materials Science and Nanotechnology
Advisor: Hayrettin Köymen
December 2020

Several studies have reported airborne ultrasound transmission systems focused on achieving beamforming. However, beam steering and beamforming for capacitive micromachined ultrasonic transducers (CMUTs) at high intensity remains to be accomplished. CMUTs, like other ultrasonic transducers, incorporate a loss mechanism to obtain a wide bandwidth. They are restricted to a limited amount of plate swing due to the gap between the radiating plate and the bottom electrode, along with a high dc bias operation.

CMUTs can be designed to produce high-intensity ultrasound by employing an unbiased operation. This mode of operation allows the plate to swing the entire gap without collapsing, thus enabling higher intensity. In this study, we use an equivalent circuit-based model to design unbiased CMUT arrays driven at half the mechanical frequency. This model is cross verified using finite element analysis (FEA). CMUT arrays are produced in multiple configurations using a customized microfabrication process that involves anodic wafer bonding, a single lithographic mask, and a shadow mask.

We use impedance measurements to characterize the microfabricated devices. We experimentally obtained the highest reported intensity using a microfabricated 2×2 CMUT array driven at resonance in a pulsed configuration. This array is also capable of beam steering and beamforming at a high intensity such that it can steer the entire half-space. The beam obtained from the array is in excellent agreement with the theoretical predictions. The amplitude and phase compensation for the devices remain constant that makes these arrays attractive for applications involving park assist, gesture recognition, and tactile displays.
Keywords: Airborne Ultrasound, Capacitive micromachined ultrasonic transducers, CMUT, transducer array, High Intensity, Beam Steering, MEMS, Unbiased operation, Half frequency driven, Mutual radiation impedance, Lumped element model, Large Signal Equivalent Circuit model, Array, Microfabrication.

ÖZET

YÜKSEK YOĞUNLUKLU CMUT İLETİM DİZİLERİNİN IŞIN YÖNLENDIRME UYGULAMARI İÇİN TASARIMI, ÜRETİMİ VE KULLANIMI

Talha Masood Khan
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Aralık 2020

Işın hüzmeleme hedefleyen havada ultrason iletim sistemleri bazı çalışmalarda gösterilmiş olmasına rağmen; yüksek yoğunlukta çalışan kapasitif mikroişlenmiş ultrasonik dönüştürücüler (CMUTs) için ışın yönlendirme ve hüzmeleme uygulamaları henüz başarılamadı. CMUT'lar diğer benzer ultrason dönüştürücülerde de olduğu gibi geniş bant aralığı sağlayabilmek için bir kayıp mekanizması kullanırlar. İletim plakası ve alt elektrot arasındaki boşluk ve yüksek doğru akım öngerilme faaliyeti nedeniyle, kısıtlı miktarda plaka salınımıyla sınırlıdır.

CMUT'lar öngerilimsiz çalıştırılarak yüksek şiddetli ultrason üretecek şekilde tasarlanabilir. Bu çalıştırma modu plakanın hiç çökmeden tüm boşluk boyunca salınım yapmasına müsade ederek daha yüksek şiddette çalışmasını sağlar. Bu çalışmada mekanik frekansın yarı değerinde sürülen CMUT dizileri tasarlamak için bir eşdeğer devre modeli kullandık. Kullandığımız bu modeli sonlu eleman analizi (FEA) yontemi ile dogruladık. CMUT diziler, anodik yonga levhası bağlama, bir litografi maskesi ve bir gölge maskesi içeren özelleştirilmiş mikrofabrikasyon aşamaları kullanarak çoklu konfigürasyonlarda üretildi.

Mikrofabrikasyonu tamamlanmış cihazları karakterize etmek için empedans ölçümleri yaptık. Atımlı konfigürasyon rezonans frekansında sürülen 2×2'lik şekilde üretilmiş CMUT dizisinde, dizi yüzeyi referans olarak kabul edilerek, şimdiye kadar bildirilmiş en yüksek yoğunluklu basınç degerini, 144 dB // 20μPa, deneysel olarak elde ettik. Bu dizi ayrıca bütün yarım uzayı kaplayan yüksek yoğunluklu ışın hüzmeleme ve yönlendirme kapasitesine sahiptir. Diziden elde edilen ışın profili teorik hesaplamalar ile mükemmel bir seviyede örtüşmektedir. Genlik ve faz dengesinin sabit kalması bu cihazları park yardımı, hareket tanıma ve dokunmatik ekran gibi uygulama alanlarında ilgi çekici kılmaktadır.

Anahtar sözcükler: Havada çalışan Ultrason, Kapasitif mikroişlenmiş ultrasonic çeviriciler, CMUT, çevirici dizini, Yüksek Yoğunluk, Işın Yönlendirme, MEMS,

Doğrusal (DA) Yüklemesiz Operasyon, Yarı frekansta sürülen, Ortak radyasyon empedansı, Toplu eleman modeli, Büyük-sinyal Eşdeğer devre modeli, Dizi, mikrofabrikasyon.

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dedicated to my parents, my brothers and my wife

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Chapter 1

Introduction

1.1 Ultrasound systems

Ultrasound systems are being developed for several decades but their progress has been slower in comparison to other semiconductor technologies. Today, the ultrasound related market has seen a rapid increase in development thanks to new and improved microfabrication facilities. The revival of the micro-machined ultrasonic transducer (MUT) market has brought new applications. This resurgence in the market can be owed to the following factors [1]:

- Latest applications require the push towards these technologies. Medical ultrasound market is expanding, moving the applications to hand held devices [2]. The demand for finger print sensing [3, 4] in digital electronic market is also another factor.
- The microfabrication technology is readily available. Both Capacitive MUT (CMUT) and Piezoelectric MUT (PMUT) can be manufactured using these advanced manufacturing techniques.

- Many major industries are actively investing is such technologies. This include Philips [5], Hitachi [6], STMicroelectronics [7], Dimatix [8] and Butterfly network[2], that have readied the market for mass-production.

The BioMems market dynamics show a major increase in the requirement for pressure sensors and MUT from 2019 to 2025 [9]. These include applications in park assist [10], finger print sensing [3], Non-destructive testing [11], gesture recognition [12, 13], non-contact thermoacoustic detection [14], tactile displays [15, 16], mass sensors [17], gravimeteric sensors [18] and automation. Currently this market is widely occupied by Bulk piezoelectric transducers. It is forecasted that both CMUT and PMUT's will take a major portion of this market until 2023 [1].

Ultrasonic systems for waterborne applications [19] have been widely used for imaging and nondestructive testing for several decades. As water is universally available, provides low absorption in MHz frequency range and does not chemically or physically react with industrial materials, it has been an attractive coupling medium [11]. On the other hand, water can cause permanent damage to some industrial processes. For the last decade, the demand for ultrasound devices in airborne mode have increased. Airborne ultrasonics provides a challenge in implementation due to high acoustic impedance mismatch and high attenuation.

1.2 Ultrasonic phased Arrays

Ultrasonic arrays in airborne applications are developed for these two objectives [20, 21, 22]:

i Phased arrays for far-field beam steering.

ii Obtaining high-intensity ultrasound, either to be used in the near-field of the array or to obtain a fixed narrow beam.

In order to steer the beam without limitations or side lobes, the element size must be small in comparison to the wavelength (λ). In order to obtain high-intensity ultrasound with narrow beam width, large number of elements are required in an array.

All the arrays reported in the literature have different beam-steering capabilities, operating frequency range, aperture size with respect to wavelength and the employed technologies. These variations make it difficult to make comparisons. As the far field pressure is effected by the Rayleigh distance and beamwidth, the output pressure of these studies can be compared in terms of respective surface pressure[23].

An 8-element flextentional MUT in a 1-dimensional phased array configuration is reported to provide 132 dB[1] @ 0.3 m and 123 dB @ 1 m, when measured in far field at 30 kHz [24]. The pressure at the surface of the array is estimated to be about 140–145 dB from the reported far field pressure levels. Another work [25] with novel ferro-electric materials provide phased array performance with 102 dB @ 0.2 m of pressure. For this array, it is understood that array surface pressure is low, although 102 dB is obtained at 20 cm focus distance by beamforming 32 elements.

Several works have been focused on production of high-intensity ultrasound using CMUTs using phased array systems [26, 27, 28, 23, 29, 30, 31]. Although CMUT transducers provide attractive features, they suffer from limited transmitted pressure when driven using dc voltage bias, due to collapse phenomena and the associated choice of membrane dimensions and gaps [32]. To overcome this constraint, in one study, CMUT receiver elements and piezoelectric transmitting elements have been microfabricated together [33]. This combination improves the transmit range and axial resolution of the system. A novel CMUT design replaces the traditional circular design with an annular shape reporting an increase in transmit sensitivity and power intensity [27]. Another novel CMUT design with multiple moving membranes has shown an increase in transmission

[1] All dB values in this work are referenced to 20 μPa rms

efficiency using a 1×27 element array fabricated using a multiuser MEMS processes (MUMPs) [30, 31]. Another work presents an 8×8 CMUT array operating at 40 kHz to provide real time 3D imaging using phased array [28]. A CMUT design with an embossed pattern has been fabricated to improve output pressure in a liquid medium [34]. A large, 100-mm diameter, CMUT transmitter array generating a high pressure 107 dB @ 3 m (135 dB referred to the surface) at 50 kHz, when biased at 380 V_{dc} and driven using 200 V_{ac}, has been reported for parametric array operation [23].

Many studies have also reported non-electronic phased arrays. Volumetric imaging using two row-column arrays using synthetic aperture imaging (SAI) emission sequence and beamformer is reported [35]. Airborne ultrasonic imaging based on the synthetic aperture technique that images by mechanically moving the elements is also reported [36].

In this study, we present design, production, and operation of a half-frequency driven unbiased CMUT array capable of beam steering at high intensity. When a *dc* bias is applied, the plate is depressed further at smaller drive levels and can collapse before it can reach the full swing. We demonstrate, both analytically and experimentally that an airborne CMUT transmitter array can be optimally designed to provide beam steering while providing a high surface pressure. The general physical requirements, such as element size and spacing, for better performance, is a well-studied topic. However, the requirement for linear elastic operation for CMUTs imposes limitations on the element size [37].

Lumped element equivalent circuit-based model [38] was exploited to derive a CMUT transmitter array operated at zero bias. It is shown in [39] that very high radiated pressure can be obtained from a CMUT if it is driven unbiased, where the radiation plate vibration can span the entire gap height without collapsing.

In this work, we first demonstrate the unbiased array operation by implementing beamforming and beam steering using appropriate phasing at half the operational frequency of transmission [40]. All the array elements are driven individually ensuring that they operate within the elastically linear range.

The array operation is then further extended to a very high-intensity transmission, where both beamforming and beam steering are performed at very high intensity [41]. One important finding of this study is that the required phasing for linear operation remains constant at low and high intensity levels, even though the dynamics of the radiation plates are no longer elastically linear.

Fabrication inaccuracies may produce discrepancies in frequency response and radiated pressures between different elements of the array. Fundamentally, the beam-steering requires all elements in an array to perform at the same level. In this work, we show that beam steering can be achieved to cover the entire Fourier half-space by appropriate amplitude and phase compensation, despite the fabrication inaccuracies. Our model was used to account for these deviations and losses and was further used to demonstrate an optimally compensated beam steered CMUT array. The large signal equivalent circuit model and finite element analysis findings were verified using a set of impedance and pressure measurements on several single CMUT elements and arrays. In this work, we report a design methodology for arrays that have very high-power transmission performance.

1.3 Organization of this Thesis

The rest of the thesis is organized as follows. In chapter 2, we present the design methodology for a single and array based CMUT device. We will also discuss the ka and Q limitations, in addition to constraints regarding kd for designing CMUT arrays. In chapter 3, we will discuss the fabrication process of CMUT from mask design to post-processing. This chapter also discusses production of CMUT receivers and subsequent fabrication runs. In chapter 4, we discuss the measurement of the CMUT devices, and verification of the model. Concluding remarks and discussions will follow in chapter 5. Appendix of this thesis includes LabView, ADS and FEM simulation procedures. Appendix F contains a list of author's publications during his Ph.D. at Bilkent university.

Chapter 2

Designing CMUTs

For the design and optimization of CMUT based transducer arrays, both finite element analysis (FEA) and equivalent circuit modeling have been used. Using equivalent circuit models coupled with self radiation and mutual radiation impedance yields accurate results which compare well with measurements even in large-signal airborne applications [38, 42, 43, 44]. The equivalent circuit based approach provides an advantage over the FEA when simulating arrays with multiple elements [45].

In this study, we will first use circuit modelling to design CMUT devices and then make a comparison with FEM modelling.

2.1 Unbiased CMUT operation

Top view of a 2×2 CMUT array with the cross-sectional view of a CMUT element is shown in Fig. 2.1. Here, radius of the radiation plate is shown as a, the gap height between the radiation plate and bottom electrode is depicted as t_g, the thickness of the insulator layer is shown as t_i , the thickness of the plate is denoted as t_m and the static force being exerted on the plate is shown as F_{RB}. The spacing between adjacent elements in an array is given as d.

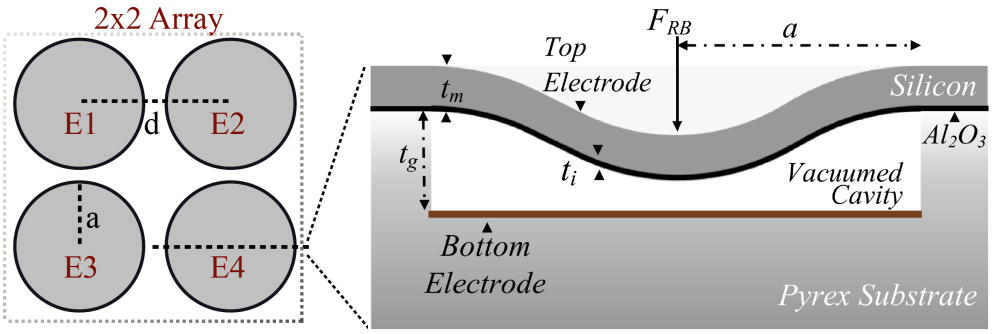


Figure 2.1: (Left) Top view of a 2×2 CMUT array, and (right) cross-section of a single CMUT cell. © *2020 IEEE.*

The top electrode, made of high conductivity *Si* substrate, is suspended over a vacuumed cavity (gap) in the *Pyrex* substrate. Bottom electrode is produced using metallization at the bottom of the cavity. An Alumina (Al_2O_3) insulator layer is deposited under the top electrode. An acoustic wave can be generated in a CMUT element by applying electrical voltage between the two electrodes.

The *dc* operation of a CMUT element puts a limit on the amount of plate swing achievable for a given gap. With a *dc* bias, the plate is depressed at no excitation and the collapse phenomenon limits the swing amplitude. Consequently, only a portion of the available gap height can be utilized for plate swing in biased operation. The unbiased *ac* operation of the CMUT employs the terminal voltage at half the desired radial frequency, ω, given as [39, 46],

$$V(t) = V_m cos(\frac{\omega}{2}t) \tag{2.1}$$

As the transduction force is proportional to the square of the potential difference between the terminals, the dynamic force on the plate is at the desired radial frequency.

A thin clamped plate displacement profile is given as [47],

$$x\left(r,t\right) = x_p(t)\left(1 - \frac{r^2}{a^2}\right)^2 \text{ for } r \leq a \tag{2.2}$$

when a uniformly distributed force acts on its surface. Here r is the radial position and x_p is the center displacement of the plate towards the gap. This profile function is maintained as long as the plate deflection is low and the vibration is within elastic linear range. As the amplitude of the deflection increases, the deflection profile gradually deviates from eq. 2.2.

The electrostatic force on a concentric narrow ring on the membrane of area $2\pi r\delta r$ of the CMUT driven using $V(t) = V_{dc} + V_{ac}(t)$ can be given as,

$$\delta F(r,t) = \frac{1}{2}V^2(t)\frac{\mathrm{d}[\delta C(x(r,t))]}{\mathrm{d}x} \tag{2.3}$$

where the capacitance of this ring can be expressed as [48],

$$\delta C(x(r,t)) = \frac{\varepsilon_0 2\pi r\delta r}{t_{ge} - x(r,t)} \tag{2.4}$$

here, $t_{ge} = t_g + t_i/\epsilon_r$, is the effective gap height, ϵ_0 is the permittivity of the gap, and ϵ_r is the relative permittivity of the insulation layer. The capacitance for full deflected plate can be found using integration:

$$C(t) = \int_0^r \delta C(x(r,t)) = C_0 g(\frac{x_p(t)}{t_{ge}}) \tag{2.5}$$

here,

$$C_0 = \epsilon_0\frac{\pi a^2}{t_{ge}} \tag{2.6}$$

and g(*) is given as,

$$g(u) = \frac{tanh^{-1}(\sqrt{u})}{\sqrt{u}} \tag{2.7}$$

2.2 *Q*, *ka* and *kd* limitations

The mechanical quality factor, Q_m, for a lossless CMUT element is given as,

$$Q_m = \frac{\omega_r L_{Rm} + X_{RR}\,(k_r a)}{R_{RR}\,(k_r a)} = \frac{k_r a}{R_1(k_r a)}\frac{t_m}{a}\frac{\rho_m}{\rho_0} + \frac{X_1(k_r a)}{R_1(k_r a)} \tag{2.8}$$

where t_m/a is calculated using the resonance condition in terms of velocity of sound in air, c_0, and the material properties as,

$$\frac{t_m}{a} = (k_r a)\, c_0 \sqrt{\frac{9(1-\sigma^2)\rho_m}{80 Y_0}} \tag{2.9}$$

Here, $\rho_m/\ \rho_0$ is the density ratio of plate material to air, (L_{Rm}) is the mass of the plate and $k_r = 2\pi/\lambda$, denotes the wave number in air at the resonance frequency, f_r. The normalized real and imaginary parts of the radiation impedance, $R_{RR}\,(k_r a) + jX_{RR}\,(k_r a)$, of the transducer are denoted as R_1 and X_1, respectively. Y_0 is the Young's modulus and σ is the Poisson's ratio of the radiation plate. Fig. 2.2 shows how Q_m and a/t_m vary with increase in ka [1].

Equation 2.8 predicts a minimum quality factor at $k_r a \approx 0.5$ for a Si plate, where the transducer bandwidth is at maximum. This value is unusable, since the corresponding a/t_m ratio found from eq. 2.9 is very large (< 130), hence requiring a very thin plate. Thin plates suffer stiffening in CMUTs with a vacuum gap when subjected to atmospheric pressure. Geometrical elastic non-linearity occurs due to excessive static center displacement. In [49], it is shown that the maximum a/t_m ratio that a silicon plate can have is about 35 for entirely linear (elastic) operation in air when no bias is applied. $a/t_m < 35$ corresponds to $k_r a > 1.95$ for a silicon plate.

In order to sample the entire Fourier half-space unambiguously, the center-to-center inter-element spacing must be less than half a wavelength [28, 50]. This requires $k_r a < 1.57$. If the element size is larger and consequently the spacing is more than half a wavelength, the grating lobes of the array emerges and gradually becomes larger [50, 51]. This effect is very significant if the spacing is close to a wavelength. However, grating lobes remain small, comparable to sidelobe levels, for element spacing up to about 90% of the wavelength.

Arrays are often steered in a smaller sector ($-\pi/3$ to $+\pi/3$) instead of the entire half space ($-\pi/2$ to $+\pi/2$), in which case the element spacing can be larger for unambiguous steering performance within the sector [51]. Considering

[1] Appendix A includes more information regarding data sets used in this study.

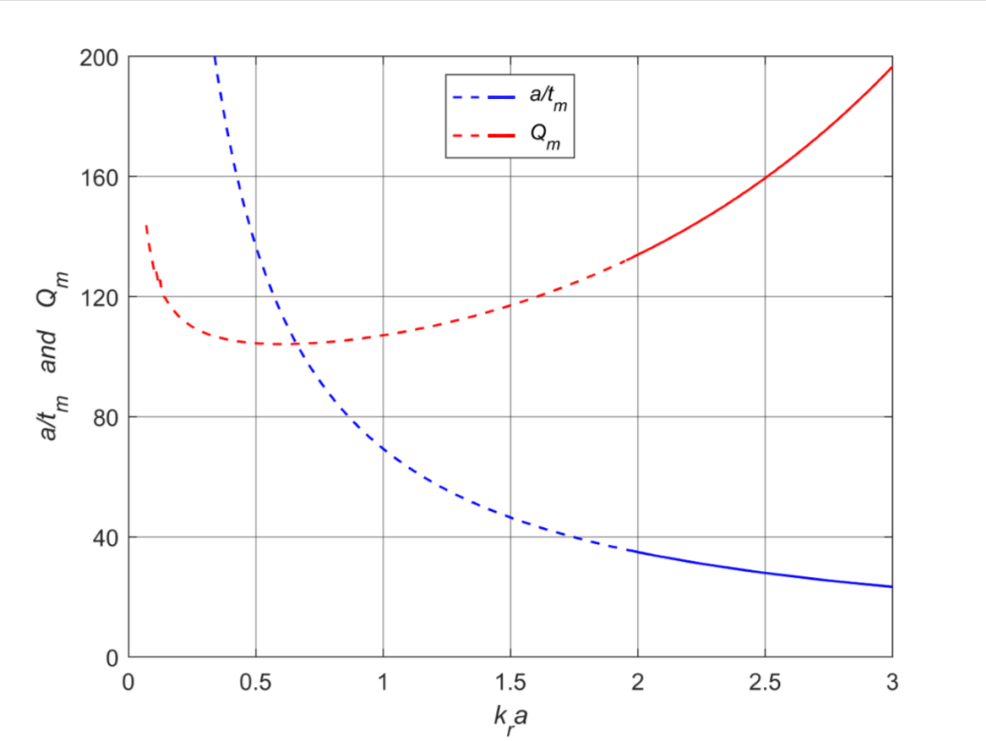


Figure 2.2: Calculated a/t_m and $k_r a$ for an airborne CMUT element

both of these issues, designing an array having elements with $k_r a \approx 2$ secures elastic linear operation for low amplitude vibrations and the resulting element spacing of 65% of a wavelength maintains beam steering in a large sector.

It is accepted that the plate motion is in elastic linear range if the center displacement is less than 20% of the thickness of the plate [52]. It is shown in [37] that CMUT resonance remains in the vicinity of the mechanical resonance frequency determined by compliance (C_{Rm}) and mass (L_{Rm}) of the plate, when driven unbiased. This resonance frequency prevails even at very high dynamic displacement amplitudes, as long as the static center deflection of the plate due to atmospheric pressure is within the linear elastic range. Duffing effect [53] on the resonance frequency due to the stiffening of plate material is overwhelmed by the increased non-linearity in the dynamic transduction force when the vibration amplitude spans the entire gap.

2.3 CMUT array operation

For a CMUT array design, in general, it is essential to study mutual or self-impedance of elements in an array [45]. The elements in an array are coupled at the acoustic terminals through an impedance matrix. Radiation impedance of the *ith* cell can be given as,

$$Z_i = Z_{ii} + \sum_{\substack{j=1 \\ i \neq j}}^{N} \frac{v_j}{v_i} Z_{ij} \tag{2.10}$$

Where, $N = MK$, are number of elements (M and K are rows and columns), v_i and v_j are respective reference velocities, and Z_{ii} is the self-radiation impedance of an *ith* element on an infinitely large rigid plane baffle. The acoustic force F with *rms* velocity v, at the radiation interface of each element can be represented in matrix form for a 2×2 array with,

$$\begin{bmatrix} F_1 \\ F_2 \\ F_3 \\ F_4 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} \tag{2.11}$$

The square matrix, $Z = [Z_{ij}]$ is known as the impedance matrix Z with *ith* and *jth* cells. In this design, we use CMUT array in an unbiased phased configuration. In this configuration, the membrane is biased using stress instead of *dc* voltage. As the force in Eq. 2.11 depends on square of input voltage, the resulting mechanical force term's frequency becomes twice the input *ac* voltage.

$$f_R(t) = \sqrt{5} \frac{C_0 V^2(t)}{2 t_{ge}} g'(\frac{x_P(t)}{t_{ge}}) \tag{2.12}$$

where,

$$g'(u) = \frac{1}{2u} \left(\frac{1}{1-u} - \frac{\tanh(\sqrt{u})}{\sqrt{u}} \right) \tag{2.13}$$

2.4 Large Signal Equivalent Circuit Model

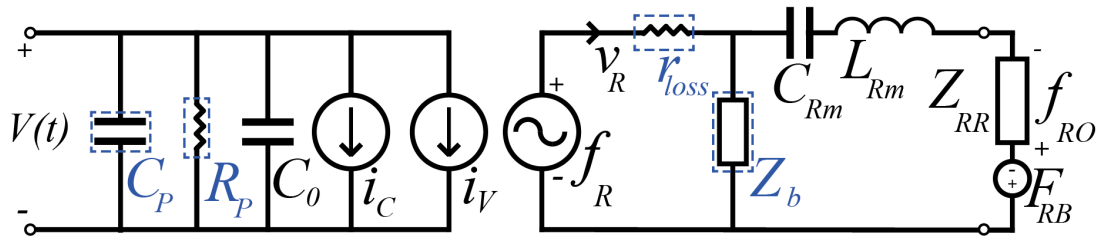


Figure 2.3: Large signal equivalent circuit model. © *2020 IEEE.*

The large-signal equivalent circuit model [38] shown in fig. 2.3 assumes that the plate is rigidly clamped over the edges. The left-hand side of the equivalent circuit represents the electrical side of the circuit, with C_o being the capacitance of the undeflected plate. i_C represents the additional current when the capacitor value is changed because of deflection. i_V is the current arising from the velocity in the mechanical side. The right-hand side is the mechanical section, with C_{Rm} and L_{Rm} representing plate compliance and mass of the plate respectively. v_R is spatial *rms* particle velocity and f_R is the nonlinear voltage-controlled voltage source generating the transduction force.

Z_{RR} is the radiation impedance at the acoustic port. f_{RO} is the transmitted force generated at the acoustic terminal while F_{RB} is the force caused by the static ambient pressure. The model includes the effects of dielectric loss (R_P) and the frictional loss (r_{loss}) and the loss to backing impedance (Z_b) [39, 54]. C_P stands for the parasitic capacitance of the cell. The model parameters are calculated using the following relations [38].

In fig. 2.1 and 2.3, the force term for a pressure P_0 is given as,

$$F_{\mathrm{Rb}} = \frac{\sqrt{5}}{3}\pi a^2 P_0 \tag{2.14}$$

The compliance of the plate is given as,

$$C_{\mathrm{Rm}} = \frac{9}{5}\frac{(1-\sigma^2)a^2}{16\pi Y_0 t_{\mathrm{m}}^3} \tag{2.15}$$

Table 2.1: Circuit Parameters for the Large Signal Equivalent Circuit model

F_{RB}	Force due to Static Ambient Pressure (SAP)
F_{RO}	Transmitted force generated at the acoustic terminal
Z_{RR}	Radiation Impedance
C_{Rm}	Compliance of the plate
L_{Rm}	Mass of the plate
v_r	Spatial *rms* velocity
f_R	Voltage source generating transduction force
i_V	Current due to velocity
i_C	Additional current due to deflection of the plate
C_0	Capacitance of the undeflected plate
Z_B	Backing loss
r_{loss}	Series loss
R_P	Dielectric loss
C_P	Parasitic Capacitance of the cell

where the mass of the plate is,

$$L_{\mathrm{Rm}} = \pi a^2 t_{\mathrm{m}} \rho_{\mathrm{m}} \tag{2.16}$$

The spatial rms particle velocity of the plate is given as,

$$v_{\mathrm{R}}(t) = \frac{\mathrm{d}x_{\mathrm{R}}(t)}{\mathrm{dt}} \tag{2.17}$$

Collapse voltage under external ambient pressure can be written as,

$$\frac{V_{\mathrm{c}}}{V_{\mathrm{r}}} \approx 0.9961 - 1.0468\frac{F_{\mathrm{Pb}}}{F_{\mathrm{Pg}}} + 0.06972\left(\frac{F_{\mathrm{Pb}}}{F_{\mathrm{Pg}}} - 0.25\right)^2 + 0.01148\left(\frac{F_{\mathrm{Pb}}}{F_{\mathrm{Pg}}}\right)^6 \tag{2.18}$$

Where F_{Pg} and F_{Pb} are given as,

$$F_{\mathrm{Pg}} = \frac{t_{\mathrm{ge}}}{5C_{\mathrm{Rm}}} \tag{2.19}$$

$$F_{\mathrm{Pb}} = \frac{1}{3}\pi a^2 P_0 \tag{2.20}$$

The collapse voltage for CMUT under vacuum can be calculated using,

$$V_{\mathrm{r}} = 8\frac{t_{\mathrm{m}}}{a^2} t_{\mathrm{ge}}^{3/2} t_{\mathrm{m}}^{1/2} \sqrt{\frac{27\epsilon_0(1-\sigma^2)}{Y_0}} \tag{2.21}$$

At the collapse voltage, the center displacement X_{Pc} can be given as [39],

$$\frac{X_{\mathrm{Pc}}}{t_{\mathrm{ge}}} \approx 0.4648 + 0.5433\frac{F_{\mathrm{Pb}}}{F_{\mathrm{Pg}}} - 0.01256\left(\frac{F_{\mathrm{Pb}}}{F_{\mathrm{Pg}}} - 0.35\right)^2 + 0.002775\left(\frac{F_{\mathrm{Pb}}}{F_{\mathrm{Pg}}}\right)^9 \quad (2.22)$$

The radiation impedance Z_{RR} is given as [48],

$$Z_{\mathrm{RR}}(ka) = R_{\mathrm{RR}}(ka) + X_{\mathrm{RR}}(ka) \quad (2.23)$$

Here, the radiation reactance and resistance in air are given as, [2]

$$X_{RR}(ka) = \pi a^2 \rho_0 c_0 X_1(ka) \quad (2.24)$$

$$R_{RR}(ka) = \pi a^2 \rho_0 c_0 R_1(ka) \quad (2.25)$$

2.5 CMUT design procedure

The CMUT elements in this study are designed by using the following approach[3],

1. Choosing $k_r a$ and a/t_m as discussed in section 2.2.
2. Determining Q_m for the chosen $k_r a$ using Eq. 2.8.
3. Finding a and t_m for the specified $k_r a$ using Eq. 2.9
4. Finding an optimum t_{ge}/t_m, so that the collapse voltage is less than the insulator breakdown voltage. (Eq. 2.21)
5. Finding F_{Pb}/F_{Pg} using Eq. 2.19 and 2.20. (< 1 for uncollapsed operation)
6. Determining d such that $2a < d < \frac{N-1}{N}\lambda$ [55].

Most of the airborne ultrasonic arrays operate between 30–100 kHz. Our CMUT cells are designed to operate in 70–80 kHz band[4]. For a silicon plate with $k_r a \approx 2.0$

[2]For a clamped plate, $X_1(ka)$ and $R_1(ka)$ are provided in [48].

[3]This process will be iterated in case if the last two conditions are not met.

[4]The attenuation in air is slightly more than 2.2 dB/m at this frequency range, and at SAP (101 kPa), and 20°C [56].

Table 2.2: Material properties and design dimensions

Physical Property	Symbol	Value	Units
Plate Thickness	t_m	40	μm
Gap Height	t_g	10	μm
Plate Radius	a	1.4	mm
Center-to-center Element Pitch	d	3	mm
Insulator Thickness (Al_2O_3)	t_i	100	nm
Young's Modulus (Si)	Y_0	148	GPa
Plate Density (Si)	ρ_m	2370	kg/m^3
Poisson's Ratio (Si)	σ	0.17	
Dielectric constant (Al_2O_3)	ε_r	9.7	

and $a/t_m \approx 35$, a mechanical resonance frequency of about 77.6 kHz is obtained by $t_m = 40\mu m$ and $a = 1.4mm$ using,

$$\omega_r = \frac{t_m}{a^2}\sqrt{\frac{80\ Y_o}{9\ (1-\sigma^2)\rho_m}} \tag{2.26}$$

To maintain the elastic linearity, the center deflection due to atmospheric pressure (X_p) must be less than 8 μm for these design parameters (Table 2.2), i.e., $X_P/t_m < 0.2$ [52]. For $X_p = 6.8\mu m$ at ambient pressure, we choose an equivalent gap height of $t_{ge} = 10.01\mu m$. For these dimensions, driving peak voltage amplitude of approximately 100 V will yield maximum swing without the plate hitting the substrate. The CMUT with these chosen parameters has a collapse voltage in air (V_c) of 250 V and in vacuum of (V_r) of 820 V. The other equivalent circuit model parameters [38] are $C_0 = 5.4pF$, $L_{Rm} = 0.58\mu H$, and $C_{Rm} = 7.2\mu F$.

A large signal equivalent circuit model was defined in Advanced Design Systems (ADS)[5]. This environment is suitable for circuit design owing to its ability to define nonlinear parametric equations in frequency and time domains. The calculated circuit parameters are used in this simulation environment[6] for both single element (Fig. A.1) and 2×2 array (Fig.A.3) to extract the f_r, X_P and other parameters (Fig. A.2).

[5]ADS v2011.10, Keysight Technologies, Santa Rosa, CA, USA

[6]The implementation of the model in ADS is presented in Appendix A.

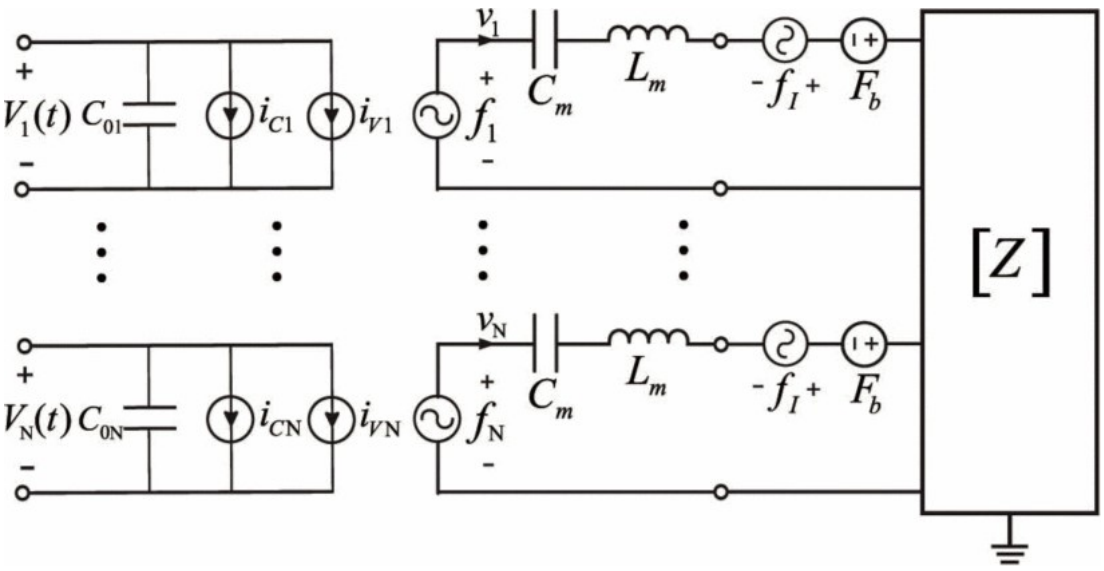


Figure 2.4: Equivalent circuit representation for an N element CMUT array terminated by a Z matrix. © *2013 IEEE* [45].

The equivalent circuit model of an N element array can be developed by combining several equivalent models (Fig. 2.3) with appropriate Z matrix (Fig. 2.4). For a 2×2 array, equivalent circuit model was simulated in ADS, terminated by this impedance matrix [45]. The mutual impedance effects on the array performance are insignificant since the acoustic impedance of air is very small compared to the mechanical branch impedance of the CMUT cells with thicker plates and narrower bandwidth. These simulation will be described further in chapter 4.

2.6 FEA Simulations

ANSYS[7] is used to perform finite element analysis (FEA) for a single CMUT element. Appropriate element type is used as a single CMUT transducer material to perform modal analysis to extract f_r. Fig. 2.5 shows a single CMUT element resonating at 77 kHz. The code for this simulation is provided in Appendix B. Further simulations and comparisons for both circuit modelling and FEA will be presented in chapter 4 with the measurements for comparison.

[7]ANSYS v.14.5, ANSYS Inc., Canonsburg, PA

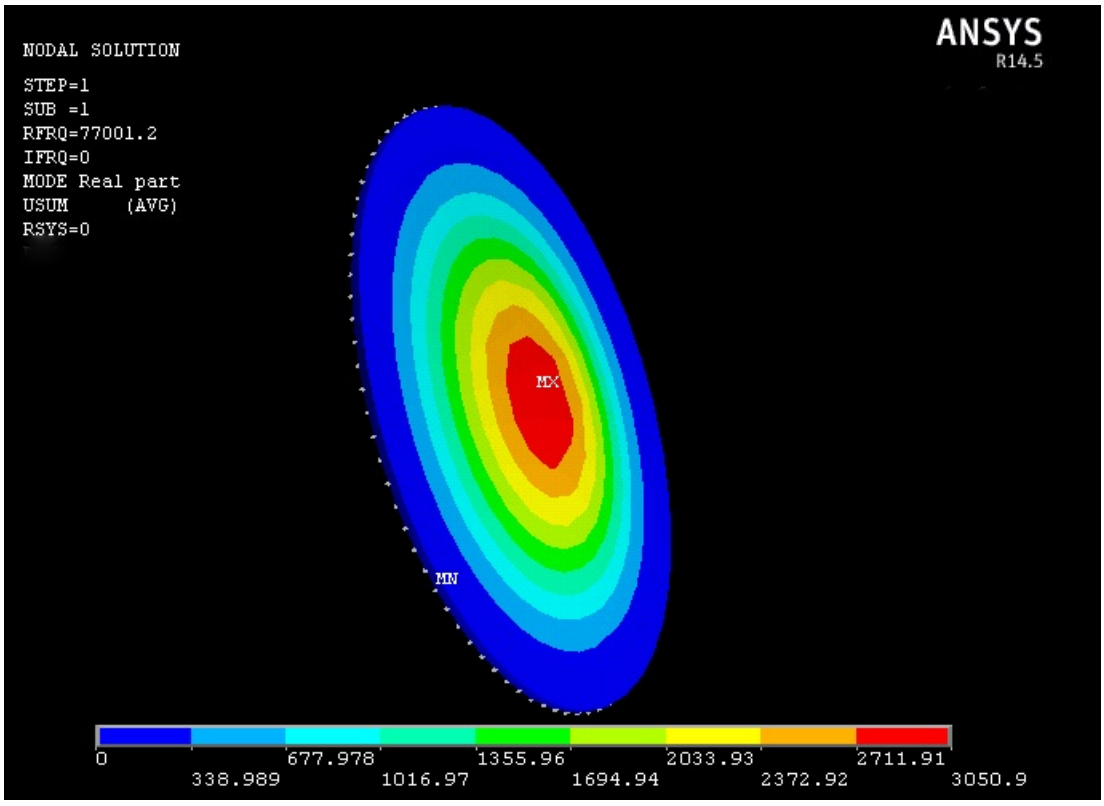


Figure 2.5: Nodal solution of a single CMUT element using ANSYS

Chapter 3

Microfabrication of CMUT arrays

CMUT devices are produced using either of the two major microfabrication approaches; surface micromachining approaches [30, 57, 58], or wafer bonding approaches [39, 59, 60]. In the wafer bonding approach, the gap region of the CMUT devices is microfabricated before the wafer bonding takes place. On the other hand, in the surface micromachining approach a sacrificial layer of material is temporarily deposited in the region that is reserved as a gap region [58]. Once the appropriate processing step is reached, the temporarily deposited sacrificial layer is removed from the reserved gap region to reveal the opening of CMUT arrays. Herein, for the important reasons stated below, wafer bonding approach is considered more advantageous for the production of the CMUT arrays that have large diameter and deep gaps, particularly in this exploratory fabrication:

1. The sacrificial layer release process may require long deposition times for the deposition of the $\approx 10.25\mu m$ thick sacrificial layer,

2. During the deposition process, the relatively thick sacrificial layer may experience permanent residual stresses that may hinder the coming steps of the microfabrication process [61],

3. The sacrificial layer release process may require long wet etching times for the wet etching removal of the sacrificial layer material,

4. The sacrificial layer approach would require critical point drying of the revealed gaps in order to prevent stiction that would happen if natural drying of the remaining liquid inside the revealed gap space is aimed [61].

Section 3.1 will include the microfabrication of the CMUT devices published in [40] and [41]. In section 3.2, we discuss subsequent microfabrication trials.

3.1 Microfabrication Process flow

In our study, we use the wafer bonding approach to develop the CMUT arrays. We developed an integration process flow that can be divided into 4 major segments: Mask design; Pyrex substrate processing; SOI substrate processing; and post-processing.

3.1.1 Mask Design

Following the design process, a single lithography mask was developed in a CAD tool[1] for producing cavities in the Pyrex wafer for arrays in 2×2 , 3×3 (Fig. D.2), 2×8 and 4×4 (Fig. D.3) configurations. Fig. 3.1 shows the full 100-mm mask design. This mask is designed with $50\mu m$ wide connection wires to extend from each individual element to the rim of the wafer with 150×150 μm electrical pads. Course alignment marks are also added to the mask design as the Pyrex wafer will be bonded to SOI wafer after the production (Marked green in Fig. 3.1 and D.1).

[1]LEdit, Layout editor, Tanner EDA, (Tanner Research Inc. USA)

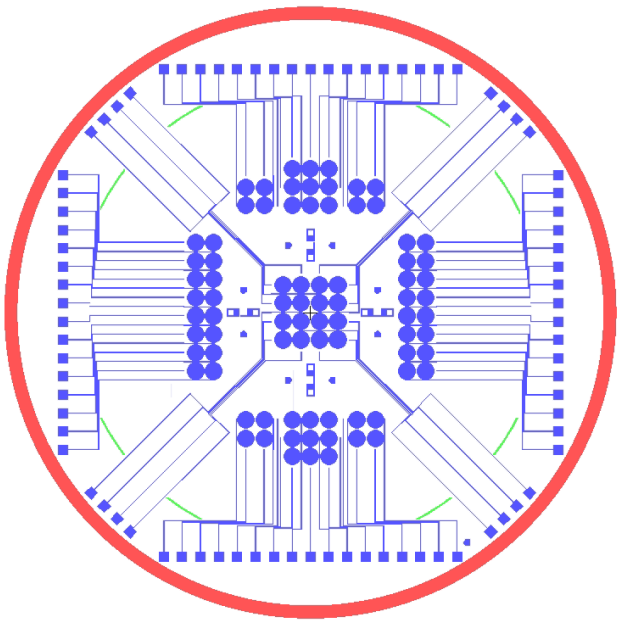


Figure 3.1: 100-mm mask design showing various arrays extended by the electrical wire connections, the green lines are guide marks for wafer bonding between Pyrex and SOI substrates.

3.1.2 Pyrex Substrate Processing

Initially, 100-mm wide and 500 μm thick Pyrex[2] substrates are cleaned from potential organic residues by using Piranha solution followed by DI water rinse before continuing with the remaining cleaning steps. The remaining cleaning steps are done with sonication in acetone, IPA (Isopropyl Alcohol), and DI water respectively. As the final step of the cleaning sequence, the Pyrex substrates are dried by blowing nitrogen gas from a nitrogen gas gun.

After the substrate cleaning, 30 nm thick layer of chromium (Cr) is blanket deposited inside an e-beam evaporator[3] chamber, on the side of the Pyrex wafer that will be used for CMUT gap formation (Fig. 3.2a). There are three main reasons for this 30 nm thick layer of Cr deposition:

[2]Borosilicate, Thickness tolerance=$\pm 25\mu$m, double side polished, 1 Semi flat, MicroChemicals GmbH, Germany (WGS4 0500 250X XXXX SNN1)

[3]Ebeam Evaporator by MIDAS PVD 1eB (Vaksis R&D and Eng., Turkey)

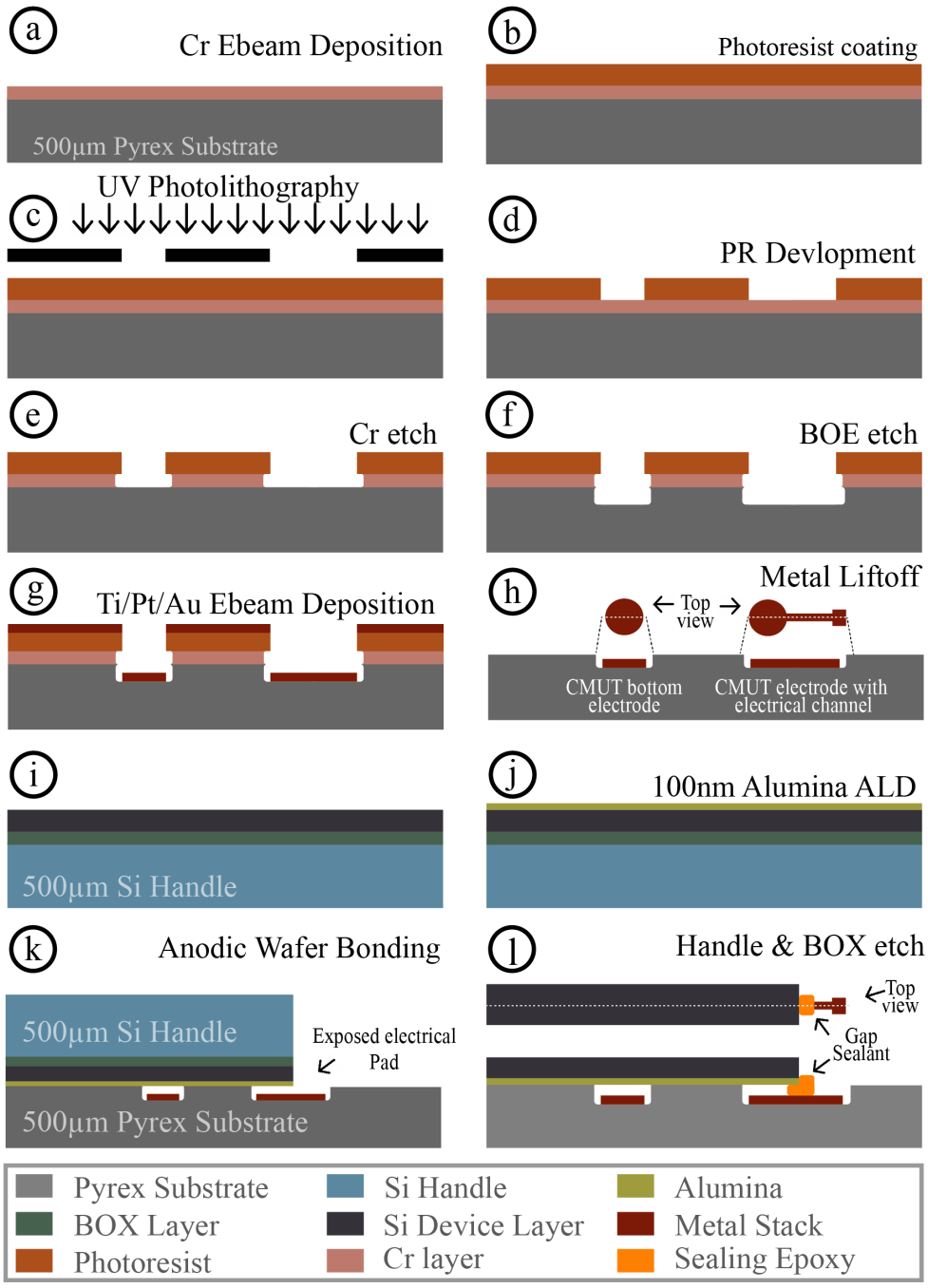


Figure 3.2: Cross-section of the process flow for CMUT fabrication: (a) Cr deposition on Pyrex wafer; (b) PR spin coat; (c) Photolithography; (d) PR development; (e) Cr etch; (f) BOE etch to open cavities; (g) Metal Deposition; (h) Metal Liftoff; (i) Initial SOI wafer; (j) ALD Alumina deposition; (k) Anodic wafer bonding of SOI and Pyrex wafer; (l) Handle and BOX layer etch. © *2020 IEEE.*

1. This Cr layer is used as an adhesion layer between the photoresist and Pyrex surface. Our initial trials with Buffered Oxide Etch (BOE) without this Cr layer caused peeling of the photoresist from the Pyrex substrate surface due to extended BOE etch times. This undesired peeling prevented us from having well defined wet etch profiles for the CMUT array gaps and good boundary for the clamping of the SOI wafer to the Pyrex wafer at these CMUT gap boundaries.

2. Furthermore, this Cr adhesion layer prevented photoresist peeling during photoresist hard baking step that is explained in the upcoming microfabrication steps.

3. This Cr layer is also used as a hard mask in case the thick layer of photoresist mask could not withstand the extended (8.5 hours) wet BOE etch for the formation of the CMUT gaps.

After the deposition of the Cr layer on the device side of the Pyrex wafer, the standard photolithography steps (photoresist spinning, prebake, UV exposure, photoresist development) for the first (and only) photolithographic mask in the entire microfabrication of the CMUT array devices is implemented by using 8µm thick photo resist[4]. (Fig. 3.2 b and c)

For the lithography purpose, HDMS was first deposited (4000 rpm, 2000 acceleration, 50 sec followed by 2 min bake at $90°C$). Photoresist was then spun at 2000 rpm, 1000 acceleration, for 60 sec followed by 50 sec bake at $110°C$. The wafer was then exposed to 100 mJ of energy on Mask aligner[5], followed by 10 mins of development in a developer solution [6]. The wafer is then descumed[7] for 5 mins.

After the development of the photoresist, the photoresist is hard baked at $120°C$ for 1 hour and at $150°C$ for 3 hours to significantly harden the photoresist

[4]AZ4562, MicroChemicals GmbH, Germany
[5]Mask Aligner, 'EVG 620, EV Group E. Thallner GmbH (AT)'
[6]AZ 400K (1:4 H_2O), MicroChemicals GmbH, Germany
[7]DSB6000 Oxygen Asher, Nanoplas, Gilbert Technologies Inc.

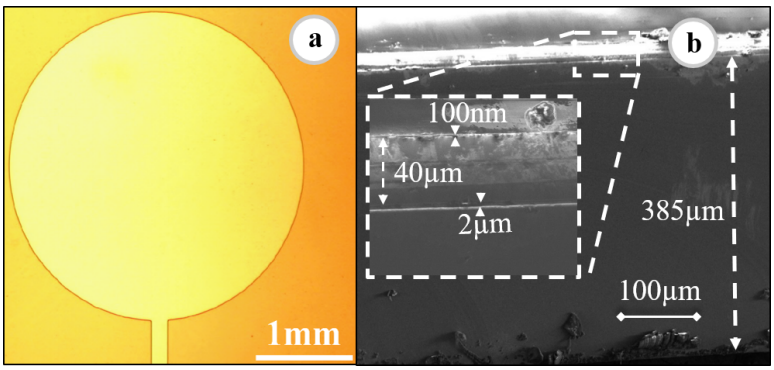


Figure 3.3: (a) Optical Image of a single CMUT element imaged through transparent Pyrex substrate, (b) Cross-sectional SEM of SOI wafer with close up of thin layers in the in-picture. © *2020 IEEE.*

for BOE wet etching process (Fig. 3.2 d). Furthermore, this photoresist hardening process is done in order for the hardened photoresist to withstand the high temperature e-beam evaporation of platinum layer of the Ti/Pt/Au metal stack that is going to be mentioned in the upcoming steps as the bottom electrode of the CMUT array devices.

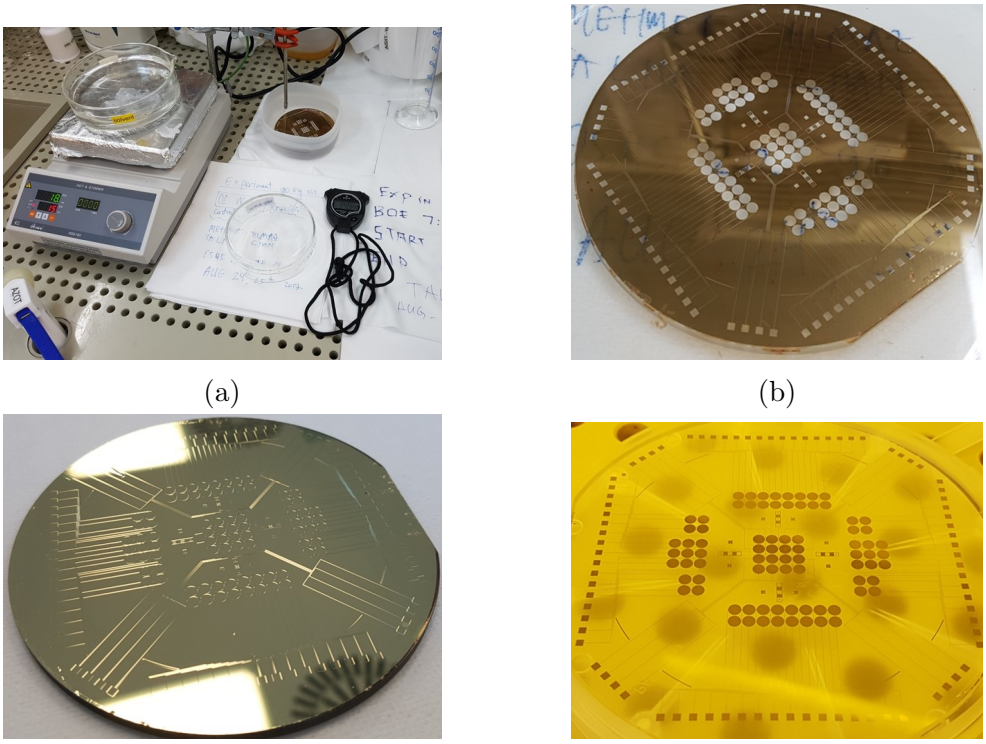
The Pyrex wafer that has the developed and hardened photoresist is then dipped into wet Cr etchant[8] to open the 30nm thick Cr film on top of the Pyrex surface (Fig. 3.2 e).

After the wet Cr etching, the wafer is immersed into BOE solution (Fig. 3.4 a) for a calculated amount of time (8 hours and 23 mins) to achieve an etch depth of $\approx 10.25\mu m$ to form the gap of the CMUT array devices. (Fig. 3.2 f and 3.4 b)

A metal stack of Ti/Pt/Au (100nm/100nm/50nm[9]) is deposited using e-beam evaporation (Fig. 3.2 g and 3.4 c). 100 nm Ti is used as an adhesion layer for Pt film. Ti and Pt film combination is used as a getter material combination [62] during anodic wafer bonding that is going to be mentioned in the upcoming process step. Au was used as conductivity enhancing layer, owing to its low resistivity compared to Ti and Pt, durability and inertness to oxidation.

[8]TechniEtch Cr01, MicroChemicals GmbH, Germany

[9]Ti crucible was placed in pocket 2, Pt was placed in pocket 1 and Au was placed in pocket 3. The input values were Ti-108nm/Pt-122nm/Au-28.82nm. Ti was deposited at 50mA@6kV at 1A/s, Pt was at 340mA@6kV at 1A/s while Au was deposited at 90mA.



(a) (b)

(c) (d)

Figure 3.4: (a) Pyrex wafer submerged inside the BOE solution to etch open cavities, (b) Pyrex wafer after the cavities have been etched to desired thickness, (c) Metallization of the Pyrex wafer, and (d) Pyrex Substrate with electrodes deposited into the cavities after the liftoff process

Since acetone or photoresist removers would be very slow removers during photoresist removal of the significantly hardened photoresist, freshly prepared Piranha solution[10] is used to etch the extremely hardened photoresist (Fig. 3.2 h and Fig. 3.4 c) from the earlier undercut region that was formed during the extended BOE wet etch (Fig. 3.2 f). In other words, the Ti/Pt/Au metal stack on the hardened photoresist is lifted off from the wafer surface while the Ti/Pt/Au metal stack inside the etched gap regions remains to form the bottom electrode of the CMUT array devices (Fig. 3.2 h and 3.3 a).

After the removal of the photoresist and metals that were on top of the photoresist layer, the Cr layer below the photoresist is revealed. Cr etchant is then

[10] H_2SO_4:H_2O_2 3:1. 30% H_2O_2 is poured slowly into conc. H_2SO_4

used to remove Cr from the entire Pyrex wafer surface. Each cavity is then optically[11] observed for defects, and then characterized using Stylus profilometer[12] to verify the depth of the cavity after metal deposition (Fig. D.4). Long wet etch process extended radius a by $25 \pm 2\mu m$ that was verified using stylus profilometer.

At this stage, the processing on the Pyrex wafer is completed, and the Pyrex wafer is ready for anodic wafer bonding part of the microfabrication integration process (Fig. 3.4 d). Next major segment of process steps involves processing of SOI wafers for anodic bonding.

3.1.3 SOI Substrate Processing

100-mm diameter SOI[13] wafers with $40\mu m \pm 0.5\mu m$ thickness of Si device layer, $2\mu m \pm 5\%$ thickness of BOX (Buried Oxide) layer and $385\mu m \pm 15\mu m$ thickness of handle layer are cleaned with freshly prepared Piranha solution for potential organic residues on the SOI substrate surfaces (Fig. 3.2i).

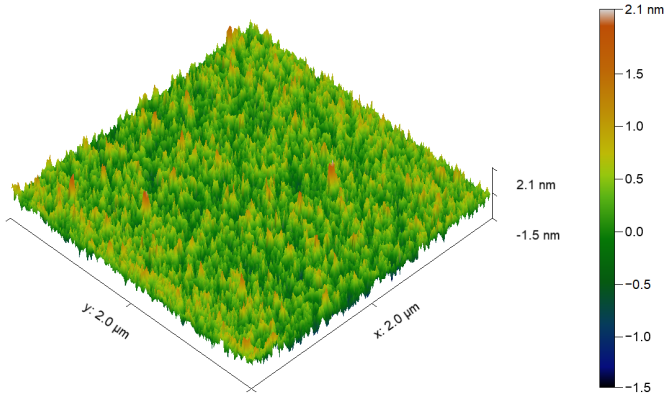


Figure 3.5: AFM measurement for the topographic profile of ALD deposited Alumina layer.

100 nm thick alumina layer (Al_2O_3) was deposited on device side of the SOI

[11]Optical Microscope, ZEISS Axio Vert.A1, Carl Zeiss Microscopy GmbH, 07745 Jena, Germany

[12]Stylus Profilometer, P6, KLA Technology, CA, USA

[13]Silicon-On-Insulator, p-type (B) (100), device $\rho < 0.0015\Omega cm$, Handle $\rho = 1 - 30\Omega cm$, Lot # 4-9975,UD-12797/UH-12802, Ultrasil Corp, USA (25/05/2018)

wafer using atomic layer deposition[14] (ALD) process (Fig. 3.2j). The ALD recipe is provided in Table E.1. Cross sectional SEM[15] image of the SOI wafer is shown in Fig. 3.3 b. An ellispometric measurement[16] was also performed to verify the thickness of the deposited layer. To check if the surface quality requirements of anodic wafer bonding is met, atomic force microscopy[17] (AFM) measurement on the ALD deposited alumina surface is performed (Fig 3.5). The measurement showed that the average surface roughness of the ALD deposited surface is 0.2 nm (Fig. D.5 and D.6). This measurement depicted sufficient surface roughness value for anodic wafer bonding process.

To reduce the lithography related processes and simplify the integration process, the SOI wafers were then diced[18] into 76mm by 76mm square shaped wafers. After the processing of SOI wafers is also competed, both Pyrex and SOI wafers are bonded to each other by using the anodic wafer bonding service of EVG[19] (Fig. 3.2k).

The wafer pairs, *F21* and *F24* both include one Pyrex and one SOI substrate each. Wafer *F21* is shown with Pyrex stacked on top of SOI wafer before being sent for bonding in fig. 3.6. EVG reported no major warpage or bow observation during their initial topography measurements [20].

The anodic bonding process involves wafer cleaning[21] followed by mechanically alligning and bonding them in the wafer bonder[22]. Wafers are heated and a mechanical force is applied at top and bottom side of the wafer pair. Voltage bias is applied to the wafer pair, with cathode at the Pyrex side and anode at the Si side. During this process, Na^+ and O^- ions form a depletion layer near the

[14] ALD Savannah, Cambridge Nanotech Inc, USA
[15] SEM, Quanta 200, FEI Company, Hillsboro, OR, USA
[16] FS-1 Multi-Wavelength Ellipsometer, Film Sense LLC, Lincoln NE, USA
[17] MFP-3D, 'Oxford Instruments Asylum Research Inc. Santa Barbara, CA, USA
[18] Dicing Saw DAD3220, Disco tech, Japan
[19] EV Group E. Thallner GmbH, Austria. Sent 27/08/18 and received 24/09/18. P180455
[20] The wafer bow reported by EVG before the bonding process F21 Pyrex ($24\mu m$), SOI ($36.4\mu m$) and F24 Pyrex ($11.5\mu m$), SOI ($35\mu m$).
[21] EVG 301, semi-automated wafer cleaning system, EV Group E. Thallner GmbH, Austria
[22] EVG 520IS 200mm semi-automated wafer bonding system, EV Group E. Thallner GmbH, Austria

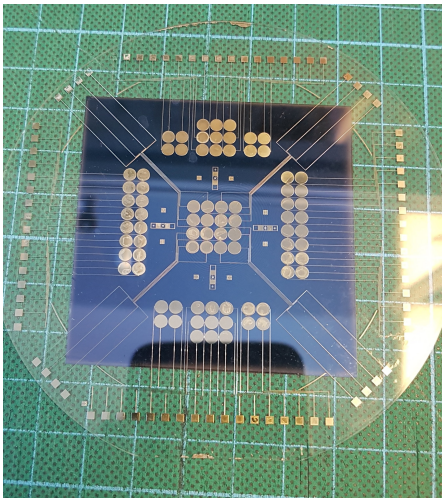


Figure 3.6: Square SOI and round Pyrex wafer stacked on top of each other before the wafer bonding process.

Glass/Si interface. This process is concluded with a topographic measurement[23] on both wafers. The bonding process was successful with some bond voids at various locations that were not close to metallized regions. The bonding process effected the metal quality, where a visible change in metal color was observed after the bonding process.

3.1.4 Post-processing

After the 100-mm diameter circular shaped Pyrex substrate, and 76mm by 76mm square shaped SOI wafer are safely bonded to each other, all the circular CMUT array gaps, and significant portion of the Ti/Pt/Au metal stack that is used for electrical wiring and base electrode formation is now under the ALD alumina coated SOI wafer, and still inside the BOE etched Pyrex channels. However, the electrical connection pads of the individual CMUT array elements (Fig. 3.2 k) are purposefully not left under the SOI wafer and are easily accessible to allow external electrical connections (Fig. D.8).

After anodic wafer bonding, the CMUT gaps of all the CMUT array elements

[23]The wafer bow reported by EVG after the bonding process F21 Pyrex (15.5μm), SOI (10.8μm) and F24 Pyrex (50.2μm), SOI (29.2μm).

are covered by the SOI wafer, however, the gaps are still at atmospheric pressure because the channels inside the Pyrex wafers are still not sealed at the entrance areas of the wiring channels (Fig. 3.2 k).

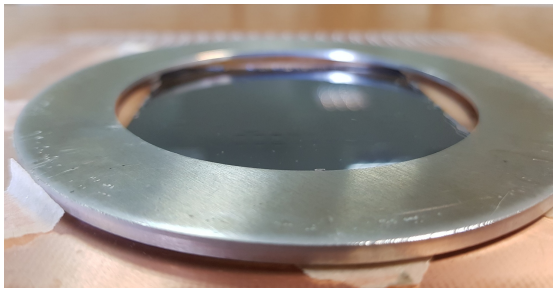


Figure 3.7: The donut shaped Al mask clamped on top of the CMUT wafer

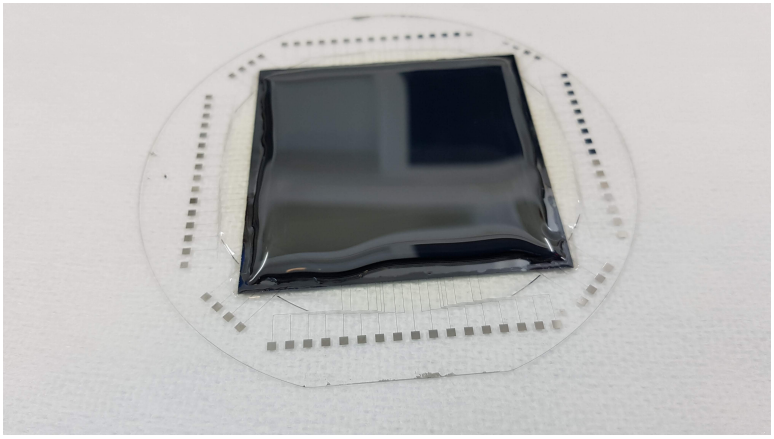


Figure 3.8: BOE carefully spread on the BOX layer of the SOI wafer using a pipette.

Before proceeding with further post-processing steps, the entrances of the wiring channels are manually sealed using a low viscosity epoxy resin[24]. Then, the wafers are placed into a vacuum chamber (2.5×10^{-7} Torr) for over 15 hours to remove air from the cavities while partially curing the low viscosity epoxy resin (Fig. D.10). After the gaps beneath the radiation plates are vacuumed, the wafers are immediately transferred to an oven for hard curing of the epoxy at $120°C$ for 6 hours (Fig. 3.2 l).

After the sealing and gap vacuuming steps, a custom-made shadow mask (Fig. 3.7) was attached to the top of the 100-mm diameter Pyrex substrate to mask

[24]10g of Biresin CR120 epoxy-resin & 3g of CH120 Hardener(Haufler composites, DE)

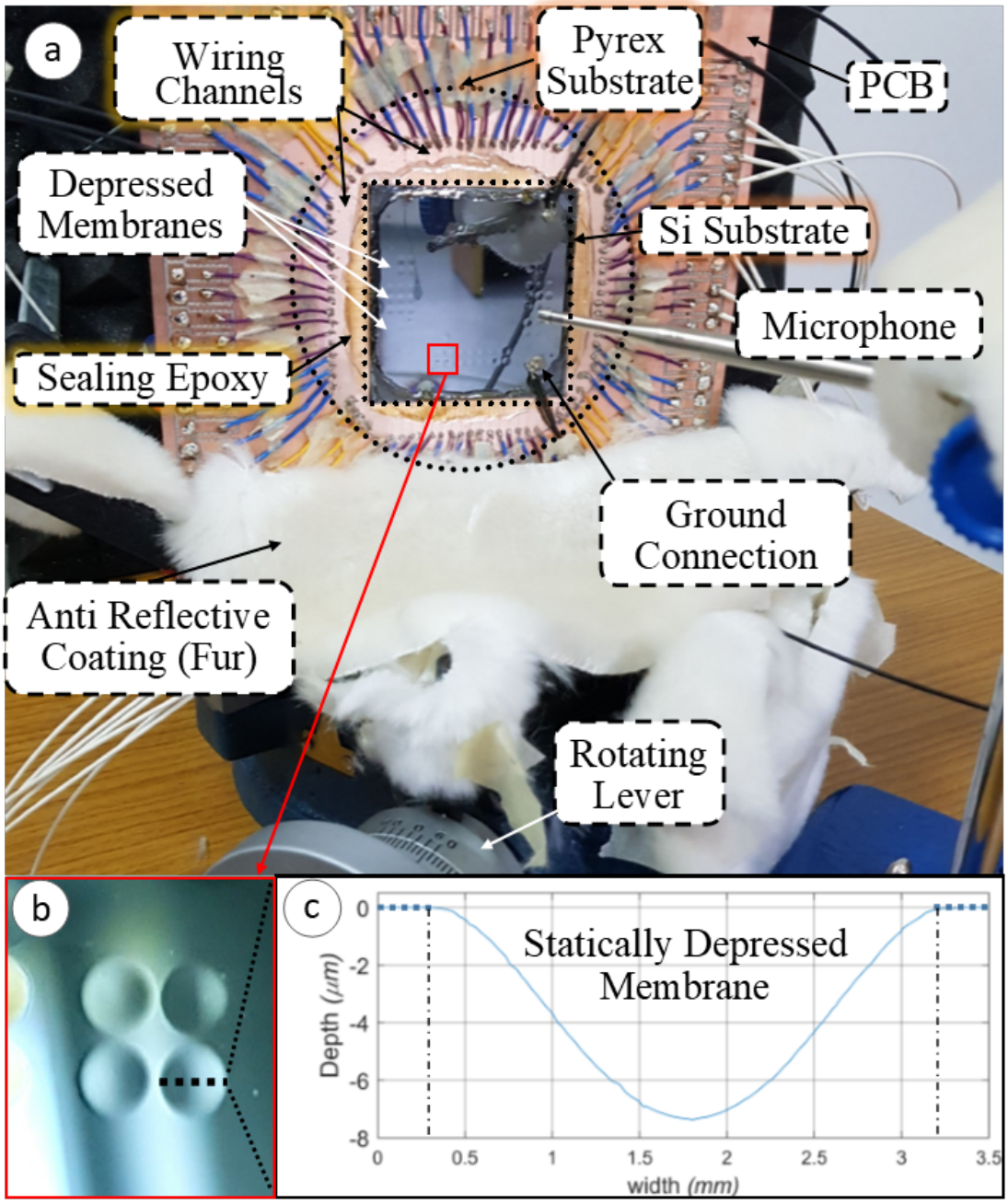


Figure 3.9: (a) CMUT array mounted onto a rotating stage. The stage as well as the microphone mounting stand are covered in ARC to absorb reflections. Both microphone and substrate are placed farther away to avoid reflecting planes. (b) Close up image of a CMUT array displaying depressed CMUT membranes. (c) Stylus profile of a statically depressed CMUT membrane.

the exposed electrodes, leaving only the handle layer of the SOI wafer available for Si reactive ion etching (RIE). SF_6 and Ar gas based RIE recipe was used in an ICP chamber[25] to isotopically dry etch the handle layer (Fig. D.9). The RIE recipe is tabulated in Table E.2. The recipe was carefully customized to account for the non-uniformity of the ICP process as it etches the edges of the handle layer faster than the center (Fig. D.11). After removal of the handle layer, 2 μm thick BOX layer is wet etched using BOE (Fig. 3.8) to reveal the device layer of the SOI wafer which forms the vibrating plates of the CMUT array devices (Fig. 3.2l). After 35 mins of wet etch, the BOE was removed and DI water was spread on top of the wafer to remove the remnant BOE.

After removal of the stiff handle and BOX layers, as the gaps between the Si device layer and Pyrex are already sealed, the Si device layer is visibly depressed under static atmospheric pressure. In order to quantify the depression depth of the CMUT plates, a stylus[26] and optical profilometer[27] was used to measure the surface profile of the depressed CMUT plate. Stylus profilometer measurements displayed on average, 7 µm depression, at the central point of each CMUT plate across the wafer (Fig. 3.9 b and c).

A PCB is used to map out electrical connections from the Pyrex wafer (Fig. 3.9 a). Electrical wire connections are made using a conductive silver epoxy[28] on the wafer side[29], while the wires are soldered onto the pads on the PCB. A ground connection is manually[30] added to the silicon plate layer using the conductive epoxy.

All 2×2, 3×3 and 2×8 array membranes are statically depressed. 4×4 array membranes are not depressed which is verified using Stylus measurements. After this step, both wafer pairs, *F21* and *F24* are now ready to be characterized. Measurements and design validation for these wafers will be discussed in chapter 4.

[25]ICP 615 (Si) (Surface Technology Systems, UK)
[26]Stylus Profilometer, DektakXT, Bruker Nano Surfaces Division, Tucson, AZ · USA'
[27]NewView 7200, Zygo Corporation, Middlefield, CT 06455, USA
[28]Silver conductive 402 2.5g TwinPak, Resin Technology group, LLC, Waston, MA, USA
[29]The silver epoxy was left in a chamber for 4 hours at $60°C$
[30]The Si surface is scratched using sand paper, immediately followed by application of epoxy.

3.2 Additional fabrication runs

Before the microfabrication process described in section 3.1, there were several microfabrication trials including received arrays [63, 64] and other fabrication runs. Following sections will discuss these fabrication runs.

3.2.1 Airborne Receiver Arrays

A microfabrication process for developing collapsed mode CMUT receiver elements was established for optimization of maximum off-resonance sensitivity. This process was essentially optimized into the process described earlier in section 3.1. Receiver CMUTs design process included 4 groups of CMUTs characterized as A1, A2 and A3 and arrays (Fig. 3.10). Following text will discuss the major differences/issues between the two processes.

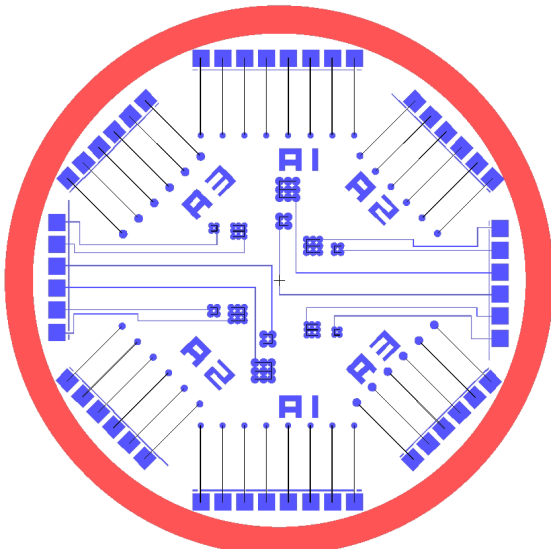


Figure 3.10: Mask design for CMUT receiver element and arrays for Pyrex cavity production. The outer red ring has a diameter of 100-mm.

For the receiver project, 3.3 mm thick Pyrex was used. We faced several issues with metallization inside the Pyrex cavities to form the bottom electrode. As *Pt* is a high melting point metal, the temperature inside the ebeam evaporation chamber increases significantly. This leads to deterioration of the photoresist,

and hence the metal is poorly lifted off (Fig. 3.11). This deterioration increased the diameter of the electrodes and produced metals that were causing short connection between the cavity and Pyrex surface. To overcome this issue we added two more unit processes:

1. We introduced a *Cr* sacrificial layer on top of the Pyrex wafer and underneath the photoresist. This ensures cavity feature to stay consistent in size and shape.

2. We divided the overall deposition time for Pt into smaller sections of 15 mins each, hence allowing it to cool down between each run.

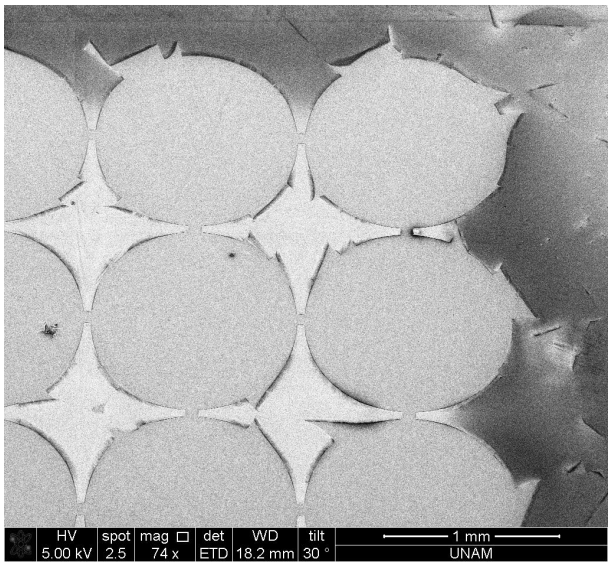


Figure 3.11: SEM image of an unsuccessful liftoff process. The metal was deformed producing abrupt edges and enlarged radius.

The receiver mask design includes a SOI wafer that was diced into an octagonal shape, as shown in Fig. 3.12. Coarse alignment marks between CMUTs and outer electrical connections were added to aid the wafer bonding process (Figure D.7). The alignment marks were introduced to allow the usage of circular, square or octagonal shaped 76 mm wide wafers. After the wafer bonding process, the collapse radius for each element was determined using stylus measurements. The CMUT wafer was attached directly to a ceramic slab without a PCB.

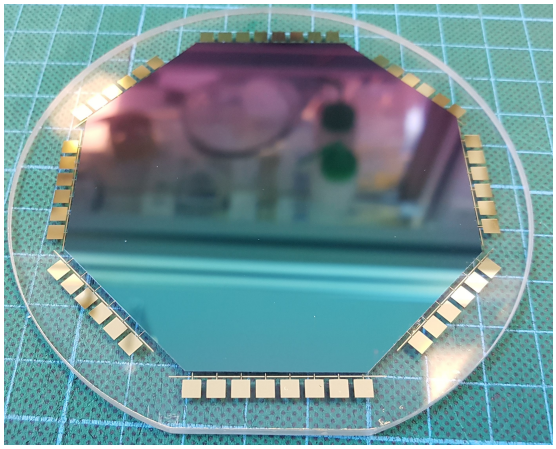


Figure 3.12: Receiver CMUT with octagonal SOI substrate on top of the round Pyrex wafer.

3.2.2 Characterization of Alumina layer

A set of microfabrication and measurement procedure is adapted to characterize the Alumina (Al_2O3) layer deposited using the ALD process. A single lithography mask is designed to produce various sizes of metal contact pads (Figure 3.13). The process is given as follows,

1. Highly conductive Si wafer (500 μm thick) was cleaned using piranha solution.
2. 100 nm thick Alumina was deposited using an ALD recipe (Table E.1).
3. Photolithography using a PR[31] is performed to produce electric pads.
4. Ti/Pt/Au (20nm/20nm/50nm) is deposited on top of the Pyrex wafer using thermal evaporator[32].
5. Metal Liftoff using acetone/IPA/DI water.

After the production, at first the CV measurements were made to extract ϵ_r for ALD deposited Al_2O3. A probe station with SCS[33] system was used for

[31] 1.4 μm AZ 5214E, MicroChemicals GmbH, Germany
[32] MIDAS PVD3T, Vaksis R&D and Eng., Turkey
[33] 4200-SCS Semiconductor Characterization System, Keithley Instruments, Inc., Ohio, USA

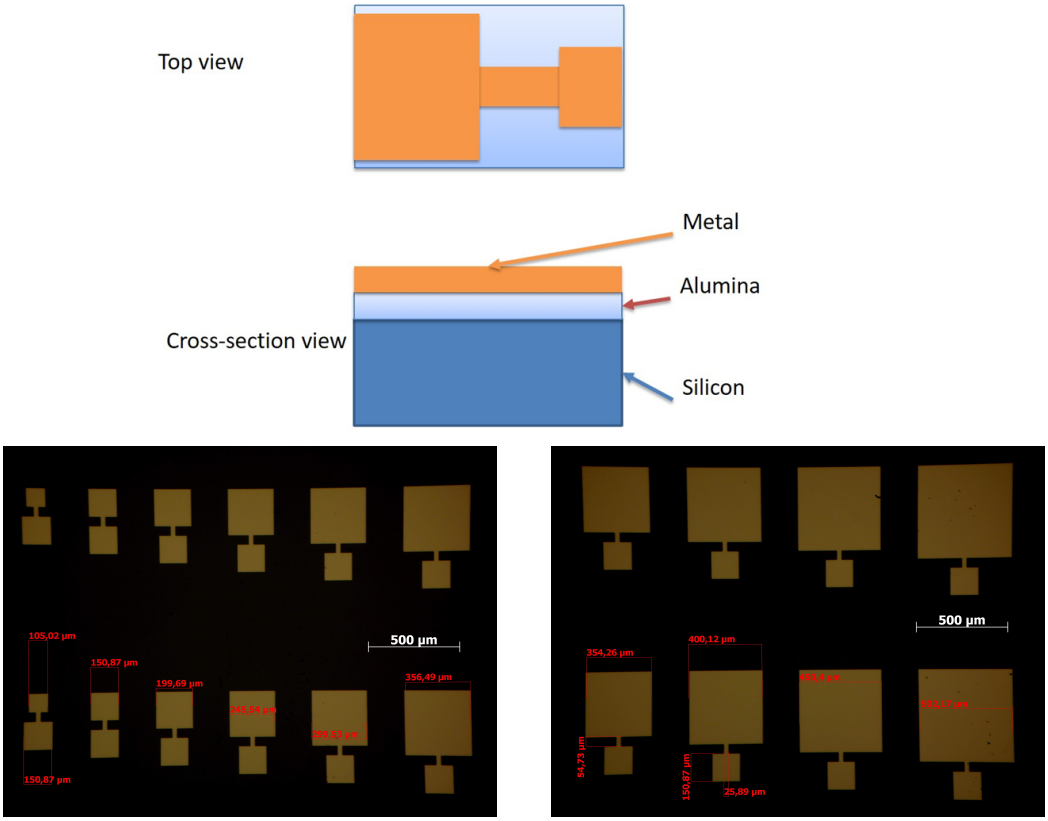


Figure 3.13: Electrical pads for Alumina layer characterization. (Top) Top and Cross-sectional view of the test chip. (Bottom) Optical image of top views of the test chip.

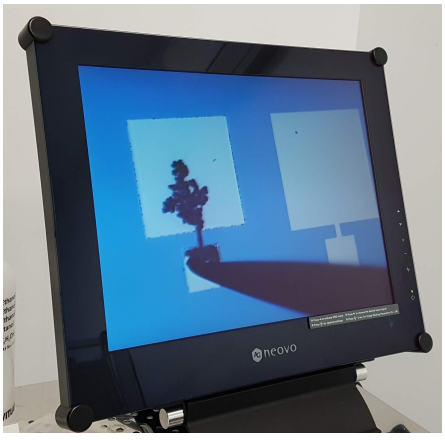


Figure 3.14: Optical image of electrical pads after the insulator broke down.

this purpose. On average, the measurement was $\epsilon_r = 9.7$. Secondly, destructive testing is made using a *dc* sweep to measure the breakdown voltage of the Al_2O_3. The voltage is swept in a controlled manner until the insulator broke (Fig 3.14). The breakdown voltage for Al_2O_3 on average was 0.65 V/nm. Extracted material parameters will be used in the design validation discussed in chapter 4.

3.2.3 Unsuccessful microfabrication trials

In this section, we will discuss unsuccessful microfabrication trails preceding the microfabrication discussed in section 3.1. These are categorized as following.

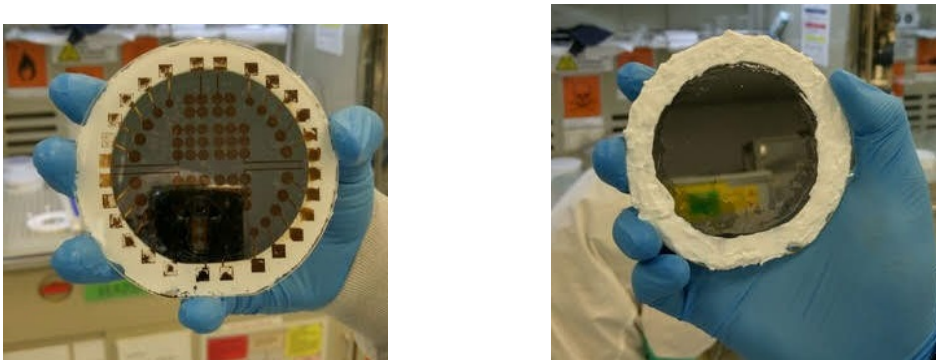
1. Bonding thick SiO_2 on SOI with Pyrex wafer.
2. Thinning thick Si wafer using a CMP process.
3. Handle Layer removal using TMAH and $HF : HNO_3$.
4. Unsuccessful wafer-bonding process resulting in deformation of Si surface.

The CMUT design described in chapter 2 can be used to produce CMUTs with different material parameters. Due to limited availability of SOI wafer stock, we initiated the production with an SOI wafer with $6\mu m$ thick BOX layer and $6\mu m$ thick thermally grown oxide on top of Si. The anodic bonding process depends on achieving a large electrostatic force at the silicon - glass interface in order to achieve anodization of the silicon bonding surface. As the oxide thickness increases there is a corresponding increase in voltage drop across the oxide which consequentially reduces the electrostatic field at the interface. This process was aborted as it was incompatible with the wafer bonder at AML[34].

To overcome this issue, a thick (800 μm), highly conductive, Si wafer was chosen. The Si wafer was thinned using a CMP[35] process. The resulting wafer

[34]AML – Wafer Bonding Machines & Services, Applied Microengineering Limited, Oxfordshire, UK

[35]Chemical Mechanical Polishing using Multiprep polishing system, Allied High tech Products Inc., Rancho Dominguez, CA, USA



(a) (b)

Figure 3.15: CMUT substrate imaged after the wafer thinning process. (a) Backside of Pyrex substrate, the leakage of TMAH inside the sealing epoxy has damaged the metallic electrodes and (b) Front side of the wafer pair with exposed Pyrex surface covered using epoxy while Si surface is exposed.

surface roughness was not compatible for the wafer bonding processes.

During the next wafer process development, ICP tool was unavailable for handle layer etching for some period of time. As an alternate, we choose to use wet etch using *TMAH*. Wafer pairs *F3* and *F5* were coated with a thick non-conductive epoxy on the edges and then placed into a single side etch tool. Although the TMAH etched Si handle layer at $80°C$, but due to a significant leakage into the sealed epoxy layer, the process was discontinued (Fig 3.15). A similar process was performed using: (1) $HF : HNO_3 : H_2O$ and (2) $HF : HNO_3 : CH_3COOH$. (1) was extremely slow for the thinning process. (2) was slightly better than former but didn't provide excellent surface quality.

Another wafer pair (*F13* and *F16*) with thick Si wafer and 2 μm of thermally grown oxide layer were produced. During the wafer bonding process, one of the wafer was damaged and was unusable (Fig. 3.16), while the other was partially functional. An RIE process (Table E.2) was used to thin the thick Si wafer to the desired membrane thickness of 80 μm (Fig. 3.17). This was partially achieved as the RIE process was non-uniform and there was a thickness variation between the elements. The non-uniformity across the wafer and roughness (2-5 μm) of the surface increased the resonance to 180 kHz with multiple conductance peaks.

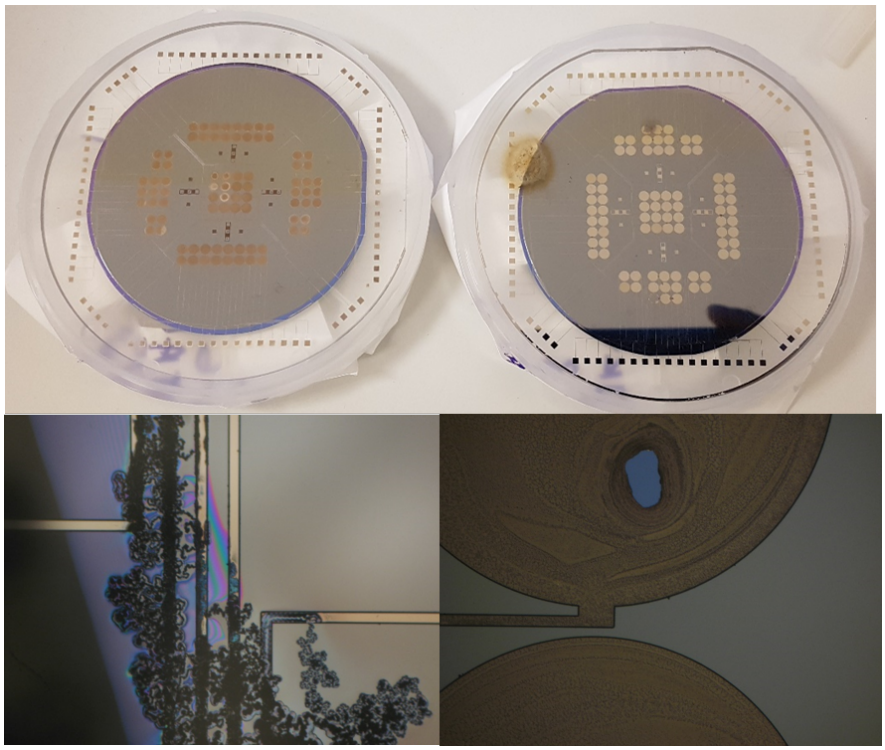
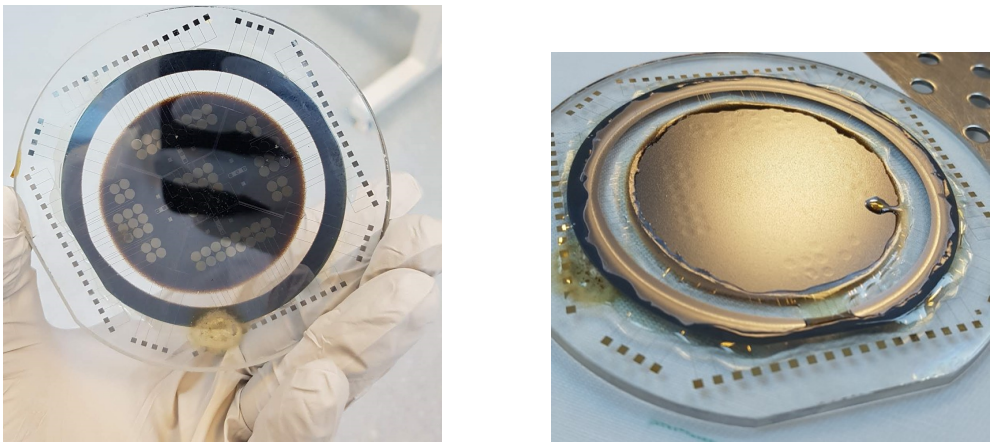


Figure 3.16: Damaged CMUT substrates, F13 and F16, after the bonding process. (Above) Metal deterioration is visible as the metallic color has now change into bluish shade. A golden colored damaged area is also observed. (Below) Metal is seen missing or roughened after the bonding process



(a) (b)

Figure 3.17: CMUT substrate imaged after the wafer thinning process. (a) Backside of Pyrex and (b) Front side of Pyrex wafer.

Chapter 4

Measurements and Model Verification

In this chapter, at first, we discuss the characterization of the microfabricated CMUT arrays using impedance measurements. A large-signal equivalent circuit model is used to validate these results. In addition to this, the design and measured results are compared. Following this, we will discuss pressure measurements and compensation of element pressure in arrays with beam steering measurements.

4.1 Impedance measurements of cells and arrays

The CMUT elements are characterized by measuring the input impedance using an impedance/gain-phase analyzer[1]. The top electrode is connected to a common ground, while the bottom electrode is biased (Fig. 4.1). The measurement is performed by sweeping the voltage bias ± 20 V with 5 V steps at an *ac* drive of 0.5 V. Long integration mode with a high averaging number was used. The

[1]HP4194A, Hewlett-Packard, Palo Alto, CA

measurements are performed in following configuration.

1. Individual element measurement in array with other elements shorted to the Ground. (Figure 4.1 a)

2. Array measurement with all elements biased in parallel with each other. (Figure 4.1 b)

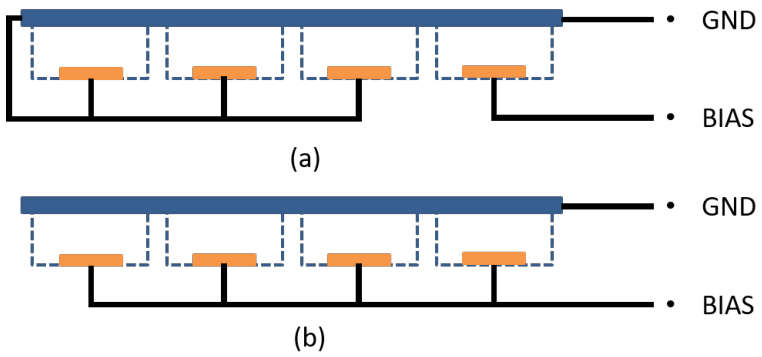


Figure 4.1: Configuration for impedance measurement of a single cell and array.

Fig 4.2 and 4.3 show an overview map of these measurement showing operational, short and deflated CMUT elements in both CMUT wafers. Fig 4.4 shows conductance measurement for each element in array S1 in wafer F21. It is observed that the resonant frequency (f_r) has shifted and is not the same for each element. For all the measured elements, 2% dispersion in resonance frequency is observed.[2]

One important thing to note here is that the conductance curves are symmetric along the zero bias which is indicative that the charge on the CMUT radiation plate is insignificant [65]. If the insulator is charged, the unbiased operation of CMUT elements is not possible. Additionally, as the electric field is alternating, the unbiased operation doesn't induce charging in the insulator layer. As Array S1 and N2 are the only arrays with all elements operational, only these two will be discussed in detail.

[2]The impedance measurements for other elements and arrays are provided in section D.2

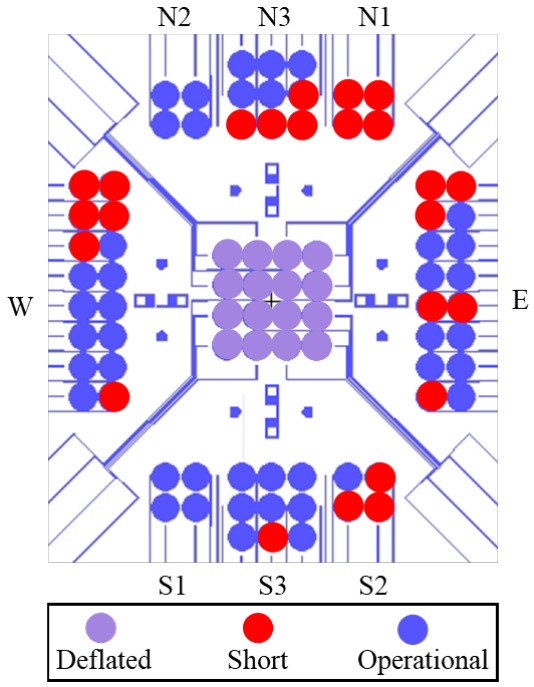


Figure 4.2: Mapped elements of CMUT wafer F21 with short, deflated and operational CMUT elements.

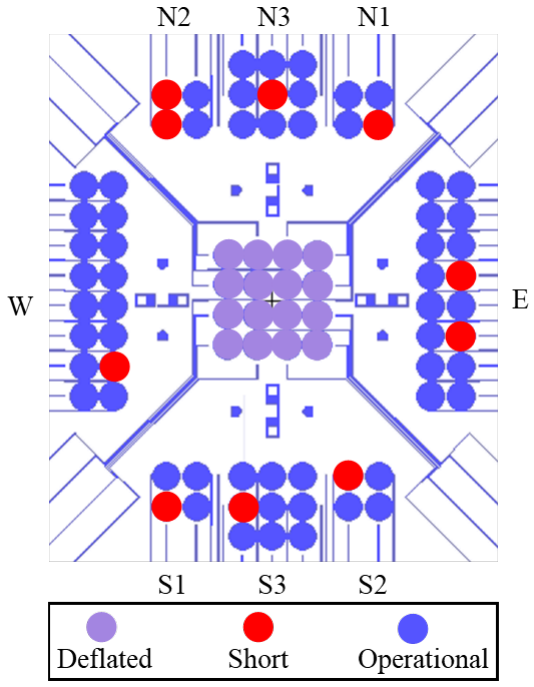


Figure 4.3: Mapped elements of CMUT wafer F24 with short, deflated and operational CMUT elements.

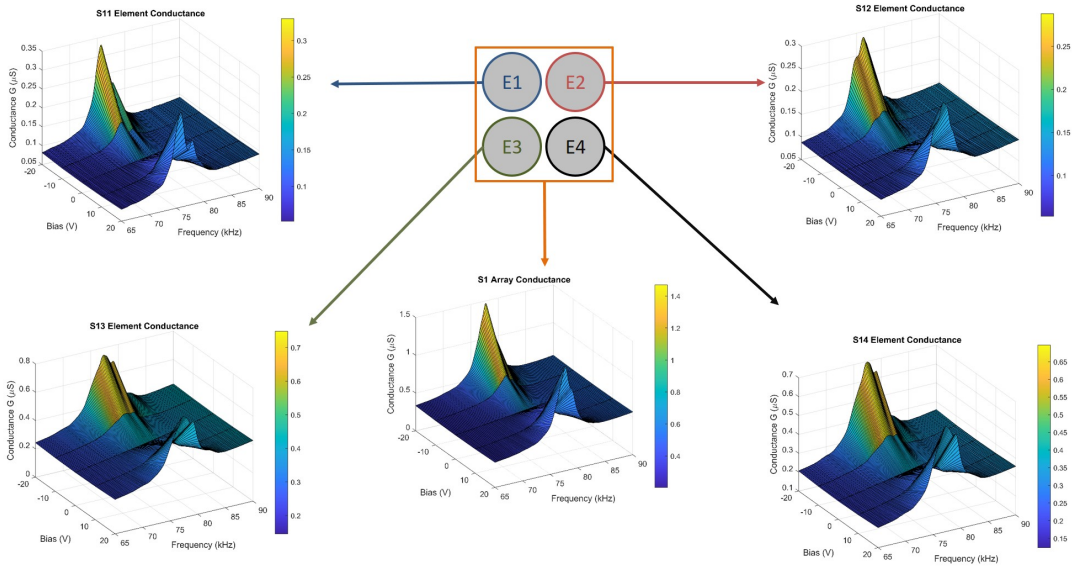


Figure 4.4: Conductance curves for Array S1 in Wafer F21.

4.1.1 Tuning Circuit model in ADS

As described in chapter 2, the model can be used to account for various losses that could occur due to different fabrication inaccuracies. We compensated for these discrepancies as described below. Each element in arrays are accounted for on individual basis. This process is described as following:

1. Resonance Frequency:

   Mechanical resonance frequency is dependent on spring softening resulting from bias, a, t_m and material constants (Eq. 2.26). These materials constants are widely used in the literature for single crystal silicon substrate. These constants are representative and can vary between different substrates. The most significant effect on the f_R is due to variation in a and t_m. Variation in a between samples is optically measured, while the variation in t_m is hard to estimate although cross-sectional image of the CMUT is used to measure it from a single edge (Fig. 3.3). Hence tuning the t_m with measured a is appropriate. For an element in array S1, $t_m = 40.84\mu m$ and a of 1.41 mm is used. The spring softening affects the peak conductance level, and will be discussed towards the end of this process.

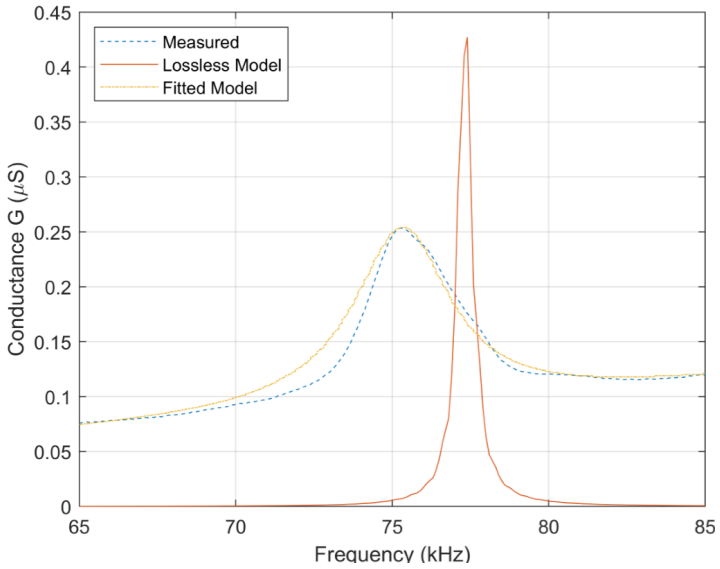


Figure 4.5: Comparison between lossless, measured and model-fitted single element CMUT conductance curves.

2. Conductance Baseline:

   The conductance baseline demonstrated in the impedance measurements in fig. 4.4 is shifted because of dielectric loss of the alumina insulator layer. The dissipation/loss factor $\tan(\delta)$ can be calculated using conductance measurement as,

   $$G = \omega C_i \tan(\delta) \tag{4.1}$$

   where insulator capacitance is $C_i = \epsilon_0 \epsilon_r \pi a^2 / t_i$. Dielectric loss, R_P is given as,

   $$R_P = \frac{1}{\omega C_{eff} \tan(\delta)} \tag{4.2}$$

   C_{eff} can be calculated using admittance measurement using,

   $$jB = j\omega C_{eff} \tag{4.3}$$

   where, $C_{eff} = C_P + C_O$. A loss tangent of 0.00014 was calculated on the average.

3. Losses and Bandwidth:

   The vibration of the radiation plates excites waves in the silicon plate at the clamped edge, and in the substrate [39]. This energy manifests itself

as loss and contributes to the enlargement of the bandwidth. This loss is modelled as a parallel impedance Z_B (Fig. 2.3). Energy loss due to trapped air in the gap is not expected to be significant. The static depression of the plate in each cell, depicted in Fig. 3.9, are in agreement with the design, which verifies that the vacuum seal is good.

The calculated quality factor together with measured conductance peaks can be used to account for losses in the elements [39]. The relation can be given as,

$$\frac{Q_{simulated}}{Q_{measured}} = \frac{R_{rr} + r_{loss}}{R_{rr}} \tag{4.4}$$

$r_{loss} = 2.21\pi a^2 \rho_0 c_0$, parasitic capacitance, C_P, is 1.76 times C_0 is calculated using the measurements.

4. Conductance Peak:

   The peak value of the conductance can be compensated by varying the t_{ge}. This doesn't result in a major shift in f_R. Here it should be noted that this value of t_{ge} and t_m are not necessarily the actual values, but its combination with CMUT dimension and assumed material parameters can be used to predict accurate CMUT transmission performance parameters [39].

   Using this technique, we are able to tune the circuit elements. Model fitting for a single element *S31* and Array *S1* are shown in Figure 4.5 and Figure 4.6, respectively. Model fitting for all elements in array S1 are shown in Figure D.20.

4.1.2 Discussions

The variations in the radius of the gap due to extended BOE etch lowers the resonance frequency by 1.8% on the average with some dispersion. Furthermore, the vibration of the radiation plates excites waves in the silicon plate at the clamped edge, and in the substrate [39]. This energy manifests itself as loss and contributes to the enlargement of the bandwidth. Table 4.1 shows a comparison between resonance frequency response obtained using circuit model, FEA and

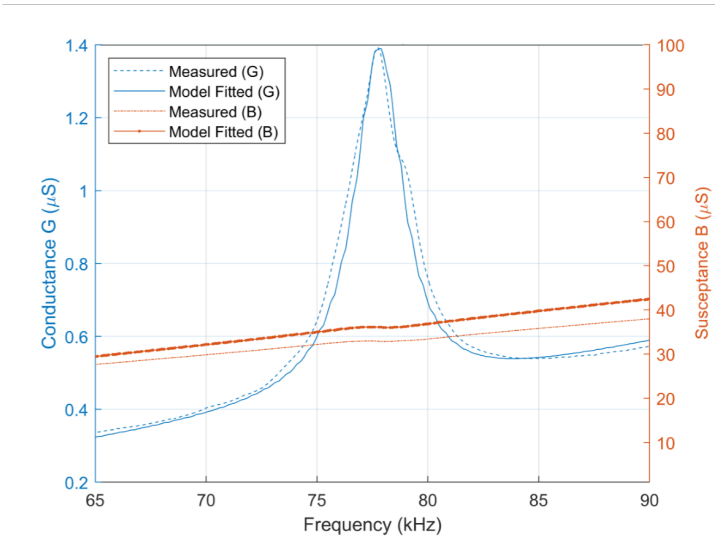


Figure 4.6: Comparison between measured and model-fitted 2×2 CMUT array conductance and susceptance curves.

average measurements. The obtained response is very close to circuit modeling and FEA.

Table 4.1: Resonance frequency obtained via Circuit Modelling, FEA and measurement

	Circuit Model	FEA	Measurement (Avg.)
Resonance frequency (f_r)	77.6 kHz	77 kHz	76 kHz

4.2 Pressure Measurements

4.2.1 Pressure and Directivity Calculation

Pressure field, p, for a clamped plate CMUT array, with N elements, located on an infinite rigid baffle, can be calculated using the equation [45].

$$p\left(r,\theta,\varphi\right) = j\frac{\rho_m c_0 k_r\ \pi a^2}{2\pi} D(\theta) \sum_{i=1}^{N} U_{R_i} \frac{e^{-jk_r r_i}}{r_i} \tag{4.5}$$

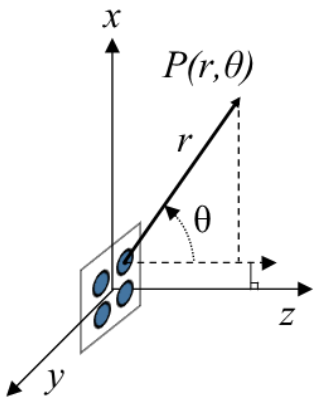


Figure 4.7: A planar array consisting of M rows and K columns with 2 elements each.

where,

$$D(\theta) = \frac{48\ J_3(k_r a \sin\theta)}{(k_r a\ sin\theta)^3} \tag{4.6}$$

is the pressure directivity pattern of a CMUT cell [66]. Here J_3 is the Bessel function of the 3^{rd} kind, U_{Ri} is the rms velocity phasor at the surface of the i^{th} cell. r_i is the radial distance of the element to the observation point in a medium. The pressure for a single element measured at a specific distance can be used to calculate the pressure at the surface of the transducer.

The directivity pattern for a 2-dimentional array can be written as [67, 55],

$$Dp\,(\theta,\phi) = \frac{\sin\{(Mk_r d_m/2)\sin\theta\cos\phi\}\sin\{(Kk_r d_K/2)\sin\theta\sin\phi\}}{M\sin\{(k_r d_m/2)\sin\theta\cos\phi\}K\sin\{(k_r d_K/2)\sin\theta\sin\phi\}} \tag{4.7}$$

As the measurements are taken in the x-z plane, ϕ becomes zero. In far field of the array, θ, for a single element CMUT becomes congruent to that of an array (Fig. 4.7). For a 2×2 array, directivity pattern, $D_p(\theta)$, can be written as,

$$D_p\,(\theta) = \frac{\sin\{(k_r d)\sin\theta\}}{4\sin\{(k_r d/2)\sin\theta\}} \tag{4.8}$$

Dashed lines in Fig. 4.8 shows normalized directivity patterns calculated using the $M = K = 2$ and $d_m = d_K = 3mm$ with design parameters provide in Table 2.2.

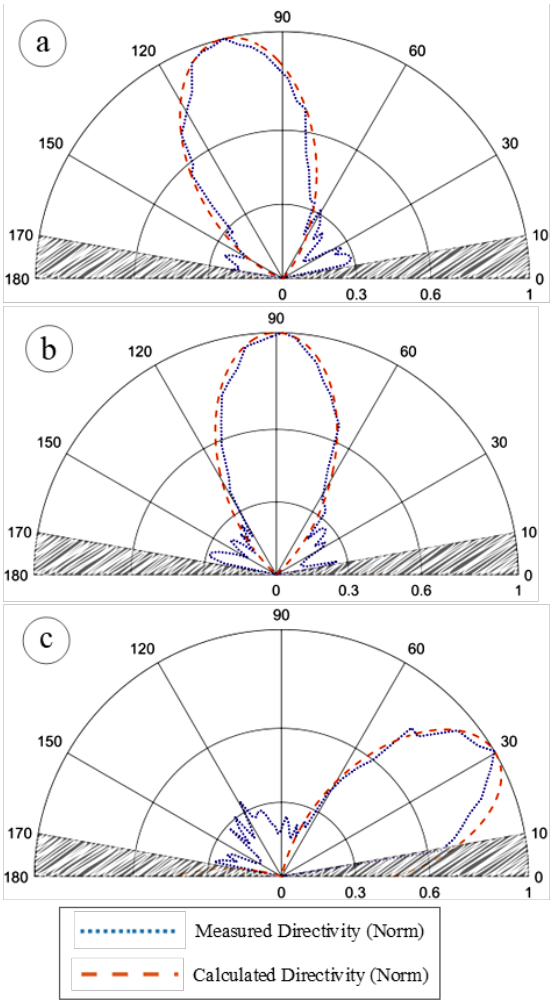


Figure 4.8: Calculated and measured directivity (normalized) for a 2×2 CMUT array in the x-z plane. (a) beam steered at 105^o, (b) 90^o and (c) 30^o with respect to the surface of CMUT array.

4.2.2 Measurement Setup

A set of measurements are performed to record *rms* pressure of each CMUT element. The CMUT elements are individually driven using a Digital to Analogue (D/A) converter[3] in a pulsed configuration (Fig. 4.9). The pulses can be varied by using a DAQ interface in LabView[4].

[3]PXI-6733 card, NI PXIe-1073 Chassis, National Instruments, USA

[4]NI Laboratory Virtual Instrument Engineering Workbench (LabView), v2016, National instruments Corp., TX, USA

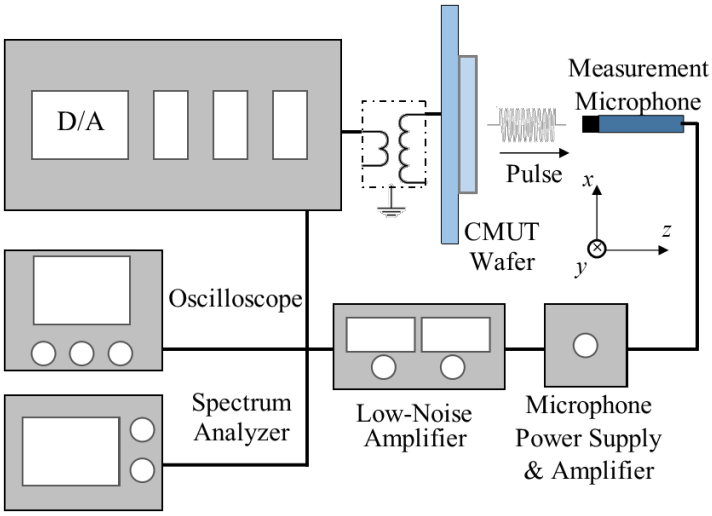


Figure 4.9: Block diagram for pressure measurements of a CMUT transmit array. CMUT array is laid in 3-dimensional space in a rigid baffle. Measurements are performed in x-z plane. In the far field, the measurement angle θ becomes congruent to the array.

A measurement microphone[5] is used to measure the radiated pressure. The dynamic range (3% THD) of this microphone is between 52.2 dB and 168 dB SPL [68, 69] the upper limit of which is well above the measured pressure levels in this work. The microphone is mounted on a preamplifier[6] using an adaptor[7] and placed at the principal axis of the array at 15 cm distance.

The microphone output is fed to a low noise amplifier[8]. The measurements were recorded in a laboratory environment where the relative humidity of 52% and temperature of 20^oC was observed throughout the whole measurement process.

The capacitance of the microphone is provided as 3.2 pF. The measurement setup is calibrated from the 1/4 inch adaptor to the spectrum analyzer, using a balanced voltage source (1 mV_{rms}) with a capacitor (3.3 pF).

The output pressure is measured separately using D/A, spectrum analyzer[9],

[5]pressure-field microphone, B&K 4138, Bruel and Kjaer, Naerum, Denmark
[6]B&K 2633, Bruel and Kjaer, Naerum, Denmark
[7]B&K UA 160, Bruel and Kjaer, Naerum, Denmark
[8]10 - 100 kHz bandpass filter with 6 dB roll-off, SR560, Stanford Research Systems, Sunnyvale, CA
[9]HP8590l, Hewlett-Packard, Palo Alto, CA

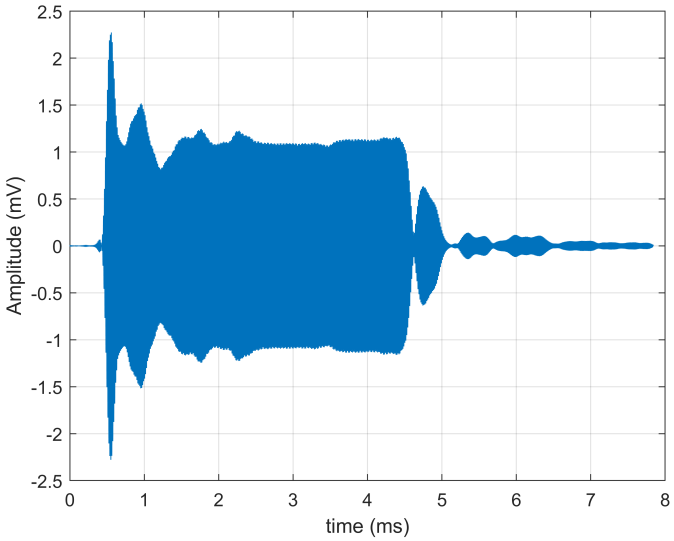


Figure 4.10: A long pulse transmitted using a 2×2 CMUT array at 77.6 kHz.

and oscilloscope[10]. The LabView environment[11] capable of producing the pulses is also programmed to record these pulses from the measurement microphone. The *rms* pressure for a time signal produced using a *4 ms* long pulse and *1 second* repetition rate is obtained using an oscilloscope (Fig. 4.10). The pressure is estimated from the amplitude at the latter part of the long pulse waveform after the transients are decayed.

Although the time signal can be recorded using all three equipment mentioned earlier, but the oscilloscope is used to record measurements to avoid aliasing in the measurements owing to its high sampling rate. For these measurement, pulse duration of 1.3 ms, 2.7 ms, 4 ms, 5.3 ms and 6.7 ms are used. It was observed that pulse duration below 4 ms was not sufficient to make the measurement as the transients do not decay in time. The pressure measurements in the upcoming sections are recorded with a pulse duration of 4 ms. Various measurement waveforms that are taken at frequencies on and off resonance and with different applied voltage and time periods are shown in Appendix D.

[10]DSO1002A, Agilent, Keysight Technologies, USA
[11]LabView VI implementation is described in Appendix C

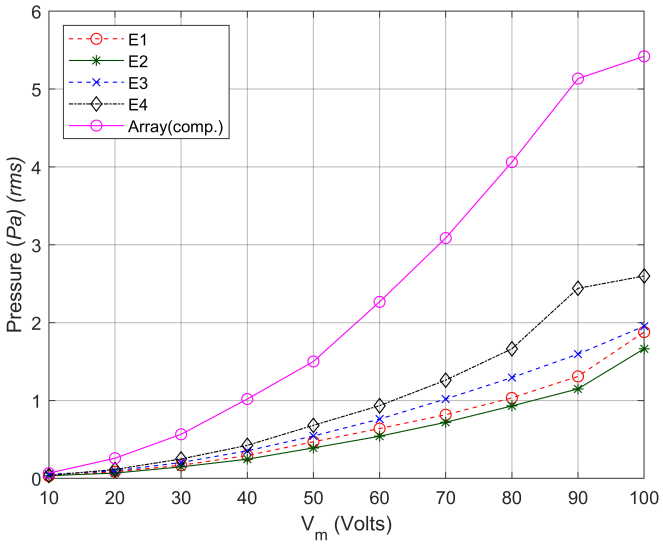


Figure 4.11: Measurement pressures of elements of a 2x2 array (E1, E2, E3 and E4) and the compensated array at 15 cm on the array axis obtained by a measurement microphone. The element pressure curves are used as calibration to obtain equalized element output pressures necessary for compensation of array S1 driven at 76 kHz. The horizontal axis is respective drive voltage amplitudes for each element in element pressure measurements and drive voltage amplitude of E2 for compensated array pressure measurement. The other elements in array pressure measurement are driven by compensated voltage amplitude and phases given in Table 4.2.

4.2.2.1 Results and Discussions

Both arrays, S1 and N2, are operated at different frequencies by sweeping applied voltage between 10-100V. Measured output pressure for each element of the array S1 individually operated at 76 kHz and 77.6 kHz are shown in Fig. 4.11 and 4.12. Additionally, this array is also operated at 75.8 kHz, 77.63 kHz and the mean of these pressures are plotted in Fig. 4.13. Array N2 is operated at same frequencies, and a comparison between both of these arrays are shown in Fig. 4.14.

For array S1, it is observed that the element E2 is the least sensitive element, while E4 is the most sensitive element. It is noted that the pressure for E4 saturates after 80 V. This is observed because at high voltage, the oscillating plate starts hitting the bottom electrode, and increasing the voltage beyond this

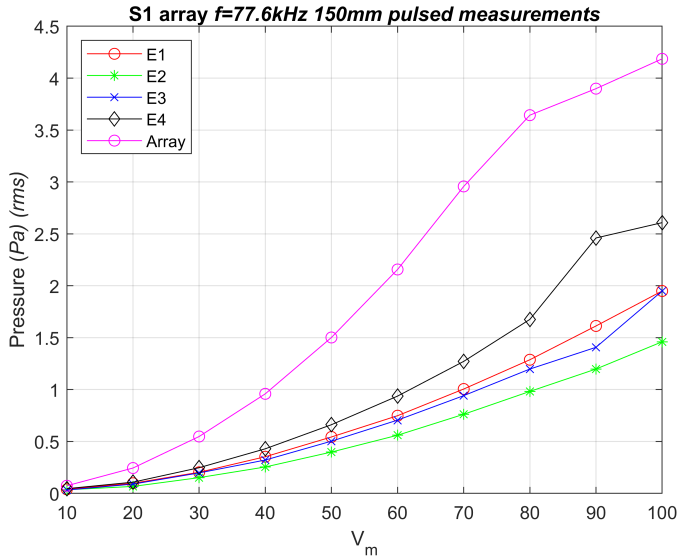


Figure 4.12: Measurement pressures of elements of a 2x2 array (E1, E2, E3 and E4) and the compensated array at 15 cm on the array axis obtained by a measurement microphone. The element pressure curves are used as calibration to obtain equalized element output pressures necessary for compensation of array S1 driven at 77.6 kHz.

point yields no effect.

As observed by the impedance measurement of elements in array N2, the elements are more lossy in comparison with array S1. For N2, the least sensitive element is E3 that saturates at 50 V, producing significantly low output pressure in comparison with array S1. These differences are due to fabrication inaccuracies discussed in section 3.1.

In addition to this, pressure measurements using spectrum analyzer also display a second harmonic which was 28 dB lower than the resonance (Figure 4.15). It should be noted that these harmonics only appear for some elements and that too at high voltages ($> 130V$). As our CMUT elements operate below 100V, this doesn't affect the performance of the array.

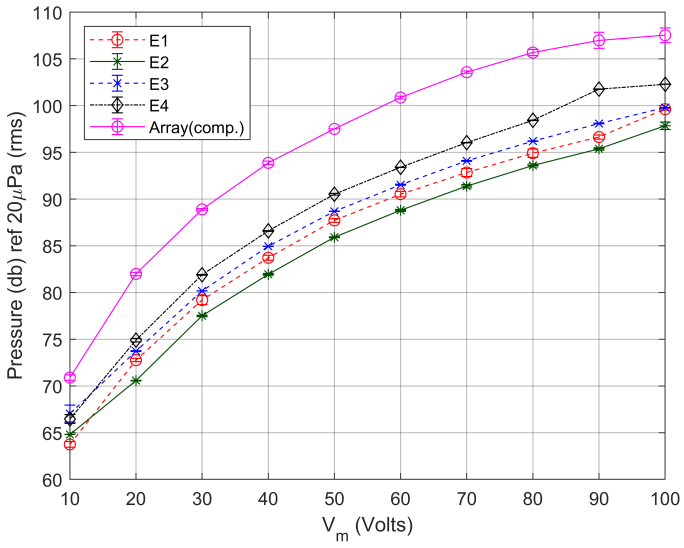


Figure 4.13: Mean of pressure measurements at a distance of 15cm for a 2×2 compensated array and its elements driven at 75.8 kHz, 76 kHz, 77.6 kHz and 78 kHz on the array axis obtained by a measurement microphone. The parallel bars show the standard deviation of pressure variation at different frequencies, which is very low below 80V. © *2020 IEEE.*

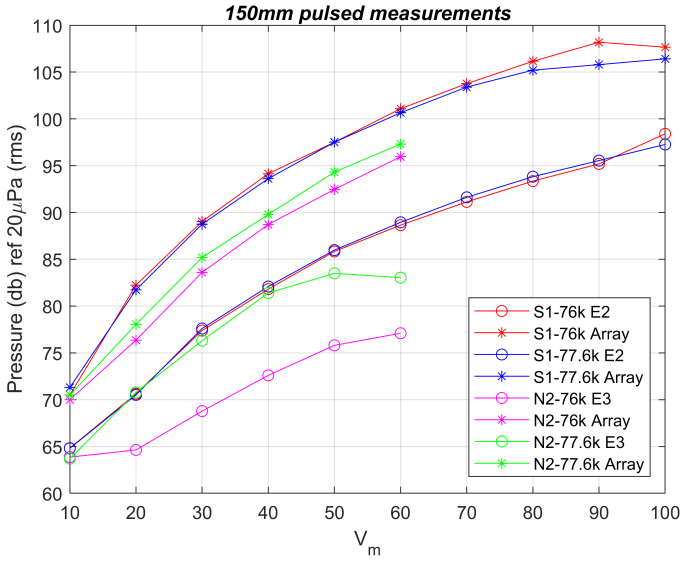


Figure 4.14: Pressure obtained by the least sensitive element and compensated array for S1 and N2 driven at 76 kHz, 77.6 kHz.

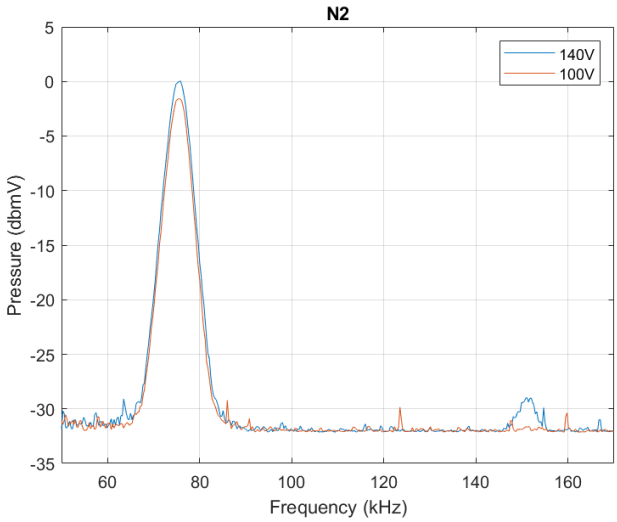


Figure 4.15: Pressure measurement of array N2 at high drive voltages.

4.2.3 Array Compensation

The CMUT elements are designed for maximum output pressure when driven unbiased at half frequency using the equivalent circuit model. Maximum pressure is obtained when the membrane swings the entire gap height, t_g, which is achieved with a minimum drive voltage amplitude at the membrane's mechanical resonance frequency. The model is modified to accommodate the deviations in dimensions and losses incurred during production and used to predict the transmit performance and drive voltage at which each cell can be operated to provide the largest possible swing.

Due to the dispersion in resonance frequencies, as discussed in earlier section, not all of the array elements can be operated at same frequency to obtain a maximum pressure (Fig. D.19 and D.20). For beam steering, it is crucial to have the same amount of pressure with controlled phase radiated from each element in an array. Owing to this requirement, compensation is necessary for both phase and amplitude of the output pressure of CMUT elements in an array.

When simulating the modified model of array S1 for peak center displacement x_p, it is observed that each element provides a different peak deflection for a fixed

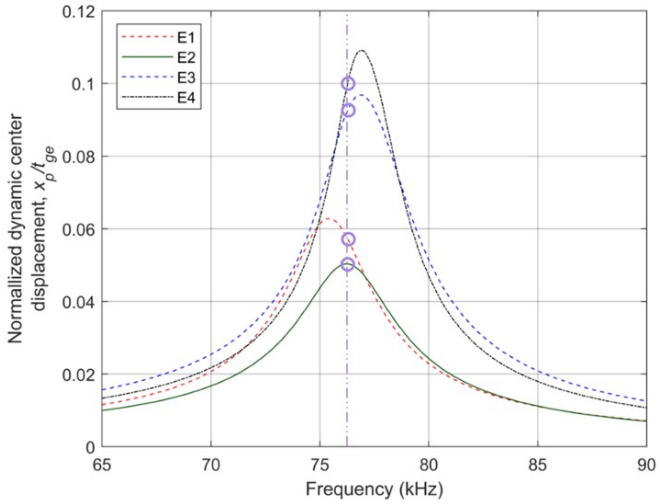


Figure 4.16: Calculated normalized peak center displacement deflection for modified circuit elements at $V_m = 50V$ for different elements of array S1 under SAP. © *2020 IEEE.*

drive voltage amplitude but at a different frequency (Figure 4.16). Element E2 in array S1 is least sensitive and has the minimum peak deflection, while E4 has the maximum deflection. For instance, when operated at 76 kHz, where E2 has its maximum peak deflection, other three elements have higher deflections, although they are not at resonance. Beam steered array operation is possible if each of these three elements are driven using a lower drive voltage amplitude so that all four elements have the same peak displacement using appropriate phasing.

This is detailed further in (Fig. 4.17), which displays normalized dynamic center displacement (x_p/t_{ge}) for each of these elements when driven at 76 kHz. By design, a lossless plate can achieve up to 0.3 times x_p/t_{ge} under ac excitation. As measured peak deflection is 7 µm, the plate can swing across the entire gap. However, the maximum displacement that each element can achieve, differs due to non-uniformity induced during production. All elements can attain a peak center displacement of up to about $x_p/t_{ge} = 0.2$, nominally, at different drive voltage.

In order to equalize the displacement amplitude amongst the elements, following approach can be used. The drive voltages of more sensitive elements: E1, E3

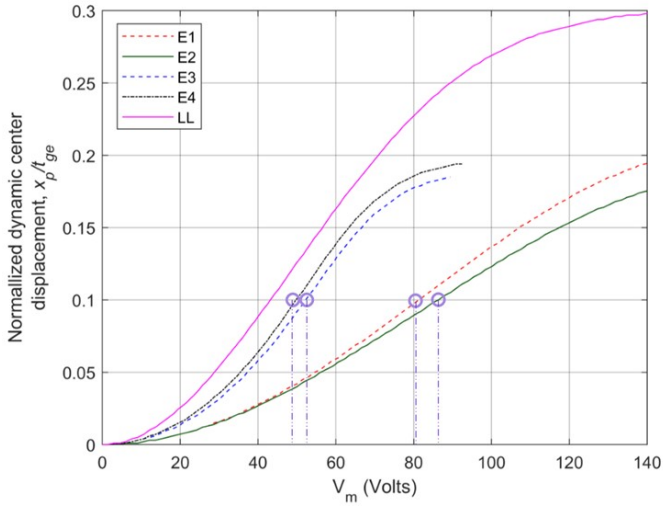


Figure 4.17: Calculated normalized dynamic center displacement, (x_p/t_{ge}) at 76 kHz vs voltage sweep of lossless (LL) and modified circuit elements E1 to E4.

and E4, can be reduced to match the peak displacement of the least sensitive element, E2. For instance, in order to obtain $x_p/t_{ge} = 0.1$, we can drive E2 at 85 V while E1, E3 and E4 drives can be reduced to 81 V, 53 V and 48 V, respectively, as shown in Figure 4.17.[12]

A larger dynamic center displacement implies a higher pressure emitted by the CMUT. Dynamic center displacement as well as radiated pressure of a CMUT element, both have a non-linear behavior with respect to drive voltage. This non-linear behavior in measured radiated pressure will be discussed in relation to the drive voltage in the following discussions.

For equalization of pressure between elements of array S1, E2 is kept as a reference element. Drive voltages for E1, E3 and E4 are reduced to equalize the pressure with E2. For instance, at 80V drive in Fig. 4.11, E2 emits 0.93 Pa, while E1, E3 and E4 produce 1.3 Pa, 1 Pa and 1.7 Pa, respectively. In order to equalize the pressure of all elements at 0.93 Pa, drive voltage of E2 is kept at 80V, while E1, E3 and E4 are reduced to 78.4 V, 62.4 V and 60.8 V, respectively. Using this measured pressure equalization, a voltage compensation factor (γ_{com}) for drive voltage is calculated and tabulated in Table 4.2.

[12]Similar analysis is also performed on different frequencies near resonance.

Table 4.2: Compensation parameters for array S1 driven at 76 kHz

	E1	E2	E3	E4
γ_{com}	0.98	1.0	0.78	0.76
$\emptyset_{com}$ (rad)	0.03 π	0	-0.14 π	-0.16 π
$\emptyset_{steer}$ (30^o)	0	1.156 π	0	1.156 π
$\emptyset_{steer}$ (105^o)	0.345 π	0	0.345 π	0

To compensate for phase variation between each element, we used two elements simultaneously at same frequency and at their respective drive voltages required for a given pressure amplitude. The output pressure under this condition is maximized as one of the element's phase is adjusted. This maximum pressure level is twice the pressure obtained when either element is driven individually. Keeping the same reference phase, this is repeated with the remaining two elements in the array. This phase equalization is performed for entire drive range, and phase difference compensation, $\emptyset_{com}$, is measured for each element and tabulated in Table 4.2.

γ_{com} and $\emptyset_{com}$ for each element remains constant from 10 V to 80 V. Beyond 80 V, as E4 pressure appears to saturate probably due to swing amplitude becoming equal to the gap height, the deviation from this compensation is evident.

Once these compensation factors are determined, we can use them to drive each element of array accordingly. AC voltage drive, $V_{(i)}$, for ith element in an array can be given as,

$$V_{(i)}(t) = V_0 \ \gamma_{com(i)} \ sin\left(2\pi ft \pm \emptyset_{steer(i)} \pm \emptyset_{com(i)}\right) \tag{4.9}$$

Here V_0 is the applied ac voltage for the least sensitive element of the array, $\gamma_{com(i)}$ and $\emptyset_{com(i)}$ are amplitude compensation factor and phase compensation respectively, and $\emptyset_{steer}$ is the phase difference that needs to be added to steer the beam in a specific direction. For beam forming normal to the surface of array, $\emptyset_{steer}$ is zero. Using this approach, the array was compensated, and the output pressure of this compensated array is given in Figure 4.11. Reference element E2 shows a peak pressure of 1.67 Pa at 100V while the compensated array emits 5.42 Pa, which is 11 dB higher than the output of E2.

These pulse measurements were repeated at 75.8 kHz, 76 kHz, 77.6 kHz and 77.63 kHz. The $\gamma_{com(i)}$ for these frequencies remain constant, but the $\emptyset_{com(i)}$ varies at each of these frequencies. Although this process causes a reduction in the radiated pressure for more sensitive elements, however, this compensation is essential for beam steering to ensure that each element emits equal pressure. In Figure 4.13, the measured pressure levels for each of these drive frequencies for an array are averaged and displayed with standard deviation between each measurement (shown as parallel bars). A homogeneous response was observed for array element at different frequencies, with a maximum deviation ± 1 dB.

It is observed that by matching each element pressure and phases in this manner, we were able to obtain an array pressure that is 11 dB higher than its least sensitive element. The limitation to this compensation arises when the plate of element E4 starts hitting bottom electrode at high drive voltages ($< 80V$).

4.2.4 Beam steering measurements

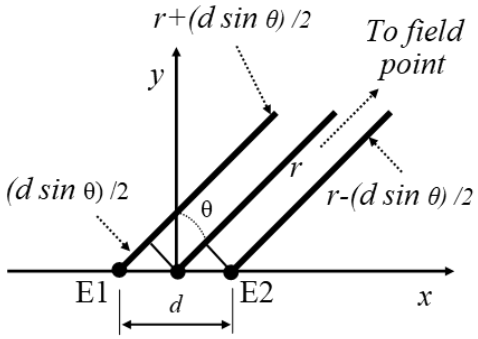


Figure 4.18: Radiation from a two source array. [55]

Geometric depiction for radiation from a 2 element line array is shown in Figure 4.18. This geometry can be extended to a 2-dimensional array elements, where, for beam steering, a phase delay, $\emptyset_{steer}$, can be calculated using a phased array geometry [70]. This calculated phase delay for steering at different angles for array S1 are tabulated in Table 4.2.

Phase delay for beam steering can be used in Eq. 4.9 to obtain drive voltage

of each element required to steer at a specific angle. This process is then implemented in LabView environment that is attached to the D/A system, which in turn individually drives all four elements. In this study, elements E1 and E3 were driven at a phase delay $\emptyset_{steer}$ with respect to elements E2 and E4 of the array to beam form at 90^o and beam steer the beam at 30^o and 105^o.

The CMUT array was operated in a continuous wave excitation mode. The microphone output was attached to a lock-in amplifier[13] with a time constant of 100 ms and a roll-off of 12 dB/octave. A reference signal of a similar amplitude and resonance frequency is also provided through D/A. Fur was used at all surrounding reflective surfaces to reduce the acoustic interference (Figure 3.9). The CMUT wafer was erected vertically on top of the 360^o stage (Figure 4.19). The stage was manually rotated from 10^o to 170^o with a 3^o step.

Figure 4.8 shows normalized directivity measurement in comparison with the normalized calculated directivity at 76 kHz. The beam pattern was symmetric on the central axis. Beam steering calculations are consistent with the measured beam pattern. Side lobes with low amplitude are visible in all three cases, as the presence of sidelobes are inevitable while making directivity measurements.

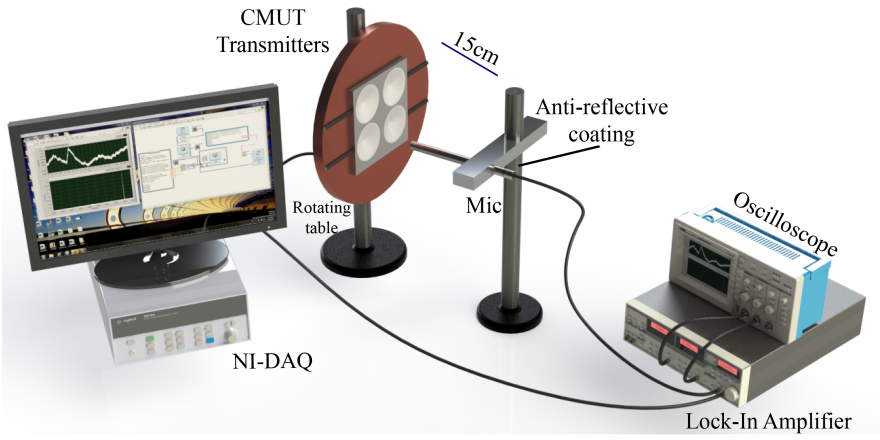


Figure 4.19: Measurement setup for an airborne CMUT array for beam steering measurements. The distance from the microphone to the CMUT is 15 cm. © *2020 IEEE.*

[13]SR850, Stanford Research Systems, Sunnyvale, CA

Chapter 5

Conclusion and Future Works

5.1 Conclusion

This work provides a methodology for design, production and operation of 2-dimensional CMUT arrays that can produce very high intensity, beam steerable, ultrasound in airborne applications. The surface pressure of the array is estimated as 144 dB from the measurements. This pressure level is higher than other reported studies. Furthermore, this array is capable of precision beam steering. The CMUTs are produced using an integrated fabrication method that involved a single lithographic process.

We achieved high transmission pressure using only *ac* drive, as we drive the CMUTs at half the operation frequency. We demonstrated that we can predict the performance of fabricated CMUTs. CMUT elements operate such that the plate movement covers the entire gap, hence providing the maximum pressure.

The measured frequency response is matched with the modified model by accounting for various production losses. The measured transmit performance provides a very close match to the calculations. The array is operated at various

frequencies (on and off-resonance), when compensated with respect to least sensitive element. For these compensated array pressure measurements, deviation at drive voltages less than 80V was negligible. As one of the element's pressure saturates beyond 80V, deviation increases to 2 dB. A 2×2 compensated CMUT array produced 11 dB higher pressure than the least sensitive element of the CMUT array.

The array can provide better performance when the dispersion of frequency is reduced between each element. For instance, if all the elements were operating similar to the most sensitive element (E4), the amount of radiated array pressure could be maximized at even lower drive voltages. In this way, the array can produce 12 dB higher pressure than its individual elements. The fact that the compensation required for each element remained constant with each drive voltage is an important asset, which makes the array easily usable in applications where beam steering is required at very high pressure levels.

As the measurements are performed under presumed material properties and other assumptions [71], deviations in resonance frequency and dynamic center displacement was observed in comparison to the circuit model.

Fabrication inaccuracies are inevitable in a multiuser cleanroom facility. Making the fabrication process more efficient can reduce the discrepancies between the elements, which both reduces the compensation requirements and increases the amount of radiated pressure of an array. With the processes optimized for industrial fabrication facilities, the elements of the array will almost be identical, in which case the same amount of pressure can be produced using 40 V amplitude.

The described ultrasound transducer can be used for gesture recognition, air-coupled imaging, generating directional or omni-directional audio in audible range, park assist, path-assist sensors for smart cars, finger print scanning, record sound (wide bandwidth microphone), tactile displays and touch sensor.

5.2 Future Directions

As a future direction to this work, CMUTs can be operated in a pitch catch configuration for applications involving gesture recognition and range finding. CMUTs discussed in this work can be designed to operate as a microphone by applying a *dc* bias. This requires a fast switching electronics that is capable of toggling *ac* and *dc* bias between transmit and receive modes. It is desirable to have narrower beamwidth. Our work was mainly focused on two major objectives: (1) to achieve beam steering that covers entire Fourier half space, (2) to achieve high intensity CMUT transmitters. As a future implementation, this work can be extended to produce narrower beamwidth that can provide more accuracy.

In order to achieve narrow beamwidth, a large array can be designed. This presents several challenges limiting ka, kd. With our current design parameters with $ka \approx 2$, and $d = 3mm$, implementing a 9×9 array will extend the active area to $27 \times 27mm^2$. This is not viable, as it will require a significant decrease in the width of electrical connection wires connecting each element to it's outer electrical pads. This decrease in the width of wires will be challenging to fabricate while keeping the yield at a high level. Keeping the width of these wires and their spacing constant, we can increase the pitch to 4.25 mm($< \lambda$), which decreases the beamwidth to 6.5^o with an active area of $36.8 \times 36.8mm^2$. This design can be implemented on a 100-mm substrate, with 81 channels that can be wire bonded on a PCB.

The fabrication process can be further optimized to improve the yield of the process and reduce the deviations between elements. Dry etching may be used to generate Pyrex cavities to lower variation in lateral dimensions. Routing channels for a large 4x4 array were designed on the corners of bonding interface. This prevented the gaps of the CMUT array devices from being efficiently vacuumed in comparison to rest of the elements. Employing efficient electrical routing on wafer, and usage of smaller die spaces with narrower or shorter electrode connections, can help to reduce the parasitic capacitance.

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Appendix A

Implementing the Circuit model in ADS

Data files used or referred to in this thesis can be requested by sending an email to talha.khan@bilkent.edu.tr or talha1msd@gmail.com.

ADS [72] is an electronic design and automation software used for microwave, RF, and digital electronic design. We have used ADS based on the following reasons [73].

- The Harmonic Balance simulator is capable of providing accurate estimation of a steady state response of Non-linear circuits in a fast manner
- The circuit simulator is able to use impedance data frequency domain.

Being able to simulate in frequency domain is important as the radiation impedance expressions defined in this work are in frequency domain. In this section, we will demonstrate implementation of the large signal equivalent model for a single CMUT element and a 2×2 array.

Self impedance is defined as a 1-port Z-parameter component. For an array, multiple elements can be cascaded together. For larger array implementation

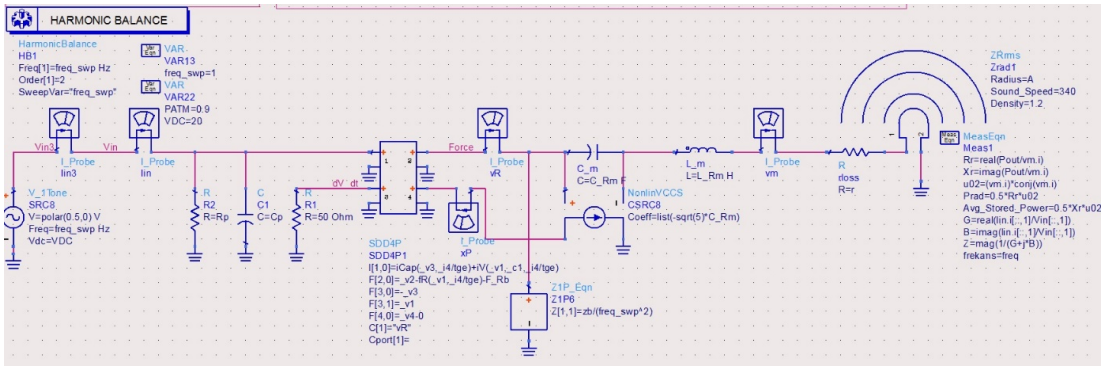

Figure A.1: ADS simulation environment for simulating Single cell CMUT

in ADS, the task of placing large number of arrays is simplified by using macros function. The radiation impedance matrix is constructed using a multi-port user-complied model written in C programming language. Further details regarding this can be found at `http://www.ee.bilkent.edu.tr/~cmut` [73].

The model is defined for a single CMUT element using $\{f_R, v_R\}$ *rms* model is implemented in ADS as displayed in Figure A.1. A non-linear component, *symbolically-defined device* (SDD), is used to define algebraic relationships, relating them to the port currents, voltages, and their derivatives. In our model, a 4-port SDD (SDD4P) is used. This SDD is used to calculate the non-linear current i_{Cap}, i_V, and force f_R.

For this *rms* model, the x_P is calculated across the C_{Rm} with the voltage controlled current source which is constantly fed back to SDD4P. Both the current and force relations are represented as functions of the applied voltage, its time derivative, x_P/t_{gr}, and v_R. Using the design variables in Table 2.2, different parameters for the CMUT design were simulated in the ADS environment and displayed in Figure A.2.

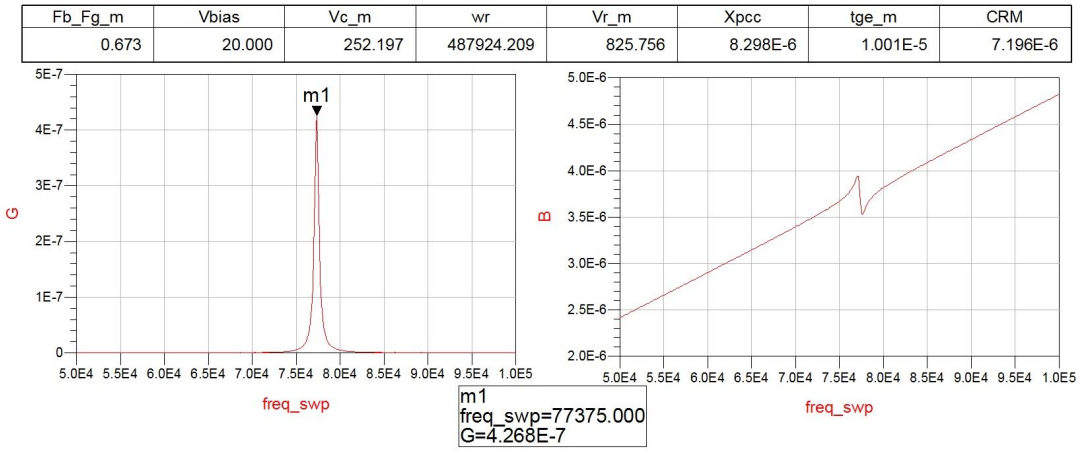

Figure A.2: GB curves for CMUT element designed using parameters in Table 2.2. The frequency is swept between 50–100 kHz, at 0.5 V *ac* and 20 V *dc*.

The susceptance and conductance simulation for a single CMUT element is calculated by,

$$G = real(\frac{I_{in}}{V_{in}}) \tag{A.1}$$

$$B = imag(\frac{I_{in}}{V_{in}}) \tag{A.2}$$

For a 2×2 array, the circuit elements are replicated in parallel with each other. They are all terminated using a Z impedance matrix defined in chapter 2. ADS simulation environment for this array is shown in Figure A.3.

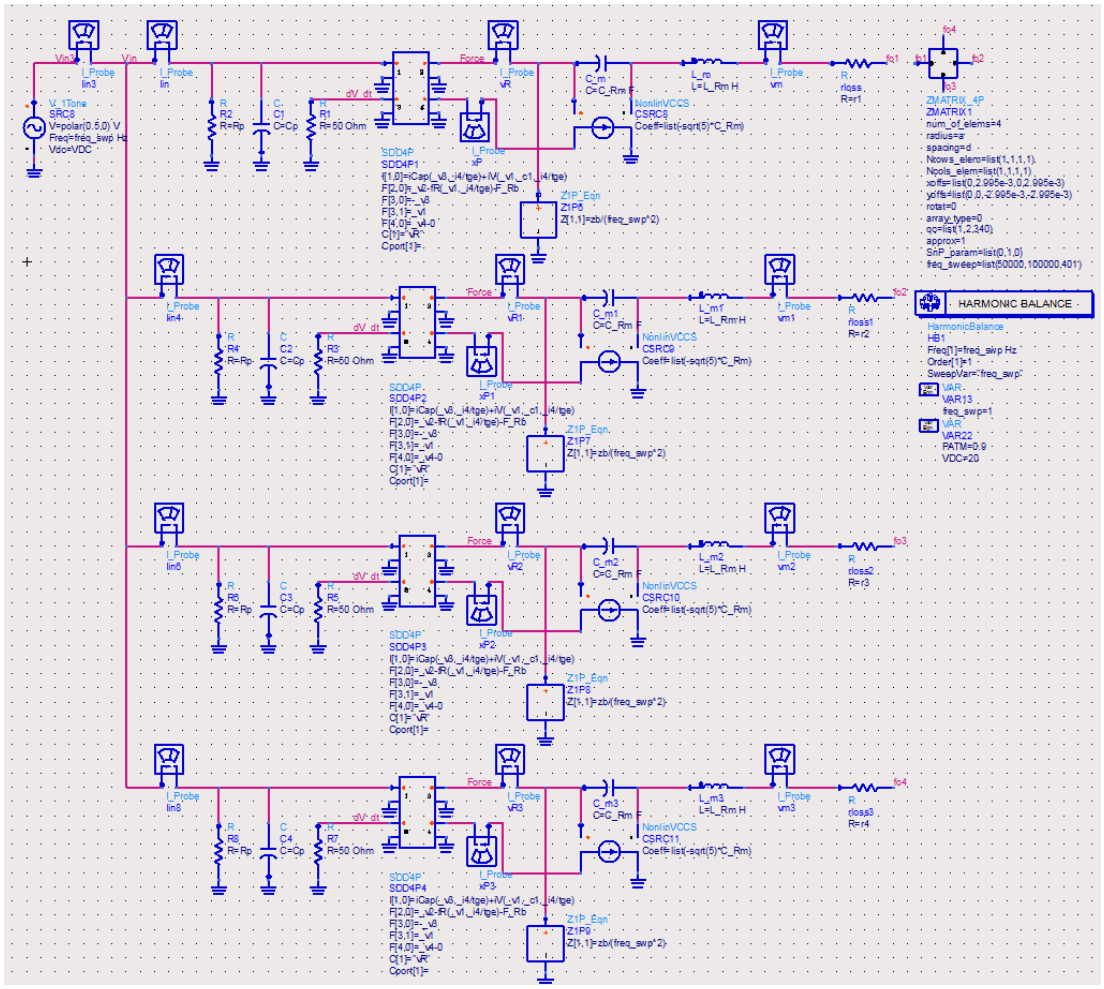

Figure A.3: ADS simulation environment for simulating 2×2 CMUT array

Appendix B

CMUT simulation using Finite Element Analysis

Following code is used in ANSYS v14 to simulate a single CMUT element using parameters provided in Table 2.2 and is displayed as Fig. 2.5.

```
finish
/clear, nostart
/prep7
! PARAMETERS!
pi = 4*ATAN(1)
! ELEMENT TYPES !
et,11,200,7     !Defining element type
ET,1,SOLID186,  !Defining element type (or Trans126)

! MATERIAL PROPERTIES !
! Material properties for silicon
e_sn        = 148e9
dens_sn     = 2370
poiss_sn    = 0.17
AL2O3_eps   = 9.7
mp, ex, 1, e_sn         ! Mat 1 (Si)
mp, dens, 1, dens_sn
```

```
mp, nuxy, 1, poiss_sn

! GEOMETRY !
cmut_rad = 1.4e-3
cmut_thick = 40e-6
cmut_gap = 10e-6
cmut_ti = 100e-9
cmut_mesh_size =  cmut_thick
cmut_mesh_div = 10

! Transducer
CYLIND,cmut_rad,0,0,-cmut_thick,0,360

! Mesh the CMUT ! Divide the thickness of the CMUT
csys,0
lsel,s,loc,z,-cmut_thick !lsel,s,loc,z,-cmut_thick/2
lesize,all,,,cmut_mesh_div
alls

csys,0
ASEL,S,LOC,Z,-cmut_thick
lsla,s
ksll,s
type,11
MSHAPE,0,2D
MSHKEY,0
*GET,A1, AREA,0,NUM,MIN
*GET,K1, KP,0,NUM,MIN
K2=KPNEXT(K1)
K3=KPNEXT(K2)
K4=KPNEXT(K3)
K5=KPNEXT(K4)
K6=KPNEXT(K5)
K7=KPNEXT(K6)
K8=KPNEXT(K7)
ESIZE,cmut_mesh_size
AMESH,ALL

vsla,s
cm,cmut_vol,volu
```

```
58
59          ESIZE,cmut_mesh_size
60          VATT,1,,1
61          VSWEEP,ALL
62          ACLEAR,ALL
63          alls
64
65          ! TRANS126
66          csys,1
67          asel, s,loc, x, 0,cmut_rad
68          asel, r,loc, z, -cmut_thick
69          nsla, s, 1
70          cm,ELECT,node
71          csys,0
72          ! Placing TRANS126 elements
73          EMTGEN, 'ELECT','MEMBRANE','GROUND', 'UZ', -CMUT_GAP ...
               -CMUT_TI/AL2O3_eps, CMUT_TI/AL2O3_eps, 1 ,8.854e-12
74          !*********************************
75          D,ground,UX,0
76          D,ground,UY,0
77          D,ground,UZ,0
78          D,ground,VOLT,0
79          ALLS
80
81          nsel, s,,, ELECT
82          cp,1,VOLT,all             ! TOP ELECTRODE COUPLED
83          *get,NTOP,NODE,0,num,min ! MASTER NODE ON TOP ELECTRODE
84          nsel,all
85
86          csys,0
87          asel,s,loc,z,-cmut_thick/2
88          asel,u,loc,x,cmut_rad/2
89          asel,u,loc,y,cmut_rad/2
90          nsla,s,1
91          D,all,UX,0
92          D,all,UY,0
93          D,all,UZ,0
94          alls
95
96          csys,1
```

```
97          asel, s,loc, x, 0,cmut_rad
98          asel, r,loc, z, 0
99          nsla, s, 1
100         cm,srf_nodes,node
101         alls
102
103         FINISH
104         /SOLU
105         ANTYPE,STATIC
106         PSTRES,ON
107
108         neqit,100
109         csys,1
110         asel, s,loc, x, 0,cmut_rad
111         asel, r,loc, z, 0
112         SFA, all, ,PRES, 0.9*101325 ! 101325 Pa = 1atm
113
114         ALLS
115         D, NTOP, VOLT, 10
116         cnvtol,u
117         ALLS
118
119         SOLVE
120         FINISH
121
122         /SOLU
123         ANTYPE,modal
124         MODOPT,UNSYM,20
125         MXPAND
126         PSTRES,on
127         allsel, all, all
128         SOLVE
129         FINISH
130         !*****************************
131         /post1
132         PLDISP,1
```

Appendix C

Implementing phased array operation using LabView Simulation Environment

NI Labview is a system-design platform and development environment that is used with visual programming language. This software provides a DAQ assistant that can be programmed to perform complex signal processing which can be used to implement phased array systems.

The NI DAQ card PXI-6733 has 5 analogue outputs, 4 of which are used to provide output to CMUT elements, and 1 additional output is used for producing reference signal for measurements. The LV environment displayed in Figure C.1, has a MATLAB coding block. This block is multiplexed into the DAQ assistant that is nested inside a while loop. The loop has a wait timer that can be used to produce pulses. The DAQ assistant generation mode is set to N samples, which writes at the rate of 750 kHz.

For reception, the DAQ assistant can be used to interface with the microphone

directly[1] to measure pressure or through microphone adaptor [2]. The DAQ assistant, is interfaced with an inbuilt digital oscilloscope and spectrum analyzer. These virtual equipment inside the VI can directly read the output signal provide by the microphone.

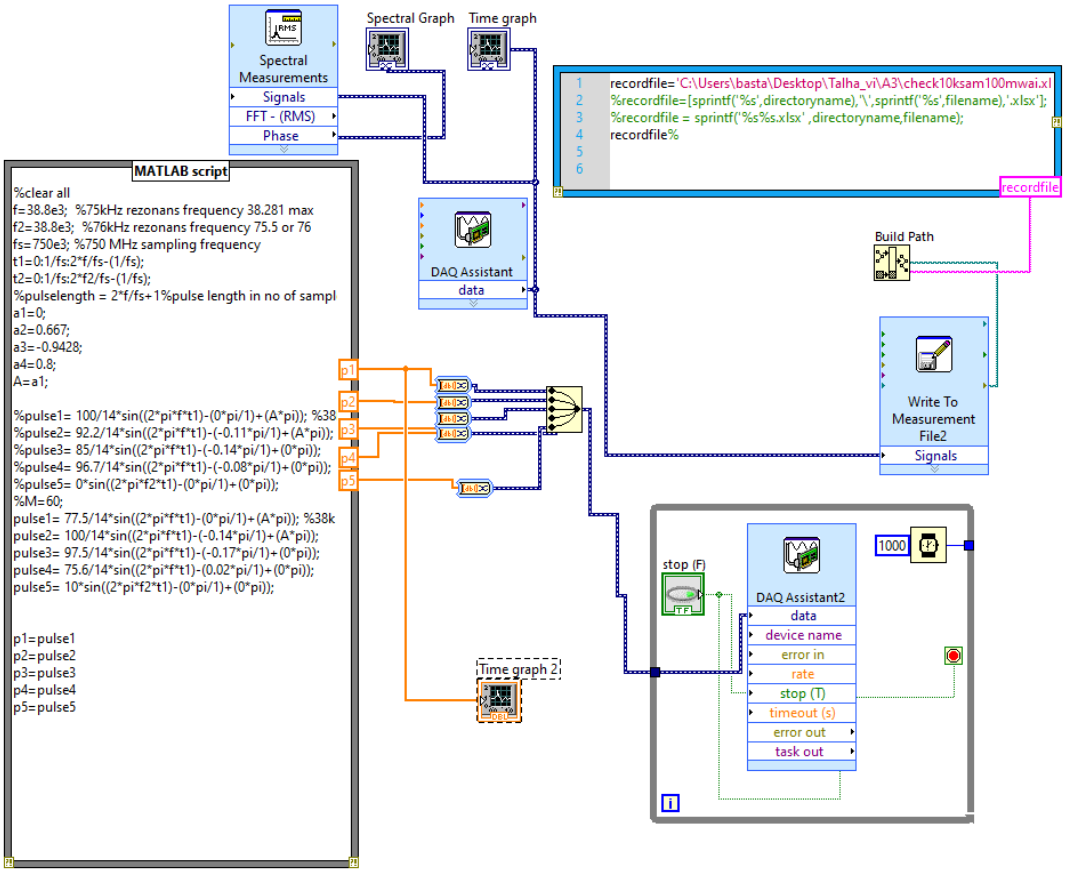

Figure C.1: NI LabView VI environment designed for pulsed transmit operation and reception. (subsection 4.2.2).

[1]GRAS 46B/E, 1/4 inch CCP free field microphone, GRAS Sound and Vibration A/S, Holte, Denmark

[2]B&K 4138, Bruel and Kjaer, Naerum, Denmark

Appendix D

Additional Figures

D.1 Microfabrication Figures

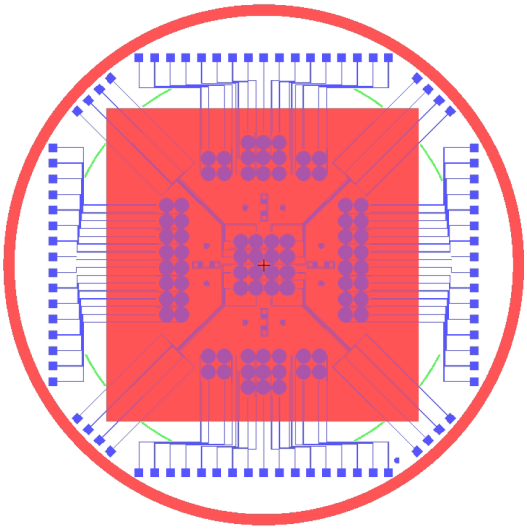

Figure D.1: Mask design of the SOI wafer covering the CMUT cavities.

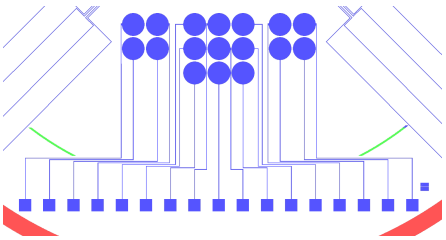

Figure D.2: 2×2 and 3 arrays extended to the edge of the wafer.

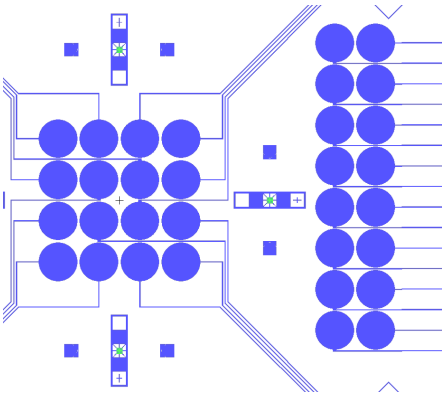

Figure D.3: 2×8 and 4 arrays extended to the edge of the wafer.

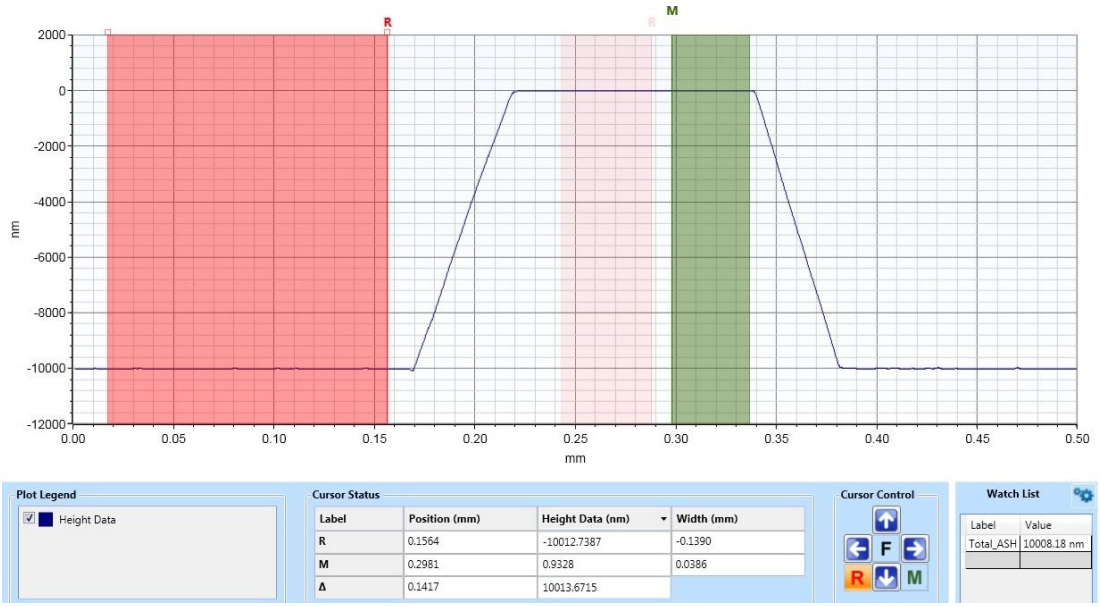

Figure D.4: Stylus measurement showing depth of Pyrex cavity $\approx 10\mu m$

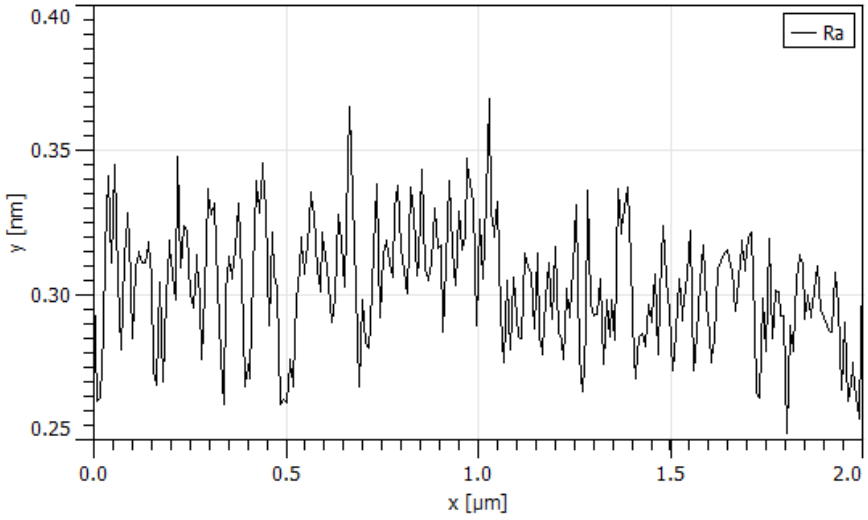

Figure D.5: Average roughness (Ra) of Si device layer of CMUT wafer F21 performed using AFM.

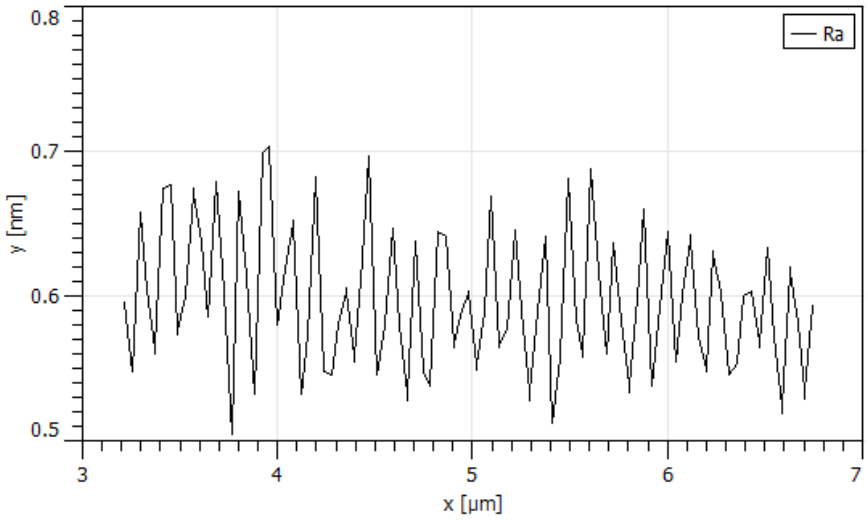

Figure D.6: Average roughness (Ra) of Si device layer of CMUT wafer F24 performed using AFM.

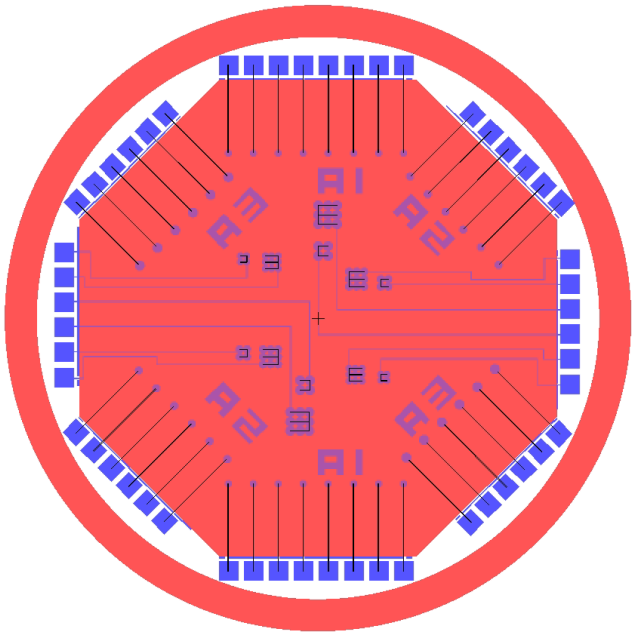

Figure D.7: Mask design for CMUT receiver elements and arrays with overlayed SOI.

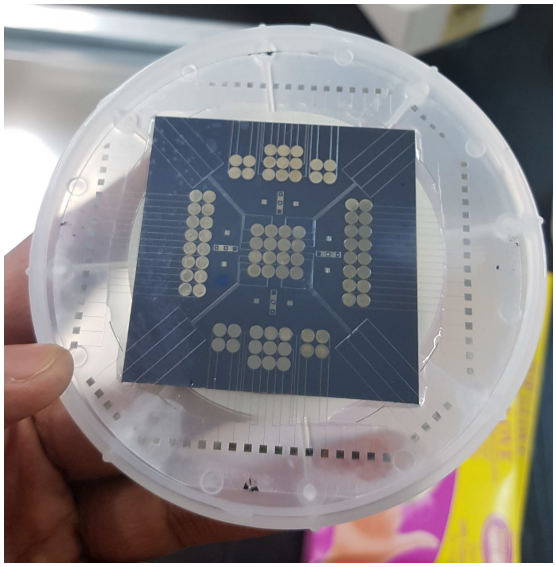

Figure D.8: Image of the CMUT wafer taken after wafer bonding. Some bond voids (Bluish markings) are observed.

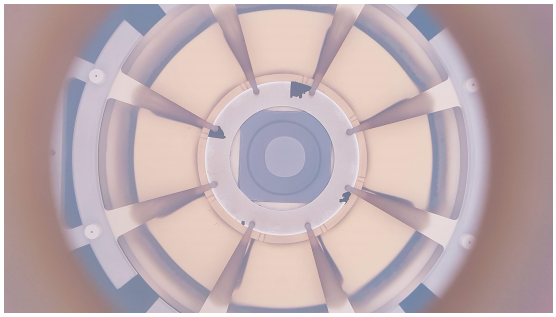

Figure D.9: ICP RIE for Handle layer removal. The donut shaped Al mask is clamped on top of the CMUT wafer

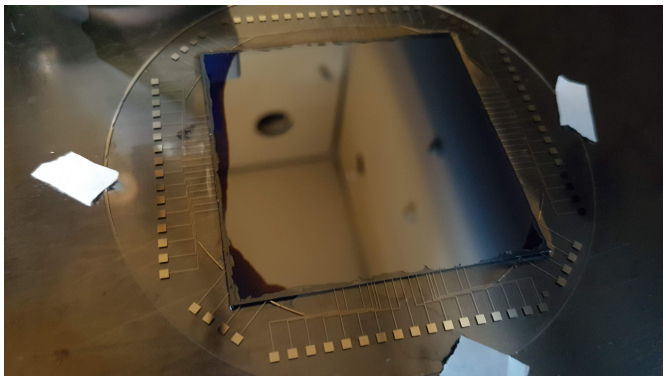

Figure D.10: Sealing Epoxy applied to the edge of the SOI wafer on all sides.

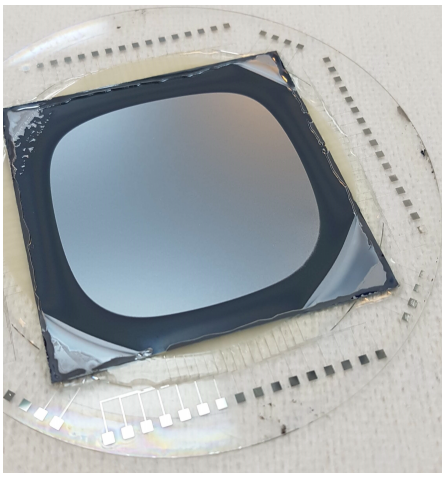

Figure D.11: Image of Si handle layer partially removed from the edges using ICP RIE process.

D.2 Impedance measurement figures

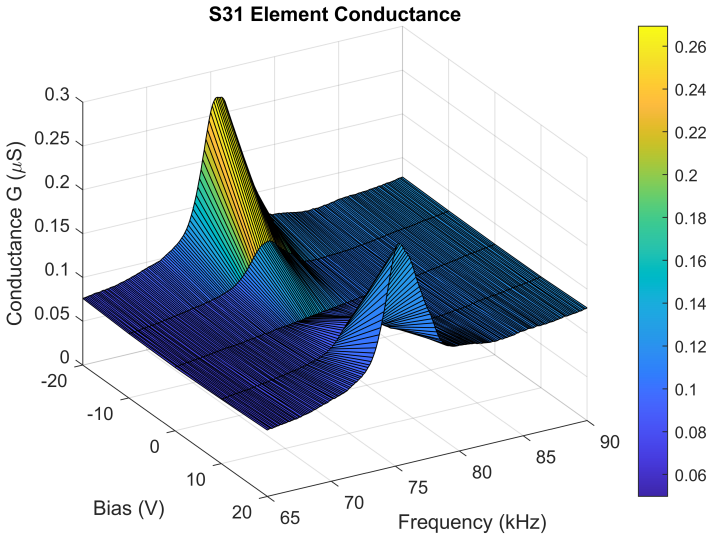

Figure D.12: Impedance measurement for element S31.

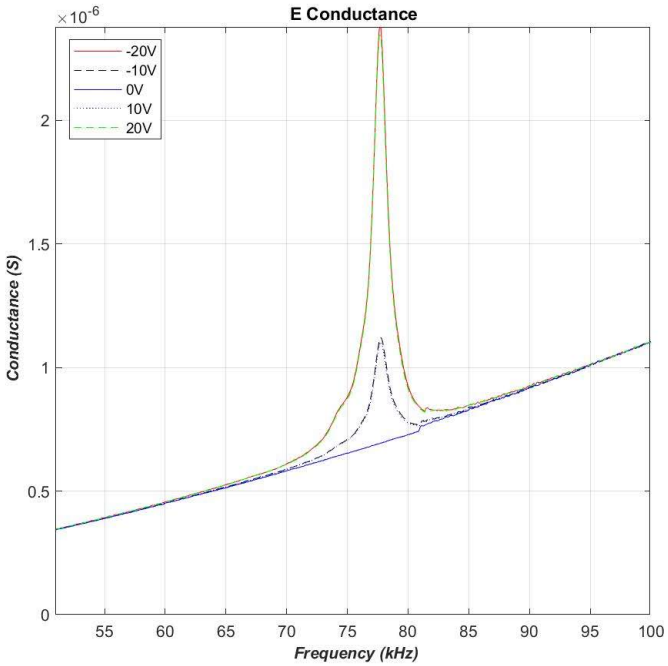

Figure D.13: Impedance measurement for Array E, with 2x4+1 elements.

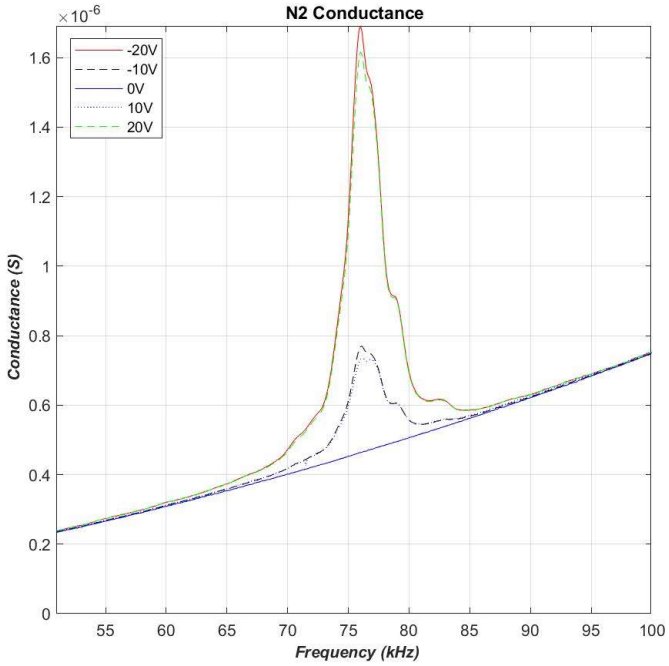

Figure D.14: Impedance measurement for Array N2 measured

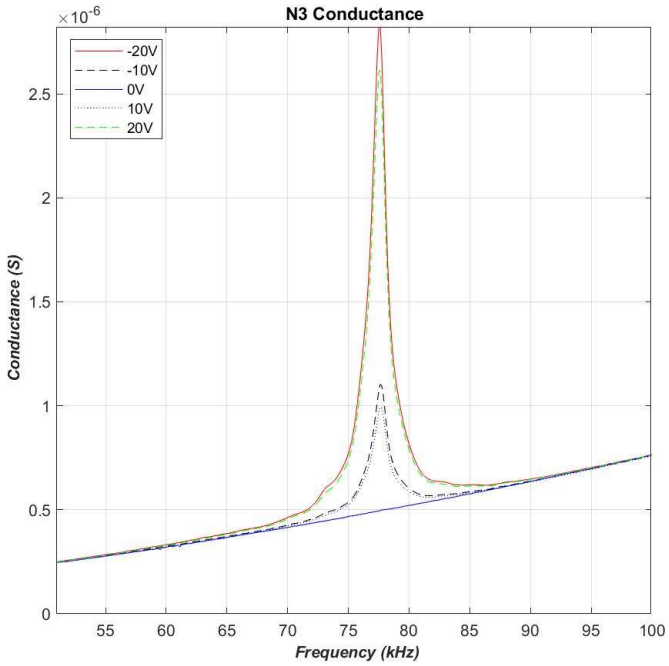

Figure D.15: Impedance measurement for Array N3, with 2x2+1 elements.

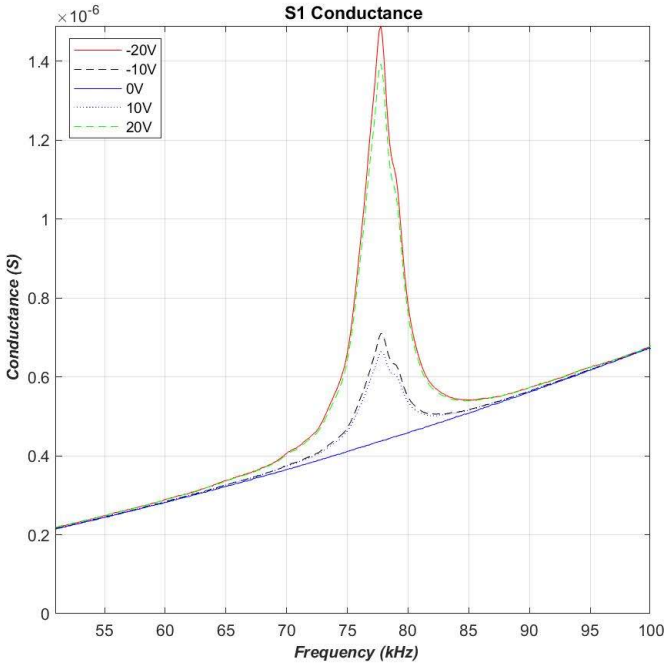

Figure D.16: Impedance measurement for Array S1.

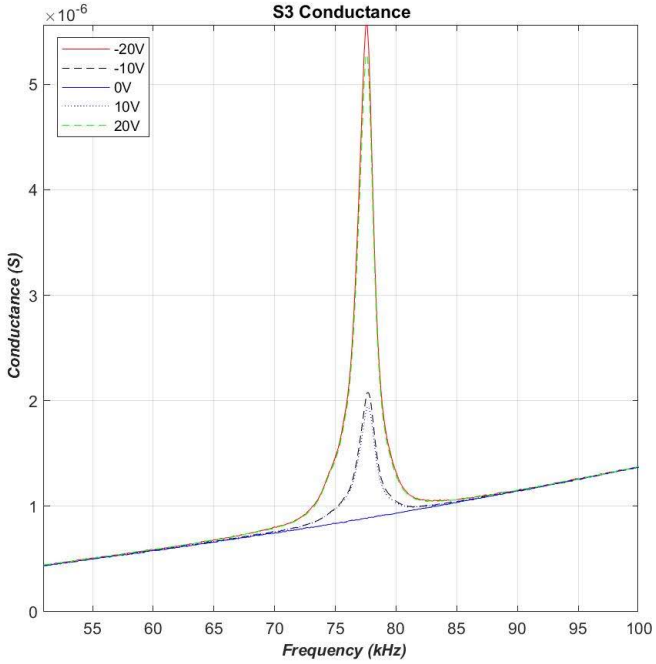

Figure D.17: Impedance measurement for Array S3.

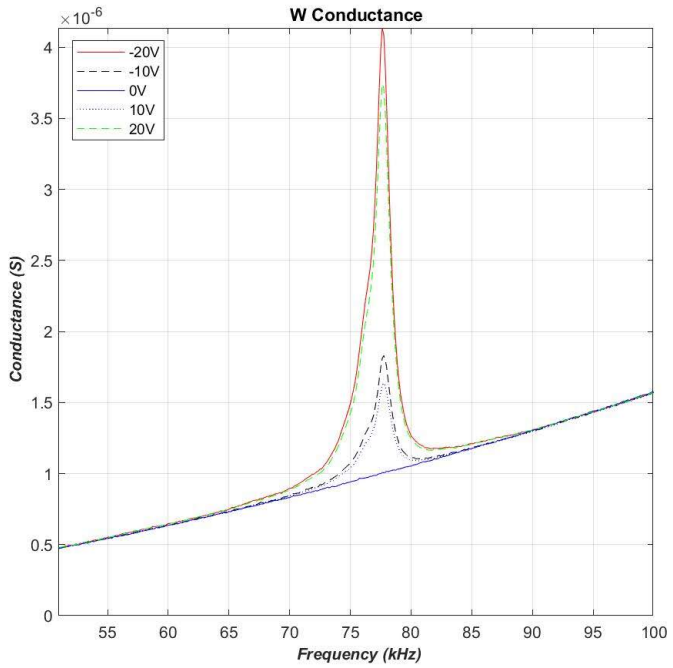

Figure D.18: Impedance measurement for Array W (2x5).

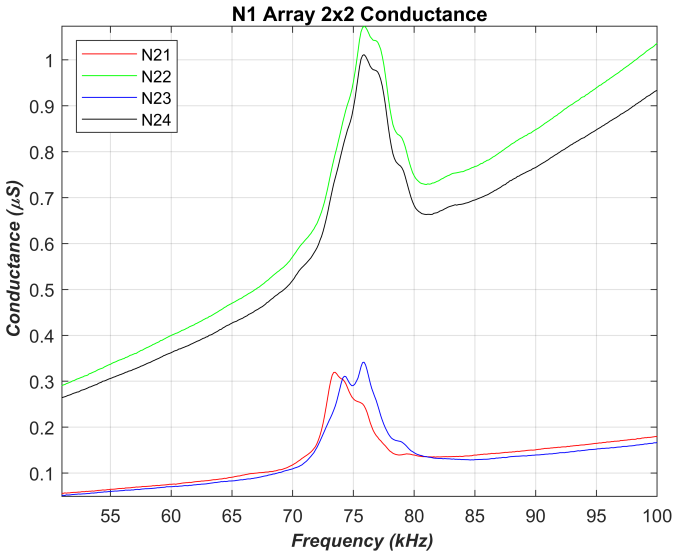

Figure D.19: Conductance measurement of different elements of array N2. It can be observed that the elements have shifted resonance frequency and different bandwidths.

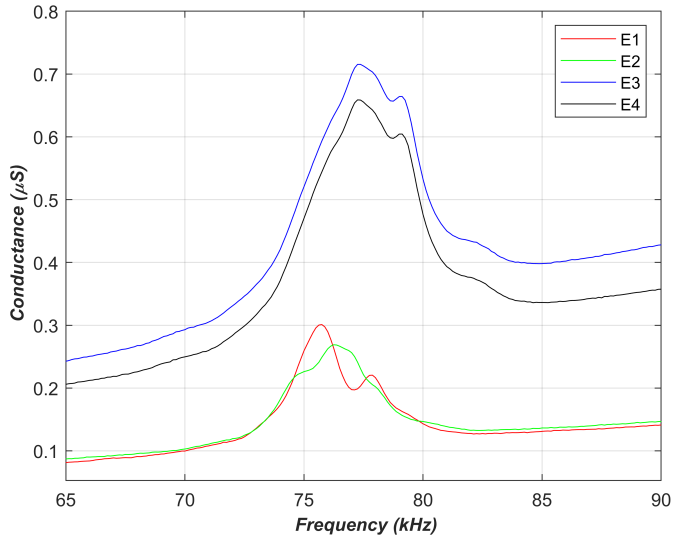

Figure D.20: Conductance measurement of different elements of array S1. It can be observed that the elements have shifted resonance frequency and different bandwidths.

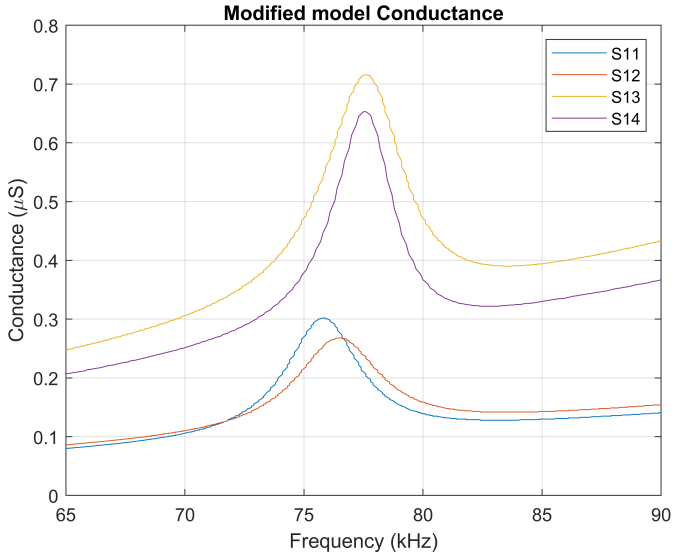

Figure D.21: Model fitted conductance curves for all 4 elements in array S1 driven at 20 V dc bias and 0.5 V ac.

D.3 Pressure measurement Figures

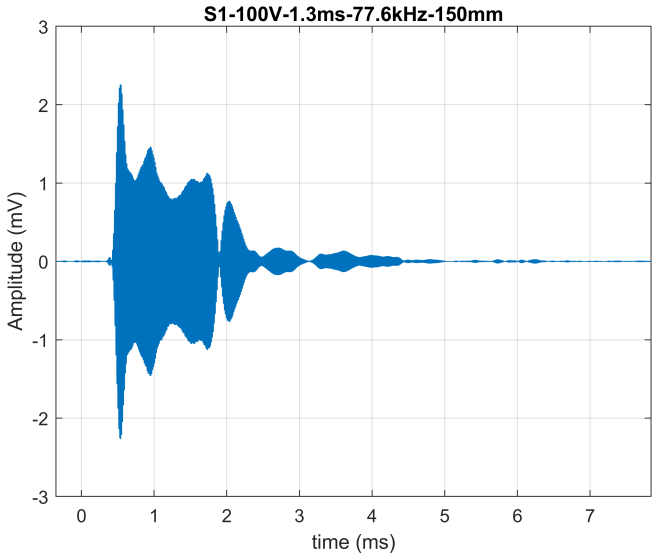

Figure D.22: Measured time signal from array S1 driven at 100 V with 1.3ms pulse duration at 77.6 kHz.

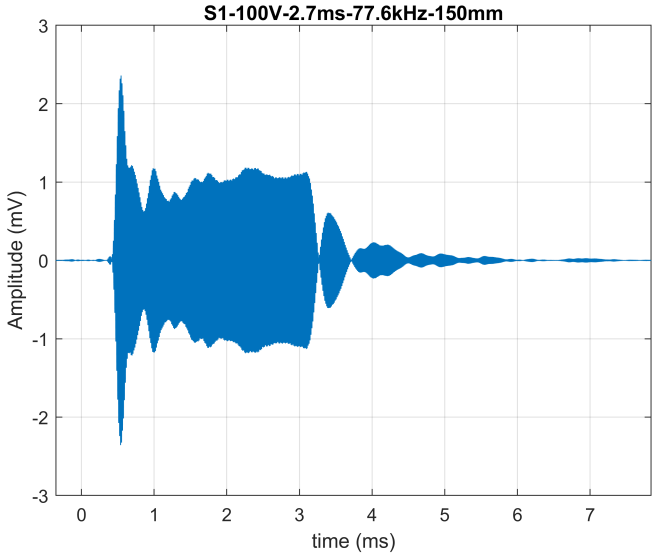

Figure D.23: Measured time signal from array S1 driven at 100 V with 2.7ms pulse duration at 77.6 kHz.

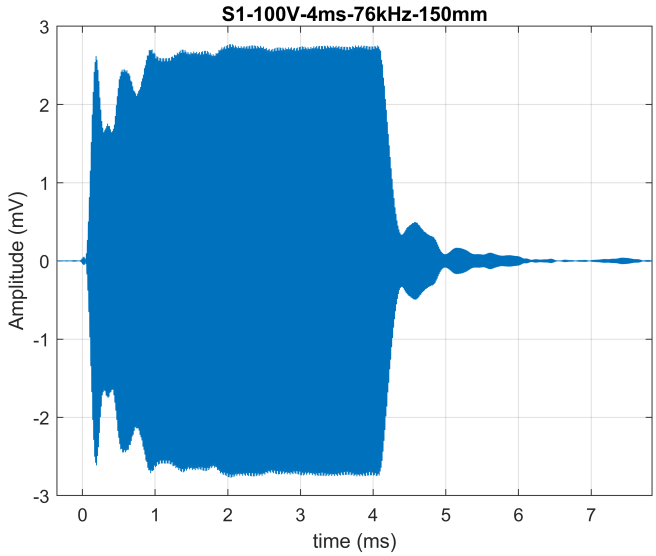

Figure D.24: Measured time signal from array S1 driven at 100 V with 4ms pulse duration at 76 kHz.

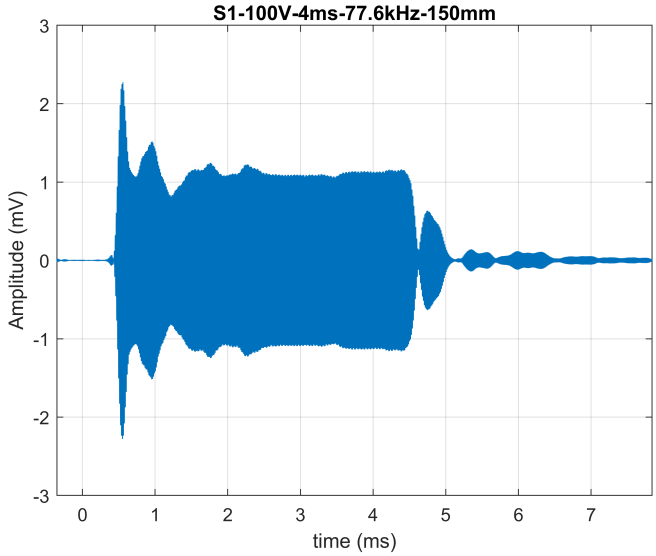

Figure D.25: Measured time signal from array S1 driven at 100 V with 4ms pulse duration at 77.6 kHz.

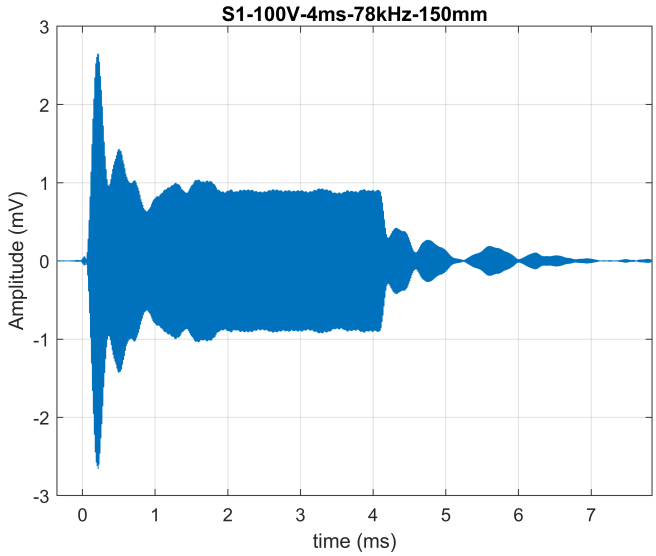

Figure D.26: Measured time signal from array S1 driven at 100 V with 4ms pulse duration at 78 kHz.

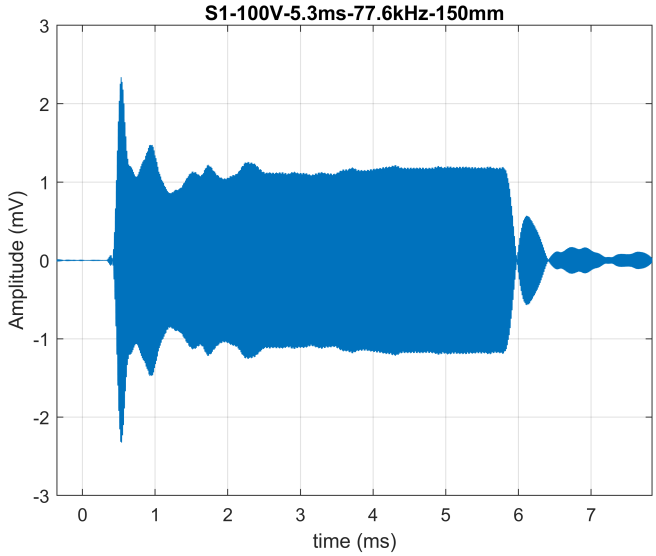

Figure D.27: Measured time signal from array S1 driven at 100 V with 5.3ms pulse duration at 77.6 kHz.

Appendix E

Microfabrication Recipes

E.1 ALD for Alumina deposition

The recipe in Table E.1 is used for ALD deposition of 100nm Alumina.

Table E.1: ALD Savannah recipe for depositing 100nm alumina

	Instruction	#	Value	Description
0	heater	9	200	Inner heater temperature ($^{\circ}C$)
1	heater	8	200	Inner heater temperature ($^{\circ}C$)
2	stabilize	9	200	
3	stabilize	8	200	
4	wait		600	wait for stabilization
5	flow		20	N_2O flow (sccm)
6	wait		60	
7	pulse	0	0.015	H_2O (sccm)
8	wait		8	
9	pulse	3	0.015	Trimythylaluminum (TMA) (sccm)
10	wait		8	
11	goto	7	1000	Repeat for 1000 times
12	flow		5	N_2O flow (sccm)

E.2 ICP recipe for RIE

The recipe (CMUT-NC-SOI-Thin-V005) is used for RIE of Si Handle Layer (Table E.2). The RIE recipe is used in 4 sessions, with each session preceded by a dummy process to condition the chamber. Before each session, the wafer is covered by BOE using a pipette for 3 mins to remove native oxide. It took 5 hour 15 mins of cumulative etch time to completely remove the handle layer.

Table E.2: RIE recipe for removal of Si Handle layer

General	
Generator Connection mode	Platen HF
Platen position	Up
Stabilization	Enabled
Stabilization time	15 sec
Switching enabled	No
Start Phase	N/A
End Phase	N/A
Deposition Time	N/A
Etch Time	N/A
Generators	
Platen Power	30 W
13.56 MHz Coil Power	700 W
Gasses	
SF_6 flow	130 sccm
Ar flow	3 sccm
Pressure and Temperature	
Platen Chiller	$20°C$
Lid Temperature	$45°C$
Main Pressure	35 mTorr

Appendix F

List of Publications

Following list contains various publications during the author's PhD tenure at Bilkent University listed in descending order. Only the publications related to CMUT technologies are included in this thesis.

A. Journal Publications

1. **T. M. Khan**, A. S. Taşdelen, M. Yilmaz, A. Atalar and H. Köymen, "High-Intensity Airborne CMUT Transmitter Array With Beam Steering," *Journal of Microelectromechanical Systems*, vol. 29, no. 6, pp. 1537–1546, 2020, doi: 10.1109/JMEMS.2020.3026094.

2. A. Ali, K. Topalli, M. Ramzan, M. Alibakhshikenari, **T. M. Khan**, A. Altintas, P. Colantonio, "Optically Reconfigurable Planar Monopole Antenna for Cognitive Radio Application", *Microwave and Optical Technology Letters*, vol. 61, no. 4, pp. 1110–1115, 2019, doi: 10.1002/mop.31678.

3. A. Ali, K. Topalli, M Ramzan, **T. M. Khan**, A. Altintas, P. Colantonio, "Optical characterization of high and low resistive silicon samples suitable for reconfigurable antenna design", *Microwave and Optical Technology Letters*, vol. 61, no. 1, pp. 107–110, 2019, doi: 10.1002/mop.31506.

4. P. Deminskyi, A. Haider, H. Eren, **T. M. Khan**, N. Biyikli, "Area-Selective Atomic Layer Deposition of Noble Metals: Polymerized Fluorocarbon Layers as Effective Growth Inhibitors", ChemRxiv. Preprint, 2019, doi: 10.26434/chemrxiv.8970470.v3.

5. M. Khan; **T. M. Khan**, A. Tasdelen, M. Yilmaz, A. Atalar, H. Koymen, "Optimization of a Collapsed Mode CMUT Receiver for Maximum Off-Resonance Sensitivity", *Journal of Microelectromechanical Systems*, vol. 27, no. 5, pp. 921–930, 2018, doi: 10.1109/JMEMS.2018.2857444.

6. A. Ghobadi, **T. M. Khan**, O. O. Celik, N. Biyikli, A. K. Okyay, K. Topalli, "A performance-enhanced planar Schottky diode for Terahertz applications: an electromagnetic modeling approach", *International Journal of Microwave and Wireless Technologies*, vol. 9, no. 10, pp. 1905–1913, 2017, doi: 10.1017/S1759078717000940.

7. M. Ramzan, **T. M. Khan**, S. Bolat, M. Nebioglu, H. Altan, A. Okyay, K. Topalli, "Terahertz Bandpass Frequency Selective Surfaces on Glass Substrates Using a Wet Micromachining Process", *Journal of Infrared Millimeter, and Terahertz Waves*, vol. 38, no. 8, pp. 945–957, 2017, doi: 10.1007/s10762-017-0397-7.

8. A. Haider, P. Deminskyi, **T. M. Khan**, H. Eren, N. Biyikli, "Area-Selective Atomic Layer Deposition Using an Inductively Coupled Plasma Polymerized Fluorocarbon Layer: A Case Study for Metal Oxides", *The Journal of Physical Chemistry C*, vol. 120, no. 46, pp. 26393–26401, 2016, doi: 10.1021/acs.jpcc.6b09406.

B. Patent

9. A. K. Okyay, N. Biyikli, K. Topalli, **T. M. Khan**, A. Haider, P. Deminskyi, H. Eren, M. Yilmaz, "A Method for Area Selective Atomic Layer Deposition and Thereof", Republic of Turkey Patent Institute, TR 2016/08790, 2016.

C. Conference Proceedings

10. **T. M. Khan**, A. Tasdelen, M. Yilmaz, A. Atalar, H. Koymen, "Beam steering in a Half-Frequency driven Airborne CMUT transmitter array", Proceedings of IEEE IUS 2019, 6-9 Oct 2019, SEC, Glasgow, Scotland, UK, doi: 10.1109/ULTSYM.2019.8925995.

11. A. Atalar, M. Khan, **T. M. Khan**, A Tasdelen, M. Yilmaz, H. Koymen, "Increasing the receive sensitivity of a collapsed-Mode airborne CMUT in snap-back region", 17th conference on Micromachined Ultrasonic Transducers, 7-8 June 2018, MUT 2018 - CORSICA.

12. **T. M. Khan**; A. Ghobadi; O. Celik; C. Caglayan; N. Biyikli; A. Okyay; K. Topalli; K. Sertel, "On-chip characterization of THz Schottky diodes using non-contact probes", Proceedings of 2016 41st International Conference on Infrared, Millimeter, and Terahertz waves (IRMMW-THz), doi: 10.1109/IRMMW-THz.2016.7758606.

13. A. Haider, P. Deminskyi, M. Yilmaz, **T. M. Khan**, H. Eren, and N. Biyikli, "Nano-Scale Selective Deposition of TiO2 via Polymers as Growth Inhibition Surfaces", MRS Fall Meeting, Boston, MA, Nov 27 – Dec 2 (2016).

14. A. Haider, P. Deminskyi, **T. M. Khan**, H. Eren, M. Yilmaz, S. Altuntas, F. Buyukserin, N. Biyikli, "Area-Selective Atomic Layer Deposition Using Inductively Coupled Plasma Polymerized C4F8 Layer – A Case Study for Metal-Oxides", MRS Fall Meeting, Boston, MA, Nov 27 – Dec 2 (2016)

15. **T. M. Khan**, M. Yilmaz, K. Topalli, N. Biyikli, "Custom Fabricated MEMS-based Microgripper for Biological Cell Characterization", Abstracts of 3rd International Congress on Biosensors (2016)