

Compact and Wideband CPW Wilkinson Power Dividers for GaN MMIC Applications

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Abstract—This paper presents two types of modified CPW Wilkinson power dividers at X-band using GaN MMIC technology on a SiC substrate. Lumped element equivalents of the transmission line arms are used and they are capacitively loaded to achieve a reduced circuit size of $\lambda/14 \times \lambda/8$. A symmetrical series *RLC* circuit in the isolation network is used to compensate for the bandwidth degradation after circuit miniaturization maintaining a fractional bandwidth of 29% for input/output return losses and isolation better than 20 dB with an extra insertion loss less than 0.35 dB.

Keywords—coplanar waveguide, compact power divider, Wilkinson power divider, MMICs.

I. INTRODUCTION

The Wilkinson power divider is a symmetrical device commonly used in microwave engineering to divide the input signal into equiphase and equiamplitude output signals. It provides good port matching and high isolation between the output ports while maintaining a low loss operation [1]. Although the Wilkinson power divider is preferred for monolithic microwave integrated circuits (MMIC) due to its ease of fabrication and planar structure, it is not useful in wideband applications and consumes valuable chip area because of its quarter-wave length arms. In order to address the first issue and improve the bandwidth, multisection hybrids with a number of cascaded transmission line arms and bridging resistors [2] and a modified isolation network with a series *RLC* circuitry [3], [4] have been proposed. Regarding the second issue to reduce the circuit size, lumped element π -network and T-network equivalents of the quarter-wave length arms [5], [6] and capacitive or inductive line loading [7], [8] have been suggested. On the one hand, techniques proposed for wideband operation require more circuit area; on the other hand, modifications suggested on the original divider to reduce its size decrease the bandwidth of operation.

In this work, two types of modified power dividers are proposed. Type-I is a miniaturization of the original Wilkinson power divider using lumped elements achieving a small circuit area. Type-II is a further miniaturized lumped element Wilkinson power divider utilizing capacitive loading at the ends of the divider arms while preserving operational bandwidth by having a symmetrical series *RLC* circuitry in the isolation network. Analytical design equations of the component values for proposed dividers are presented. Dividers of both types are designed at X-band

using coplanar waveguide (CPW) technology with practical design considerations. The measured input/output return loss, isolation and insertion loss parameters of the fabricated dividers are presented.

II. ANALYSIS AND DESIGN

A. Type-I Power Divider

Proposed network for the divider of type-I is depicted in Fig. 1. Quarter-wave transmission line arms of the Wilkinson power divider are replaced by their lumped element T-network equivalents. The bridging isolation network is composed of a resistor only. The required inductor and capacitor values are found by equating the ABCD parameters of the Wilkinson divider transmission line arm given in (1) and ABCD parameters of the lumped element T-network given in (2).

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos \beta l & jZ_c \sin \beta l \\ jY_c \sin \beta l & \cos \beta l \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 - X_L B_C & jX_L \\ jX_L(2 - X_L B_C) & 1 - X_L B_C \end{bmatrix} \quad (2)$$

where

$$Z_c = \sqrt{2}Z_0, \quad \beta l = \pi/2 \quad (3)$$

$$X_L = 2\pi f_0 L_T, \quad B_C = 1/2\pi f_0 C_T \quad (4)$$

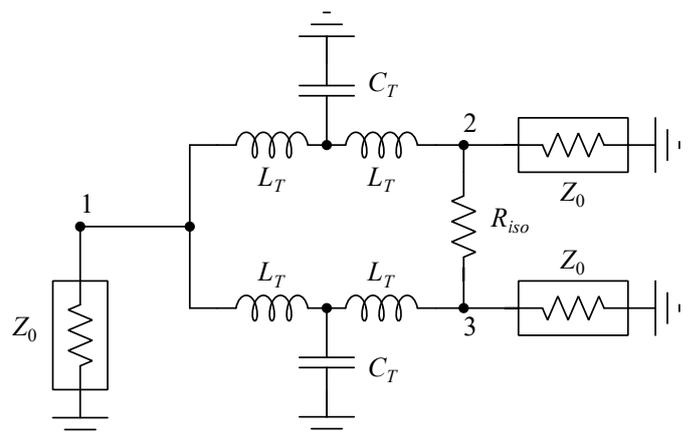


Fig. 1. Proposed network for type-I divider.

Therefore, the required component values are

$$L_T = \frac{\sqrt{2}Z_0}{2\pi f_0} \quad (5)$$

$$C_T = \frac{\sqrt{2}}{4\pi f_0 Z_0} \quad (6)$$

$$R_{iso} = 2Z_0 \quad (7)$$

where f_0 is the design center frequency and Z_0 is the characteristic impedance of the three ports. Following the described procedure, a divider at X-band is designed considering that the divider width must be less than the MMIC width and divider length is the critical dimension for total chip area. Short transmission lines are added at the input port and at the lumped element divider arms to improve bandwidth performance. Following the optimization process, shunt capacitors (C_T) are eliminated due to parasitic capacitances of the inductors. Total circuit size is $1.14 \text{ mm} \times 1.91 \text{ mm}$ ($0.09\lambda \times 0.14\lambda$). The implemented divider is shown in Fig. 2.

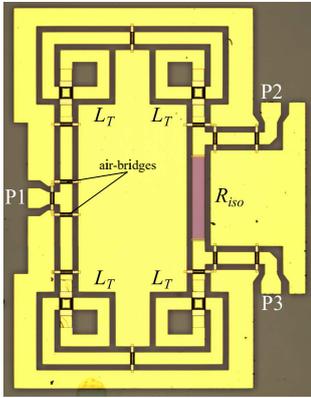


Fig. 2. Microscope image of the fabricated power divider of type-I.

B. Type-II Power Divider

In Fig. 3, the proposed network for the divider of type-II is presented. Shunt capacitors are added at the ends of the transmission line arms of the Wilkinson power divider to reduce their length. In order to compensate for the isolation bandwidth degradation a symmetrical series RLC circuit is used in the isolation network instead of a single resistor. The inductor and capacitor in the isolation network resonate at the design center frequency. Considering symmetry of the network, even-odd mode analysis is carried out to find component values for perfect port matching at all ports and perfect isolation between output ports at the design center frequency [9].

$$C_1 = \frac{\sqrt{2} \cos \beta l}{2\pi f_0 Z_0} \quad (8)$$

$$C_2 = \frac{\sqrt{2} \cos \beta l}{4\pi f_0 Z_0} \quad (9)$$

$$L_{eq} = \frac{\sqrt{2}Z_0}{2\pi f_0(1 + \cos \beta l)} \quad (10)$$

$$C_{eq} = \frac{\sqrt{2} \sin^2 \beta l}{4\pi f_0 Z_0} \quad (11)$$

$$R_{iso} = 2Z_0 \quad (12)$$

$$4\pi^2 f_0^2 L_{iso} C_{iso} = 1 \quad (13)$$

where f_0 is the design center frequency, βl is the electrical length of the reduced arm at the design center frequency, and Z_0 is the characteristic impedance of the system.

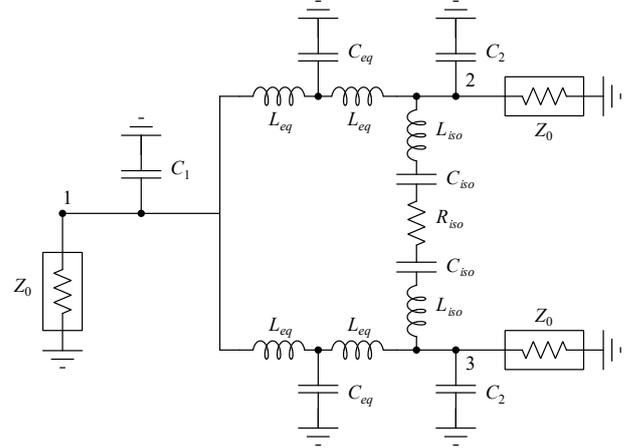


Fig. 3. Proposed network for type-II divider.

For the practical design case at X-band, isolation network is tuned for maximum bandwidth. Shunt capacitors C_{eq} and C_2 are obtained by inductor parasitic and tee junction capacitances. Inductors in the isolation arm are realized by high impedance transmission lines. The additional circuitry in the isolation network not only compensates for the bandwidth, but also increases the distance between the output ports without additional loss. The output ports need to be separated anyway for physical isolation and practical use in MMICs. Total circuit size is $0.93 \text{ mm} \times 1.66 \text{ mm}$ ($0.07\lambda \times 0.13\lambda$) with 29% size reduction compared to the divider of type-I. The implemented divider is shown in Fig. 4.

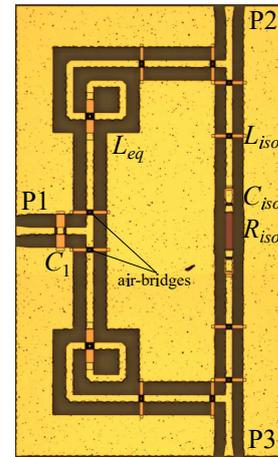


Fig. 4. Microscope image of the fabricated power divider of type-II.

III. FABRICATION AND EXPERIMENTAL RESULTS

The modified Wilkinson power divider designs are fabricated with a GaN on SiC MMIC process with a substrate thickness of $100\ \mu\text{m}$ and dielectric constant of 9.7. Two layers of interconnection metals and air-bridges are formed using gold. Thin film resistors are made of Ni-Cr with a sheet resistance of $15\ \Omega/\square$. Metal-insulator-metal (MIM) capacitors are fabricated using Si_xN_y as an insulator with dielectric constant of 7.35. Quarter-wave length at 10 GHz is approximately 3.3 mm for reference.

3-port calibration and measurements are performed using Cascade¹ RF wafer probe station, GGB² GSG150 picoprobes and R&S³ ZVA40 vector network analyzer. Simulation results⁴ and measurement results of the dividers are in good agreement. Figs. 5–8 show the simulated and measured S-parameters of divider type-I. The measured input reflection and output reflection coefficients are less than $-20\ \text{dB}$, the isolation is at least 20 dB and the excess insertion loss is less than 0.35 dB from 8.3 GHz to 10.6 GHz with a fractional bandwidth of 24%. The amplitude imbalance and phase imbalance at the output ports are less than 0.1 dB and 0.8° , respectively. We measured three more power dividers and they show similar performance.

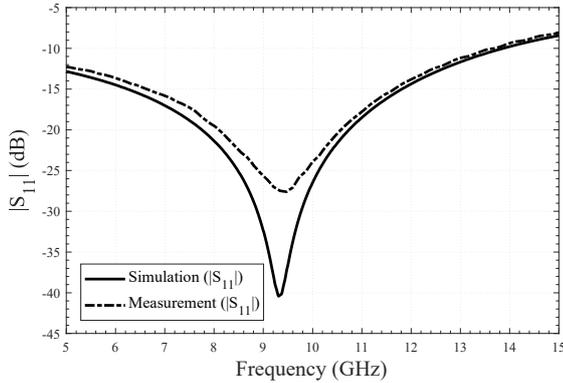


Fig. 5. Simulated and measured values of $|S_{11}|$ of divider type-I as a function of frequency.

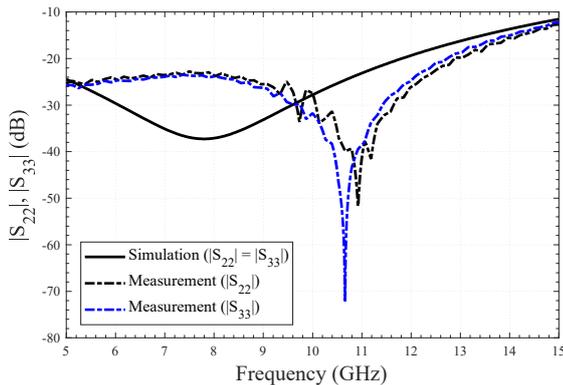


Fig. 6. Simulated and measured values of $|S_{22}|$ and $|S_{33}|$ of divider type-I as a function of frequency.

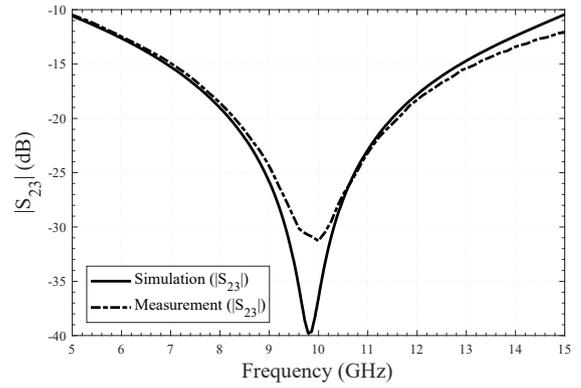


Fig. 7. Simulated and measured values of $|S_{23}|$ of divider type-I as a function of frequency.

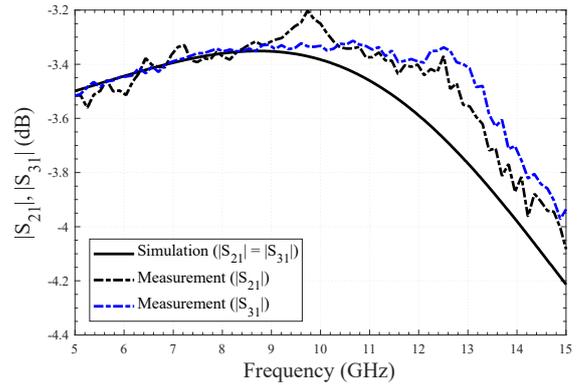


Fig. 8. Simulated and measured values of $|S_{21}|$ and $|S_{31}|$ of divider type-I as a function of frequency.

Figs. 9–12 compare the simulated and measured S-parameters of divider type-II. According to the measurement results, the input and output return losses are better than 20 dB, the isolation is at least 20 dB and the extra insertion loss is less than 0.35 dB from 8.9 GHz to 11.9 GHz with a fractional bandwidth of 29%. The amplitude imbalance and phase imbalance at the output ports are less than 0.05 dB and 0.4° , respectively. Simulation and measurement results for both dividers have been summarized in Table 1.

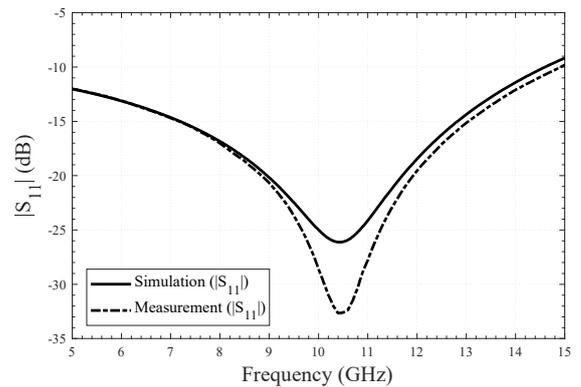


Fig. 9. Simulated and measured values of $|S_{11}|$ of divider type-II as a function of frequency.

¹Cascade Microtech, Inc., Beaverton, OR 97008, USA

²GGB Industries, Inc., Naples, FL 34104, USA

³Rohde & Schwarz GmbH & Co. KG, Munich, Germany

⁴ADS 2016.01, Keysight Technologies, Inc., Santa Rosa, CA 95403, USA

Table 1. Simulated vs. measured input return loss, output return loss, isolation and insertion loss bandwidths for both types of power dividers.

| Performance Parameter | Input RL (20 dB) | | Output RL (20 dB) | | Isolation (20 dB) | | Excess IL (0.45 dB) | | Operational Region | |
|-----------------------|------------------|---------|-------------------|---------|-------------------|---------|---------------------|---------|--------------------|---------|
| | BW (GHz) | FBW (%) | BW (GHz) | FBW (%) | BW (GHz) | FBW (%) | BW (GHz) | FBW (%) | BW (GHz) | FBW (%) |
| Type-I Simulation | 7.8 – 10.7 | 31 | 4.0 – 11.8 | 99 | 8.2 – 11.5 | 34 | 5.9 – 10.9 | 60 | 8.2 – 10.7 | 26 |
| Type-I Measurement | 8.1 – 10.6 | 27 | 3.5 – 12.8 | 114 | 8.3 – 11.6 | 33 | 6.2 – 12.8 | 69 | 8.3 – 10.6 | 24 |
| Type-II Simulation | 9.0 – 11.7 | 26 | 7.2 – 13.6 | 62 | 8.3 – 12.4 | 39 | 6.3 – 12.4 | 65 | 9.0 – 11.7 | 26 |
| Type-II Measurement | 8.9 – 11.9 | 29 | 8.5 – 16.3 | 63 | 8.0 – 12.0 | 40 | 6.1 – 13.2 | 74 | 8.9 – 11.9 | 29 |

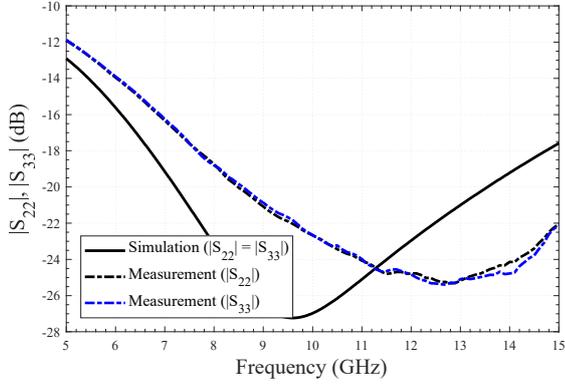


Fig. 10. Simulated and measured values of $|S_{22}|$ and $|S_{33}|$ of divider type-II as a function of frequency.

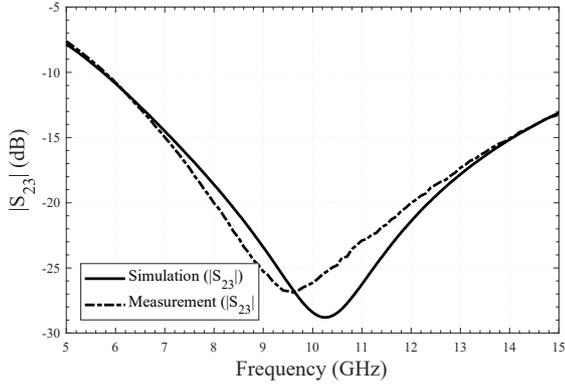


Fig. 11. Simulated and measured values of $|S_{23}|$ of divider type-II as a function of frequency.

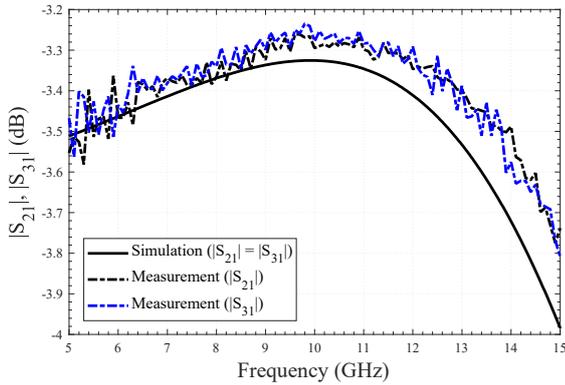


Fig. 12. Simulated and measured values of $|S_{21}|$ and $|S_{31}|$ of divider type-II as a function of frequency.

IV. CONCLUSION

Two types of miniaturized lumped element Wilkinson power dividers are proposed, analyzed and design equations are presented. Design examples at X-band are fabricated using GaN on SiC CPW MMIC technology. Divider length reduction up to 72% is achieved compared to the original Wilkinson power divider without bandwidth degradation thanks to lumped element T-network equivalents, capacitive loading and a symmetrical series RLC circuit in the isolation network. The measured circuits demonstrate at least 20 dB port matching, at least 20 dB isolation and at most 0.35 dB excess insertion loss from 8.9 GHz to 11.9 GHz with a fractional bandwidth of 29%.

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