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High-Frequency Performance of Submicrometer Transistors That Use Aligned Arrays of Single-Walled Carbon Nanotubes

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ABSTRACT

The unique electronic properties of single-walled carbon nanotubes (SWNTs) make them promising candidates for next generation electronics, particularly in systems that demand high frequency (e.g., radio frequency, RF) operation. Transistors that incorporate perfectly aligned, parallel arrays of SWNTs avoid the practical limitations of devices that use individual tubes, and they also enable comprehensive experimental and theoretical evaluation of the intrinsic properties. Thus, devices consisting of arrays represent a practical route to use of SWNTs for RF devices and circuits. The results presented here reveal many aspects of device operation in such array layouts, including full compatibility with conventional small signal models of RF response. Submicrometer channel length devices show unity current gain (f_i) and unity power gain frequencies (f_{max}) as high as ∼5 and ∼9 GHz, respectively, with measured scattering parameters (*S*-parameters) that agree quantitatively with calculation. The small signal models of the devices provide the essential intrinsic parameters: saturation velocities of 1.2×10^7 cm/s and intrinsic values of f_i of ∼30 GHz for a gate length of 700 nm, increasing with decreasing length. The results provide clear insights into the challenges and opportunities of SWNT arrays for applications in RF electronics.

Fundamental experimental[1] and theoretical studies[2,3] suggest that single-walled carbon nanotubes (SWNTs) electronic devices can respond on picosecond time scales, corresponding to frequencies approaching the terahertz regime. Transistors that exploit the small capacitances[4] (∼100 aF/μm), large mobilities[5−8] (∼10^4 cm^2/(V s)), and high degree of linearity[9] of SWNTs to achieve amplifiers,[10] oscillators,[11] circuits,[12,13] and systems[14] with operating speeds in this range are of considerable interest. Evaluating the scattering parameters (*S*-parameters) provides the most established and accepted procedure for determining the frequency responses in individual transistors. For devices that use single SWNTs, such measurements are confounded by parasitic capacitances and large impedance mismatches between the instrumentation and the devices. De-embedding and other procedures can, in principle, minimize the effects of parasitics but only with substantial uncertainties, mainly because the capacitances of the SWNTs are orders of magnitude smaller than the parasitics.[15−19] The use of multiple SWNTs deposited from solution in random or partially aligned configurations[15,20] can reduce some of these problems, but the low output resistances and limited switching capabilities of reported devices (due, presumably, to a preponderance of metallic SWNTs in the channel) are undesirable for measurements and practical devices.[21,22] Length scaling of properties has not been

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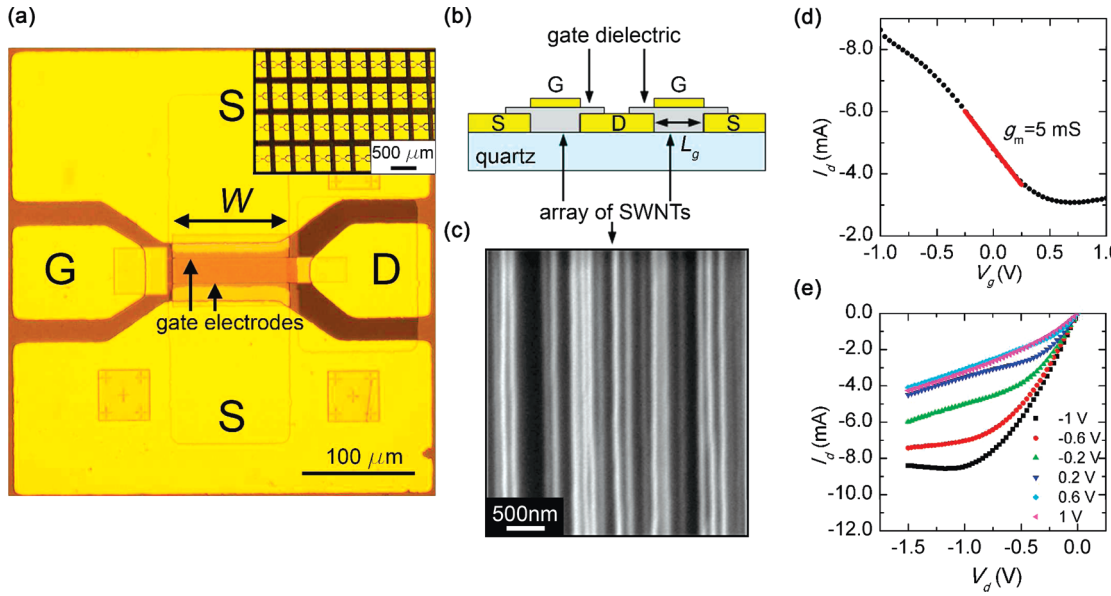

Figure 1. Optical and scanning electron micrographs, cross sectional schematic illustration, and representative data from RF SWNT array transistors formed on a quartz substrate: (a) optical microscope images of a typical device and a collection of devices (inset) showing the RF probe pad configuration and double gate layout. The channel regions of the transistors were fabricated by two electron beam lithography processes; the contact pads with ground−signal−ground coplanar structure were formed by photolithography. The dark region at the center of the device shown in (a) is due to the gate dielectric (50nm thick HfO_2). The channel width (W) and length (L_g) of this device are 100 μm and 700 nm, respectively. (b) Schematic cross sectional illustration of the device layout. (c) Scanning electron micrographs of aligned SWNTs used for the fabricated devices. The nanotube density is 5 tubes/μm. (d) Transfer characteristics of the device shown in panel b, measured at a drain bias (V_d) of −1 V. (e) Output characteristics of this device, for gate voltages (V_g) between −1 and 1 V, measured in steps of 0.4 V.

reported for either type of device. Here we present systematic studies of radio frequency (RF) transistors each of which incorporates large numbers (i.e., hundreds) of perfectly aligned, parallel SWNTs. Due to their reduced contribution from parasitic capacitances for practical channel widths (greater than micrometers) and dramatically improved impedance match to common measurement systems, these devices represent an attractive approach to SWNT RF electronics. Additionally, the comparatively high level of reproducibility in the device properties, the large transconductances, and low impedances allow comprehensive evaluation of their modes of operation, though some degree of uncertainty remains due to variations in nanotube density, distributions of nanotube diameters, and relative populations of semiconducting and metallic nanotubes. The results establish quantitatively accurate and predictive small signal RF device models that provide guidelines for implementation of SWNTs in high-frequency electronics.

Figure 1a shows an optical micrograph of a characteristic device on a quartz substrate, which involves hundreds of perfectly aligned, SWNT in a linear array (at densities of 2 or 5 SWNTs/μm) grown by chemical vapor deposition (CVD).[23−25] The device layout consists of two separately fabricated parts: the probing pads and the active device. The active region was defined first. It employs a double channel configuration in which two gate electrodes and two source electrodes surround a common drain electrode. Fabrication involved two electron beam lithography (Raith, eLine) processes to define the source/drain and the gate levels with accurate registration to maximize the width of the gate and to minimize the capacitances associated with overlap between the source/drain and the gate. A layer of HfO_2 (50 nm) deposited by electron beam evaporation (Temescal CV-8) served as the gate dielectric. Photolithography defined comparatively large probing pads that provided electrical contact to the smaller features of the active region. The configuration of the pads (3 nm Ti/100 nm Au), as defined by photolithography, matches that of conventional ground−signal−ground (GSG) microwave probes (150 μm pitch). Figure 1a,b presents an optical micrograph of a representative device and a cross sectional schematic illustration, respectively. An array of devices was formed in the manner described above (Figure 1a inset). These devices had channel lengths (L_g) between 900 and 300 nm and channel widths (W) between 100 and 25 μm. The double channel geometry means that the total device width used for calculations is twice W. For the remainder of the text, W will be used for the purposes of discussion. DC performance was evaluated using conventional setups (Agilent E5270B Precision Measurement Mainframe). The source monitor units were connected through two Agilent 11612B bias networks to a pair of 150 μm pitch Picoprobe microwave probes, just prior to high-frequency measurements. Figure 1d,e shows transfer and output characteristics of a typical device (L_g = 700 nm; W = 100 μm; 5 SWNT/um), respectively. The devices show p channel behavior, with a moderate degree of ambipolar operation as is often observed with top-gated SWNT transistors, either in array[8] or in single tube[26] formats. For the device of Figure 1, the on-state current is ∼8.5 mA at a drain bias (V_d) of −1 V. The peak transconductance (g_m) is ∼5 mS (25 mS/mm of channel width), at a drain bias of −1 V and gate bias (V_g) of 0 V. For the same bias, the output resistance,

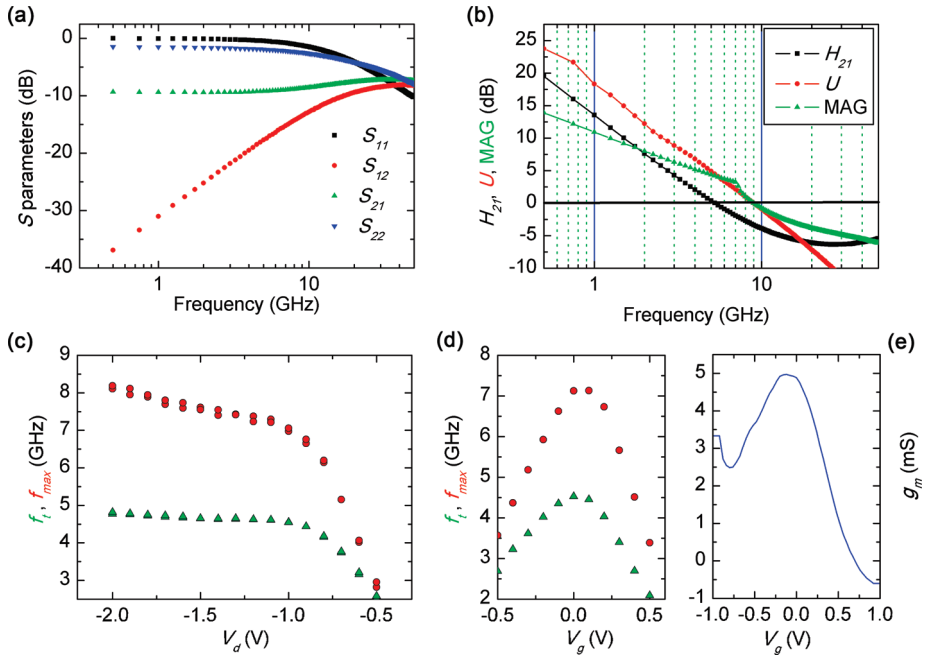

Figure 2. RF characteristics of a SWNT array transistor whose DC characteristics appear in Figure 1: (a) amplitude plots of *S*-parameters for frequencies between 0.5 and 50 GHz; (b) amplitude plots for current gain (H_{21}), unilateral power gain (U), and maximum available gain (MAG) for frequencies between 0.5 and 50 GHz. The unity current gain frequency, f_t, and unity power gain frequency, f_{max}, are around 5 and 9 GHz, respectively. (c) Plots of f_t and f_{max} as a function of drain bias (V_d) at a gate bias (V_g) of 0 V. (d) Plots of f_t and f_{max} as a function of V_g at $V_d = -1$ V. (e) Plot of transconductance, as calculated from the slope of transfer curve in Figure 1d, as function of V_g. The maximum frequencies and the peaks in transconductance appear at approximately the same V_g, as expected.

R_o, is ~520 Ω, corresponding to a gain ($G = R_o g_m$) of ~2.6. With interdigitated devices, it is possible to reach high values of g_m, up to 80 mS, and output currents, up to 0.1 A (Figure S1, Supporting Information). In all cases, the ratio of the on-state to off-state current is close to three, due to the substantial (1/3) population of metallic nanotubes.

To determine the high-frequency behavior, we measured the *S*-parameters directly, using standard procedures with a vector network analyzer over a frequency range of 0.5−50 GHz (Agilent 8364A). Calibration was performed to the probe tips using off-wafer short-open-load-through (SOLT) standards on a GGB Industries CS-5 calibration substrate. Figure 2a shows the *S*-parameters for the device presented in Figure 1d,e. Figure 2b presents current gain (H_{21}), maximum available gain (MAG), and unilateral power gain (U), all derived from the *S*-parameters at a drain bias of −1 V and gate bias of 0 V. The details of these conversions can be found in the Supporting Information. These results indicate a unity current gain frequency, f_t, and a unity power gain frequency, f_{max}, of 5 and 9 GHz, respectively; f_t corresponds to the frequency for which the drain and gate currents are equal, and thus, their ratio is unity. At this frequency the current gain, H_{21}, crosses the 0 dB line. The f_{max} parameter is the maximum frequency of oscillation, and it is determined by the point at which the unilateral power gain (U) is equal to 0 dB. Figure 2c presents the dependence of f_t and f_{max} on drain bias. With increasing negative bias (−0.5 to −0.9 V), both f_t and f_{max} increase linearly until they saturate at a drain bias of approximately −1 V, which corresponds to an electric field of ~5 kV/cm. This electric field approaches that needed to saturate the carrier velocity.[27]

Figure 2d presents the dependence of f_t and f_{max} on gate bias. Both f_t and f_{max} reach maximum values near $V_g \approx 0$ V, coinciding with the peak in g_m (Figure 2e, from DC measurements), as expected. If we assume that $f_t \approx g_m/[2\pi(C_{gs} + C_{gd})]$, where C_{gs} and C_{gd} are the capacitance between the gate and source electrodes and the gate and drain electrodes, respectively,[6,19] then we estimate that $C_{gs} + C_{gd} \approx 171$ fF at the point of maximum g_m. This expression is reasonable when parasitic resistances are small relative to output resistance, which is the case (shown subsequently) for these devices.

Scaling studies provide additional information. Figure 3a,b shows the dependence of f_{max} and f_t, respectively, on L_g for two different device sets with average tube densities of ~2 SWNT/μm and 5 SWNT/μm, each with $W = 100$ μm. Both f_{max} and f_t increase with decreasing L_g, qualitatively consistent with expectation. The precise form of the scaling with channel length cannot be determined conclusively from these data. Some insights can, however, be obtained by noting that the transconductances determined from DC measurements (extracted in the same manner as Figure 2e), as well as those extracted through analysis of RF data (as described subsequently) yield similar values, with only a weak dependence on L_g (Figure S2a, Supporting Information). This is possibly due to the combined effects of contact resistance, near ballistic transport, and systematic shifts in threshold voltage that we observed to increasingly positive values with decreasing channel length. As a result, one can conclude that for these devices, increases in operating frequency with decreasing L_g result mainly from decreases in gate capacitances, C_{gs} and C_{gd}, rather than increases in g_m, as is

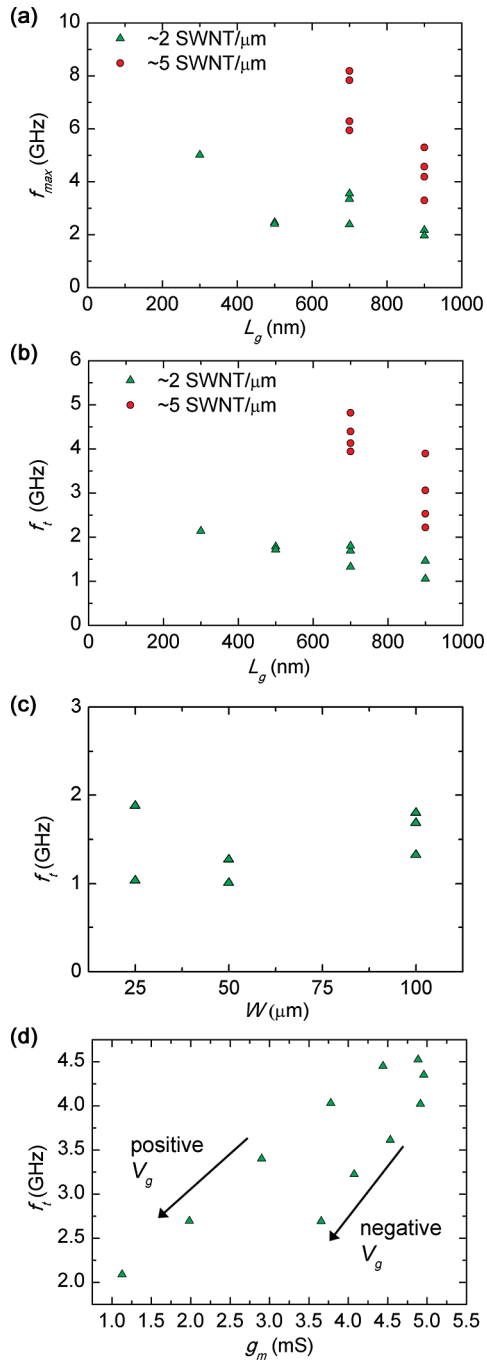

Figure 3. Variation of response frequencies f_t and f_{max} with channel length (L_g) and channel width (W) and dependence of f_t on g_m: (a, b) Plots of f_t and f_{max} evaluated at $V_d = -2.5$ V and $V_g = 0$ V as a function of L_g for devices with $W = 100$ μm; (c) Plot of f_t at $V_d = -2.5$ V and $V_g = 0$ V as a function of W for $L_g = 700$ nm. All devices here have a nanotube density of 2 SWNTs/μm. (d) Plot of f_t as a function of g_m obtained from data shown in Figure 2d,e.

confirmed by the RF device analysis presented next. The scaling with W is as expected: g_m, C_{gs}, and C_{gd} all increase roughly linearly with increasing W (Figure S4, Supporting Information), thereby yielding values of f_t that are independent of W, as shown in Figure 3c for devices with $L_g = 700$ nm and a density of ~2 SWNT/μm. Additional information can be obtained by examining the dependence of f_t on g_m, as shown in Figure 3d, derived from data collected at various V_g (Figure 2d,e). The approximate linear scaling that is observed over certain regions is consistent with values of C_{gs} and C_{gd} that do not vary strongly with V_g, thereby suggesting a relatively small contribution of the semiconducting tubes to the overall gate capacitance, as is confirmed through analysis described in the following.

To understand more fully the nature of device operation, we used hybrid-pi models, common for two-port small-signal response in conventional transistor and circuit modeling, in which the behavior around a bias point is analyzed in the context of an equivalent circuit with linear physical quantities (such as capacitance, inductance, and resistance). For sufficiently small signal variations, the response of the circuit is assumed to be linear with a behavior consistent with this model. The main parameters for the model, which was implemented with commercial software tools designed for this purpose (Agilent Advanced Design System), are the output resistance (R_o), the transconductance (g_m), the inductances (L') and resistances (R) of each of the metal electrodes (i.e., L'_g, R_g, L'_d, R_d, L'_s, and R_s, where subscripts g, d, and s refer to gate, drain, and source, respectively), and the capacitances between gate and drain (C_{gd}), gate and source (C_{gs}), and drain and source (C_{ds}). L'_s is also set to zero due to the minimal inductance expected based on the layout of the source electrode. The remaining parameters and their topology within the model are shown in Figure 4a. The modulation of the semiconducting tubes by the gate is represented by a voltage-controlled current source located between the source and drain.

In principle, the parameters extracted from analysis of such a model can provide physically meaningful characteristics of the devices. The relatively large number of variables (10) and the complex topology of the error surface associated with the fitting process, however, create difficulties. To reduce the number of free variables, we performed measurements on test structures with geometries exactly the same as those of the active devices but without the SWNTs and used information from these models as well as other techniques to constrain other parameters of the model. The test structures, which we refer to as "open" devices, were evaluated using the same frequency-dependent measurements as the active devices, and with similar models (parameters and topology in Figure S3a, Supporting Information), for the purpose of de-embedding and to evaluate the parasitic capacitances due only to the electrode geometry. An optimized fit of the data to a somewhat simpler model (eight free variables), shows good agreement (Figure S3b, Supporting Information), up to 20 GHz. The resulting parameters (Table S1, Supporting Information) provide information useful for fitting of data from the active devices. In particular, we can use the values of R_s, R_d, R_g, L'_d, and L'_g determined from the open devices for modeling the active devices (the resistances are within a factor of 3 of values calculated using the electrode geometries and bulk resistivities;[28] Table S1, Supporting Information). Although the capacitances from the "open" devices cannot be used in a similar manner, due to the absence of contributions from the SWNTs, they can be used with the results from the active device to yield insights

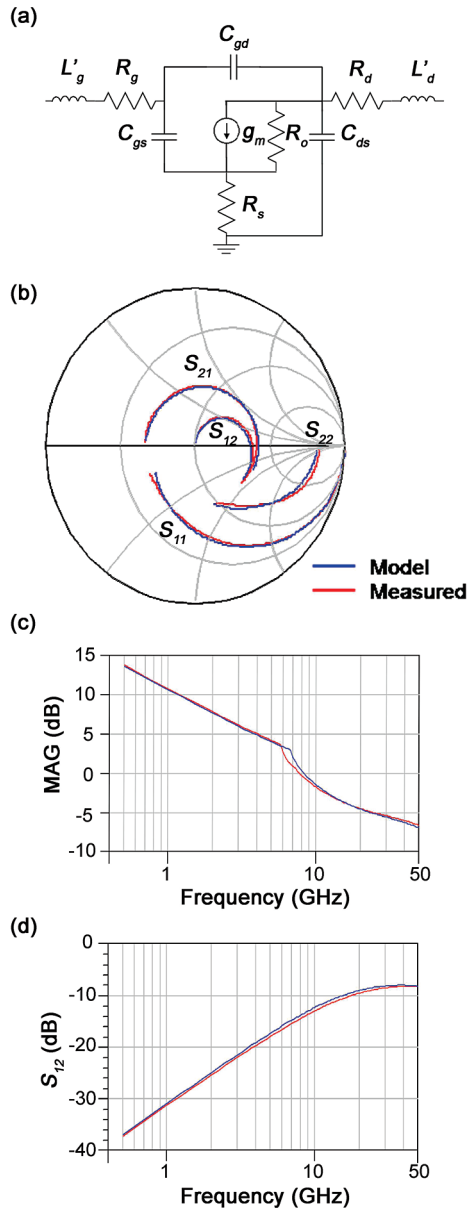

Figure 4. Measured and modeled RF response of a SWNT array transistor in a 50 Ω system with channel width (W) of 100 μm and a channel length (L_g) of 700 nm, biased at $V_g = 0$ and $V_d = -1$ V. The device here has a nanotube density of 5 SWNTs/μm. (a) Circuit schematic of the model, with key variables identified. (b) Smith chart of measured and simulated S-parameters. (c) Frequency dependence of MAG, the gain if the device were impedance matched. (d) Frequency dependence of S_{12}, the reverse isolation. Here, the single-pole roll off with decreasing frequency is due to C_{gd}. C_{gd} is directly extracted at low frequencies, in this case at 0.2 GHz.

about the relative contributions to device capacitances, as described subsequently.

Further constraints can be imposed on the active device variables. For example, C_{gd} can be obtained from the single-pole roll off of S_{12} (Figure 4d) with decreasing frequency. At low frequencies C_{gd} is the dominant element determining reverse feedback through the transistor; C_{gd} is manually adjusted to make the modeled and measured S_{12} curves coincide at 200 MHz. The output resistance was set to the DC value, $R_o = 520$ Ω. Collectively, these considerations

Table 1. Values for Device Parameters Calculated from RF Modeling

L'_g	L'_d	R_g	R_s	R_d	R_o	C_{gs}	C_{gd}	C_{ds}	g_m
pH	pH	Ω	Ω	Ω	Ω	fF	fF	fF	mS
50	50	16	0	24	520	65	52	15	3.8

allow for a reduction of the fitting variables from 10 to 3, by fixing R_s, R_d, R_g, R_o, L'_d, L'_g, and C_{gd}. We found that the three remaining parameters could be determined reliably by fitting, independent of starting values, to within a few femtofarads (C_{gs} and C_{ds}) and tenths of millisiemens (g_m). For the final optimization, the value of C_{gd} was adjusted slightly following fitting of other parameters to improve the overall fit.

The final optimization yielded good fits to S-parameter data (Figure 4b,d) measured from the device discussed in Figures 1 and 2 over two decades of frequency, up to 50 GHz. The maximum available gain, which is derived from these S-parameters (Figure 4c), also shows excellent agreement. The values found for the optimization parameters appear in Table 1. As mentioned earlier, g_m extracted from RF analysis are similar to DC values (Figure 2e). The same model was used to evaluate the channel length (Figure S2, Supporting Information) and channel width (Figure S4, Supporting Information) scaling of parameters for the devices presented in Figure 3 with 2 SWNT/μm. In all cases, values of g_m extracted in this manner correspond well to those determined from DC measurements (also in Figure S2 and S4, Supporting Information), indicating no systematic variation with channel length. The capacitances determined for the active device are similar to those for the open device (Table S1, Supporting Information), consistent with the conclusion that contributions due to semiconducting nanotubes are relatively small compared with parasitics, as also suggested by the relationship between f_t and g_m (Figure 3d). The value of $C_{gs} + C_{gd}$ from this RF analysis yields ~135 fF, which is comparable to that determined from direct measurements of f_t and g_m and the approximate relationship between these quantities, as discussed previously. Parameters C_{gs} and C_{gd} were also found to scale with increasing channel length and width (Figure S2 and S4, Supporting Information), as is expected with an increasing gate area. As mentioned previously, this scaling is most likely responsible for the trends observed in f_t.

To gain additional insights into the capacitances, we examined their dependence on V_d.[29] Because the devices studied here operate in depletion mode, at small source/drain bias (e.g., $-0.5 < V_d < 0$ V), the devices are in the linear response regime, such that we can assume that the charge distributions on the SWNTs are spatially symmetric. Figure 5a shows the output response due only to semiconducting SWNTs, generated by subtracting the current due to metallic SWNTs (i.e., the device in its off state). At high bias (e.g., $-1.5 < V_d < -0.5$ V), the devices are in saturation and the charge distributions are asymmetric (Figure 5). Figure 5b shows C_{gs} and C_{gd}, extracted via fitting of RF data for the device described in Figures 1 and 2, as described above, as a function of V_d. In the linear region, C_{gs} and C_{gd} have similar values, which we write as $(C_p + C_{ox})/2$, where C_{ox} is the

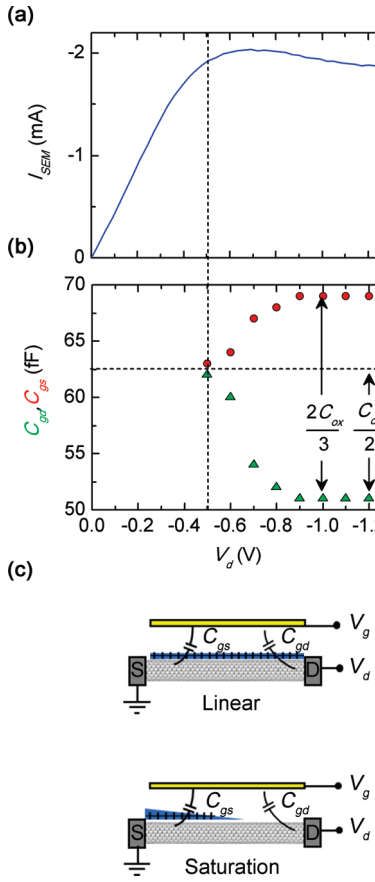

Figure 5. Capacitance contributions in SWNT array transistors: (a) Plot of drain current (I_d) associated with the semiconducting SWNTs (i.e., $I_{sem} = I_d - I_{off}$ where I_{off}, the off state current, is associated with metallic tubes and is extracted from the minimum in current as a function of V_g) for a transistor with $L_g = 700$ nm at $V_g = 0$ V as a function of drain voltage, V_d. The device saturates at a drain bias of $V_d = -0.5$ V. The device here has a nanotube density of 5 SWNT/μm. (b) Plot of C_{gd} and C_{gs}, extracted from RF modeling, as function of drain voltage. (c) Schematic representation of charge distribution on SWNT at linear and saturation regimes of behavior.

capacitance contribution associated with the coupling of the semiconducting tubes to the gate electrode and C_p is associated with all other contributions (i.e., metallic tubes, fringing fields, overlaps, etc). In saturation, as the drain voltage is decreased, C_{gd} decreases, due to the asymmetry of the charge distribution; the value of C_{gd} in this regime gives C_p directly.[29] By similar reasoning, C_{gs} increases to $2C_{ox}/3 + C_p$ in saturation. This analysis yields the parasitic capacitance, $C_p \approx 51$ fF, and the gate oxide capacitance, $C_{ox} \approx 22$ fF. Calculations that include full effects of fringing fields and screening of tubes in the arrays and the quantum capacitances, with device dimensions reported previously and a dielectric constant of ~14 for the HfO_2, yield a computed C_{ox} of ~30−40 fF for tube densities of 4−5 SWNTs/μm, with negligible effects of nonuniform tube−tube spacings in the array. See Supporting Information for details. The quantity C_p has contributions from fringing fields between the metal electrodes (C_f) and from the metallic SWNTs (C_m), the latter of which we consider also as parasitic because these tubes contribute capacitance without contributing to g_m. If we assume a 2:1 ratio of semiconducting to metallic tubes,[30] then the parasitic capacitance of the metallic tubes is $C_m \approx 10$ fF, which yields $C_f \approx 40$ fF. This value of fringing capacitance is in the same range as values obtained by finite element modeling (~55 fF, Figure S11, Supporting Information). These parameters, together with the carrier velocity (v_s), determine the intrinsic switching time of the device. For a short channel device, the carrier velocity can be written as $v_s = g_m L_g / C_{ox}$. With parameters outlined above, this equation yields $v_s \approx 1.2 \times 10^7$ cm/s, which agrees well with previous reported values ($\sim 2 \times 10^7$ cm/s).[27] The intrinsic cutoff frequency can be evaluated by considering a device that is free of parasitics, such that $f_t = g_m/(2\pi C_{ox})$. Here we find the intrinsic cutoff frequency to be ~30 GHz, which is at least 6 times higher than the measured devices, all of which are dominated by parasitics. This metric defines performance expected for a single nanotube transistor free of parasitics. In addition, it represents the upper limit achievable with array-based SWNT transistors with densities sufficiently high to eliminate the significance of the parasitics and with metallic SWNTs removed, thereby eliminating their contributions to capacitance.

In summary, we constructed high speed nanotube transistors from aligned arrays of hundreds of parallel nanotubes and assessed their performance by evaluating scattering parameters in the RF range. Interpretation of the results relied on small signal modeling of the RF response and on scaling analysis of properties in the DC and RF range. The results indicate that the gate capacitances, including significant contributions from parasitics for the devices examined here, have a dominant effect on the RF behavior and on f_t and f_{max} in particular. The relative contributions to this capacitance by semiconducting and metallic nanotubes as well as fringing fields between device electrodes were assessed. Performance not limited by parasitics (not including those associated with metallic tubes) corresponds to the case where $C_{ox} \gg C_f$. Devices that involve sufficiently high densities of SWNTs can reach this regime. Further improvements (~1.5× for the case when C_f is small) are possible by eliminating the metallic tubes and, therefore, their contribution to capacitance. These two conclusions define goals for future work on growth and purification of arrays of SWNTs for applications in high speed electronics.

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Supporting Information Available: Additional experimental and theoretical details. This material is available free of charge via the Internet at http://pubs.acs.org.

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