A Fully Integrated K-Band Power Amplifier Design Using Digital 0.18 μm CMOS Technology

A THESIS

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND

ELECTRONICS ENGINEERING

AND THE GRADUATE SCHOOL OF ENGINEERING AND SCIENCES

OF BILKENT UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

MASTER OF SCIENCE

By

Ceyhun KELLECİ

June 2011

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Prof. Dr. Abdullah ATALAR(Supervisor)

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Prof. Dr. Ekmel ÖZBAY

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Prof. Dr. Cemal YALABIK

Approved for the Graduate School of Engineering and Sciences:

Prof. Dr. Levent Onural
Director of Graduate School of Engineering and Sciences

ABSTRACT

A Fully Integrated K-Band Power Amplifier Design Using Digital 0.18 μm CMOS Technology

Ceyhun KELLECİ
M.S. in Electrical and Electronics Engineering
Supervisor: Prof. Dr. Abdullah ATALAR
June 2011

Applications at K-Band frequencies (the part of the electromagnetic spectrum defined by IEEE to be from 18 GHz to 27 GHz) like K-Band satellite communication, vehicular short range radars, point-to-point (PTP) radio bring the need for low cost, environment friendly RF blocks. Among them, the design of power amplifiers (PAs) is one of the most challenging. In this work, a three-stage PA is developed in 0.18 μm digital CMOS technology. The design and simulations are based on the models obtained from the foundry. The final design has been fabricated at the foundry and measurements show +16.9 dBm of linear output power and a power added efficiency (PAE) of 12.3% at 20 GHz at the P_{1dB} point.

Keywords: Power Amplifier, K-Band, CMOS, 0.18 μm

ÖZET

DİJİTAL 0.18 μM CMOS TEKNOLOJİLİ BİR TAM ENTEGRE K-BAND GÜÇ YÜKSELTECİ TASARIMI

Ceyhun KELLECİ
Elektrik ve Elektronik Mühendisliği Bölümü Yüksek Lisans
Tez Yöneticisi: Prof. Dr. Abdullah ATALAR
Haziran 2011

K-Band frekanslarındaki (Elektromanyetik spektrumun IEEE tarafından 18 GHz ile 27 GHz arasında tanımlanmış kısmı) K-Band uydu haberleşme, kısa menzilli araç radarı, noktadan noktaya radyo gibi uygulamalar düşük maliyetli, çevre dostu RF bloklarına olan ihtiyacı da beraberinde getirmektedir. Bunlar arasında, en zahmetli olanlardan birisi güç yükselteci tasarımıdır. Bu çalışmada, 0.18 μm dijital CMOS teknolojisi kullanarak tasarlanmış ve üretilmiş üç katlı bir güç yükselteci mevcuttur. Tasarım ve simülasyonlar üreticiden alınmış modeller üzerine kuruludur. Üretilen çip, +16.9 dBm lineer çıkış gücü ve P_{1dB} noktasında, 20 GHz'de %12.3'lük bir verim göstermektedir.

Anahtar Kelimeler: Güç yükselteci, K-Band, CMOS, 0.18 μm

ACKNOWLEDGMENTS

I would like to thank my supervisor Prof. Abdullah ATALAR for his guidance and support throughout my time in Bilkent.

The financial support of TÜBİTAK through the Graduate Study Scholarship Program is greatly appreciated.

I would also like to thank Dr. Selim Olçum, Dr. Niyazi Şenlik, Akif Alperen Coşkun, Kağan Kaya, Muhammed Acar, Elif Aydoğdu and Kazım Peker for their valuable support.

Contents

List of Figures

List of Tables

Dedicated to my beloved family.....

Chapter 1

Introduction

IEEE defines the K-Band as the part of the electromagnetic spectrum from 18 GHz to 27 GHz. Applications at this frequency interval include K-Band satellite communication, vehicular short-range radars used for traffic safety, point-to-point (PTP) radio and point-to-multipoint communication. These applications bring the need for low cost, environment friendly RF blocks. Among them, the design of power amplifiers (PA) is one of the most challenging.

Although one can choose among GaAs, GaN or Si technologies in designing K-Band PAs, using the Si technology has many advantages over others. First of all, it is cheap and since the technology is already present and being used, it does not require a lot of R&D. Si technology is also suitable for mass production.

Si transistors dominate the digital design sector. Microprocessors of the computers that we use in our daily life are fabricated using Si. Nowadays, the gate length of the digital transistors is as small as 35 nm, but for an analog designer, such gate lengths may not always be practical. In choosing the gate length to be used, one must keep in mind that f_T of the transistors increases with decreasing gate length but the maximum supply voltage that can be used decreases since the

gate oxide thicknesses are smaller. On the other hand, the cost of the fabrication is higher for smaller gate lengths.

Various designs exist in the literature using two-stage cascode configuration [1], [2], two-stage cascode configuration with power combiner [3], three-stage common source (CS) configuration [4], four-stage mixed cascode and CS configurations [5], either in 0.18 μm or in 0.13 μm gate lengths.

In this thesis, we used the digital 0.18 μm 1P6M (1 poly 6 metal) CMOS technology of United Microelectronics Corporation (UMC) to design and fabricate a three-stage PA at 20 GHz. Transistors of this technology allow the usage of 1.8 V drain bias voltage and they have an f_T above 40 GHz which shows that these transistors can be used in a K-Band amplifier design.

In chapter 2, power amplifier concepts such as load matching, efficiency, simulation techniques that can be used will be revisited. Chapter 3 will be composed of the design of a three-stage K-Band power amplifier using the concepts mentioned in the previous chapter.

In chapter 4, measurements made on the fabricated chip will be presented and compared to the simulation results obtained previously.

Chapter 2

Power Amplifier Basics

2.1 Definition

A power amplifier (PA), usually used to drive antennas, is an amplifier for which the signal level is comparable to its bias level which results in nonlinear behavior. Since the signal level that is wanted to be transferred to the load is relatively high, efficiency becomes important. Thus, the two key words for a PA are **efficiency** and **linearity**.

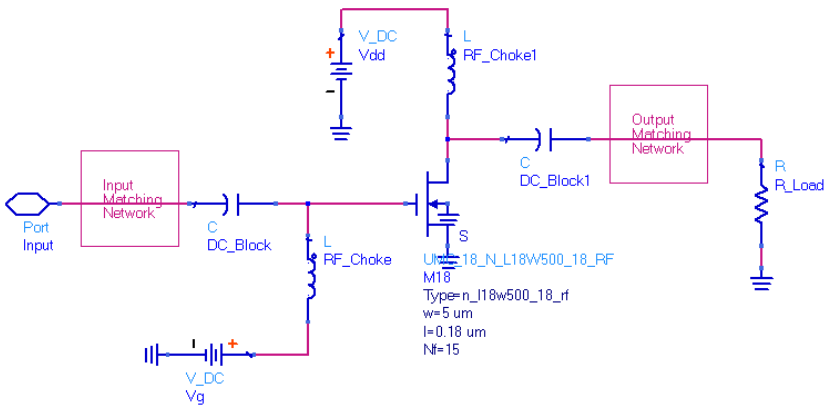


Figure 2.1: General power amplifier configuration.

2.2 Power Amplifier Concepts

2.2.1 Simulation Techniques Used

For better understanding of power amplifier concepts, it's necessary to know about the simulation techniques used for the design. Note that in this thesis, all simulations are made using Agilent Advanced Design System (ADS) software.

Small signal S-parameters (SSSP) simulations

A power amplifier is a two-port network and the representation of this network is done through "scattering parameters" (S-parameters) defined usually relative to 50 Ω. Small signal S-parameters simulations give the characteristics of the two-port network under test when a small level of signal is applied to the network.

Large signal S-parameters (LSSP) simulations

The only difference between small signal and large signal S-parameters simulations is the level of the signal that is applied to the network. As it can be deduced from the name, for large signal S-parameters characterization of a two-port network, a relatively high signal is applied, thus, the nonlinear effects are taken into account.

Load-pull simulations

The maximum power transfer theorem, stating that to maximize the power transfer, the impedance of the load should be conjugately matched to that of the source, does not apply for power amplifiers [6], but there is a relation between output power level and output match [7]. To investigate this relation, a load-pull

simulation can be made in the following way: Sweep the load impedance with the help of a tuner and measure the power that is transferred to this load. The result is contours on the Smith chart that are named load-pull contours.

Intermodulation distortion (IMD) simulations

Because of the nonlinear nature of the amplifiers, when two or more sinusoidal signals are applied at the input, additional frequencies, which are called intermodulation products, are observed at the output. When two tones of frequencies f_1 and f_2 are applied at the input, the products at frequencies $2f_1-f_2$ and $2f_2-f_1$ (third order products) are of special importance since they are very close to f_1 and f_2 and thus limit the dynamic range of the amplifier [8].

Third order intercept point (TOI) is defined as the point where the extrapolated output power levels of the main tones and the third order products are equal to each other. The input power of main tones at TOI is the IIP3 and the output power of main tones at TOI is the OIP3.

2.2.2 Efficiency

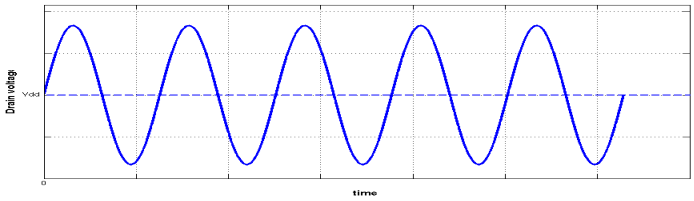
Since we are dealing with power amplifiers, the power levels wanted to be transferred to the load are relatively high. On the other hand, to design an environment friendly amplifier, one should not waste energy which is expensive. Thus, the term efficiency becomes important. The efficiency definition that will be used in this work is that of the power added efficiency (PAE). PAE is the delivered RF power by the amplifier to the load over the DC power fed to the amplifier when the RF input power is taken into account [7].

$$PAE = \frac{P_{RF_{out}} - P_{RF_{in}}}{P_{DC}} \tag{2.1}$$

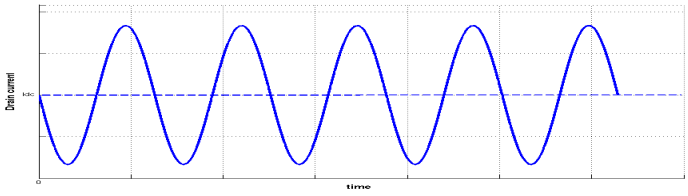
2.2.3 Power amplifier classes

One can use a transistor in two ways when designing a power amplifier; first as an active device to make amplification, second as a switch. Amplifiers using the first idea are called linear amplifiers and amplifiers using the latter idea are called switching mode amplifiers. In switching mode amplifiers, to be able to use the transistor as a switch that turns ON and OFF almost instantaneously, the amplifier needs to be overdriven compared to linear amplifiers and this causes the gain to drop by many dBs [7]. Since the gain is scarce at K-band with 0.18 μm technology, a switching mode amplifier design is not adopted in this work.

Class A, AB, B and C amplifiers are linear amplifiers. What makes an amplifier to function in a specific class is its biasing, i.e., given an amplifier configuration, one can choose to make it work in class A, AB, B or C by properly designing the bias networks.

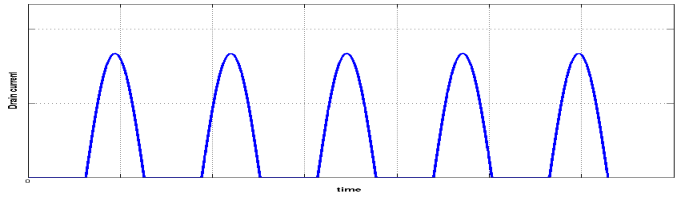


(a) Drain voltage swinging around Vdd.

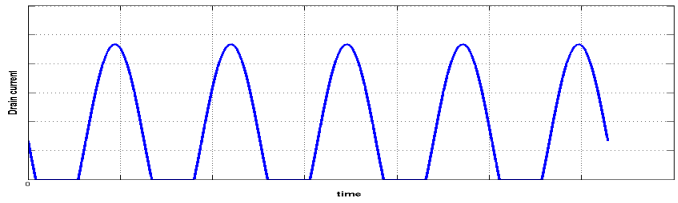


(b) Drain current for class A power amplifier. The current is never zero, i.e., the transistor is always in its ON region.

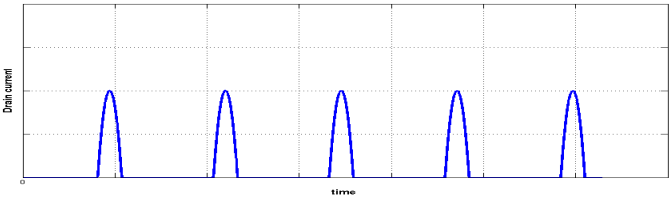
Class A amplifiers are known as the most linear amplifiers, since the transistor is always in its ON region (in the active region for bipolar transistors, whereas in the saturation region for MOS transistors.) and regions causing distortion are avoided. Although high linearity sounds good, class A amplifiers are also known to be the least efficient amplifiers. The theoretical value for maximum efficiency



(c) Drain current for class B amplifier. The current is zero for half of the cycle.



(d) Drain current for class AB amplifier. The current is zero for less than half of the cycle.



(e) Drain current for class C amplifier. The current is zero for more than half of the cycle.

Figure 2.2: Drain voltage and current waveforms for different amplifier classes.

is 50% for a class A power amplifier [6]. This weak performance in efficiency is primarily due to the DC current fed to the transistor to keep it in its ON region.

Class B amplifiers are more efficient, but less linear than class A amplifiers. In this class, the transistor is in its ON region only for half of the cycle, thus the DC current fed to the transistor is zero. The corresponding theoretical maximum efficiency is 78.5% [6]. Class B amplifiers are generally used in push - pull configuration composed of two transistors, one working in positive half cycles and the other working in negative half cycles.

In class C amplifiers, the transistor is kept in its ON region less than half of the cycle, whereas in class AB amplifiers the transistor is kept in its ON region

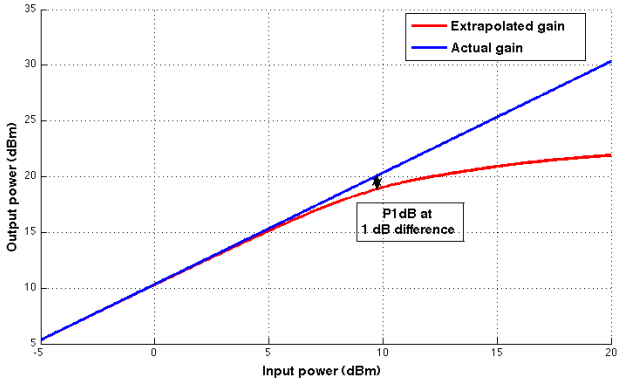


Figure 2.3: P_{1dB} example: The small signal gain is 10 dB. When the input power reaches 9.5 dBm, the gain is 1 dB smaller. Thus, input referred P_{1dB} is 9.5 dBm, whereas output referred P_{1dB} is 18.5 dBm.

for more than half of the cycle. The term conduction angle is defined as the angle during which the transistor is ON [7].

Going from class A to C, as the conduction angle drops, the linearity decreases and the efficiency increases but also the gain of the amplifiers becomes lower. Again, since the gain is scarce at K-band with 0.18 μm technology, a class A power amplifier design is chosen in this work.

2.2.4 Gain compression

An amplifier does not give constant gain for all input power levels. When the input power is increased and it's no more a "small signal", the transistor starts to saturate and the gain decreases. The point at which the gain is 1 dB smaller than its small signal value is called 1 dB compression point (P_{1dB}). P_{1dB} is a measure of the linear power level that can be obtained from a PA. The input and output powers at this point are called output referred and input referred P_{1dB} respectively.

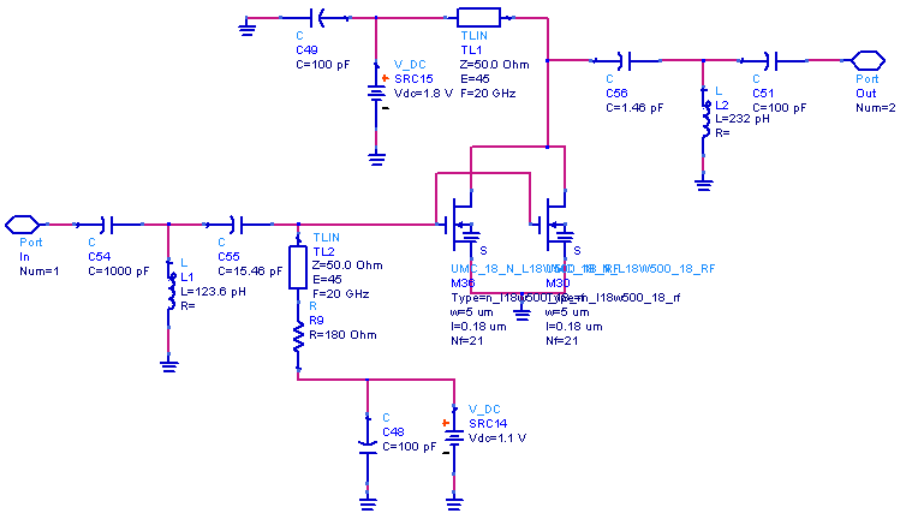


Figure 2.4: The test circuit that is used to compare conjugate matching and load matching.

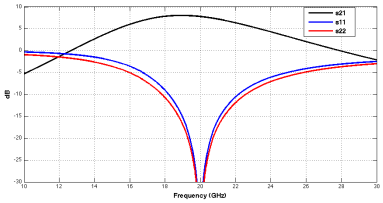
2.2.5 Load matching

Load matching is the matching of the output of a transistor or of an amplifier to the optimum load impedance, i.e., to the load resulting in maximum output power. The optimum load can be approximated by the following formula:

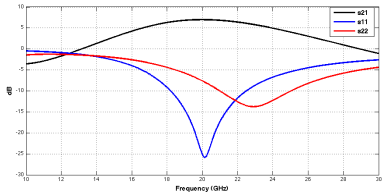
$$R_{opt} = \frac{V_{dd}}{I_{dc}} \tag{2.2}$$

The exact value of the optimum load can be found using the load-pull simulations. The output power difference between these two cases is usually about 2 dB [7].

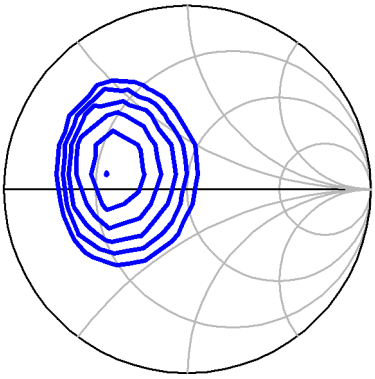
Here is an example of the difference in P_{1dB} between a conjugately matched and load matched amplifier that use lossless matching components and CMOS 0.18 μm transistors: The conjugately matched amplifier results in 14.1 dBm whereas the load matched amplifier results in 16.2 dBm output referred P_{1dB} value. It can be observed in figure 2.5(d) that the center of the load pull contours



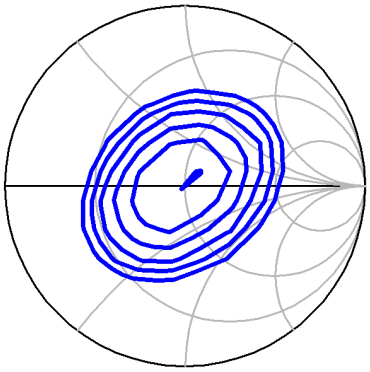
(a) The SSSP simulation plot for conjugate match.



(b) The SSSP simulation plot for load match.



(c) The load pull simulation plot for conjugate match.



(d) The load pull simulation plot for load match.

coincides with the center of the Smith chart, i.e., the maximum power is reached by connecting a 50 Ω load to the output.

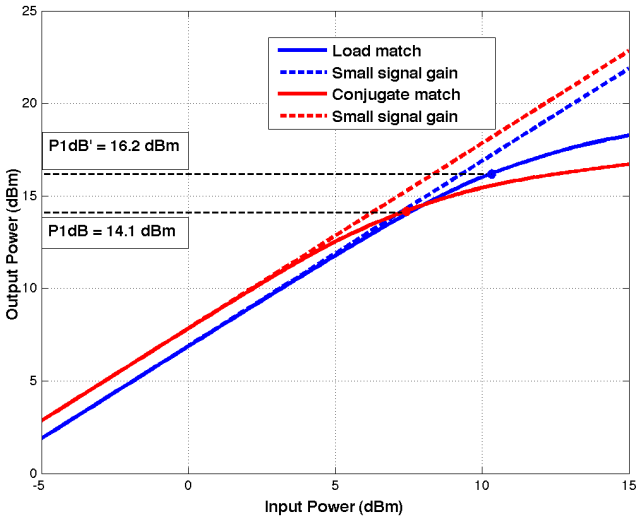
2.2.6 Stability

An amplifier is said to be stable, if it can maintain its intended function whatever are the input and output load conditions. The stability is frequency dependent, and an amplifier is called unconditionally stable if it's stable for all frequencies [8]. The stability of an amplifier can be investigated either graphically using stability circles, or analytically. In this work, stability is investigated analytically using the two-parameter test criterion (K-Δ Test) [8] with:

$$K = \frac{1 - \mid s_{11} \mid^2 - \mid s_{22} \mid^2 + \mid \Delta \mid^2}{2 \mid s_{12} s_{21} \mid} \tag{2.3}$$

and

$$\Delta = s_{11} s_{22} - s_{12} s_{21} \tag{2.4}$$



(e) This is the comparison of output power vs input power plots for both cases. The P_{1dB} of the load matched case is 2.1 dB higher whereas its small signal gain is 1 dB lower than the conjugate matched case.

Figure 2.5: Conjugate matching vs load matching.

The amplifier is unconditionally stable if the following two inequalities are correct;

$$K > 1 \tag{2.5}$$

$$| \Delta | < 1 \tag{2.6}$$

If a transistor is not unconditionally stable, to make it so, either series or parallel resistors can be used at the input or at the output. But since this is a power amplifier, using resistors at the output side would decrease the efficiency significantly. In this work, in the designs that use ideal components, a parallel resistor is placed at the input side, but in the designs with lossy elements, no resistors are needed for unconditional stability due to the metal loss of the transmission lines.

2.3 Design Steps

Starting to an "application specific integrated circuit" (ASIC) design from scratch, here are the steps taken in this work.

2.3.1 Front end design

The processes of choosing the components to be used, biasing the transistors, making input, output and interstage matchings, doing necessary simulations and optimizations can be classified as parts of the front end design.

2.3.2 Layout design

After completing the front end design, the physical circuit should be drawn with the use of an appropriate layout editor. The one preferred in this work is Cadence Virtuoso. One has to go back and forth between front end and layout design steps or even to do them in a simultaneous fashion to ensure that the simulated circuit is physically realizable. For instance, assume that the simulated circuit has a straight transmission line of length 1.6 mm. The chip area allocated for this work is only 1.5 x 1.5 mm^2. Thus, it's not possible to fit this transmission line inside the chip area unless it's S-shaped, then the front end design and corresponding simulations have to be renewed.

2.3.3 Post layout simulations

After completing the layout, a number of checks should be done before starting the fabrication.

Design Rule Check (DRC)

Each foundry have design rules for each technology. These rules define what can and can not be done in a layout and they ensure the manufacturability and/or yield of a design. Careful reading of design rule documents is a must before starting to draw the layout. After completing the layout, an automated check can be done using software tools. In this work, DRC is performed using Cadence Assura software based on the design rule file provided by the foundry.

Layout versus Schematic Check (LvS)

Once the layout is DRC error free, another check has to be performed. Layout vs schematic check is to ensure that the design on the schematic and the one on the layout are the same. The check can be realized again using automated software tools like Cadence Assura.

Antenna Rule Check

The fabrication process is done layer by layer. Suppose that during the deposition of the top metal layer electrostatic charging occurs. If there are some shapes of top metal whose areas are large so that the charging becomes significant, then electrostatic discharge may harm the components, especially transistors. This effect can be eliminated by conforming to the antenna rules. Antenna rule check investigates the shape sizes and their connections to active components and warns the user if there is a possibility of electrostatic discharge during fabrication. Especially for large scale manufacturing, the lack of antenna rule check may cause the yield to decrease significantly. In this work, antenna rule check is done with Cadence Assura using the antenna rule files provided by the foundry.

Chapter 3

A Class A Power Amplifier Design

3.1 Choice of Components

3.1.1 Choice of Transistors and Bias Levels

In this work, only cascode and common source configurations are investigated because of their simplicity. For the common source configuration, since the upper limit for the drain DC voltage feed is 1.8 V, it's chosen to be 1.8 V. For the cascode configuration, a single supply is preferred at the drain and gate of the cascode transistor for simplicity. The value of the supply is adjusted to 3.1 V so that the DC voltage at the drain of the input transistor is 1.8 V.

What is done next was to simulate the output stage for various drain currents both for cascode and common source configurations and compare the output power results. With a fixed DC drain voltage, the drain current can be adjusted by either the gate bias voltage or the transistor width.

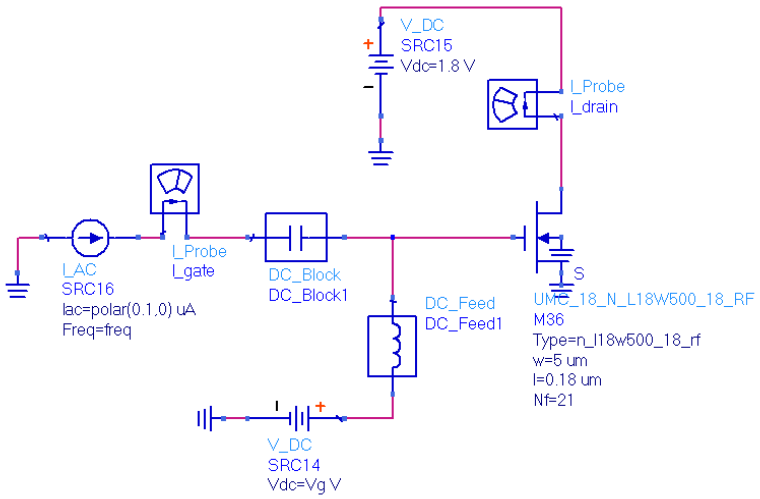
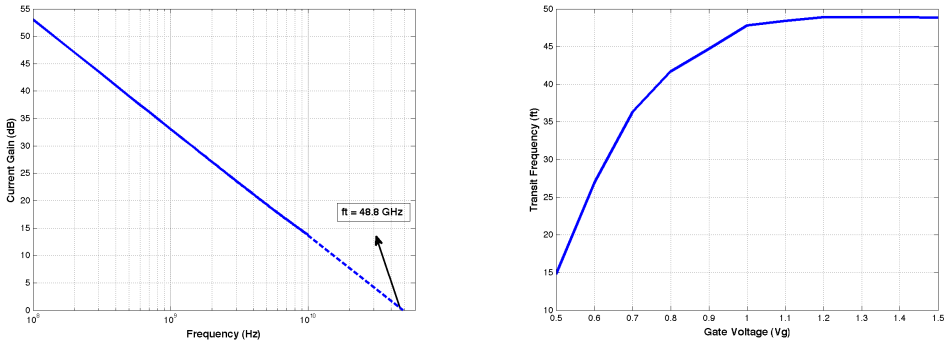
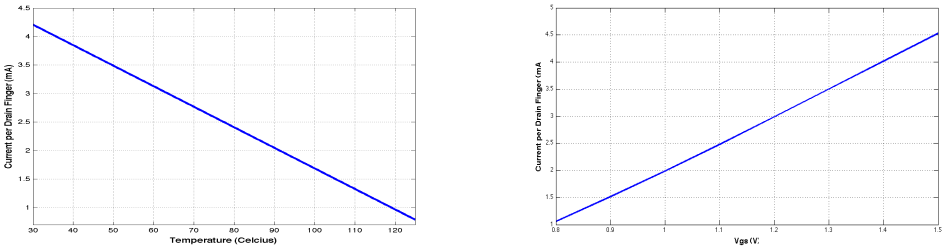


Figure 3.1: Transit frequency simulation setup.



(a) (b)

Figure 3.2: (a) Example current gain (H_{21}) vs frequency simulation for $V_{gs} = 1.5$ V. The models are valid up to 10 GHz, hence f_T is obtained by extrapolation. (b) f_T vs gate voltage (V_{gs}) for a transistor of 21 fingers. The f_T is maximized around $V_{gs} = 1.2$ V.



(a) (b)

Figure 3.3: (a) Allowable current per drain finger vs temperature. (b) Current per drain finger vs V_{gs}. For a gate voltage of 1.1 V the current per drain finger is 2.5 mA and for this value to not cause any electromigration problems, the temperature of the circuit should be less than 78° Celsius.

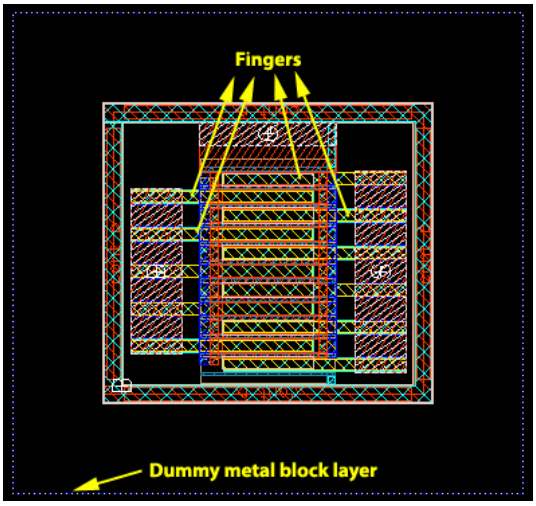


Figure 3.4: Layout top view of a transistor from Cadence Virtuoso. Fingered architecture can be seen. G: gate D: drain S: source B: bulk

One interesting point here is that the f_T of the transistors depends on the gate bias level, it is maximized at 1.2 V and for gate voltages higher than this value, it stays the same, roughly at 49 GHz. On the other hand, electromigration rules state that the allowable current per drain finger is limited. The relation between this limit and the temperature can be seen in figure 3.3(a). For a gate to source voltage of 1.2 V, the maximum temperature at which the chip can maintain its proper functioning is 63°C, the f_T is 49 GHz, whereas these values become 78°C and 48.4 GHz respectively for 1.1 V. Thus, to increase the temperature margin, 1.1 V is chosen as V_{gs}.

Therefore, the only parameter left to change the drain current is the transistor width. As the transistors of this process have a fingered architecture (see figure 3.4), the number of fingers are adjusted to control the current. Since the maximum number of fingers is 21, in cases more than 21 fingers are needed, transistors are connected in parallel.

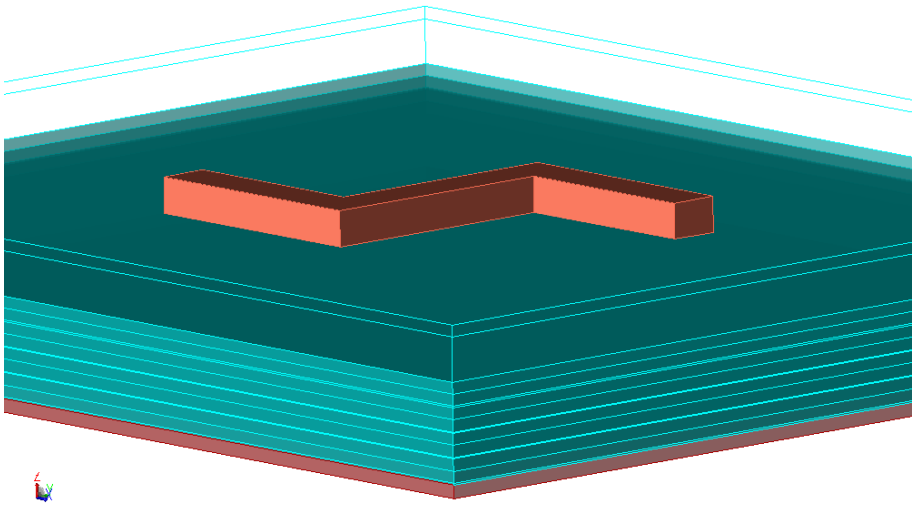


Figure 3.5: 3D illustration of an example microstrip line in the CMOS 0.18 μm process where the multi-layered dielectric architecture between the signal and ground layers can be seen.

3.1.2 Choice of Passive Components

Transmission Lines

The transmission lines used in this work are microstrip lines. The CMOS 0.18 μm process is a 1 poly 6 metal (1P6M) process. Therefore, the top metal layer is used as the signal layer, whereas the bottom metal layer is used as the ground. The dielectric between signal and ground layers has a multi-layer architecture and the relative permittivity (ϵ_0) is not constant. Hence, the entire architecture is modeled and all transmission lines are simulated with ADS Momentum.

Since the metal loss is high at K-Band, and this loss depends on the metal width, before choosing the metal width of the transmission lines, the loss is simulated for various widths. As it can be seen in figure 3.6, the loss decreases with increasing transmission line width. On the other hand, electromigration rules state that, the current density passing through a metal structure is limited. Thus, a higher width helps to prevent electromigration problems. But the width can't be increased indefinitely; the maximum metal width that can be used

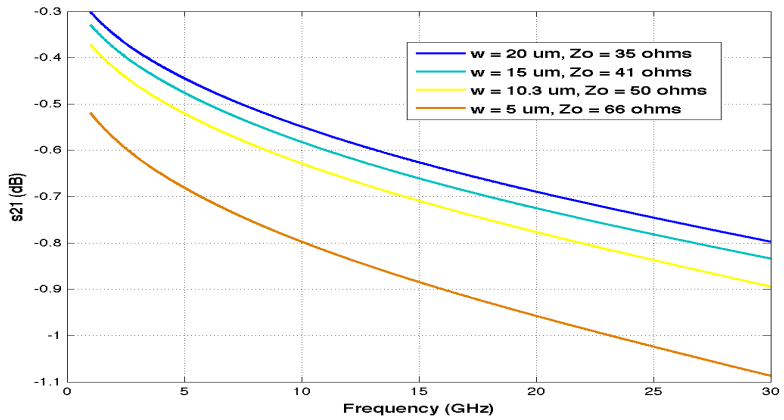


Figure 3.6: s_{21} vs frequency for various transmission line widths for a length of 1500 mm. The s-parameters are relative to the characteristic impedance of each transmission line.

without slotting (see section 3.6) is 20 μm. Therefore, all of the transmission lines used in this work have a width of 20 μm with a characteristic impedance of 35 Ω.

Although the design kit provided by the foundry has inductors within, the minimum inductance that can be obtained with these inductors is 586 pH which is very high compared to the inductances needed in matching. Therefore, instead of inductors, transmission lines are used.

Capacitors

The design kit has necessary capacitors present within. These capacitors are parallel plate capacitors and their capacitances are adjusted by changing the area of the plates. The capacitors that are used for bypass reasons are chosen to have the maximum capacitance allowed which is 4.921 pF (70 x 70 μm^2).

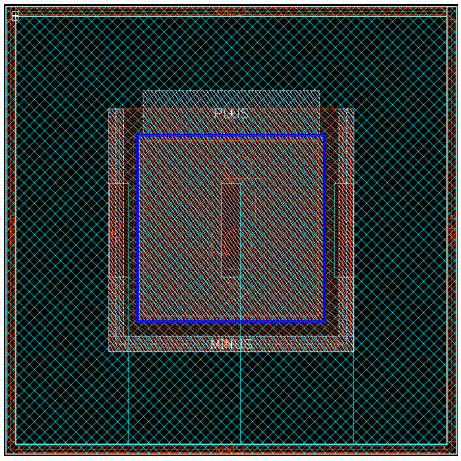


Figure 3.7: Layout top view of a capacitor from Cadence Virtuoso. Top metal plate (marked with the blue rectangle) size is 20 x 20 μm^2 which corresponds to a capacitance of 406 fF.

Pads

In order to make RF and DC connections between the chip and the outside world, pads are needed. The pads used in this work are again from the design kit. They are composed of two metal layers: the top metal layer for the connections and the bottom metal layer for shielding the top layer from the substrate.

Although the chip is coated with an insulator in order to prevent oxidation, pads are left open since they will either be wire bonded or be touched by probes. The area of the pads is 65 x 65 μm^2.

3.2 Output Stage Design

The most important and challenging part of a power amplifier is the design of its output stage. Thus, we will start the design backwards, i.e., first design the output stage and then design driver and gain stages accordingly.

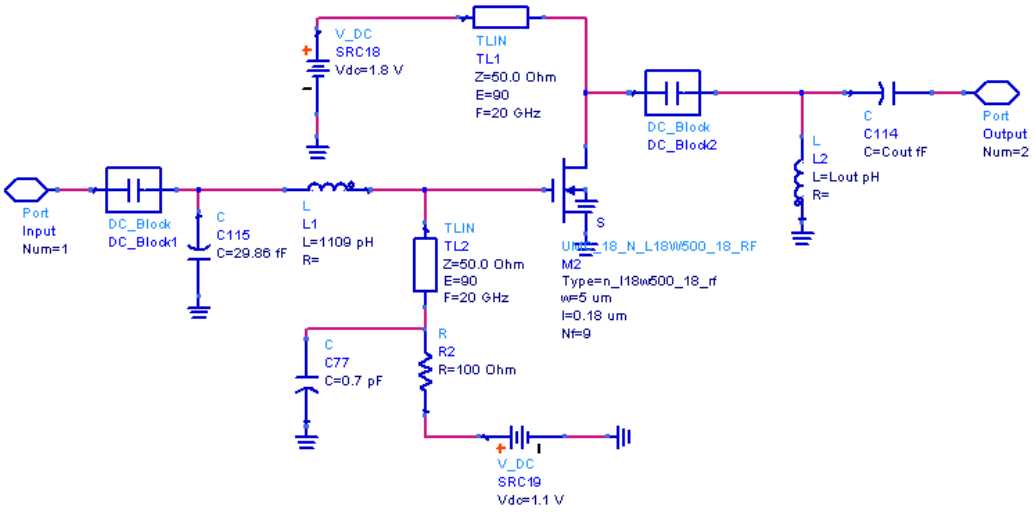


Figure 3.8: The schematic of the test circuit for common source configuration.

The first step in the design is to choose the topology and the transistor(s) to be used at the output stage, i.e., cascode or common source configuration with appropriate transistor widths.

The algorithm used is the following:

- Bias the transistor under test through $\lambda/4$ transmission lines.
- Make the transistor unconditionally stable using a resistor on the gate bias line.
- Match the output to $R_{opt} = V_{dd}/I_{dc}$.
- Conjugate match the input.
- Use load - pull simulations to optimize output referred P_{1dB} value.
- Conjugate match the input and go to previous step until convergence is achieved.

The output referred P_{1dB} value increases with increasing drain current for both common source (figure 3.10) and cascode (figure 3.11) configurations and

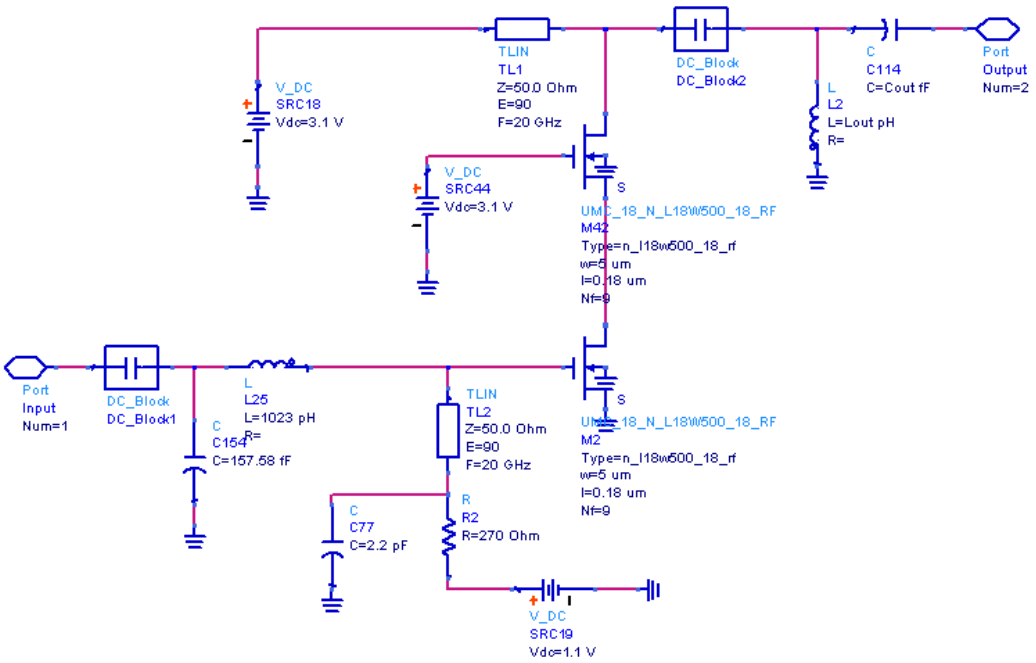


Figure 3.9: The schematic of the test circuit for cascode configuration.

given a specific value for the DC power fed to the circuit, the value is higher for common source configuration, i.e., the efficiency is better (See figure 3.12). Therefore, the common source configuration is preferred as the output stage topology. The transistor width is chosen such that the DC drain current is around 100 mA and this current is achieved if 4 transistors of 21 fingers are connected in parallel. The corresponding P_{1dB} is 19 dBm with a small signal gain of 9.5 dB.

Once the output stage's topology and bias values are decided, the design now will be repeated this time using actual lossy passive capacitors, transmission lines, DC and RF pads.

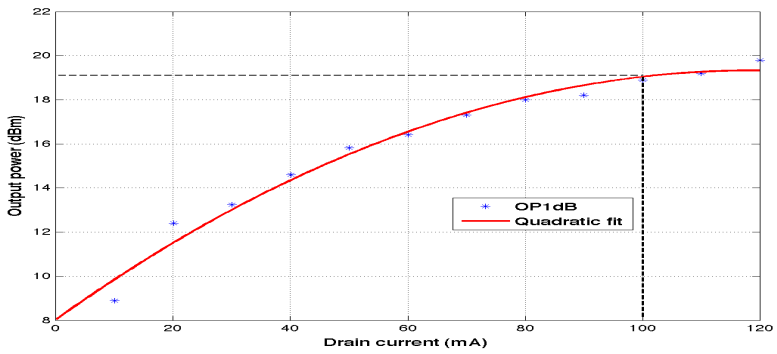


Figure 3.10: Drain current vs output referred P_{1dB} for common source configuration.

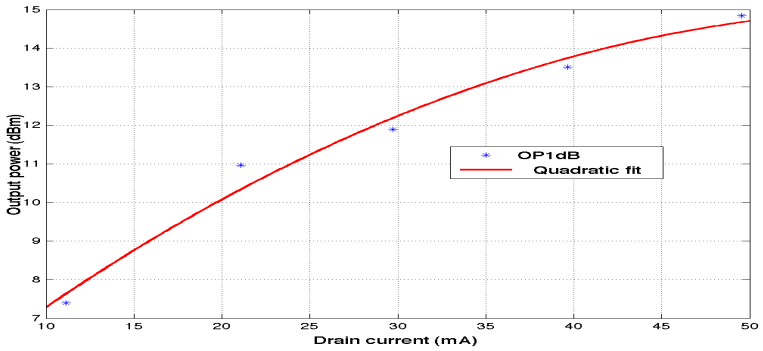


Figure 3.11: Drain current vs output referred P_{1dB} for cascode configuration.

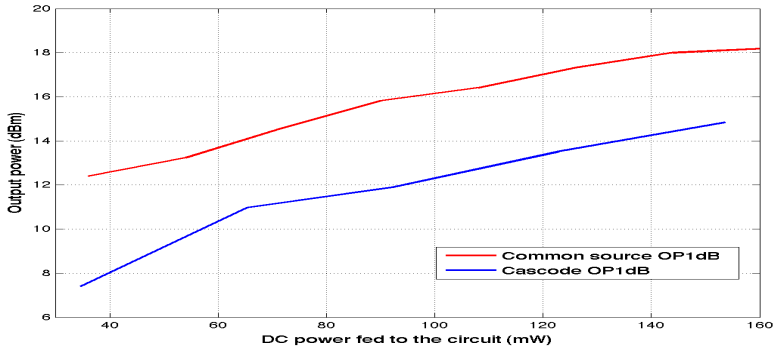


Figure 3.12: Comparison of P_{1dB} values between common source and cascode configurations.

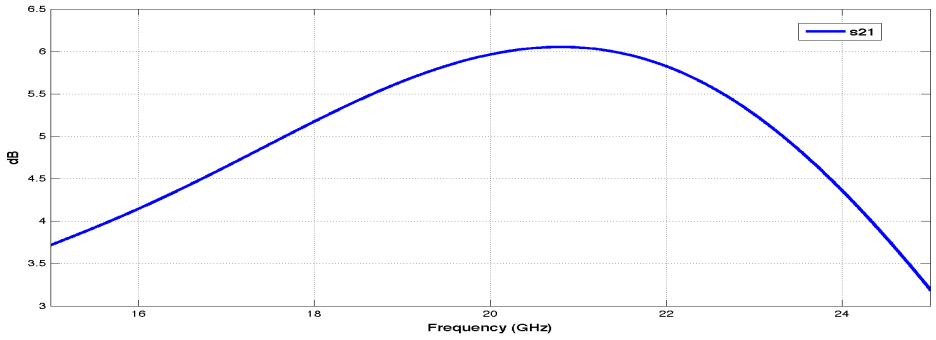


Figure 3.13: s_{21} vs frequency for the output stage. The gain at 20 GHz is 5.97 dB.

Choice of matching networks

Since the loss is very high at this frequency and the area is limited, in order to prevent complexity, unnecessary losses, and to be able to fit the design in the allocated area, a minimum number of components have to be used. On the other hand, $\lambda/4$ transmission lines or inductors as RF chokes at the gate and drain bias lines occupy large areas. Therefore, Π-matching is preferred as the matching topology. At the output matching network, the first element is a transmission line acting as an inductor and also used to give bias to the drains of the transistors. At the inter-stage matching networks, for the first matching element, the same idea is applied and the last matching element, again a transmission line used as an inductor, is used to give bias to the gates of the transistors.

Output stage

After replacing ideal components with lossy ones, the output of the stage is matched such that a 50 Ω load maximizes the P_{1dB} level. The designed output stage is stable for all frequencies, gives a small signal gain of 5.97 dB and a P_{1dB} value of 16.8 dBm (See Figs. 3.13 − 3.17). These values show that, using lossy elements caused the P_{1dB} and small signal gain to decrease by 2.2 dB and 3.5 dB respectively.

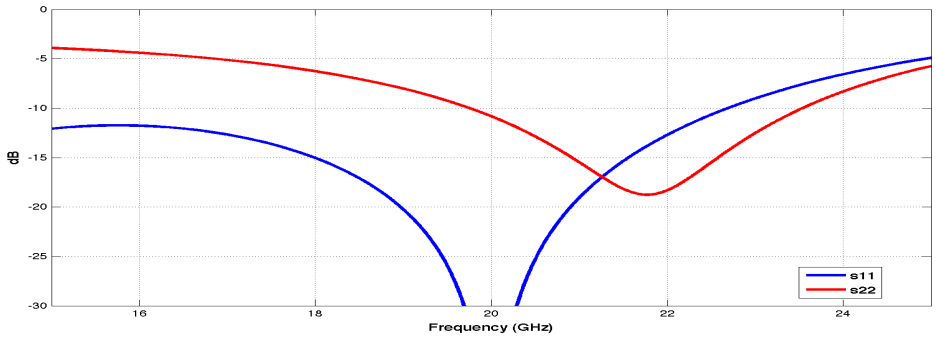


Figure 3.14: s_{11} and s_{22} vs frequency for the output stage.

It can be seen in Fig. 3.17(a) that the center of the load pull contours does not coincide with the center of the Smith chart as expected. This is done intentionally because, bringing the optimum load to 50 Ω results in a lower output power (see Fig. 3.17(b)). The reason is that, bringing the optimum load to 50 Ω with the output matching network results in more loss due to the elements used in matching, i.e., longer transmission lines, smaller capacitances. Thus, instead of using load pull analysis at this point, an optimization to maximize the output power for a 50 Ω load is made using ADS.

3.3 Driver Stage Design

For the designed output stage, the output power (P_{1dB}) reaches 16.8 dBm but the small signal gain is only 6 dB. Thus, it's needed to drive the output stage with an input power level of 11.8 dBm at the P_{1dB} point.

Moreover, the stage that's providing this power level shold be running at a point where there is no gain compression in order to keep the output P_{1dB} at 16.8 dBm. One can design the driver stage to be exactly the same as the output stage and running it at some back-off as done in [4] to prevent gain compression, but that would cause the efficiency to drop. For the choice of the driver stage, there is a tradeoff between efficiency and gain compression. At 3-dB back-off, a

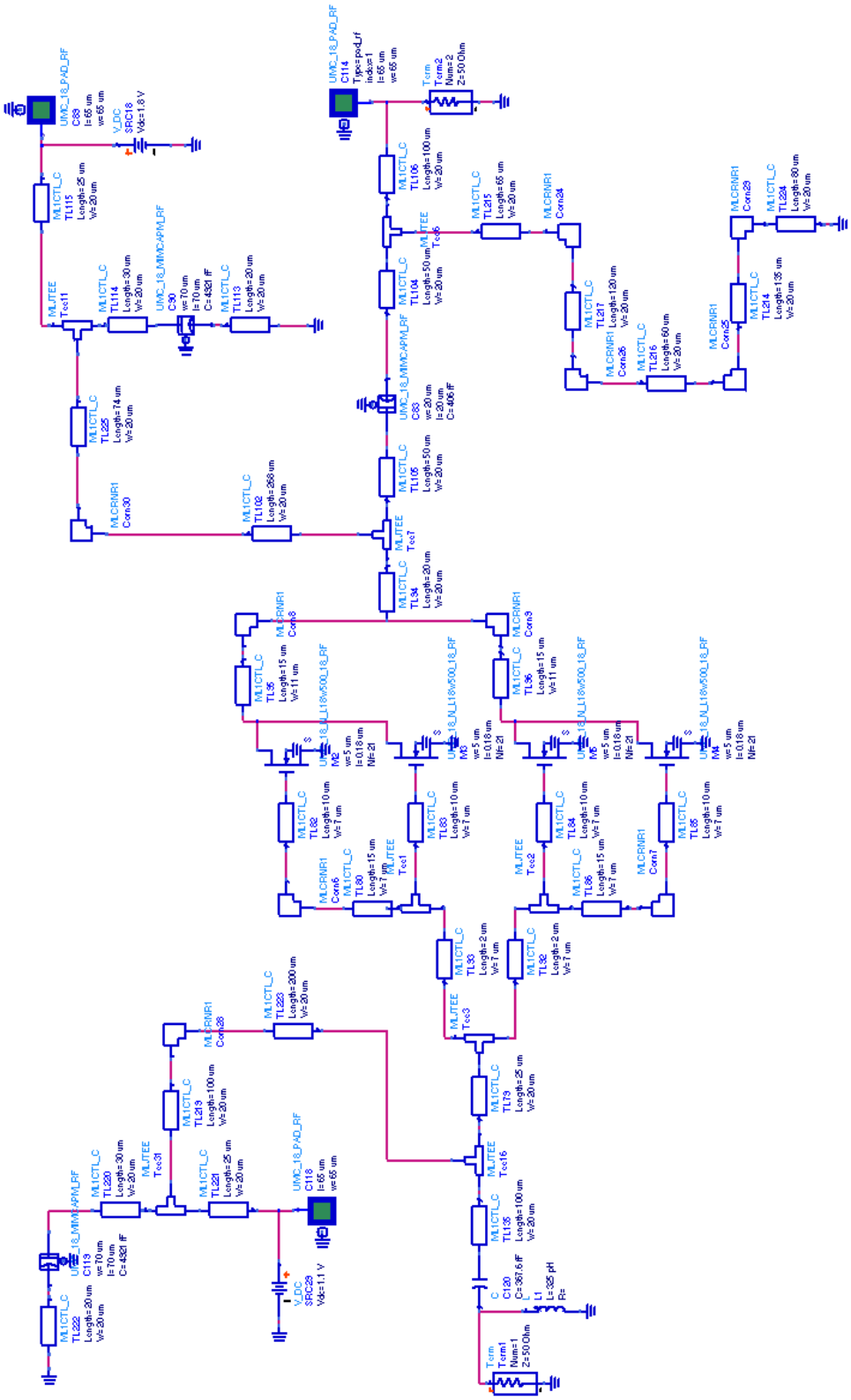
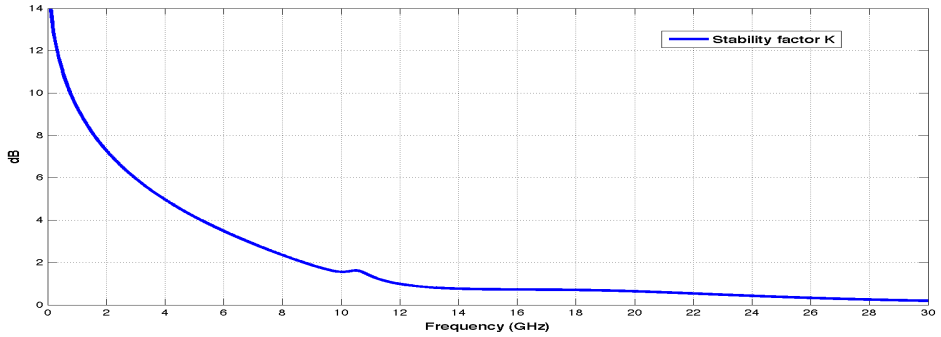
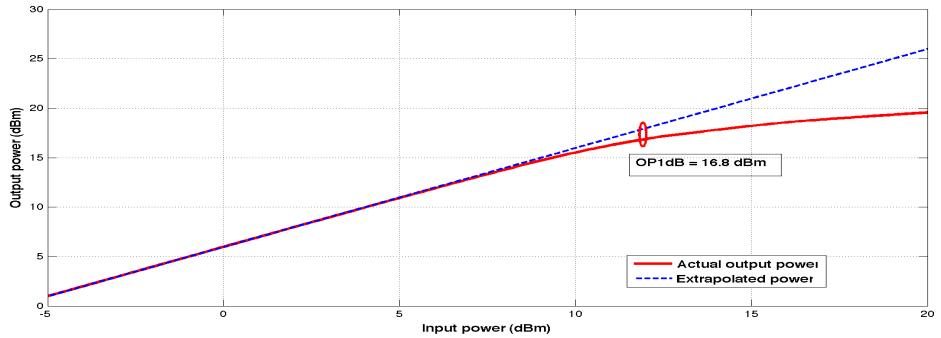


Figure 3.15: Schematic of the output stage.

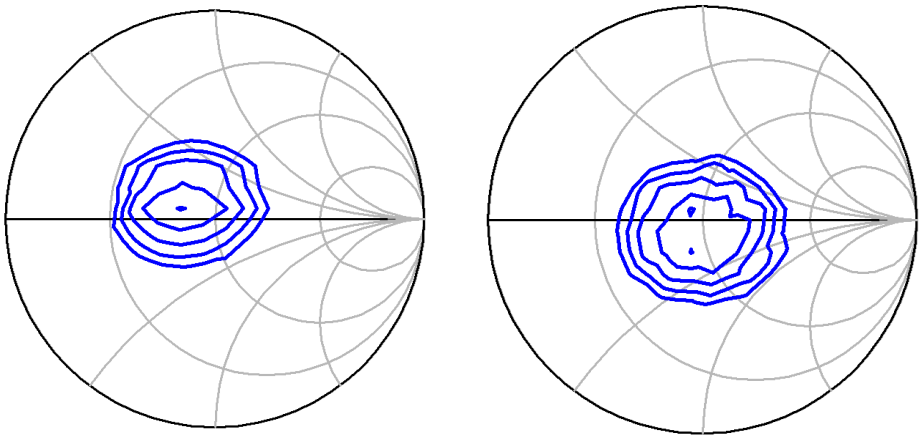


(a) Stability factor K in log scale vs frequency.



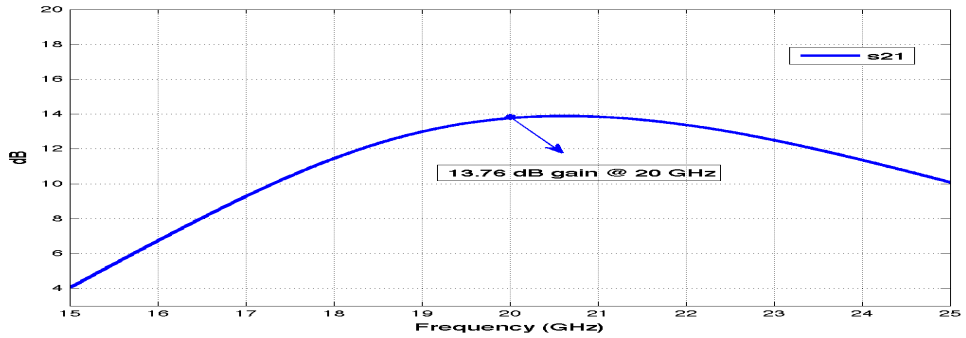
(b) Output power vs input power. The OP_{1dB} level is 16.8 dBm, whereas the saturated output power reaches 19.5 dBm.

Figure 3.16: Stability and large signal simulation results for the output stage.

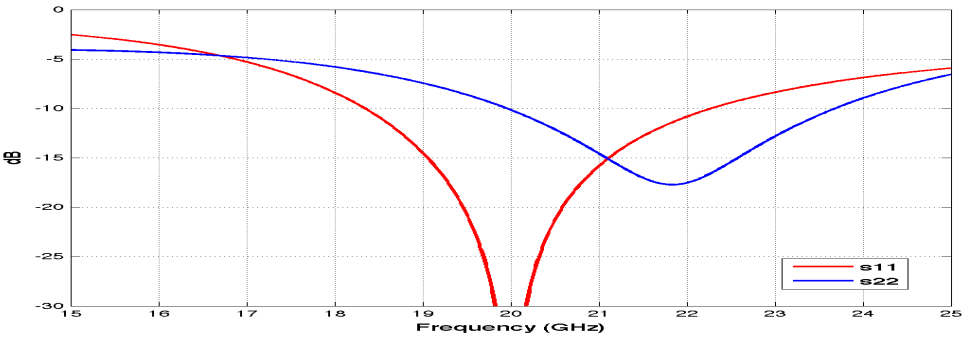


(a) (b)

Figure 3.17: Output stage load pull contours. The input of the stage is matched to 50 Ω and the contours are separated by 0.2 dB in both cases. (a) The optimum load is not brought to 50 Ω. The maximum output power transferred to the optimum load is 17 dBm whereas the power transferred to a 50 Ω load is 16.8 dBm. (b) The optimum load is 50 Ω and the power transferred is only 16.45 dBm.



(a) s_{21} vs frequency. Gain at 20 GHz is 13.77 dB.



(b) s_{11} and s_{22} vs frequency.

Figure 3.18: S-parameter simulations results for the driver and output stages combined.

stage gives around 0.25 dB gain compression whatever the size of the transistor is. In this design, that compression level is assumed acceptable and the driver stage is designed accordingly.

The inter-stage matching between output and driver stages is not done conjugately because running the driver stage at 3-dB back-off and having a power level of 11.8 dBm means that P_{1dB} of the driver stage has to be around 14.8 dBm which is still high.

Assuming that using lossy elements would decrease the P_{1dB} by around 2.2 dB like in the output stage, the driver stage that will be chosen (assuming ideal matching elements) has to give a P_{1dB} of 17 dBm. A drain current of 70 mA (4 transistors of 15 fingers each) results in 17.3 dBm output power, thus the driver stage's transistor width is defined.

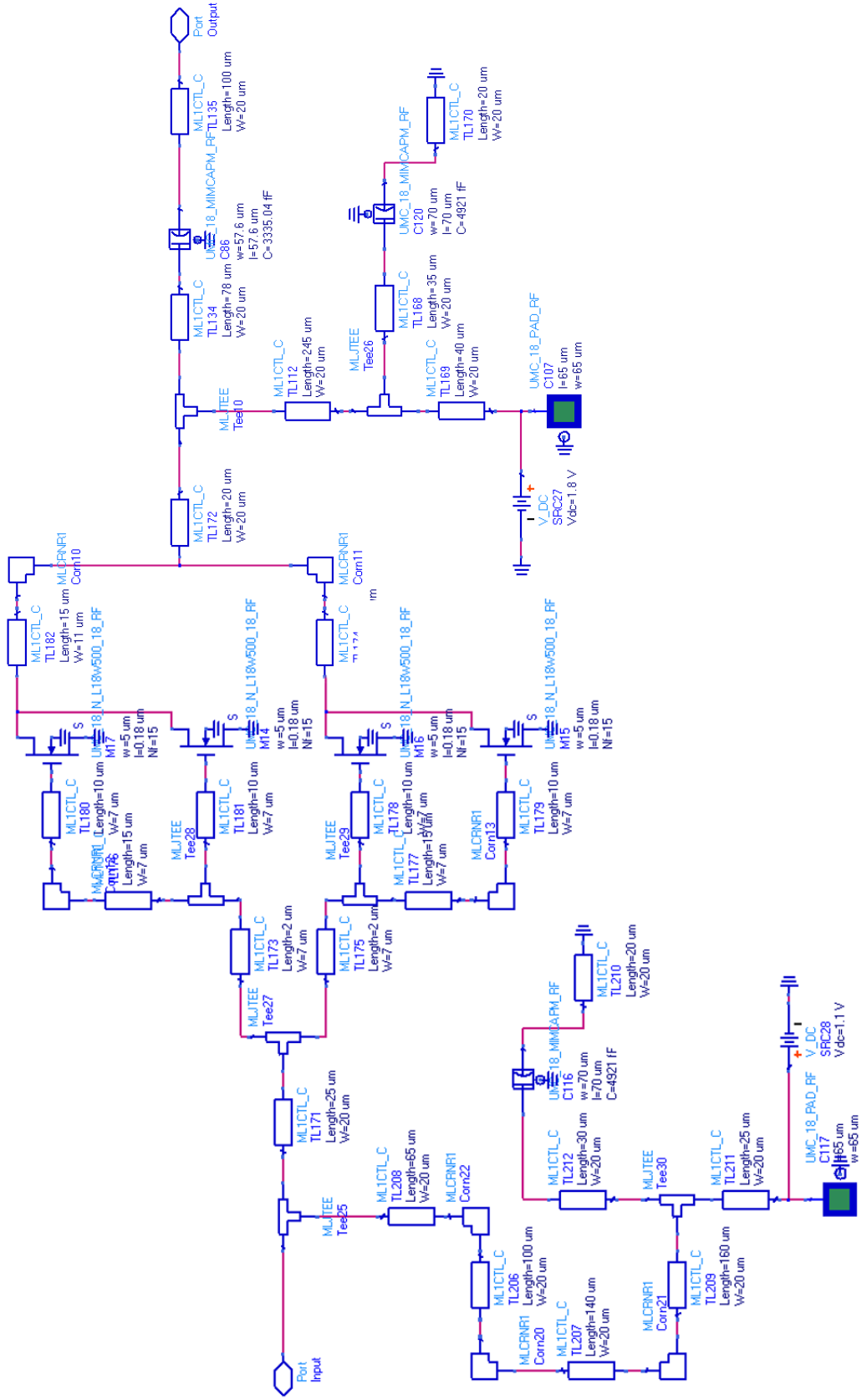
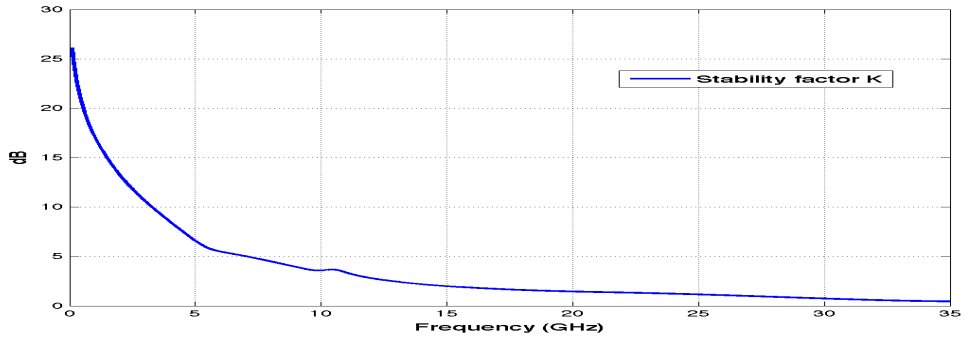
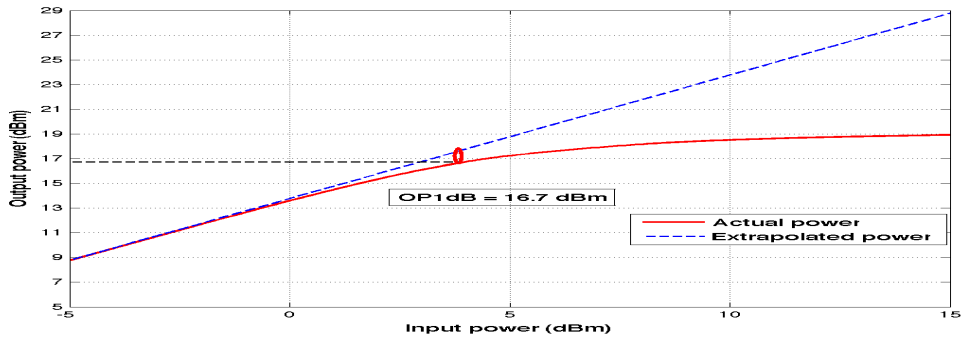


Figure 3.19: Schematic of the driver stage.



(a) Stability factor K in log scale vs frequency. The amplifier is unconditionally stable.



(b) Output power vs input power. The OP_{1dB} level is 16.7 dBm, whereas the saturated output power reaches 19.4 dBm.

Figure 3.20: Stability and large signal simulation results for the driver and output stages combined.

s_{11} of the output stage is $50(0.399 - j0.099)$ Ω. Therefore, when designing the driver stage, 50 Ω is brought to this impedance first, then the output of the driver stage is matched such that this load maximizes power transfer. After combining driver and output stages, the P_{1dB} optimization at the output is renewed since the needed 11.8 dBm is transferred to the output stage with some gain compression.

3.4 Gain Stage Design

With the last two stages designed, the small signal gain reaches 13.8 dB (see Fig. 3.18(a)) and the input referred P_{1dB} is 4 dBm (see Fig. 3.20(b)). Therefore, to drive these two stages, 7 dBm of input power is required with the same gain

compression assumption made before. It's not difficult to obtain this power level whether the configuration is common source or cascode. Since the cascode configuration results in more gain, and efficiency of the stage does not affect the overall efficiency as much as the last two stages, in order to boost the gain of the overall amplifier, that's the configuration chosen. Assuming that 3 dB loss will occur between ideal and actual cases and the output power will decrease by 3 dB when the stage is conjugately matched at the output instead of load matching, the ideal stage has to give at least 13 dBm output power. A current level of 35 mA results in 13 dBm of output power (see figure 3.11), thus the transistor widths for the gain stage are defined.

s_{11} of the last two stages combined is $50(0.472 - j0.383)\ \Omega$. Thus, while designing the gain stage, 50 Ω is brought to this impedance first and the output of the gain stage is conjugately matched.The gain stage gives 9.6 dB gain by itself and has an output P_{1dB} value of 6.8 dBm.

After combining all three stages, the P_{1dB} optimization at the output is again renewed since the needed 4 dBm is transferred to the driver stage with some gain compression.

3.5 Overall Design

The overall amplifier gives a P_{1dB} of 16.1 dBm with a corresponding PAE of 9.37%, a saturated power of 19 dBm with a peak PAE of 17.20% and a small signal gain of 23.8 dB. The 3-dB bandwidth of the amplifier is 3.8 GHz and the output IP3 value reaches 24.4 dBm.

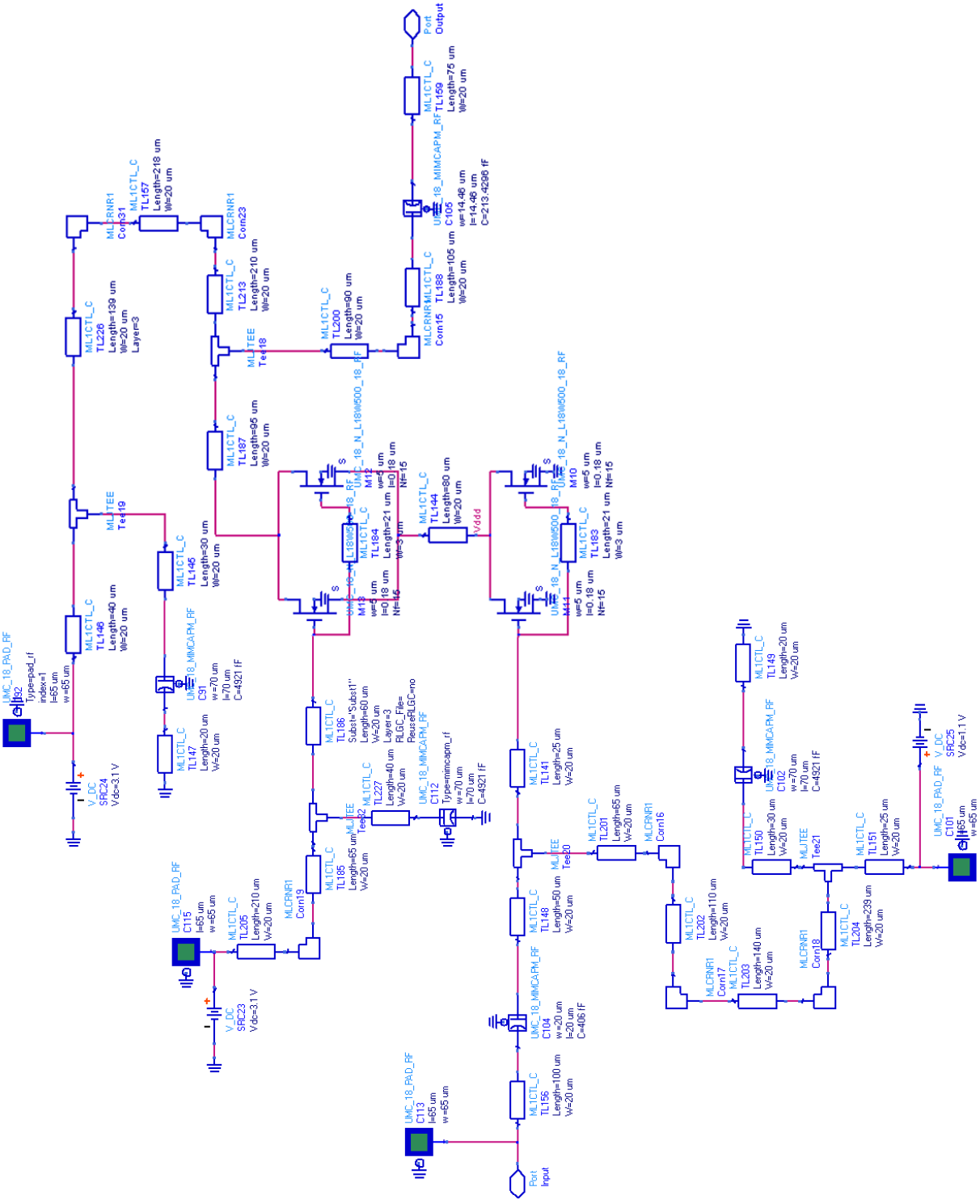
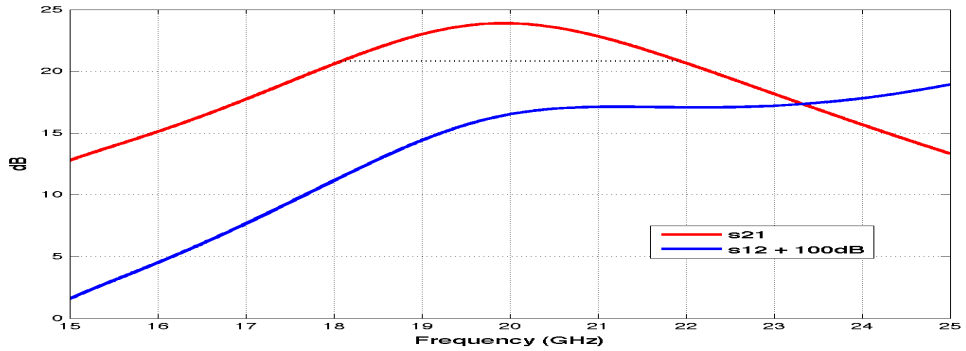
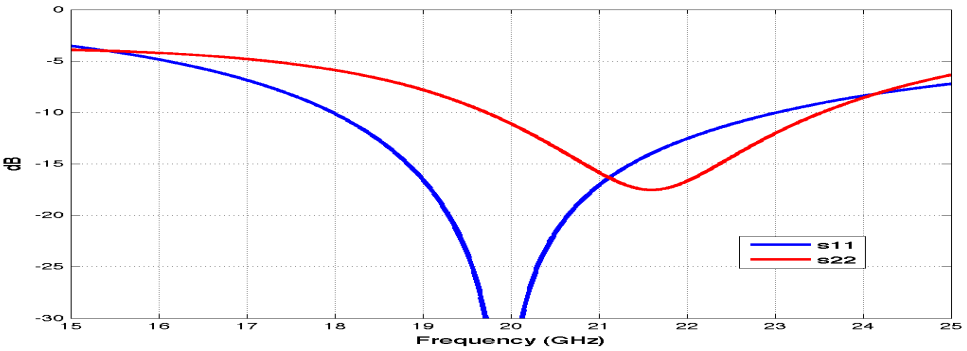


Figure 3.21: Schematic of the gain stage.



(a) s_{21} and s_{12} of the amplifier. Maximum gain is 23.9 dB and occurs at 20 GHz. The 3-dB bandwidth of the amplifier is 3.8 GHz (From 18.1 GHz to 21.9 GHz) Within the band, s_{12} is always less than -80 dB.



(b) s_{11} and s_{22} of the amplifier. Within the band, s_{11} is less than -10.5 dB and s_{22} is less than -6 dB.

Figure 3.22: S-parameter simulation results for the overall design.

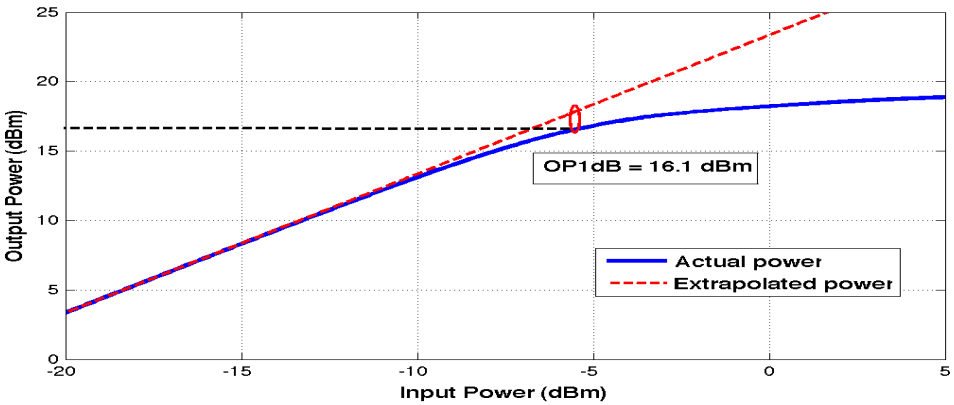


Figure 3.23: Output power vs input power. Output referred P_{1dB} is 16.1 dBm.

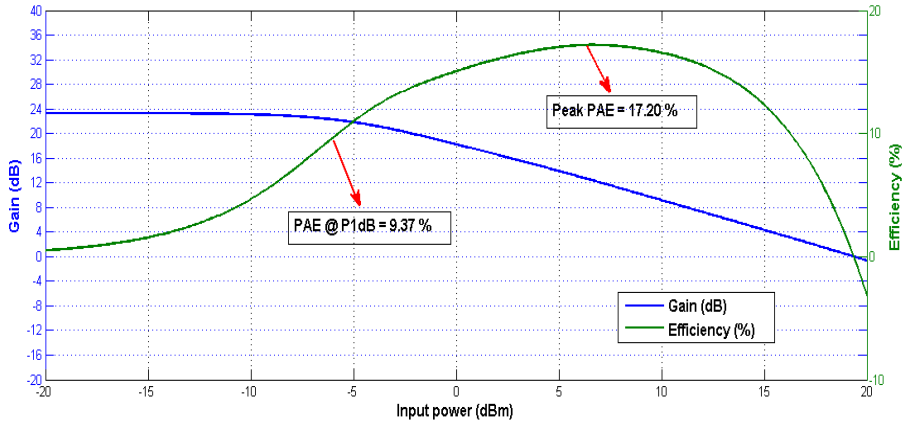
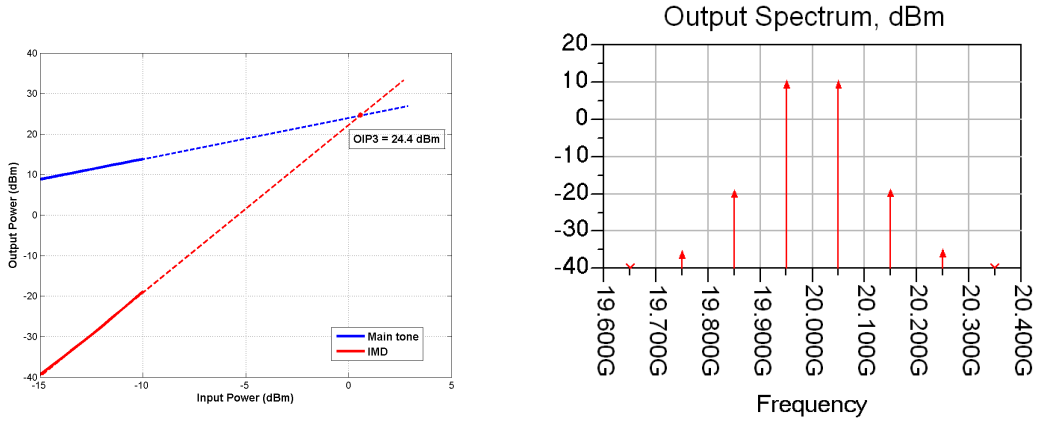


Figure 3.24: PAE and gain vs input power. PAE @ P_{1dB} is 9.37% whereas peak PAE reaches 17.20%.



(a) (b)

Figure 3.25: IMD simulation results for the overall design. (a) Two-tone simulation of the amplifier. The tones, separated by 100 MHz, are applied at 19.95 GHz and 20.05 GHz The resulting output $IP3$ is 24.4 dBm. (b) The frequency spectrum of the output of the amplifier when two tones of -10 dBm are applied at the input.

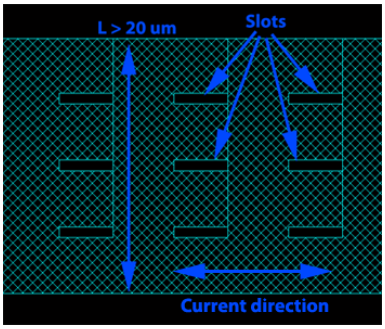


Figure 3.26: Slotting example on bottom metal layer.

3.6 Layout Design and Final Layout

Slotting

While drawing the layout, one should pay attention to the rule documents provided by the foundry. Layout rule documents specify what can and can not be done for proper fabrication of a design. One of the important points in these documents is the metal slotting. Metal slotting is the rectangular shaped openings made on a metal layer for metal stress relief reasons. The metal slotting rule states that every metal shape having a width larger than 20 μm has to be slotted and the direction of the slots has to be parallel to that of the current (see Fig. 3.26).

Except for the dummy metal shapes, the only place where slotting is needed is the bottom metal layer which is used as the ground layer. The slots of this layer are placed such that their direction is parallel to the current direction passing through the transmission lines, and that there are no slots under the signal layer of the transmission lines (see Fig. 3.27).

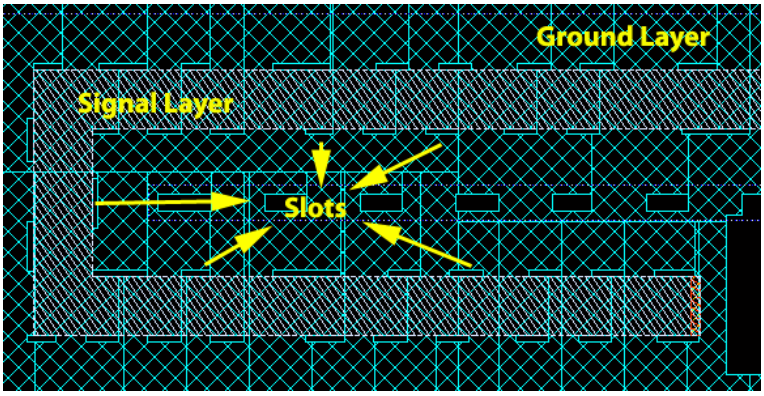


Figure 3.27: Slots are always parallel to current flow direction and never coincides with the signal layer of the transmission lines.

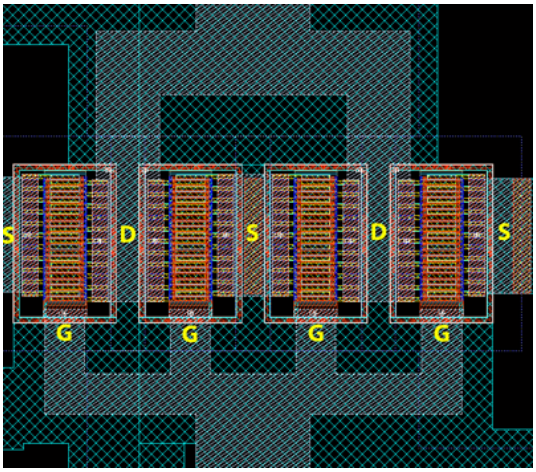


Figure 3.28: Transistors connected in parallel. S: Source G: Gate D: Drain

Transistors in parallel

All of the components' layouts have layers called dummy metal block layers (See Fig. 3.4). These layers prevent the placement of dummy metals near the components. For the simulation models to maintain their reliability, one should pay attention not to add any metals inside these areas. On the other hand, when connecting transistors in parallel, one would want to realize this in a minimum possible area, with a minimum length of transmission line in order to prevent losses. Thus, transistors are connected in parallel such that they are as close to each other as much possible and that there is no metal shapes (except transmission lines) inside the forbidden zones (see Fig. 3.28).

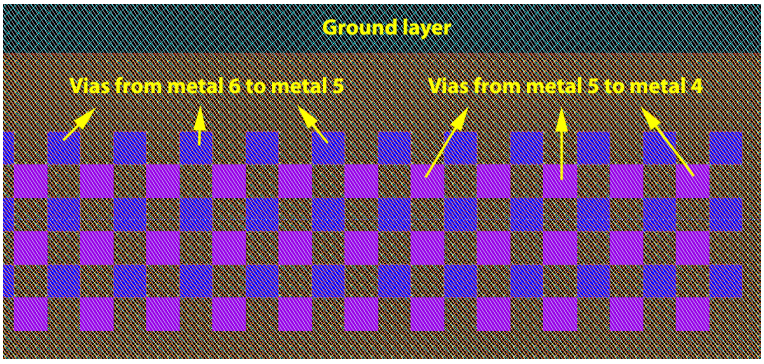


Figure 3.29: The top view of a ground connection.

Ground connections

Since the bottom metal layer is used as the ground layer, all ground connections have to end up in the bottom metal. On the other hand, the top metal layer is chosen to be the signal layer because it's the thickest metal layer. Therefore, all ground connections have to be made from the top metal (6^{th} metal layer) to the bottom metal (1^{st} metal layer). Unfortunately, there are no direct vias between these two layers. For a ground connection, one should add vias between all consecutive metal layers, and since the via size is fixed for this technology, for every ground connection, multiple vias are used to decrease the overall inductance and resistance caused by the vias (see Fig. 3.29).

Dummy metal

One of the design rules specified by the foundry is that the ratio of the coverage of a metal area to the entire chip's area has to be higher than a given percentage and also, the metal coverage should be distributed as evenly as possible over the entire chip. To conform to the rule, the unused places of the chip are covered with dummy metal shapes and the circuit is distributed over the chip as evenly as possible. During fabrication, the foundry adds further dummy metal to the blank spots and there is a possibility that these dummy metals are placed too close to the transmission lines so that the simulations are no longer valid. In

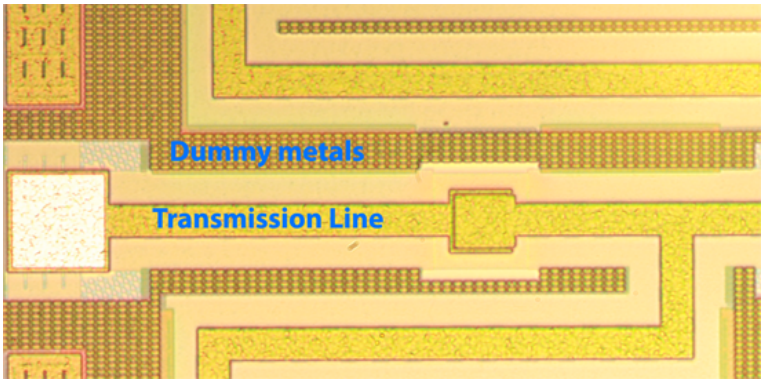


Figure 3.30: Photo of the fabricated chip under microscope. Dummy metals are added by the foundry to the blank spots of the chip. The entourage of the transmission lines is clean since dummy metal block layer was added to the layout.

order to prevent this possibility, the surroundings of the transmission lines are covered with dummy metal block layers (see Fig. 3.30).

Final layout

After drawing the layout, DRC, LvS and antenna rule checks are performed. The error free final layout for the K-band amplifier can be seen in Fig. 3.31. For better visualization of the layout and to make a comparison between the layout and the fabricated chip, a layout view where only the signal layer is present is added (see Fig. 3.32(a)). The photo of the fabricated amplifier is in Fig. 3.32(b).

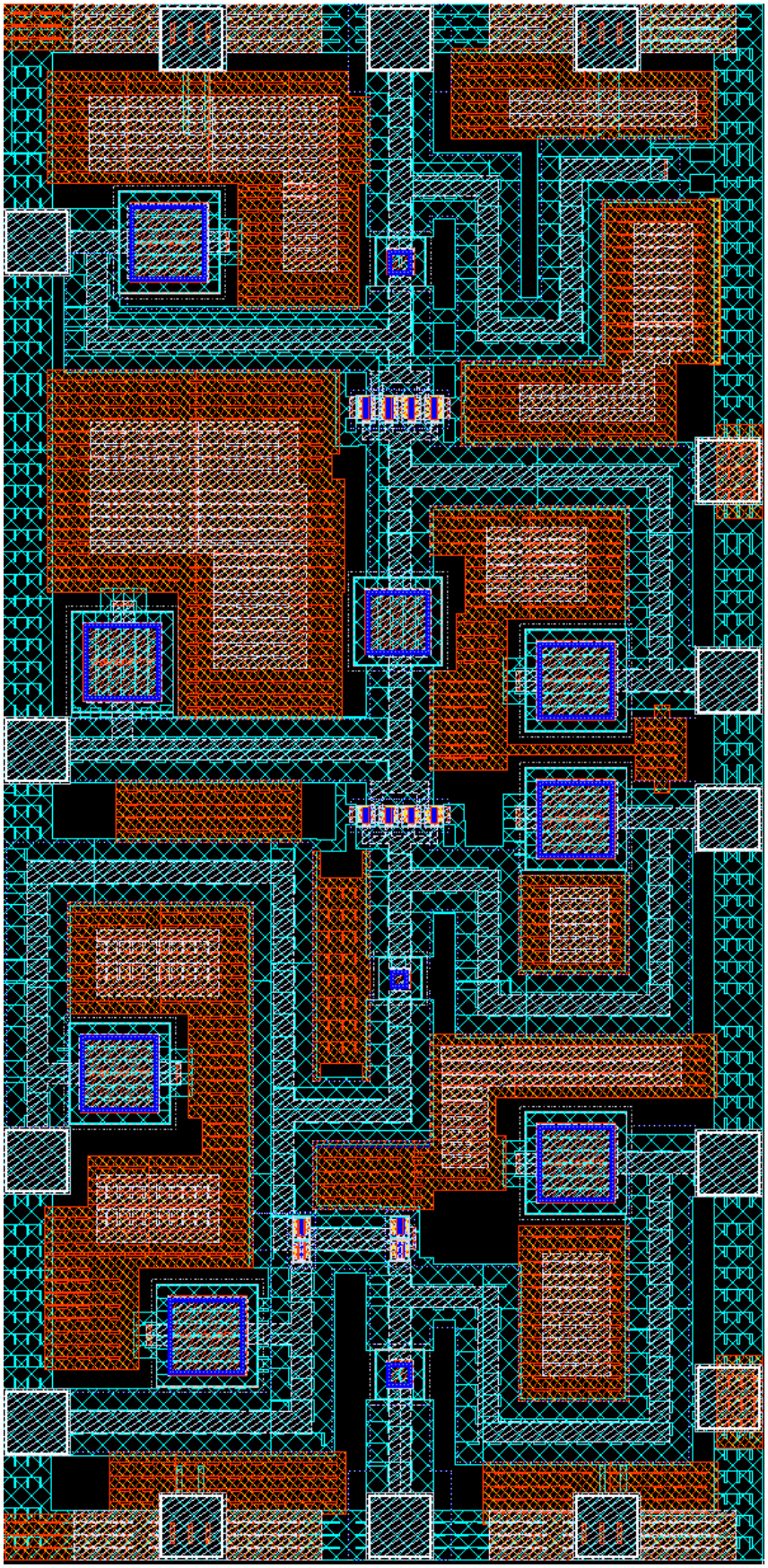
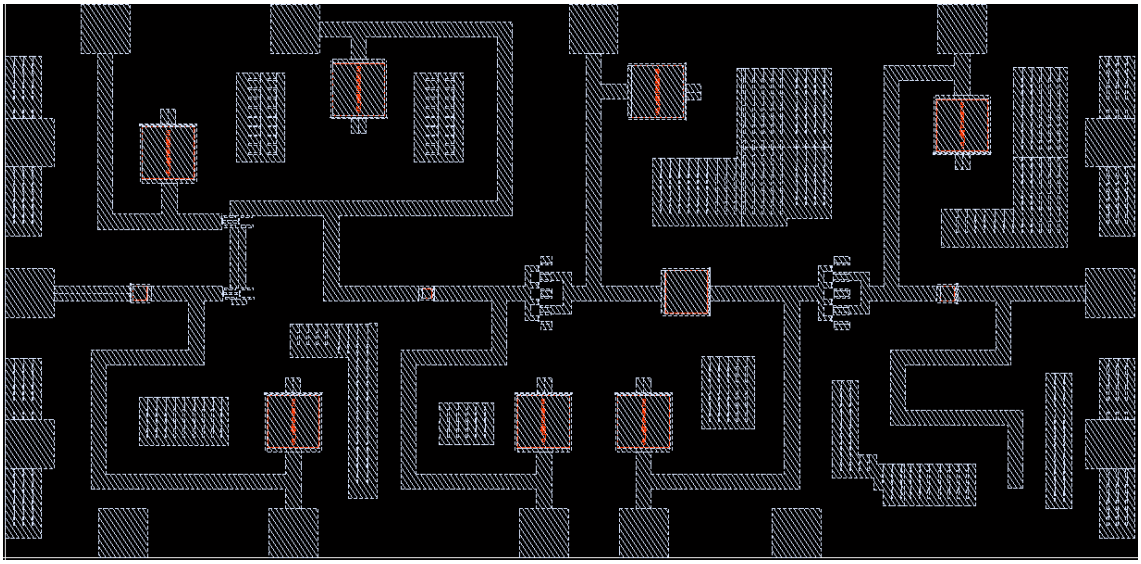
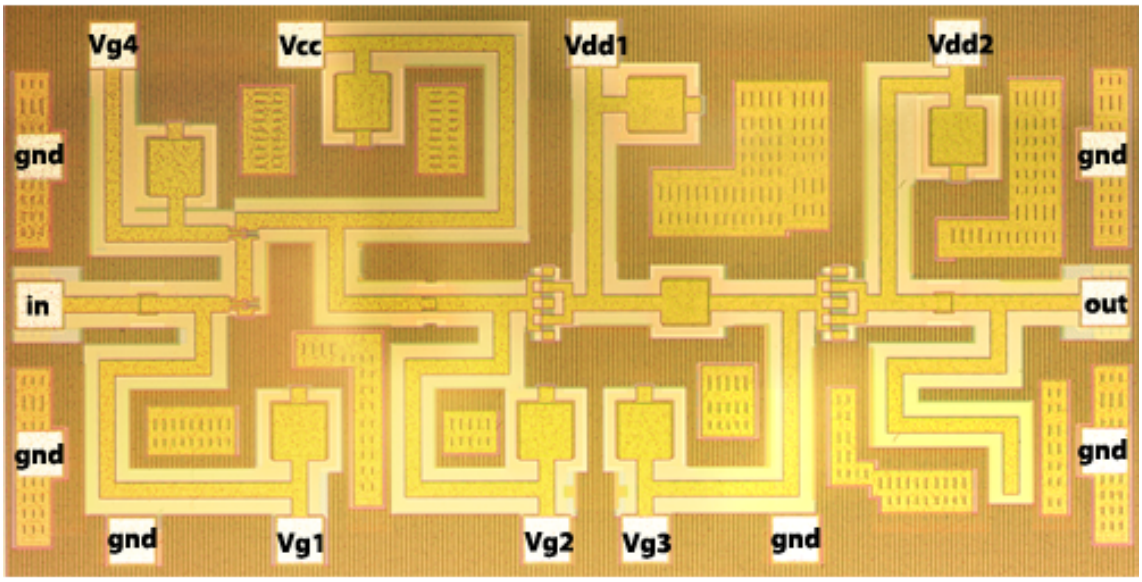


Figure 3.31: Layout top view of overall circuit from Cadence Virtuoso.



(a)



(b)

Figure 3.32: a) Top metal layer top view of K Band amplifier. b) Photo of the fabricated amplifier. The chip size is 1.5 x 0.7 mm^2

Chapter 4

Measurement Results

4.1 Measurement Preparation

Once the chip is fabricated, measurements can be made using DC and RF probes on a probe station. In the design, there are 7 DC bias connection pads and 2 RF pads; the input pad and the output pad which makes 9 pads in total. Since the chip is very small, it's not practical to make all these 9 connections using probes. Thus, another approach is taken; A bias "printed circuit board" (PCB) is prepared to deal with DC bias connections. The chip is placed at the center of

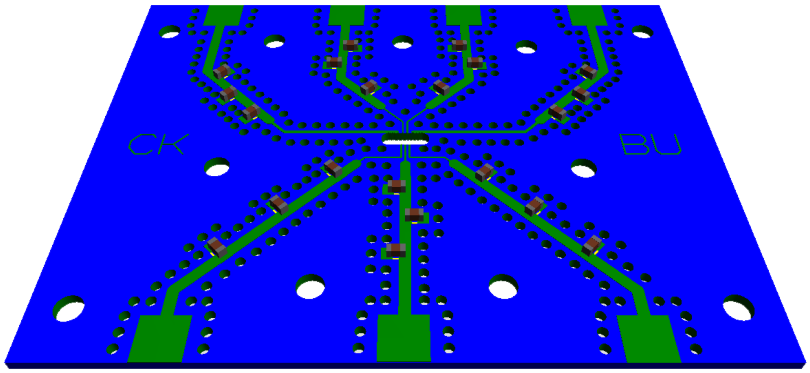


Figure 4.1: Bias printed circuit board illustration

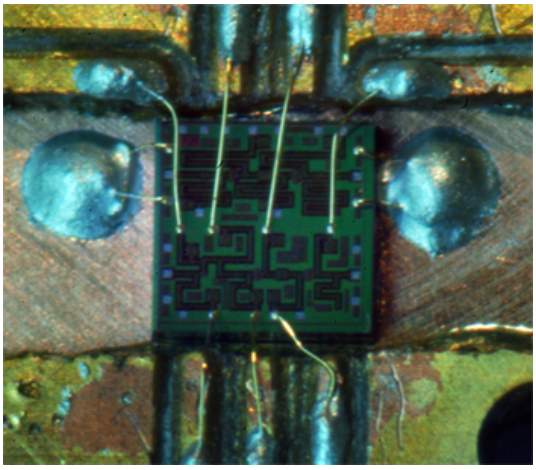


Figure 4.2: Wirebonded chip photo.

this PCB and DC pads are wire bonded to the DC bias lines of the PCB. That way, the number of probes needed is decreased to 2.

PCB's metal layers are made of copper, the chip's pads are made of aluminum while the wire that is used by the wire bonder is made of gold. Bonding gold to aluminum is straight forward but bonding gold to copper is problematic since they don't stick together. To overcome the problem, PCB's top metal layer is gold coated before bonding and contacts are strengthened using conductive epoxy after bonding.

4.2 Measurement Results

All measurements are made on the probe station with the help of two RF probes, one for the input, the other for the output. Necessary DC voltage supplies are connected to the bias PCB. The chip draws 160 mA from the 1.8 V supply and 35 mA from the 3.1 V supply.

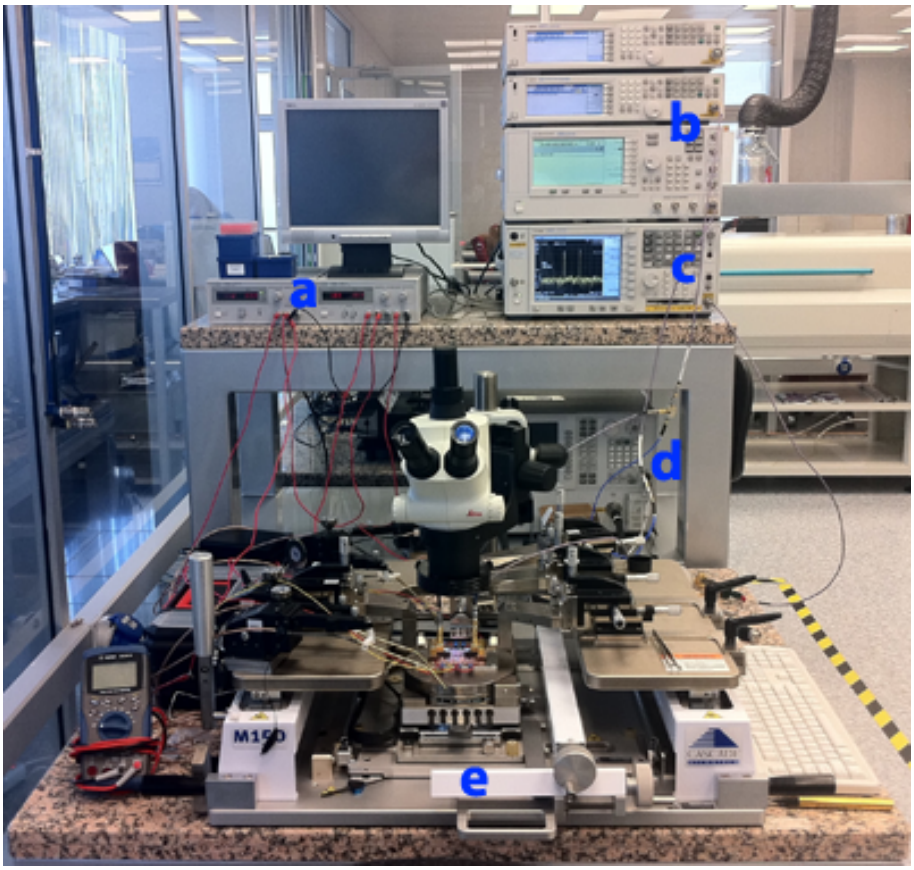


Figure 4.3: Measurement setup. a) DC power supplies. b) Signal generators. c) Spectrum analyzer. d) Network analyzer. e) Probe station.

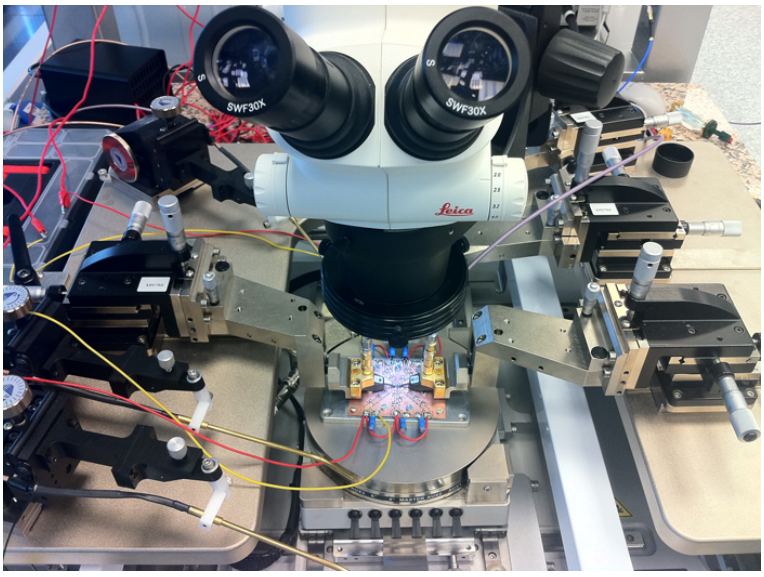
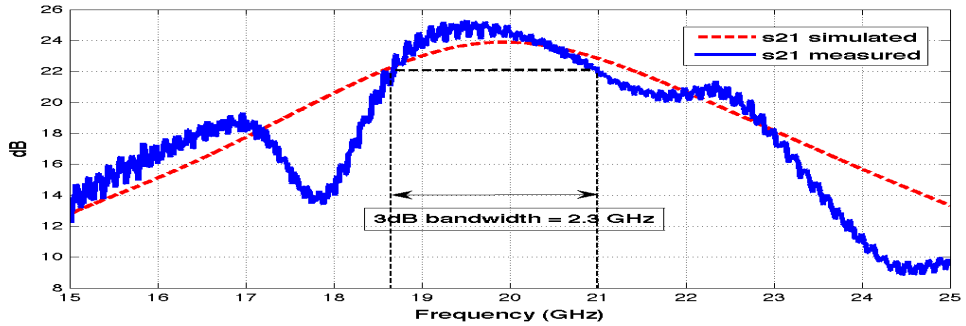


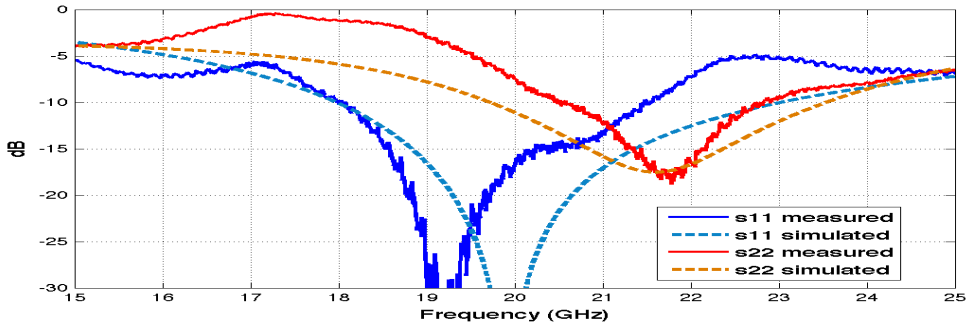
Figure 4.4: The chip under the probe station. Two RF probes are used to connect the input and output pads.

4.2.1 S-parameters measurement

S-parameters measurement is taken using a network analyzer. The small signal gain of the amplifier is 24 dB at 20 GHz. The 3-dB bandwidth is 2.3 GHz, from 18.7 GHz to 21 GHz. Within the band, s_{11} is less than -13 dB and s_{22} is less than -2 dB. At 20 GHz, these values are -16.9 dB and -7.5 dB respectively.



(a) Simulated and measured gain of the amplifier.



(b) Simulated and measured input and output reflection coefficients of the amplifier.

Figure 4.5: S-parameters measurement results for the fabricated design.

4.2.2 P_{1dB} measurement

The P_{1dB} measurement is taken using a signal generator and a spectrum analyzer. When two RF probes are directly connected to each other via a thru, i.e., the

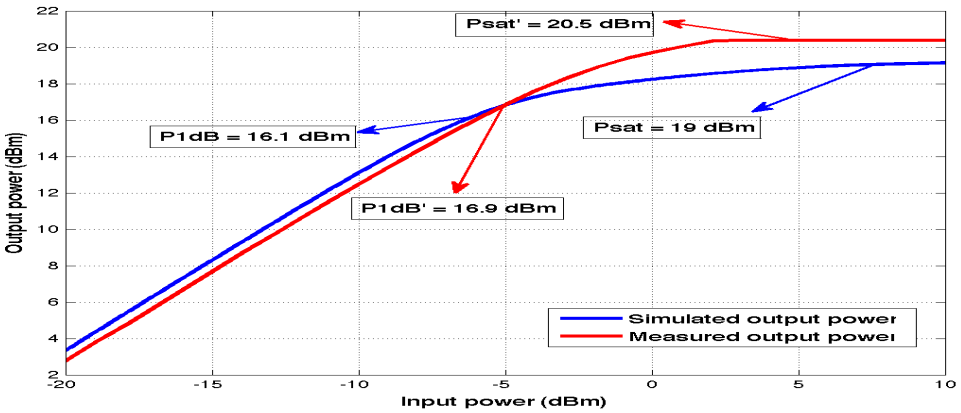


Figure 4.6: Output power vs input power. The output referred P_{1dB} measured is 16.9 dBm, whereas the saturated output power reaches 20.4 dBm.

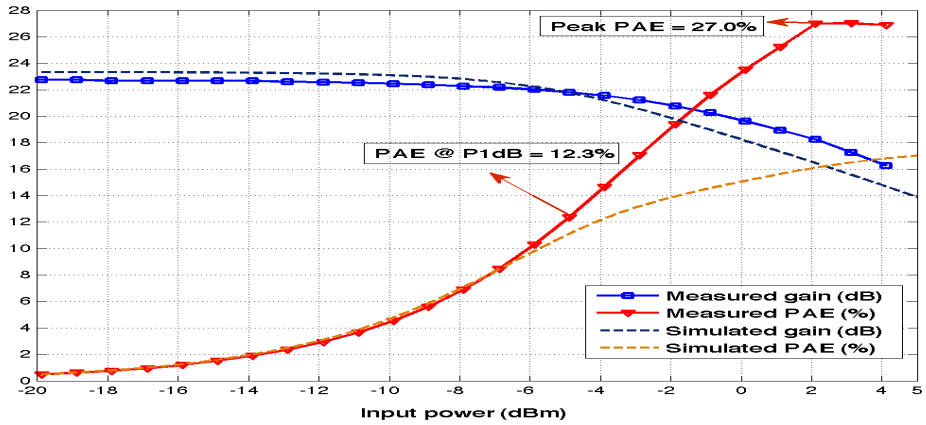


Figure 4.7: The power added efficiency and gain vs input power. PAE @ P_{1dB} is 12.3% whereas peak PAE is 27.0%

signal generator is directly connected to the spectrum analyzer, 19.76 dB loss is observed at 20 GHz. Since the connections at the input and output sides are identical, it's assumed that half of this loss occurs at the input and half of it occurs at the output. Subtracting the loss effect from the measurements, the output referred P_{1dB} level is 16.9 dBm with a corresponding PAE of 12.3%.

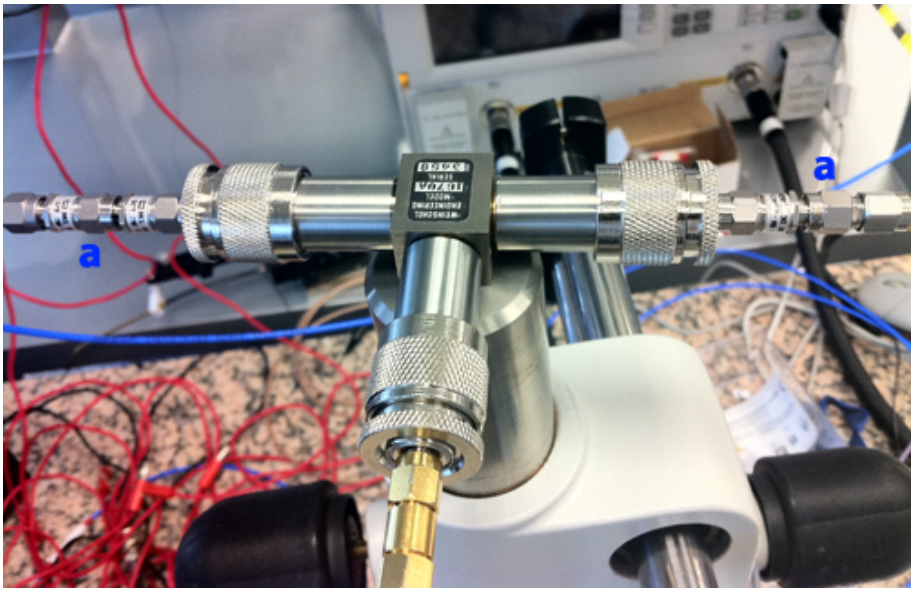


Figure 4.8: a) The 10 dB attenuators at the signal generator sides of the power combiner.

4.2.3 IP3 measurement

For the IP3 measurements, two tones separated by 100 MHz (at 19.95 GHz and at 20.05 GHz) are applied at the input like in [1]. Two tones are combined with a power combiner. Two 10 dB attenuators are added at the signal generator sides to increase the isolation between the signal generators to prevent any nonlinear effects that may be caused by other than the device under test. The resulting OIP3 value is 29.3 dBm.

4.2.4 Simulation vs measurement

Table 4.1 summarizes simulation and measurement results of the fabricated amplifier.

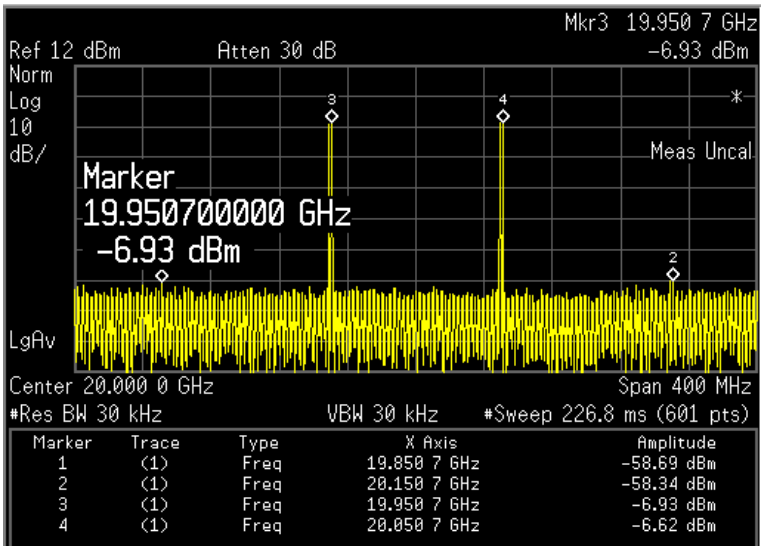


Figure 4.9: Spectrum analyzer screenshot for the output signal. The OIP3 value is 29.3 dBm when the loss is taken into account.

	Simulation	**Measurement**
s_{21} @ 20 GHz	23.8 dB	24 dB
3dB Bandwidth	3.8 GHz	2.3 GHz
P_{1dB} @ 20 GHz	16.1 dBm	16.9 dBm
P_{sat} @ 20 GHz	19 dBm	20.5 dBm
PAE @ P_{1dB}	9.37%	12.30%
peak PAE	17.20%	27.00%
OIP3	24.4 dBm	29.3 dBm

Table 4.1: Summary of simulation & measurement results.

4.2.5 Comparison to previous works

Table 4.2 summarizes the characteristics of the amplifiers fabricated in previously published works and includes a figure of merit (FoM) for each amplifier that serves to make a comparison. The FoM is defined as

$$FoM = P_{out} \times Gain \times PAE \times f^2 \tag{4.1}$$

where the output power is in watts, gain is in linear scale and f is in GHz [9]. The FoM of the amplifier presented in this work is the highest in works published so far.

Ref.	Tech.	Conf.	f (GHz)	P_{1dB} (dBm)	P_{sat} (dBm)	Gain (dB)	PAE (%)	FoM
[1]	0.18 μm	2-stages cascode	24	11	14.5	7	6.5	5.3
[2]	0.18 μm	2-stages cascode	24	13.3	19.1	18.8	15.6	554.0
[3]	0.18 μm	2-stages cascode w/ combiner	22	14.3	16.8	16.3	10.7	105.7
[4]	0.18 μm	3-stages common source	26.5	10.5*	12.5	12	8	15.8
[5]	0.13 μm	4-stages cascode / common source	18	-20*	10.9	26*	23.5	372.9
[10]	0.18 μm	2-stages series-bias	23	15*	17.7	9.5	10.4	28.9
[10]	0.18 μm	3-stages series-bias	23.5	11*	17.5	17.3	8.8	146.8
[11]	0.18 μm	1-stage w/ 4-way combiner	24	20	22	8	20	115.2
[12]	0.18 μm	3-stages cascode w/ combiner	20	16	20.1	22.5	9.3	676.9
[13]	0.18 μm	2-stages cascode	24	13.6	17.5	16.2	22.5	303.8
[14]	0.18 μm	3-stages common source	27	12.5*	14	14.5	13.2	68.1
[15]	0.18 μm	3-stages cascode	27	10.5*	14	17	6.7	61.5
[16]	0.13 μm	2-stages push-pull	17	15	17.1	14.5	9.3	38.8
[17]	0.13 μm	1-stage cascode w/ combiner	20	14.6	18.3	5.6	17	16.7
[18]	0.13 μm	1-stage push-pull	25.7	11*	13	8.4	13.2	12.0
This work	0.18 μm	3-stages cascode / common source	20	16.9	20.5	24	27	3043.2

Table 4.2: Comparison with previous works. *The value is not given explicitly but is approximated from the figure.

Chapter 5

Conclusions

In this work, the aim was to design and fabricate a K-band power amplifier using the digital 0.18 μm 1P6M CMOS technology. For this purpose, different topologies are investigated based on the models provided by the foundry. As a result, a three-stage amplifier topology (the first stage being in cascode configuration and the last two stages being in common source configuration) is adopted. The output and inter-stage matchings between second and third stages are optimized so that the P_{1dB} is maximized and input and inter-stage matchings between the first and second stages are adjusted to maximize the gain.The transistor widths are chosen so that the PAE is maximized without significantly decreasing the linearity of the amplifier. The overall design gave an output referred P_{1dB} of 16.1 dBm with a PAE of 9.37%, a saturated output power of 19 dBm with a peak PAE of 17.20% and a small signal gain of 23.8 dB in simulations.

The designed amplifier has been fabricated at the foundry and measurements are made on the fabricated chip. The measurement results are better than the simulation results. The chip gave an output referred P_{1dB} of 16.9 dBm with a PAE of 12.3%, a saturated output power of 20.5 dBm with a peak PAE of 27.00% and a small signal gain of 24 dB. The difference between measurement

and simulation results can be tied to the models provided by the foundry. These models were unfortunately valid up to 10 GHz and thus, in this work, they are used after extrapolation and it's stated in the model documents that the RMS error of the models can reach 10% is some cases.

As future work, models provided by the foundry can be extended and made more reliable for K-Band by adding some parasitic elements whose values can be found by making on-wafer measurements of the transistors as done in [4].

The difference in the output power between stages realized with ideal matching elements and lossy matching elements is about 2.2 dB. This loss may be decreased if other matching elements such as inductors instead of transmission lines are used. Such inductors can be designed and simulated using electromagnetic simulation tools since the design kit does not include them.

To further increase the output power that is obtained, power combining techniques can be used as done in [3], [11] and [17]. On the other hand, since the gates of the transistors draw zero current, gates can be biased with voltage division, which would allow to use only two supplies instead of three.

Bibliography

[1] A. Komijani, A. Natarajan, and A. Hajimiri, "A 24 GHz, +14.5 dBm fully integrated power amplifier in 0.18 um CMOS," *IEEE J JSSC*, vol. 40, no. 9, pp. 1901–1908, 2005.

[2] J.-L. Kuo, Z.-M. Tsai, and H. Wang, "A 19.1-dBm Fully-Integrated 24 GHz Power Amplifier Using 0.18-um CMOS Technology," in *Proc. European Microwave Integrated Circuit Conf. EuMIC 2008*, pp. 558–561, 2008.

[3] Y.-N. Jen, J.-H. Tsai, C.-T. Peng, and T.-W. Huang, "A 20 to 24 GHz 16.8 dBm Fully Integrated Power Amplifier Using 0.18 um CMOS Process," *IEEE J MWCL*, vol. 19, no. 1, pp. 42–44, 2009.

[4] J.-W. Lee and S.-M. Heo, "A Ka-Band CMOS power amplifier using new substrate-shielded coplanar waveguide," *Microwave and Optical Technology Letters*, vol. 50, pp. 2815–2817, November 2008.

[5] C. Cao, H. Xu, Y. Su, and K. K. O, "An 18-GHz, 10.9-dBm fully-integrated power amplifier with 23.5 % PAE in 130-nm CMOS," in *Proc. 31st European Solid-State Circuits Conf. ESSCIRC 2005*, pp. 137–140, 2005.

[6] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 1998.

[7] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*. Artech House, Inc., 2 ed., 2006.

[8] M. M. Radmanesh, *Radio Frequency and Microwave Electronics Illustrated*. Prentice Hall PTR, 2001.

[9] T. Yao, M. Q. Gordon, K. K. W. Tang, K. H. K. Yau, M.-T. Yang, P. Schvan, and S. P. Voinigescu, "Algorithmic Design of CMOS LNAs and PAs for 60-GHz Radio," *IEEE J JSSC*, vol. 42, no. 5, pp. 1044–1057, 2007.

[10] J.-W. Lee and S.-H. Hwang, "+17 dbm high-efficiency CMOS power amplifiers operating at high voltage for 24 GHz radar sensor," *IET Circuits, Devices & Systems*, vol. 4, no. 2, pp. 131–137, 2010.

[11] P.-C. Huang, J.-L. Kuo, Z.-M. Tsai, K.-Y. Lin, and H. Wang, "A 22-dBm 24-GHz power amplifier using 0.18-um CMOS technology," in *Proc. IEEE MTT-S Int. Microwave Symp. Digest (MTT)*, pp. 248–251, 2010.

[12] C.-C. Hung, J.-L. Kuo, K.-Y. Lin, and H. Wang, "A 22.5-dB gain, 20.1-dBm output power K-band power amplifier in 0.18-um CMOS," in *Proc. IEEE Radio Frequency Integrated Circuits Symp. (RFIC)*, pp. 557–560, 2010.

[13] H. Portela, V. Subramanian, and G. Boeck, "Fully integrated high efficiency K-band PA in 0.18 um CMOS technology," in *Proc. SBMO/IEEE MTT-S Int. Microwave and Optoelectronics Conf. (IMOC)*, pp. 393–396, 2009.

[14] J.-W. Lee and S.-M. Heo, "A 27 GHz, 14 dBm CMOS Power Amplifier Using 0.18 um Common-Source MOSFETs," *IEEE J MWCL*, vol. 18, no. 11, pp. 755–757, 2008.

[15] H. Shigematsu, T. Hirose, F. Brewer, and M. Rodwell, "Millimeter-wave CMOS circuit design," *IEEE J MTT*, vol. 53, no. 2, pp. 472–477, 2005.

[16] A. V. Vasylyev, P. Weger, W. Bakalski, and W. Simbuerger, "17-GHz 50-60 mW power amplifiers in 0.13-um standard CMOS," *IEEE J MWCL*, vol. 16, no. 1, pp. 37–39, 2006.

[17] M. Ferndahl, T. Johansson, and H. Zirath, "20 GHz Power Amplifier Design in 130 nm CMOS," in *Proc. European Microwave Integrated Circuit Conf. EuMIC 2008*, pp. 254–257, 2008.

[18] A. Vasylyev, P. Weger, and W. Simburger, "Ultra-broadband 20.5-31 GHz monolithically-integrated CMOS power amplifier," *Electronics Letters*, vol. 41, no. 23, pp. 1281–1282, 2005.