HIGHLY EFFICIENT 300 W MODIFIED CLASS-E RF AMPLIFIERS FOR 64 MHz TRANSMIT ARRAY SYSTEM

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Highly Efficient 300 W Modified Class-E RF Amplifiers for 64 MHz Transmit Array System

By Fatima Tu Zahra
December, 2017

We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

Highly Efficient 300 W Modified Class-E RF Amplifiers for 64 MHz Transmit Array System

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M.S. in Electrical and Electronics Engineering

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December, 2017

The conventional MRI system uses high power linear RF amplifiers which are placed away from scanner room, have low efficiency, high cost and need a cooling system. We aim to use parallel transmit system with on-coil amplifiers that has shown to be advantageous in improving B1 field homogeneity, slice selectivity and SAR reduction.

In this work the on-coil class-E RF switching amplifier is suggested for MRI to decrease the cost and complexity of the current system while improving performance. The amplifier is digitally controlled and for pulse generation purpose supply modulation is used. The transmit coil acts as the load network of the amplifier so the need for matching circuit is eliminated. The amplifier has an output power of 300 W with maximum efficiency of 92%. The efficiency does not drop below 75% in 1 MHz bandwidth. The performance of amplifier at high temperature is also evaluated and it is established that at low duty cycles due to high efficiency no cooling system is required but for high duty cycle applications a cooling system might be needed for the uninterrupted operation. The ultimate goal of this research is to design a 32-channel transmit array using on-coil amplifiers, as a step forward towards this goal a prototype for two channels is designed. Our results depict that the behavior of the class-E amplifiers under coupled operations is acceptable. The dual-channel prototype was tested on Scimedix 1.5 T and no artifacts were observed in the images due to the presence of amplifiers near transmit coils inside the bore.

To sum up, the class-E amplifier is proved to be a favorable candidate for on-coil applications in RF excitation due to its small size, reduced complexity and high efficiency

Keywords: RF amplifier, Class-E amplifier, Digital control, Parallel transmission

ÖZET

64 MHz Verici Dizisi Sistemi için Yüksek Verimli 300 W Değiştirilmiş Class-E RF Yükselteci

Fatima Tu Zahra

Elektrik ve Elektronik Mühendisliği, Yüksek Lisans

Tez danışmanı: Ergin Atalar

Aralık, 2016

Günümüzde kullanılan MRG sistemleri doğrusal ve yüksek güçteki RF yükselteçleri ile çalışır. Bu yükselteçler görüntüleme odasının dışında olmakla birlikte düşük verimli, yüksek maliyetli ve soğutma sistemlidir. B1 türdeş alanı oluşturmada, kesit seçiminde ve SAR azaltımında avantajlı olduğu gösterilmiş olan paralel verici sisteminde bobin üzeri yükselteçler kullanmayı hedefledik.

Bu çalışmada MRG için performansı geliştirmekle birlikte maliyeti ve karmaşası az olan bobin üzeri class-E tipi RF anahtarlama yükselteci önerilmiştir. Yükselteç sayısal olarak kontrol edilebilir ve sinyal üretimi için besleme kiplemesi kullanmaktadır. Verici bobin, yükseltecin yük ağı olarak davrandığı için uydurma devresi gerekliliğini ortadan kaldırılmıştır. Yükseltecin çıkış gücü 300 W ve maksimum verimliliği %92'dir. Verimlilik 1 MHz bantta %75'in altına düşmemektedir. Yüksek sıcaklıklardaki yükselteç performansı ayrıca değerlendirilmiştir ve yüksek verimliliğinden dolayı düşük görev döngüsü durumunda soğutma sistemine ihtiyaç yoktur. Araştırmada nihai hedef 32 kanallı bobin üzeri yükselteç dizisi tasarlamaktır. Bu hedefe atılacak adımlardan birisi olarak 2 kanallı prototip tasarlanmıştır. Sonuçlarımız class-E tipi yükselteçlerin kuplaj durumlarında kabul edilebilir olduğunu göstermiştir. Çift kanallı prototip Scimedix 1.5T sisteminde test edilmiştir ve görüntülerde verici bobinlerin yanında çalışan yükselteçlerden dolayı bozulma gözlenmemiştir.

Özetle, class-E tipi yükselteçlerin RF-uyarım uygulamalarında küçük boyutu, basit olması ve yüksek verimliliği ile bobin üzeri yapılarda tercih edilebilir bir aday olduğu kanıtlanmıştır.

Anahtar Kelimeler: RF yükselteç, Class-E yükselteç, Sayısal kontrol, Paralel vericiler

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CHAPTER 1

INTRODUCTION

Magnetic resonance imaging (MRI) is a noninvasive imaging technique that uses strong magnetic field (Bo), radio frequency field (B1) and linear gradient fields (G) to produce detailed high quality images of the inside of body [1]. In magnetic resonance imaging (MRI), the radio frequency (RF) transmit chain is an important building block of the system for imaging. It consists of a frequency synthesizer, modulator, an amplifier and a transmit coil. This block is used to generate the continuous sinusoidal carrier wave at the Larmor frequency, modulate it to form the appropriate pulse shape in the order of milliseconds, amplify it at a required level and then transmit it to the body under examination to get the image.

In the commercial scanners, linear low efficiency amplifiers are used. They need bulky cooling system due to high power loss in them so they are placed in the system's room outside the scanner's room, far from the transmit coil inside the scanner. The transmit coils are however located either within the inner walls of the scanner or as free-standing devices placed near or on the patient. So the overall complexity of the system increases due to the distance between transmit coil and amplifier. Long transmission cables are used which causes the efficiency to decrease even further and increases the cost of the system.

The image quality is quantified on several criteria such as the resolution of image, imaging speed, amount of artifact and the signal level with respect to the noise level commonly the signal-to-noise ratio (SNR). The birdcage coil [2] has been widely used as transmit coil due to its high transmit efficiency and homogeneity. However, It was observed that in high fields (>3T) birdcage coils performance degrades and SNR decreases. As a solution to this problem, multichannel transmits systems are proposed as an alternative to the current system. Graesslin et al. integrated a complete 8 channel Tx/Rx system on 3T Philips scanner [3]. There are various advantages of parallel transmission as outlined by [4]. It has more degree of freedom as multiple elements can be controlled in a transmit array separately. The B1 filed uniformity and homogeneity is improved [5] [6] [7]. The several independent transmission coils presents higher degree of freedom for local area excitation and multiple slice selectivity. The localized excitation can take very long time if only single coil is used but with multiple transmission coils it can be achieved that in less time [8] [9] [10]. Parallel transmission has also shown advantage in improving RF-shimming and increasing the imaging speed [11] [12] [13]. The maximum speedup factor is nearly equal to the number of coil elements used in parallel transmission [14]. On top of that, parallel transmission is advantageous in the reduction of specific absorption rate (SAR), as RF power can be applied only to volume of interest so the overall SAR given to the patient can be decreased [15] [16]. Eryaman's and Silemek's work shows that RF heating on long metallic implant can also be reduced by controlling the electric field using parallel transmission [17] [18]. Although parallel transmission is beneficial in some regards but it poses some difficulties when it comes to implementing it. As the number of elements increases in the system, its complexity increases as the cabling increases sue to separate power lines and control signals for each channel. The major problem faced is coupling between the adjacent transmit coils. This causes not only the efficiency to decrease but also artifacts in the images to unwanted B1+ field in the neighboring coils.

The main focus of the previous works on RF chain is to develop the pulse modulator, amplifier and transmission coil separately. However recently many researchers are trying to integrate these three units into a single unit to simplify the design. Several novel

designs of on-coil amplifiers have been proposed to replace the low efficiency RF amplifiers [19]. RF amplifier module for 3 T was presented [20]. Gudino proposed a current-mode Class-D switching amplifier. She tested her design for 1.5 T and also for higher fields [21] [22] [23]. We chose to work on class-E amplifier as it is suitable for on-coil amplifier applications. The class-E amplifier was proposed initially by Sokal and Sokal [24] and later Raab [25] and some other authors [26] [27]further worked on deriving the design equations for it. It is a switching type of amplifier which includes a choke inductor, a switch, a shunt capacitor and an RLC load network. This amplifier was presented before with 100 W output power and maximum efficiency of 65% [28] [29] then the efficiency was improved to 88% in later work [30]. The transmit coil was designed such that it can acts as the RLC load network for amplifier eliminating the need of 50 ohm matching circuit. Since the amplifier is placed near the coil the need for long transmission cables carrying RF power from amplifier to transmit coils was eliminated. In this work 2-channel transmit array is presented as a step toward a 32-channel TxArray RF chain. The amplifier is improved further, it is completely digitally controlled and for pulse generation supply modulation technique is used. The developed system is tested in Scimedix 1.5 T and the results are quite promising. With this work, it was aimed to decrease the complexity and cost while improving the performance as compare to the current conventional system.

CHAPTER 2

THEORY

In this chapter the design of class-E amplifier is explained. Firstly the working and design equations for conventional class-E amplifier are discussed. After that the modifications that were done in the amplifier are described. The choke inductor of class-E amplifier was replaced by a transmission line of similar behavior. The design equations for this purpose are given. Load pull analysis was done in order to design the load network of the amplifier and also to tune it so that it can provide 300 W output power with maximum possible efficiency. The design of the driver circuit that is used to drive the main transistor of amplifier is explained in detail. The driver is capable of driving the main transistor of output power 300 W at 64 MHz. As the output is required to be in specific pulse shapes in the order of millisecond, supply modulation block was used to achieve this purpose. In the end, the details of main theory behind supply modulation block are discussed.

2.1. Conventional Class-E Amplifier

Class-E amplifier is a switching type amplifier that can theoretically achieve 100% efficiency. The conventional class-E amplifier as shown in Fig. 2.1 consists of a dc supply voltage (V_{dc}), a dc feed choke inductor (L_{choke}), a switch (M1), a shunt capacitor (C_{sh}), a

shifting inductor (L), a series resonator made up of a resonant capacitor (C_0) and a resonant inductor (L_0) and a load resistor (R).

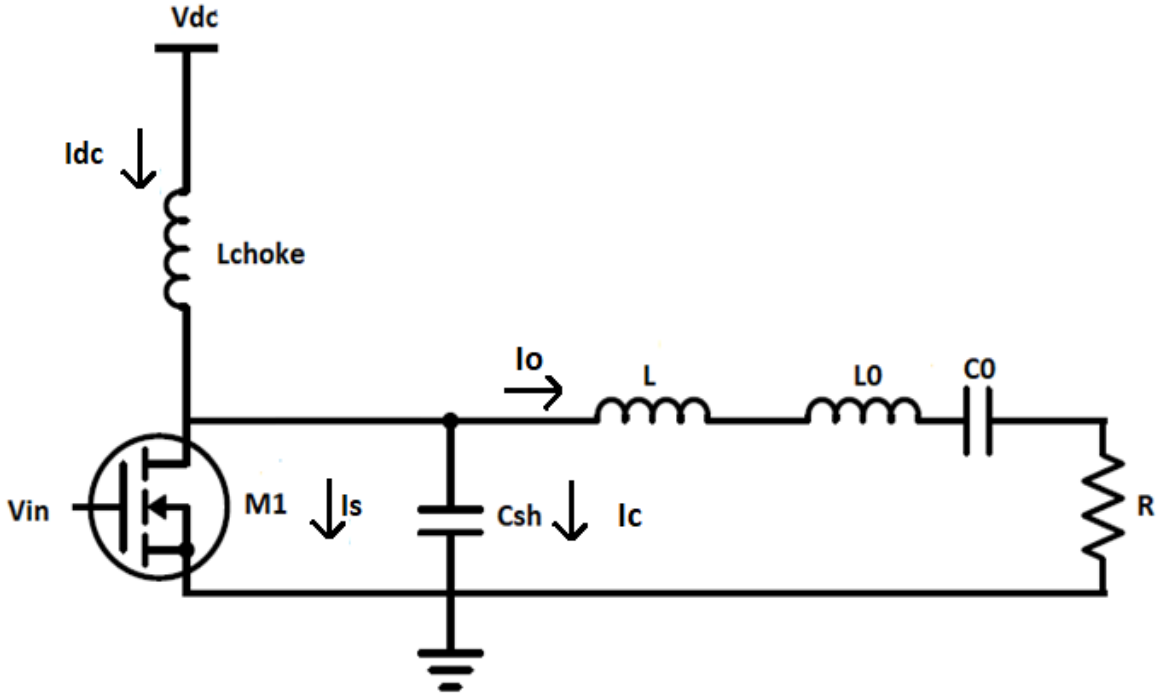


Fig. 2. 1: Conventional class-E amplifier

While driving the equations of class-E amplifier following assumptions has been made.

- Input voltage is a square wave with approximately 50% duty cycle.
- The value of choke inductor is high enough to block the RF signal
- The parasitic drain to source capacitance of MOSFET is linear.
- The MOSFET is assumed as an ideal switch which means $R_{on} = 0$.
- The current is purely sinusoidal due to high value of loaded quality factor (Q) of series resonator circuit.
- All the components in the circuit are ideal (non-lossy)

Under this ideal case, the source power can be delivered to the load with 100% efficiency.

In the case of Class-E amplifier the ZVS (zero voltage switching) and ZDVS (zero derivative of voltage at switching) is satisfies assuring no power loss in the MOSFET. The switch voltage and switch current diagram is shown in Fig. 2.2.

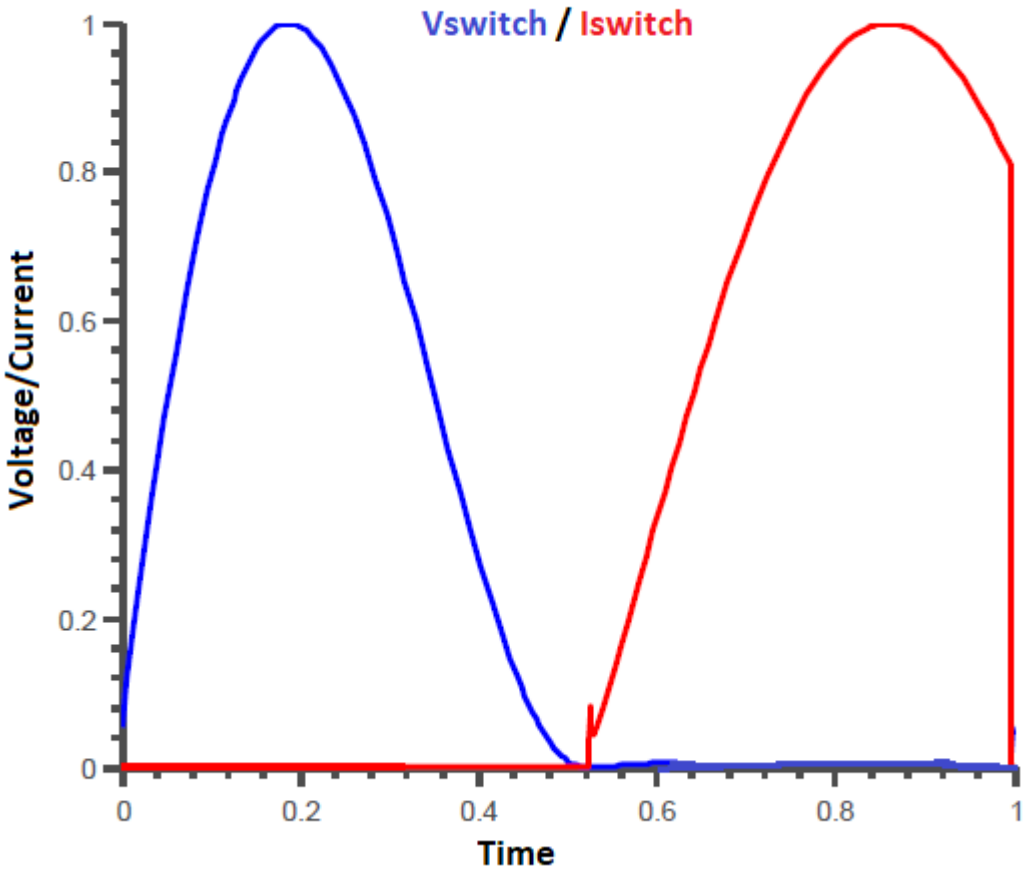


Fig. 2. 2: Switch current (red) and switch voltage (blue) of class-E amplifier

It is shown in the figure that for the first half cycle when the input voltage is 0 the switch voltage is high and no current flows though the switch and for the second half cycle when the input voltage is 1 the switch voltage is 0 and current flows through the switch. The design equations for class-E amplifier have been developed. The derived equations for class-E amplifier taken from [24] [25] [27]are given below.

During the first half period the input voltage is off so the current in the switch is zero. This means

$$I_{dc} = i_0 + i_c \tag{2.1}$$

$$i_c = C_{sh} \frac{d}{dt} V_{sh} \tag{2.2}$$

As output current is purely sinusoidal it can be written as

$$i_0(t) = I_0 \sin(\omega_s t + \varphi)\, V_{sh} \tag{2.3}$$

Where I_0 is the amplitude and ω_s is the fundamental frequency and φ is the phase shift. The current in the shunt capacitor can be written as:

$$C_{sh} \frac{d}{dt} V_{sh} = I_{dc}(1 - \alpha \sin(\omega_s t + \varphi)\, V_{sh} \tag{2.4}$$

So by solving this the switch voltage comes out to be

$$V_{sh} = V_s = \frac{I_{dc}}{\omega_s C_{sh}} (\omega_s t + \alpha(\cos(\omega_s t + \varphi) - \cos \varphi))) \tag{2.5}$$

As for class-E amplifier ZVS and ZDVS should be satisfied so using these boundary conditions we can calculate the values of α and φ.

$$\alpha \approx 1.86 \quad ; \quad \varphi \approx -32.5°$$

After solving the equations and finding all the unknown switch voltage for both when the switch is on and when the switch is off can be calculated as following.

$$V_s(t) = \begin{cases} \frac{I_{dc}}{\omega_s C_{sh}} (\omega_s t + \alpha(\cos(\omega_s t + \varphi) - \cos \varphi))) ; & 0 \le \omega_s t \le \pi \\ 0 \quad ; & \pi \le \omega_s t \le 2\pi \end{cases} \tag{2.6}$$

Similarly the equations for switch current can be derived as

$$I_s(t) = \begin{cases} 0 \quad ; & 0 \le \omega_s t \le \pi \\ I_{dc}(1 - \alpha \sin(\omega_s t + \varphi) \quad ; & \pi \le \omega_s t \le 2\pi \end{cases} \tag{2.7}$$

The literature can be followed to find the set of equations that are derived to design the Class-E amplifier. From [24] the component values of class E amplifier can be found using the following equations

$$R = \frac{V_{dc}^2}{P_{out}}\ 0.58\left(1 - \frac{0.451759}{Q} - \frac{0.4}{Q^2}\right) \tag{2.8}$$

$$C_0 = \left(\frac{1}{2\pi f_0 R}\right)\left(\frac{1}{Q-0.1}\right)\left(1 + \frac{1}{Q-1.8}\right) - \frac{0.2}{(2\pi f_0)^2 L_{choke}} \tag{2.9}$$

$$C_{sh} = \frac{1}{34.2\ f_0 R}\left(1 + \frac{0.9}{Q} - \frac{1}{Q^2}\right) + \frac{0.6}{(2\pi f_0)^2 L_{choke}} \tag{2.10}$$

$$L_0 = \frac{QR}{2\pi f_0} \tag{2.11}$$

Where R is the load resistance, Q is the quality factor of resonator circuit,f_0 is the fundamental frequency and P_{out} is the desired output power.

For our design the transmit coil was designed such that V_{dc}=30 V P_{out} =300 W. The inductance of the transmit coil is L_0=256 nH ,f_0=64 MHz and Q=70. Using the above equations we can calculate C_0=24.5 pF, R=1.47 Ω and C_{sh}= 315 pF.

In case of non-ideal switch, the efficiency calculations in [24] and [31] leads to the power loss in the MOSFET as

$$P_{RdsOn} = 1.37\ \frac{R_{dsON}}{R}\ P_{out} \tag{2.12}$$

And the efficiency of the amplifier in this case can be calculated by the following equation.

$$\eta = \frac{R}{R+1.37\ R_{dsON}}\ 100\% \tag{2.13}$$

2.2. Modified Class-E Amplifier

To use the class-E amplifier for RF excitation in MRI, the conventional Class-E amplifier design is modified to meet the design requirements of the on coil RF amplifier for MRI. For this purpose the choke inductor was replaced with a short transmission line. The load network of modified amplifier consist of the transmit coil that is used for excitation. The inductance of the transmit coil acts as the resonant inductance L0. There are three distributed capacitors C1, C2 and C3 connected in series on the transmit coil for tuning purposes. The equivalent of these three capacitors forms the resonant capacitor C0 of the class-E amplifier. The load resistance R comes from the loading of the coil by the body or phantom. The amplifier is completely digitally controlled through FPGA and to drive the MOSFET a driver was designed. As in the RF amplifiers for MRI, a pulse in the order of milliseconds with some specific shape such as sinc, gauss, triangular etc. is required. It was achieved by envelop modulation. For this purpose, supply modulation block was used. Fig. 2.3 shows the proposed modified class-E amplifier.

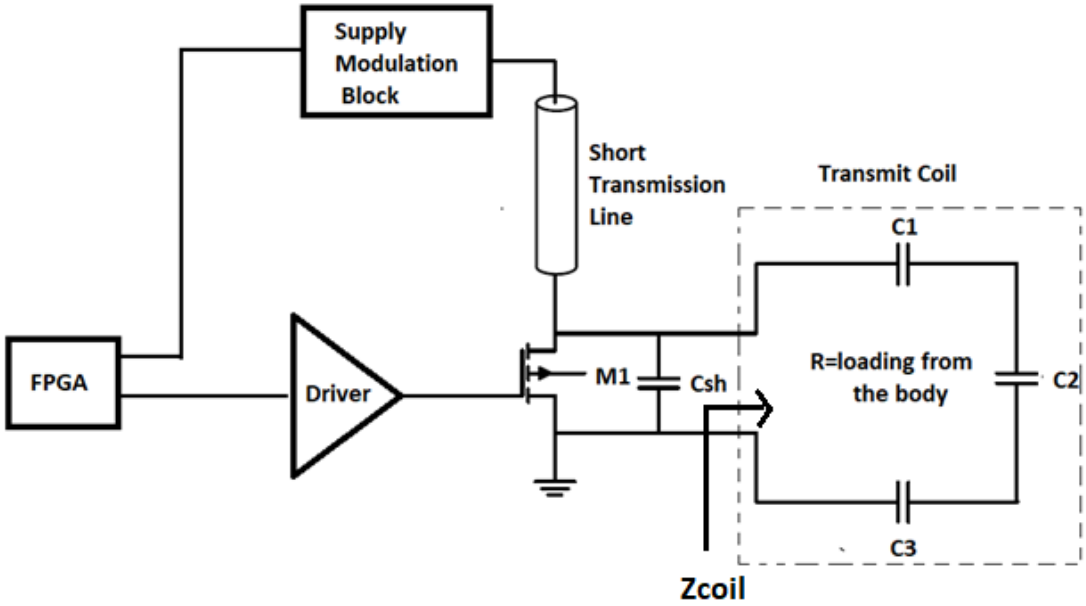


Fig. 2. 3: Proposed modified class-E amplifier

2.2.1. Coaxial Transmission Line Instead of Choke Inductor

In class-E amplifier design an ideal current source is needed at the drain of main MOSFET. For this purpose, a large inductor is used as an RF choke, the current drawn from the RF choke inductor consists of DC current with a small AC ripple. The magnitude of this AC ripple depends on the value of choke inductor. The main power of this AC ripple is in the fundamental frequency and as the number of harmonics increases the power each next harmonic has decreases. To analyze the current of choke inductor in time domain, both switch on and switch off cases should be considered. The analysis is done by Poni in detail [30].

During the switch on case the equation for current in the choke inductor can be written as:

$$I_{Lchoke}(t) = I_{Lchoke}(t_0) + \frac{(t-t_0)V_{dd}}{L_{choke}} \quad (2.14)$$

V_{dd} is the supply voltage and L_{choke} is the choke inductance. As the switch will be on for half period so at the end of half period the current increase in the choke inductor can be written as:

$$\Delta I_{Lchoke}(t) = \frac{V_{dd}T}{2L_{choke}} \quad (2.15)$$

In the second half period when the switch is off the choke inductor current will decrease because in switch off state the voltage on the capacitor C_{sh} will be higher than the supply voltage. So the choke inductor current will be :

$$I_{Lchoke}(t) = I_{Lchoke}(t_0) + \int_{t_0}^{t} \frac{V_{dd}-V_{sh}(t)}{L_{choke}} dt \quad (2.16)$$

The waveform of current in the choke inductor as mentioned in [30] is shown in Fig. 2.4.

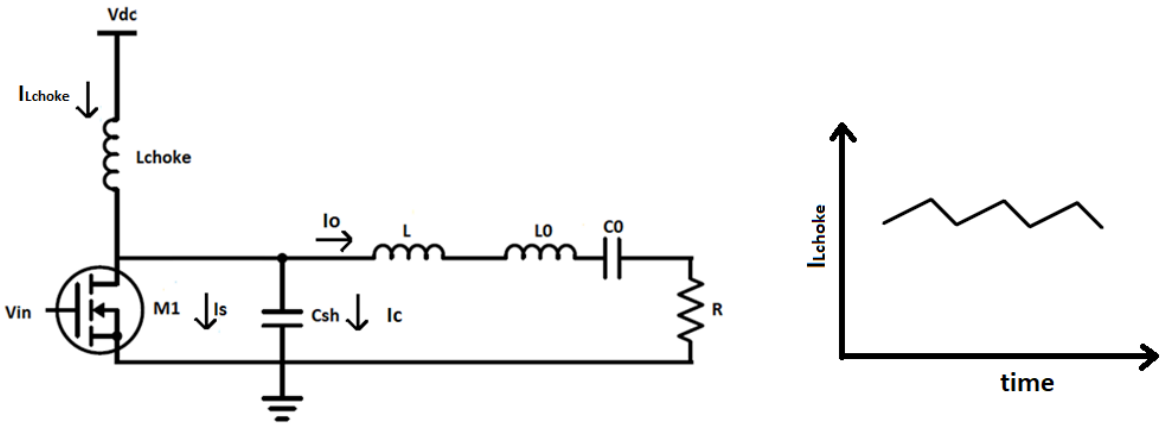


Fig. 2. 4: RF choke inductor current waveform

The high DC current on the choke inductor may cause an unwanted perturbation to the main magnetic field. This can cause unwanted artifacts in the images. To avoid this, the choke inductor is replaced by a short length coaxial transmission line. It has a property of keeping the magnetic and electric field confined between its inner and outer conductor, this makes it the best choice for our application. To replace the choke inductor with transmission line, it should be designed such that its behavior is similar to the choke inductor. So if the frequency domain is considered, the impedances of both states as done in [30] can be analyzed separately as shown in Fig. 2.5.

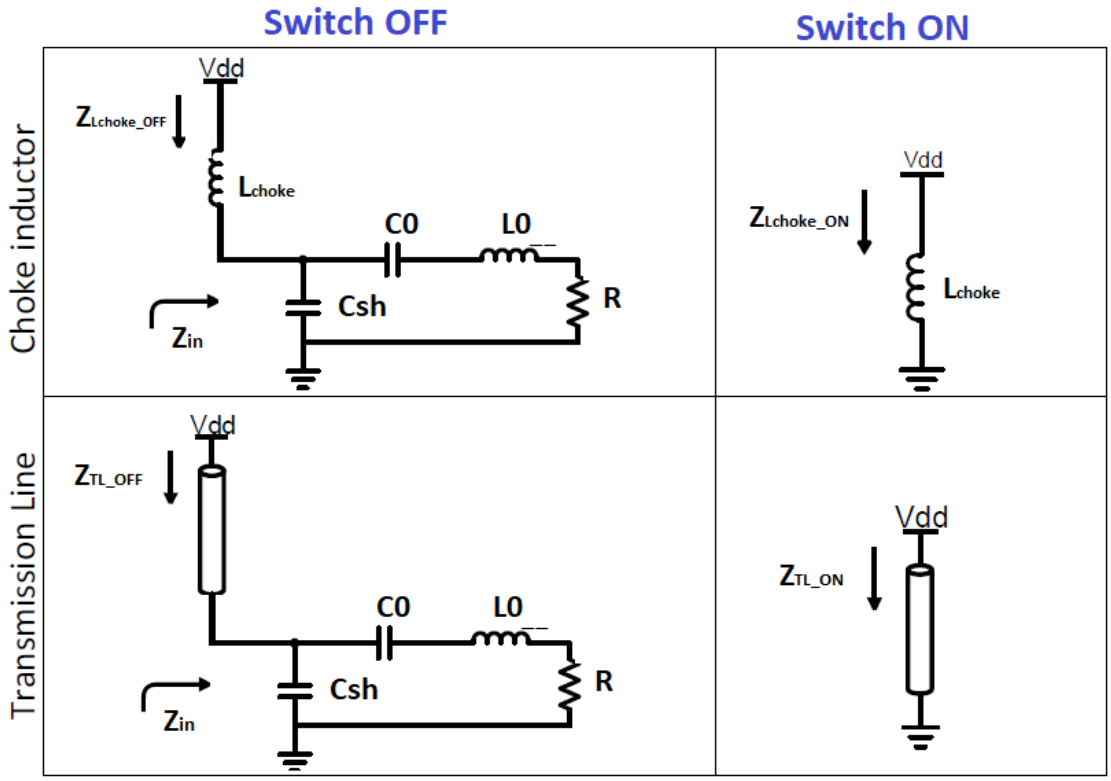


Fig. 2. 5: Impedances by using transmission line and choke inductor for both switch on and switch off cases in class-E amplifier design

During switch on state the impedance seen from V_{dd} when choke inductor is used is:

$$Z_{Lchoke\_ON} = j2\pi f L_{choke} \tag{2.17}$$

And Impedance if transmission line is used is:

$$Z_{TL\_ON} = jZ_0 \tan\left(\frac{2\pi f l}{v}\right) \tag{2.18}$$

where

Z_0 = characteristic impedance of transmission line.

v= speed in transmission line.

l= length of transmission line.

And during the switch off case the impedance is:

In case of choke inductor:

$$Z_{Lchoke\_OFF} = Z_{in} + j2\pi f L_{choke} \tag{2.19}$$

In case of transmission line:

$$Z_{TL\_OFF} = Z_0 \frac{Z_{in} + jZ_0 \tan(\frac{2\pi fl}{v})}{Z_0 + jZ_{in} \tan(\frac{2\pi fl}{v})} \quad (2.20)$$

So if both cases are analyzed. For switch on case when $\frac{2\pi fl}{v} \leq 0.5$ it can be approximated to be linear so Z_{TL_ON} becomes:

$$Z_{TL\_ON} = jZ_0 \frac{2\pi fl}{v} \quad (2.21)$$

If $L_{choke} = \frac{Z_0 l}{v}$ then $Z_{TL\_ON} = Z_{Lchoke\_ON}$

Similarly for switch off case again the same assumption is made that $\frac{2\pi fl}{v} \leq 0.5$ so Eq.2.20 becomes

$$Z_{TL\_OFF} = Z_0 \frac{Z_{in} + jZ_0 \frac{2\pi fl}{v}}{Z_0 + jZ_{in} \frac{2\pi fl}{v}} \quad (2.22)$$

If $|Z_{in}| \leq 10 \; and \; Z_0 \geq 50\Omega \; then \; Z_{TL_{OFF}}$ becomes:

$$Z_{TL\_OFF} = Z_0 jZ_0 \frac{2\pi fl}{v} \quad (2.23)$$

So again If $L_{choke} = \frac{Z_0 l}{v}$ then $Z_{TL\_OFF} = Z_{Lchoke\_OFF}$

So from the above analysis it was deduced in [30] that when $L_{choke} = \frac{Z_0 l}{v}$ then the choke inductor can be replaced by a transmission line whose length is long enough to be equal to a large inductor and short enough so that this approximation is valid for maximum frequency. As $\frac{2\pi fl}{v} approched \; to \; \frac{\lambda}{2}$ or at certain nth harmonic our transmission line will act as short circuit regardless of its length. So while designing the transmission line it is very essential to choose the frequency f such that f is much higher than f_0 so that accurate results can be obtained.

2.2.2. Load Network of Class-E Amplifier

The transmit coil acts as the load network of modified class-E amplifier. There are quite a few expected benefits that are expected to be achieved by this.

1. The transmit coil is used both for tuning of amplifier and as the load network for applying the RF power to the body or phantom.
2. If the hardware is considered, being an on coil amplifier, there is no need for 50 matching circuit. This will simplify the design and reduce complexity.
3. There will be no need for long transmission cables carrying RF power from amplifier to the transmit coils so transmission line losses are avoided.

When designing the amplifier the equations and conditions mentioned in [32] are also taken into consideration.

$$P_{out} = \frac{V_{dc1}^2}{1.74R} \tag{2.24}$$

Where V_{dc1} is the modulated supply voltage at the drain of the MOSFET as shown in Fig. 2.7. The relation for maximum drain to source voltage in case of Class-E amplifier is

$$V_{ds\_max} = 3.56V_{dc1} \tag{2.25}$$

So as it can be seen from Eq.2.24 that output power is directly proportional to V_{dc1} and so is V_{ds_max}. Now if the output power is to be increased, there is a limit to increase it without burning the MOSFET. So MOSFET with high limiting V_{ds} is needed for our purpose. This is a well-known problem in designing Class-E amplifier and there are several studies to reduce the peak V_{ds} for Class-E amplifier [33] [34] [35].

Also it can be seen from Eq.2.13 that efficiency is inversely proportional to R_{ds_on}. So from that formula it can be deduced that there is a lower limit for the load resistor value. The resistor value cannot be less than or comparable to R_{ds_on} to have high efficiency. So a transistor is required that has low R_{ds_on} and high V_{ds}. In MRI the RF amplifiers have peak output power of approximately 10 KW that is delivered to the body coil. It is aimed to design a 32 channel transmit array with on-coil amplifiers. So if each amplifier can deliver 300 W output power then as a unit the 32 channel transmit array will be able to deliver approximately 10 KW output power. So a 300 W LDMOS RF power transistor (Ampleon, BLF573, Nijmegen, The Netherlands) is chosen. BLF 573 has R_{dsON}=0.09 Ω and V_{ds_max} =110V. So due to its low R_{ds_ON} and high limiting V_{ds} it is a best choice for us. At 300 W output power V_{dd} = 32 V. The modulated voltage from supply modulation block is V_{dc1}≈ 30V so calculated V_{ds_max} = 106 V and calculated efficiency from Eq. 2.13 is 92.5%.

A transmit array system for 1.5 T is needed in our lab so we decided to work with 64 MHz. The inductance of the transmit coil forms the resonant inductor L_0. The coil is tuned at 64 MHz by 3 distributed capacitors connected in series. The capacitor C_{sh} is chosen such that ZVS and ZDVS conditions are satisfied also the nonlinear behavior of the drain to source capacitor of transistor is minimized. Load pull analysis was done in ADS to find the nest tuning point to get maximum efficiency at 300 W output power.

2.2.3. Driver

To drive the LDMOS transistor BLF 573, a 3 stage wideband digitally controlled driver explained in [30] is designed. The input to the driver is sent from KCU105 FPGA evaluation board (Xilinx Inc., California, USA) as low voltage differential signals. LVDS signaling has better noise performance as compared to single ended signals.

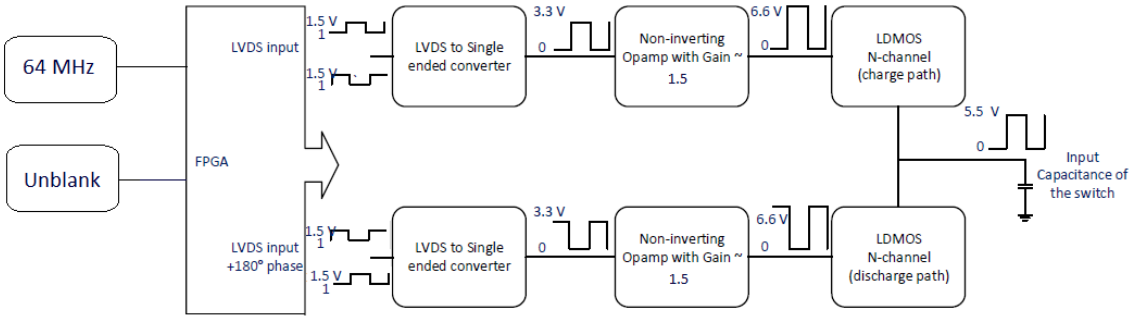


Fig. 2. 6: Driver Design

The Inputs of FPGA are 64 MHz signal and unblank signal from signal generator. FPGA converts the 64 MHz signal into two identical LVDS signals with 180^o phase shift to control the high and low side of the driver. At first stage, these LVDS signals are converted into single ended signals which then input into the noninverting amplifiers with approximately 1.5 gain to drive the MOSFETs in the third stage which in turn drive the main transistor by charging and discharging its input capacitance. During the design of driver it was taken care of that the MOSFETs in the 3^{rd} stage of driver do not turn on at the same time to save

losses in the MOSFETs. So a dead time is added and the duty cycle of the LVDS signals sent from the FPGA were adjusted to resolve this issue.

2.2.4. Supply Modulation

The output pulse of the amplifier needed to have some specific shape like sinc, gauss, triangular etc. So there is a need to add envelope modulation to the pulse.so the following form can be achieved.

$$f(t) = A(t)\sin(2\pi f_0 t + \theta) \tag{2.26}$$

Where:

A(t)= desired envelop modulation

f_0 = Carrier frequency (64 MHz in our case)

θ = Phase of the modulated pulse

As the amplifier is fully digitally controlled so both envelop and phase are controlled by FPGA. For the envelope modulation purpose supply modulation is preferred. There is a linear relationship between supply voltage and output voltage in ideal case. But practically there are some losses and non-linearity due to the switch used for supply modulation purpose. To correct the waveform, feedback circuitry can be used. Our design proposed in [30], a half bridge converter is similar to buck converter [21] but two switches followed by a low pass filter were used. While designing the supply modulation block it was taken care of that switching frequency is higher as compared to the bandwidth of the desired modulated pulse and the delay due to low pass filter is kept to minimum. So the switching frequency of 1 MHz was used. In half bridge topology,

$$V_0 = V_{dd} \times D \tag{2.27}$$

Where D is the duty cycle. MATLAB was used to calculate D for various pulse shapes that were intended to achieve. In FPGA 5ns step size was used so the output range of half bridge circuit is in the range of 5% to 95% of Vdd with 0.005Vdd resolution. The bitstream of the desired pulse shape is generated on PC via MATLAB, which then loaded into FPGA

that controls the PWM of half bridge circuit. The supply modulation block design is shown in Fig. 2.7

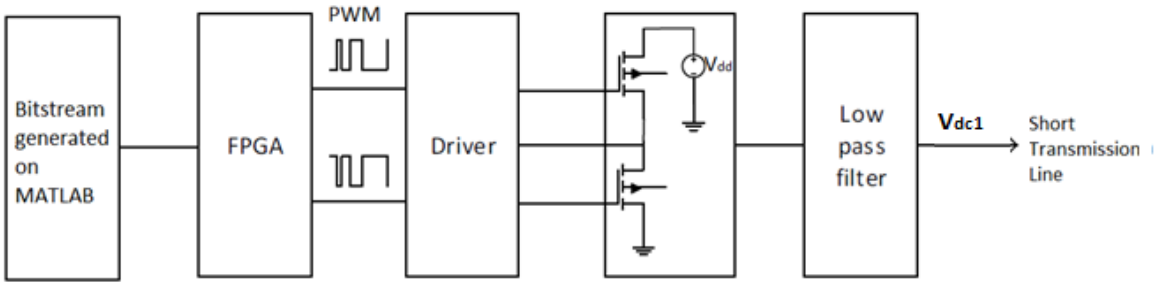


Fig. 2. 7: Supply modulation design

CHAPTER 3

METHODS

In this chapter the methods used for designing and modifying the class-E amplifier are explained. The changes that are made in driver and supply modulation blocks are discussed. The load pull analysis for designing the load circuitry of class-E amplifier is described. The experimental and measurement setup is also explained in detail. The techniques used for the measurement of power, efficiency, coupling and temperature are shown. In the end the experimental setup developed for MRI experiments are discussed in detail.

3.1. Driver Implementation

The amplifier is driven by a 3-stage wideband digital driver which is controlled by a KCU105 FPGA evaluation board (Xilinx Inc., California, USA). As input to FPGA a 64MHz signal and trigger signal from signal generator are used. The amplifier signals are then given by the FPGA by the Low-Voltage Differential Signaling (LVDS) though a CAT7 cable (a common Ethernet cable). An external 8 V is given by power supply which is then converted to 3.3 V and -3.3 V by LF33ABDT and MAX1861 to give as input to other components in the PCB. The LVDS signals from FPGA are converted into single ended signals at the first stage of driver circuit by DS90LT012A. These single ended signals make

the input of current feedback amplifiers THS3202 with proper gain to drive the 300 W LDMOS RF power transistor (Ampleon, BLF573, Nijmegen, The Netherlands) in the second stage of driver circuit. In the third stage MRF1513 MOSFETS are used to provide the adequate current to charge and discharge the gate capacitance of main MOSFET.

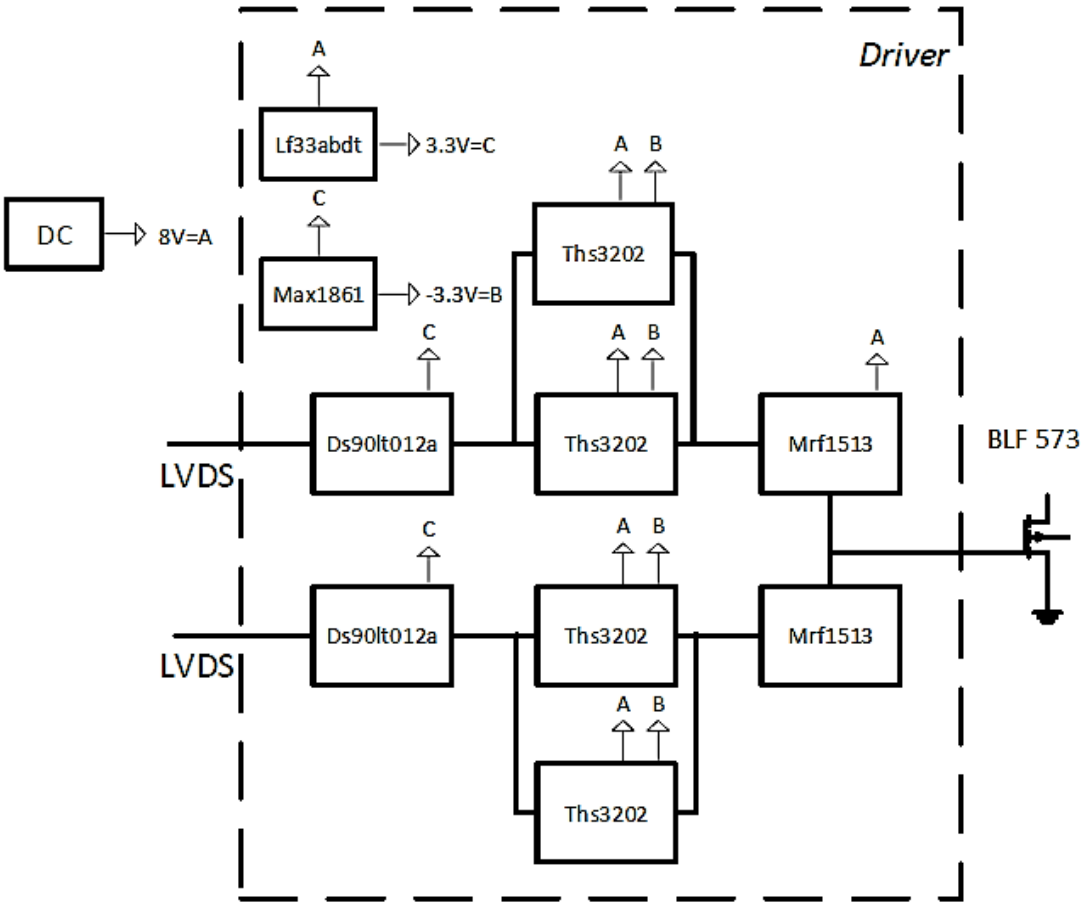


Fig. 3. 1: Driver circuit and the components used in driver

The earlier proposed driver circuit was able to drive a 100 W LDMOS RF power transistor (Ampleon, BLF871, Nijmegen, The Netherlands). The task at hand was to modify the circuit such that it is able to drive 300 W LDMOS RF power transistor (BLF 573). As it was desired to work with 1.5 T (64 MHz). Even at 64 MHz it was hard to drive this MOSFET because the characteristic parameters of both MOSFETS were very different as can be seen from Table.3.1.

Characteristic Parameters	*BLF 871*	*BLF 573*
Output Power (W)	100	300
Drain-Source On Resistance $R_{DS(on)}$ (mΩ)	210	90
Feedback Capacitance C_{rs} (pF)	1	2.3
Input Capacitance C_{iss} (pF)	95	300
Output Capacitance C_{oss} (pF)	30	103
Maximum V_{ds} (V)	89	110
Threshold Voltage V_{th} (V)	2	2

Table 3. 1: Comparison of characteristic parameters of BLF 871 and BLF 573

The rise time, fall time and amplitude of the driver output should be adjusted such that it can drive the input capacitance of 300 pF. ADS 2016 (Keysight, Santa Rosa, CA) was used for simulations. It was observed that if the rise and fall time is between 1.5 ns to 2 ns and the pulse amplitude is between 3V to 4.5V, the maximum efficiency was achieved in simulations with the MOSFET model of BLF571 provided by ADS for simulations. The circuit diagram for ADS simulations is shown in Fig. 3.2. The gain of the feedback current

amplifiers (THS3202) in the second stage of driver was changed to achieve the desired pulse of 3.5V and approximately 1.8 ns rise and fall time

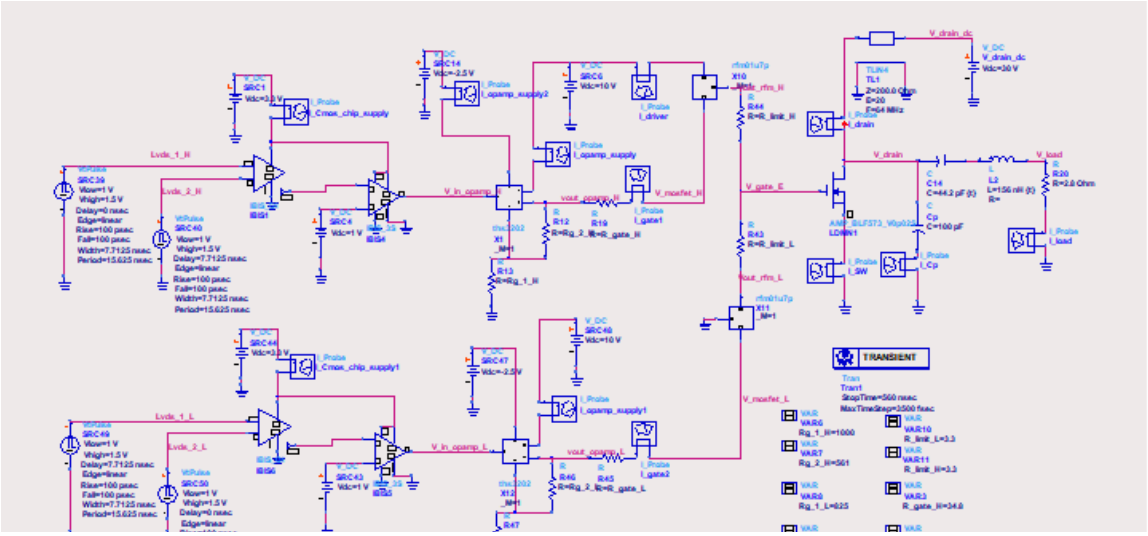


Fig. 3. 2: Driver circuit for ADS simulations

3.2. Supply Modulation Implementation

Specific pulse shapes of milliseconds duration are required to excite the slice in MRI. To achieve the specific pulse shape like rectangular, sinc, gauss etc. supply modulation technique was used. The half bridge topology was used to implement supply modulation block. Supply modulation block also consists of three stages. A bit file generated by MATLAB of specific pulse shape is loaded into FPGA. The code for FPGA is written in Vivado (Xilinx, Inc. San Jose, CA). This bitstream generated by FPGA is then transferred to supply modulation block by Low-Voltage Differential Signaling (LVDS) at 1 MHz. LVDS signals are converted into single ended signals at first stage by DS90LT012A. In the second stage MIC4104 is used to drive the half bridge MOSFETS. In the third stage IRFH7194PBF MOSFETS are used as half bridge MOSFETS to obtain the desired pulse shape. This supply modulation block is followed by an LC low pass filter, which is made of 1 mH inductor and 10 pF capacitor to reduce the ripple content from our modulated signal. The output of

this filter is fed into the drain of our main MOSFET BLF573 with a high impedance transmission line acting as choke inductor. The transmission line is used as choke inductor to make our amplifier amiable to MRI environment. The supply modulation block and the components used in it are shown in the Fig. 3.3.

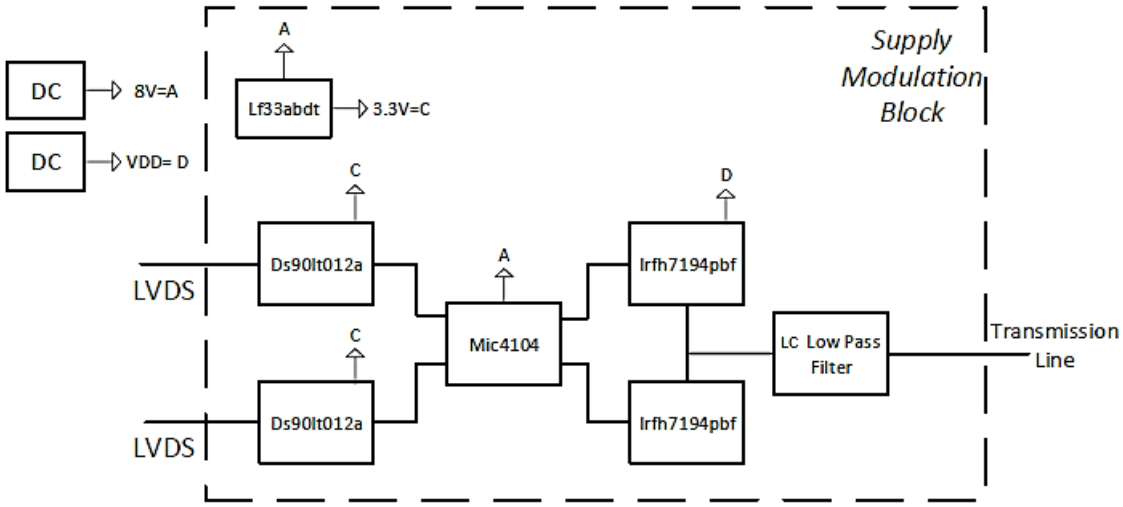


Fig. 3. 3: Supply modulation block and the components used in it

The supply modulation block was introduced in the previous work but it had following problems.

1. The output of supply modulation block was getting distorted at high voltages.
2. It was pulling very high and unstable current.
3. The ripple content was very high.

The solution of these problems was investigated and it was concluded that the dead time of the MOSFETs used in third stage is not proper and the previously used π-filter was the not working efficiently. So the dead time of the MOSFETs was adjusted and π-filter was replaced with newly designed LC low pass filter and all of these three problems were solved.

3.3. Load Pull Analysis

The block diagram of our PCB is shown in Fig.3.4.

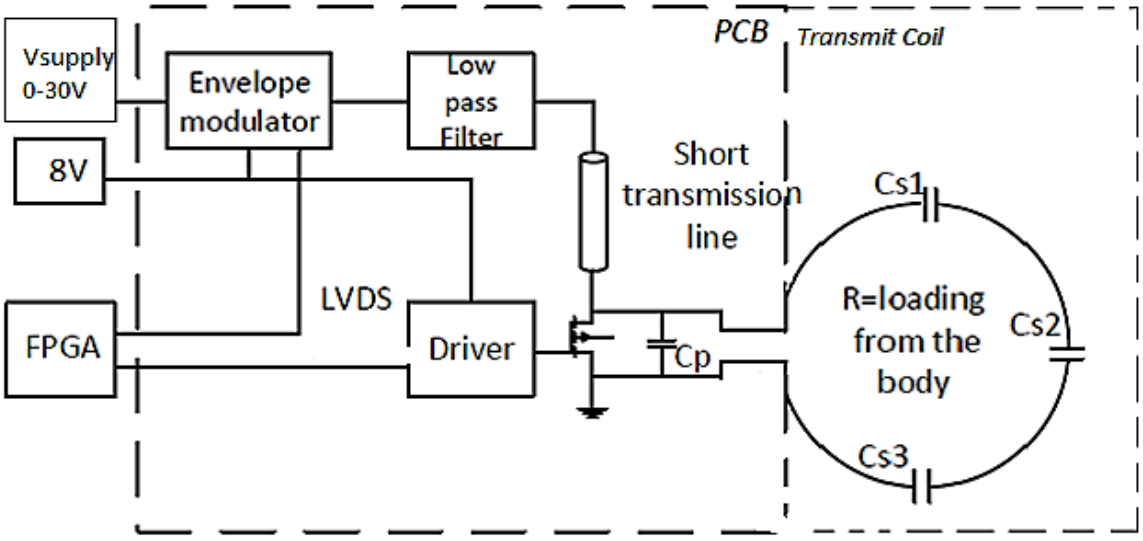


Fig. 3. 4: Block diagram of complete PCB and load network

The most important part of designing the amplifier is designing the load network of amplifier. For locating the optimum output load impedance load pull analysis is performed in ADS 2016 (Keysight, Santa Rosa, CA). The amplifier is simulated with a constant available source voltage while the load reflection coefficient is swept to find the best tuning point so that the amplifier can deliver 300 W power with maximum efficiency. It was observed that at when impedance is approximately 1.2-j0.9 ohm our amplifier can deliver maximum power with highest possible efficiency. In hardware the load network of amplifier consists of transmission coil and phantom. The tuning of transmit coil is crucial for maximum output power and high efficiency as coil itself is used for matching and tuning network and a separate matching network is not required. So the transmission coil we made has L_0 = 256 nH with Q=70. It was tuned with three distributed tuning capacitors C_{s1}, C_{s2} and C_{s3} at 64 MHz. The value of each tuning capacitor is ~ 70 pF ± 1 pF. The inductance of the coil and the tuning capacitors together acts as LC resonator circuit of class-E amplifier. Load was then added afterwards and the coil was fine-tuned again so

that the impedance is approximately 1.25-j1 ohm in hardware for best results of output power and efficiency. The parallel capacitor C_p was also tuned so that ZVS and ZDVS conditions are satisfied and its value was set to be 60 pF. The output capacitance of BLF 573 varies with $V_{DS.}$ So for our purpose The value of C_p can be between 60 pF to 200 pF. It depends on at what voltage you want to get the maximum efficiency.

3.4. Experimental Setup

The amplifier PCB (dimensions: 100mm*50mm) with transmission coil of 12 cm diameter and 4 distributed capacitors are shown in Fig. 3.5.

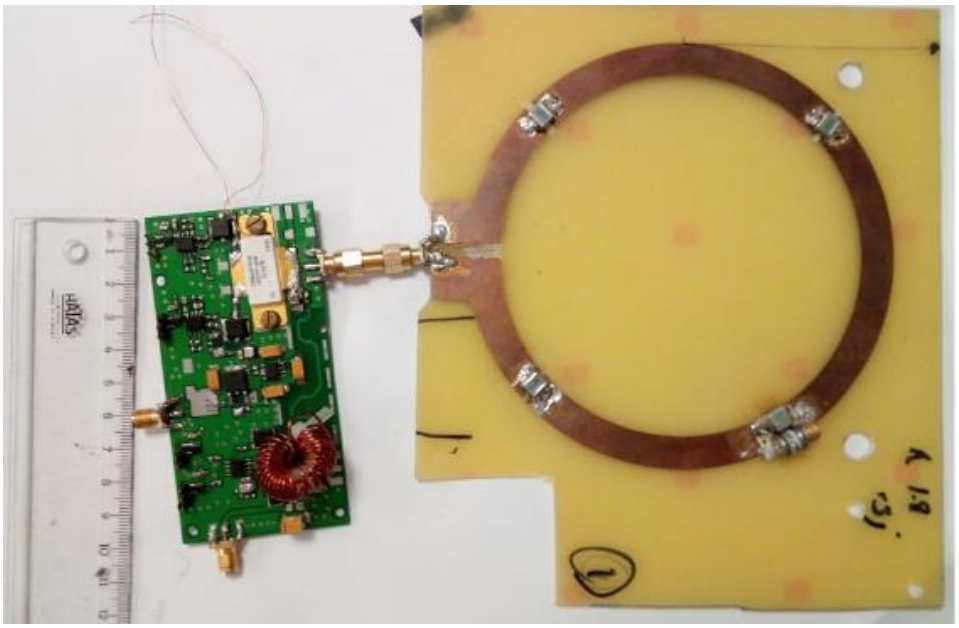


Fig. 3. 5: Class-E amplifier's PCB with transmission coil

For output power and efficiency measurements the experimental setup is shown in Fig. 3.6

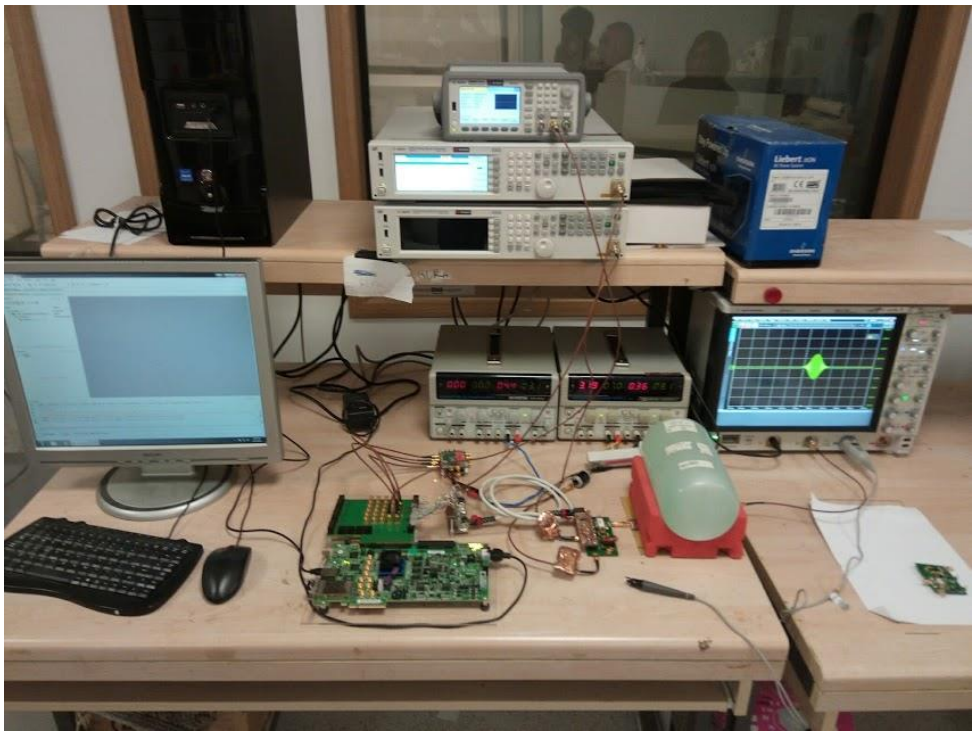


Fig. 3. 6: Measurement setup

3.4.1. Power and Efficiency Measurements

For output power and efficiency measurement we placed our system like it is shown in Fig. 3.7.

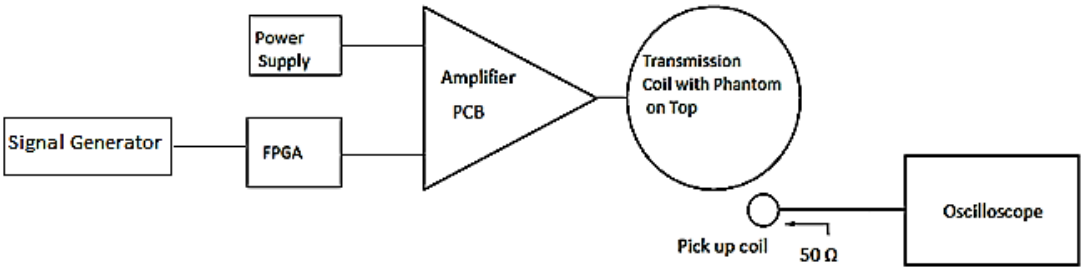


Fig. 3. 7: Measurement setup for power and efficiency calculations

A small pickup coil matched to 50 ohm and tuned to 64 MHz was made and placed near the main coil. The S-parameters were recorded to measure the coupling between the two coils with two different methods. In first method we directly connected the main coil with

port 1 and pickup coil with port 2 and recorded the S-parameters. In second method we used a matching circuit to match our main coil impedance to 50 Ω and again recorded the S-parameters. The power in the pickup coil can be calculated as follows:

$$P_{Pickup} = \frac{V^2_{(rms)pickup}}{R_{pickup}} \quad (3.1)$$

Here $V_{rms(pickup)}$ is the measured voltage from the pickup coil and R_{pickup} is 50 ohm.

If we know the power in the pickup coil then the power in the main coil can be calculated by finding the relation between main coil power and pickup coil power by the following method.

- Connect port 1 of network analyzer to main coil and port 2 to pick up coil.
- Find S11, S21 parameters.
- Calculate the reflected power from mail coil using the following formula

$$P_{reflected} = 10^{s11/10} \quad (3.2)$$

- Calculate the power transmitted from main coil to pick up coil using the following formula

$$P_{transmitted} = 10^{s21/10} \quad (3.3)$$

- Calculate the real S21 of the system α by the following formula.

$$\alpha = \frac{Power\ in\ Large\ Coil}{Power\ in\ small\ coil} = \frac{1 - P_{loss} - P_{reflected}}{P_{transmitted}} \quad (3.4)$$

  Where P_{loss} is the power loss occurring in matching circuit. For method 1 where we are not using matching circuit P_{loss} is zero.

- Finally calculate the power in the main coil by using the following relation.

$$P_{out} = P_{main\_coil} = \alpha\ P_{pickup} \quad (3.5)$$

Once the output power in the main coil is calculated we can calculate the efficiency as follows.

$$P_{in} = V_{supply} \times I_{supply} \quad (3.6)$$

$$\eta_{drain} = \frac{P_{out}}{P_{in}} 100\% \quad (3.7)$$

The efficiency reported may have an error due to an error in the calibration. In method 1, since there is high reflection, the calculation of the amount of delivered power is prone to error. On the other hand, in method 2, additional loss in the matching circuit is should be considered in the calculation. This value was estimated by considering equivalent series resistance of the matching inductor using the skin effect calculations and also quality factor measurement of the inductor as around 30mohm. This results in approximately 3% loss in matching circuit, resulting decrease in the calibration value. This loss has been incorporated while reporting the final efficiency values

3.4.2. Power and Efficiency Measurements in 1 MHz Bandwidth

The amplifier should have a bandwidth of 1 MHz or more so that it could be further used to pre-distort the generated pulse for better slice selection in MRI. To check the performance of amplifier in 1MHz bandwidth the operating frequency was varied in the range of 63.5MHz to 64.5MHz and the efficiency of the amplifier was recorded keeping the output power at 300 W in ADS simulations and as well as in measurements and the results were compared.

3.4.3. Temperature Measurements

As the main power loss occurs in the transistor BLF573, it is critical to monitor that the maximum junction temperature limit (225℃) is never reached. Heating performance of the amplifier was therefore recorded by measuring the case temperature of the transistor with thermistor model MF51E103E3950; duty cycle of the amplifier was varied from 1% to 20% and the temperature rise was recorded for a total duration of 1 minute in each case. A 2ms sinc pulse was used initially with a TR of 200ms and temperature rise was recorded after one minute. The MOSFET was then allowed to cool down to room

temperature. The TR was reduced and the temperature rise was again recorded after 1 minute. The process was repeated until TR was 40ms. The drain efficiency was also recorded for different duty cycles to observe the effect of temperature on the efficiency of amplifier.

At low TR, the temperature increases and the turning point gets shifted a little so the efficiency of amplifier also drops. We attached a small heatsink on the top of BLF 573 with thermal glue as shown in Fig. 3.8 and repeated our experiment to observe the difference.

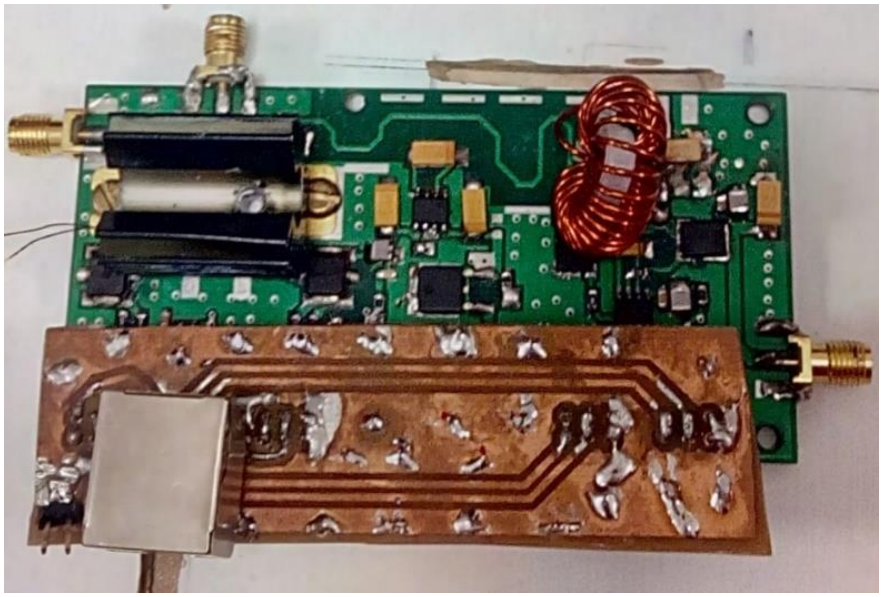


Fig. 3. 8: Small heat sink in on top of BLF 573

3.4.4. Effect of Load Variation on Efficiency

The real part of the load circuit of the amplifier is varied between 0.25 Ω and 3.5 Ω by changing the phantom position. When the phantom is directly on top of the transmit coil the loading from the phantom increases so the real part of Z_{coil} (Fig. 2.3.) increases and when the phantom is moved away from the coil loading decreases hence R decreases. The effect of the variation of real part of the load network on the efficiency and power of amplifier is then measured by keeping the supply voltage constant at 10 V. It is also noted that the change in the position of phantom mostly affects the real part of the load network and its imaginary part remains approximately constant.

This is because the imaginary part of load network is consists of C_0 and L_0 and by changing the position of phantom we are not changing these parameters.

3.4.5. Coupling Measurements and Tuning for Dual Coil

3.4.5.1. Coupling and Tuning in Simulations

Two amplifiers working simultaneously were simulated together in ADS 2016 with the mutual inductance coefficient K ranging from 0.1 to 0.9. We replaced our driver with ideal driver to simplify the design and reduce the simulation time. The ideal driver is a square wave signal generator with amplitude of 3.5V and rise and fall time of 1.5ns same as our designed driver.

The amplifiers were decoupled and tuned at 64 MHz by altering the capacitors in the series resonators of both class-E amplifiers such that maximum efficiency can be achieved at 300 W output power when they are working together. The tuning circuit in ADS is shown in Fig.3.9.

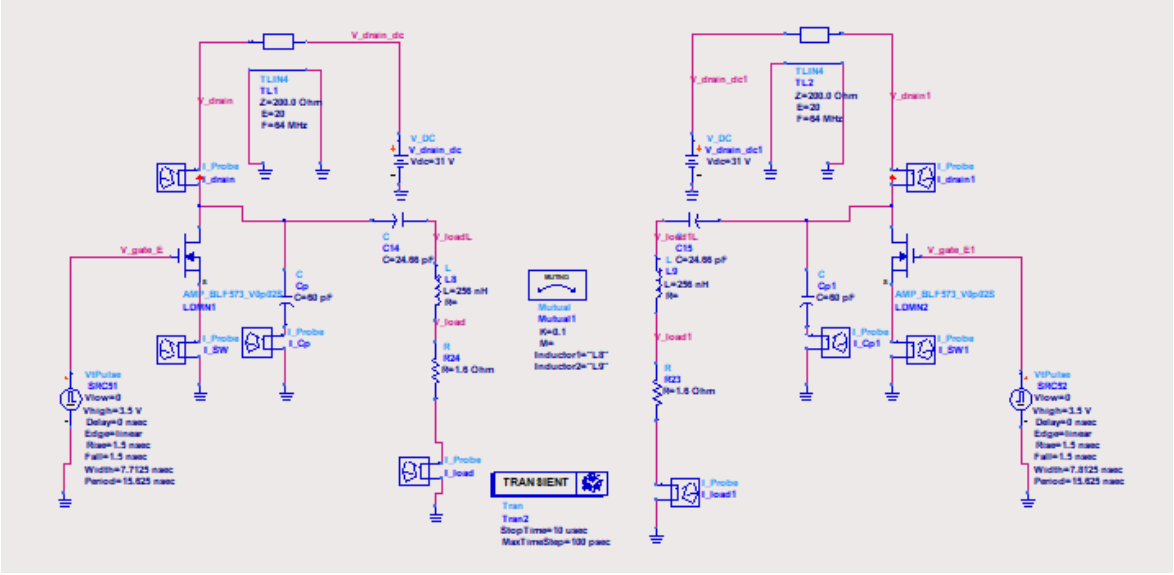


Fig. 3. 9: Coupling and tuning circuit used for simulations in ADS 2016

3.4.5.2. Coupling and Tuning on Hardware

This amplifier is aimed to be used in parallel transmit and the ultimate goal is to make an array of 32 amplifiers working together and not effecting each other performance. It is essential to measure the coupling between the amplifiers and decouple them for better efficiency and performance. ADS simulations were done to see the effect of coupling on the performance of amplifiers. They were decouple by changing the tuning capacitors on the transmit coil. On hardware 2 amplifiers with separately tuned transmit coils at 64 MHz were put together at a distance of 7 cm in between them. For each transmit coil there was a separate 50 ohm matched pickup coil. It was made sure that the pickup coils are far from each other and are completely decoupled from each other. As the two transmit coils put near to each other the inductance changed so the tuning point changed and the performance of the amplifiers was degraded. The output pulse was distorted and the output power and efficiency of the amplifiers was decreased. So the amplifiers were tuned again by changing the tuning capacitors for maximum output power and efficiency. The measurement setup for coupling measurement is shown in Fig. 3.10. Both amplifiers were fed 64 MHz and the output power and efficiency for both of them was measured for same input powers.

Fig. 3. 10: Measurement setup for coupling and tuning

3.5. MRI Experiments

After the satisfactory results of amplifier, MRI experiments were performed on 1.5 T (Scimedix Inc., Incheon, South Korea) to analyze the performance of amplifier inside the scanner. First experiment was performed with single amplifier. The amplifier was placed inside the bore with transmit coil on top of the receiving head coil as shown in Fig. 3.11a. As for receiving, the Scimedix 8-channel head coil was used. The FOV for this experiment was 250 mm. A 1900 ml standard Siemens plastic phantom was used as load. The second experiment was performed to check the coupling with two amplifiers and two 1900 ml standard Siemens were placed on top of transmit coils as shown in Fig. 3.11b. The FOV for this experiment was 400 mm. For reception, the body coil was used. In experiments, FPGA (Xilinx Inc., KCU105, California, USA) and power supplies were placed in the systems' room of 1.5T as shown in Fig. 3.11c. FPGA was given 63.8MHz (the central frequency of Scimedix 1.5 T) and unblank signal from the scanner. The amplifier signals were given by FPGA by LVDS signaling though a CAT7 Ethernet cable. For both experiments gradient

echo sequence was used for imaging with 5 mm slice thickness and a 2ms sinc pulse was used for excitation with TE/TR=15/200 ms.

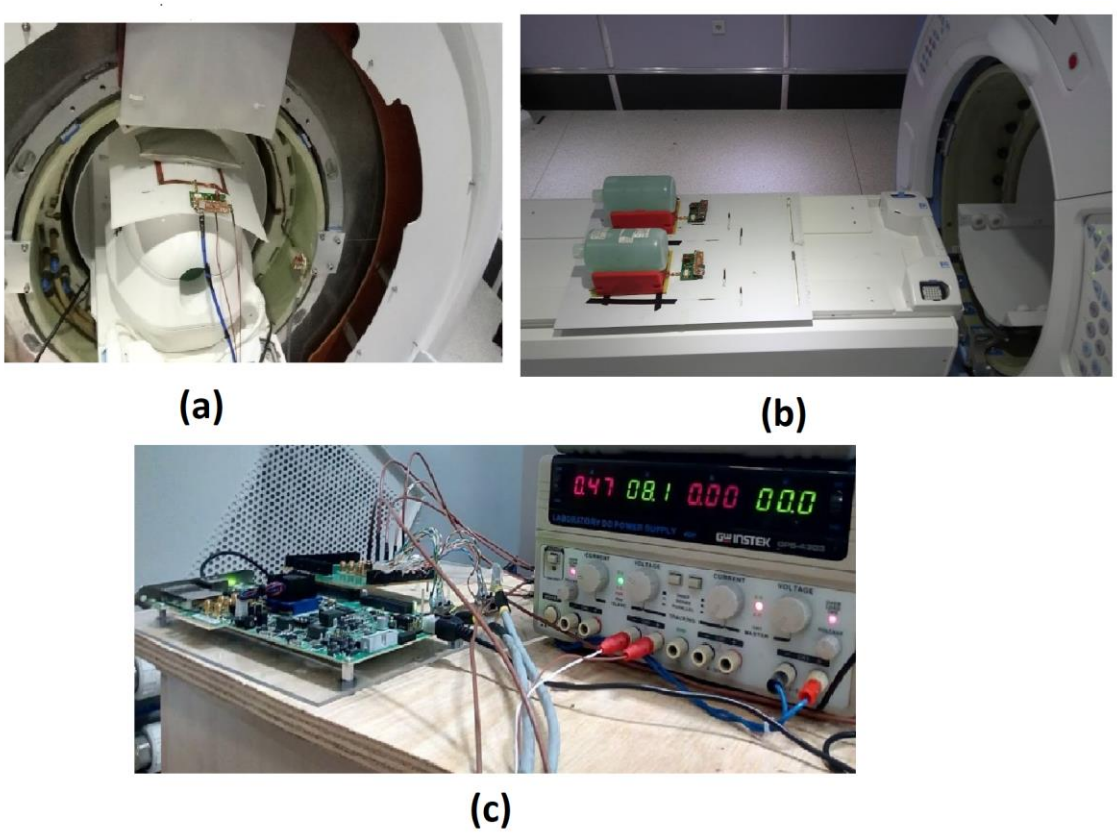


Fig. 3. 11: (a) Single amplifier and transmit coil on top of Scimedix 8-channel receiver head coil inside the bore (b) Two amplifiers with transmit coils and phantoms on top of transmit coils inside the bore (c) FPGA evaluation board and power supplies in systems

CHAPTER 4

RESULTS

In this chapter the simulation and measurement results are discussed. The simulation results of modified driver are presented. Load pull analysis results are shown. The power delivered, drain efficiency and constant current contours are plotted to see the behavior of amplifier at different load impedances. The measurement and simulation results of efficiency and power calculation after implementing supply modulation block are presented and compared. Next, the performance of amplifier at high temperature and in 1 MHz bandwidth was discussed. The behavior of the class-E amplifiers under coupled operations is being investigated. The initial results show that the effect is tolerable. Finally MR experiments were performed with single transmit channel and with dual transmit channels to record the behavior and performance of amplifier inside the scanner.

4.1. Driver

4.1.1. Driver Simulation Results

The model for transistor BLF 573 was provided by Ampleon for ADS 2016. After exporting that model in our design, simulations for the driver were done in ADS 2016. It was observed that when the gate voltage is 3.0 V- 4.5 V maximum efficiency can be achieved. To make sure that the amplifier deliver 300 W power tuning of the load circuit is required.

After tuning the load circuit amplifier can deliver 300 W power with 93% efficiency in simulations. The simulated results of output of driver (gate signal of BLF 573), the drain to source voltage signal, Output current and voltage and its FFT and the power and efficiency calculations done in ADS 2016 are shown in Fig. 4.1. During driver and amplifier design it was made sure that the Vds is always lower than maximum limiting Vds (110 V) of BLF 573 and the conditions of ZVS and ZDVS are always satisfied to achieve the best results.

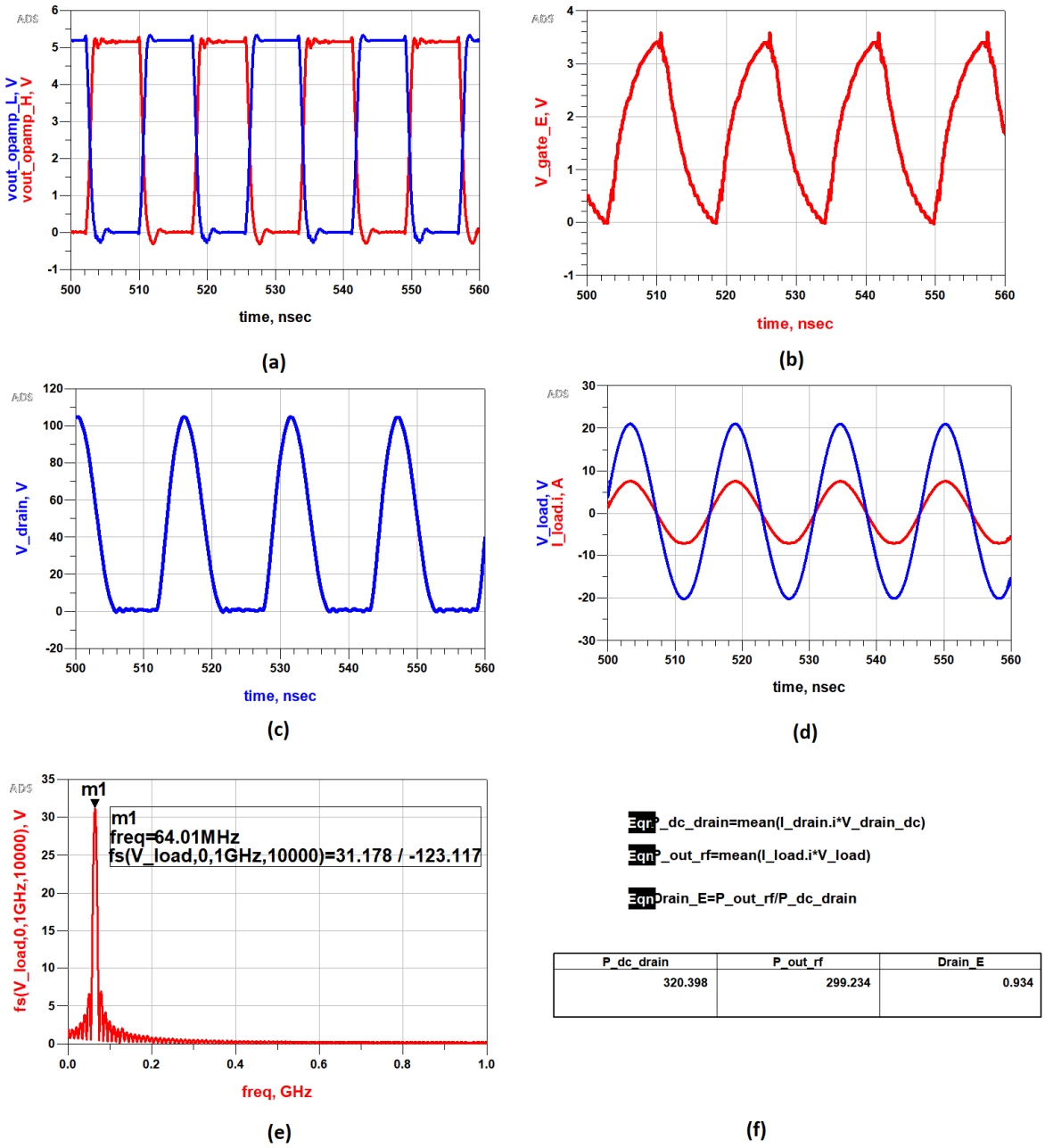


Fig. 4. 1: (a) The Signals in the driver high and low side at the input of the op-amps in the third stage of driver (b) output of driver (gate signal of BLF 573) (c) Drain to source voltage of BLF 573 (d) Load current and load voltage (e) FFT of load voltage (f) Calculations for drain efficiency

4.1.2. Driver Measurement Results

After the encouraging simulation results the driver was implemented on hardware. The hardware results are in coherence with the simulation results. The rise and fall time for the output of driver circuit is approximately 1.8 ns. In Fig. 4.2 the LVDS signals from FPGA, the gate signal (output of driver) of BLF 573 and the drain to source voltage is shown. The conditions ZVS and ZDVS conditions are satisfied through proper tuning of load circuit.

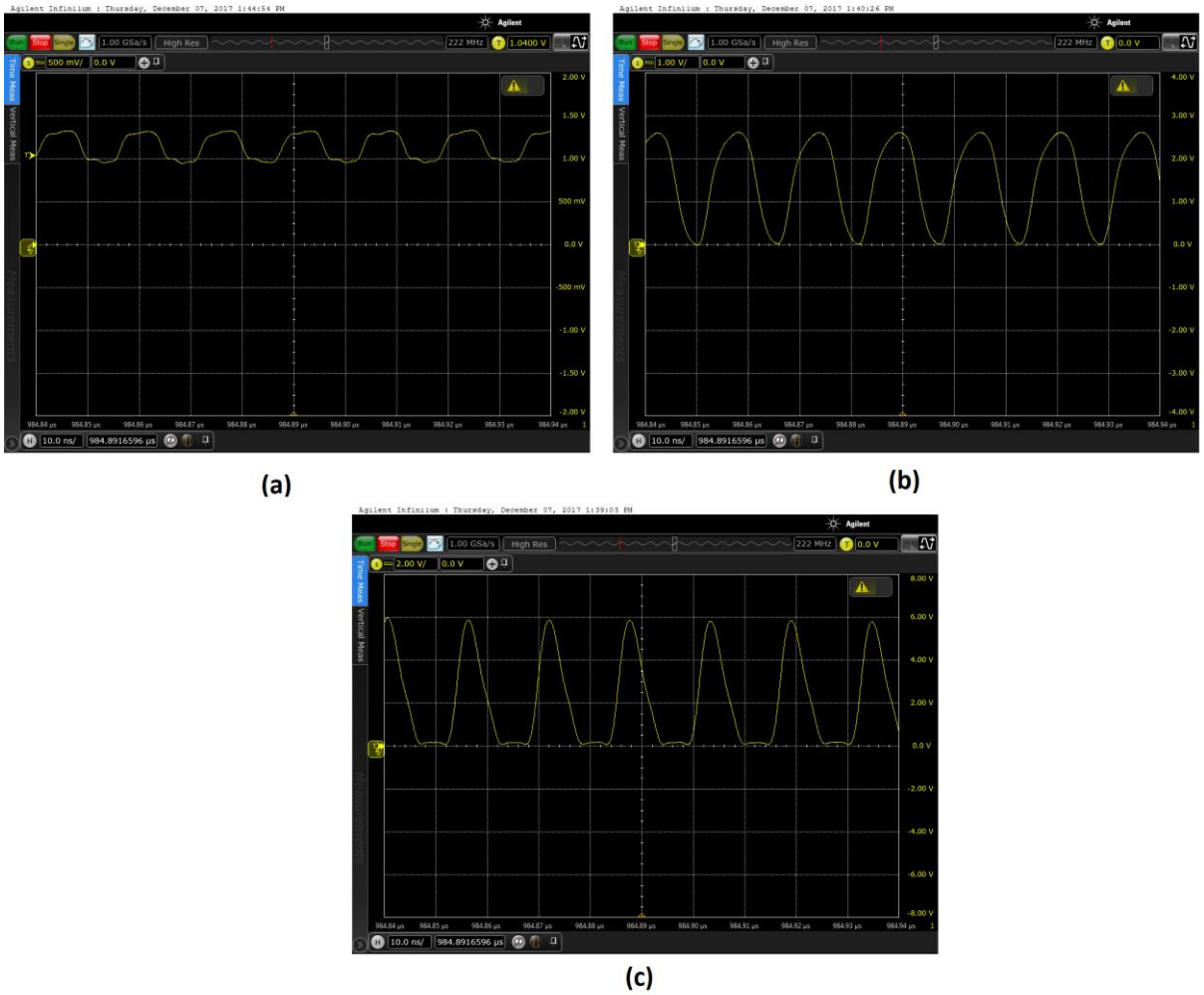
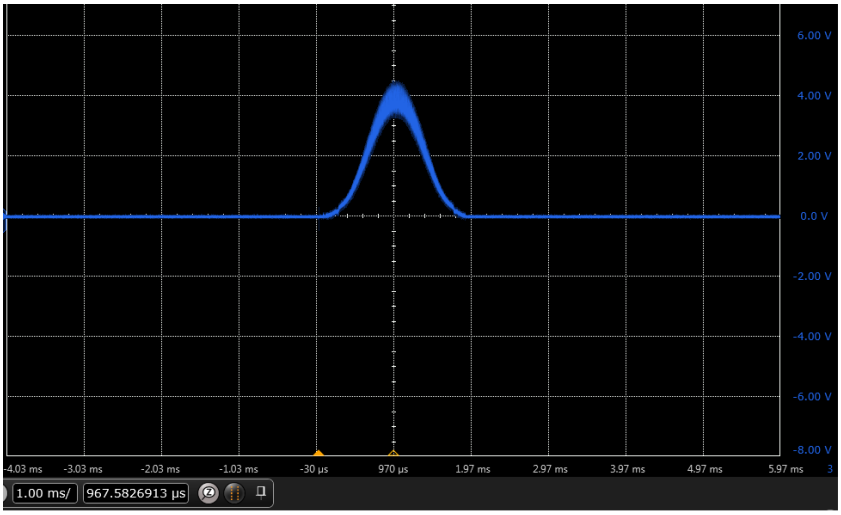


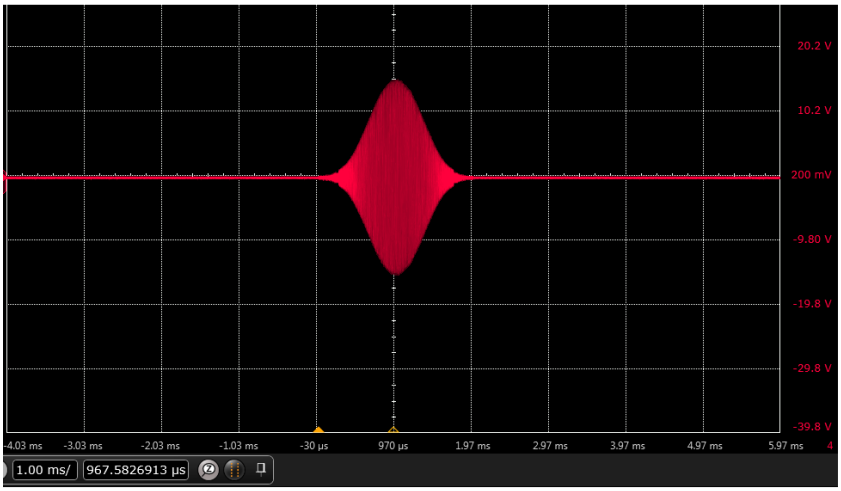
Fig. 4. 2: (a) LVDS signals from FPGA (b) Output of driver (gate signal of BLF 573) (c) Drain to source voltage of BLF 573

4.2. Supply Modulation Results

The supply modulation block was implemented with the half bridge topology followed by an LC low pass filter. Any desired pulse shape of desired time duration can be generated in MATLAB. This generated pulse shape is then converted into a bit stream of 1s and 0s. It is then loaded into FPGA which send it to the supply modulation block via LVDS signaling at 1 MHz. The output of the supply modulation blocked when a 2 ms sinc pulse was generated is shown in Fig 4.3 (a). The modulated output sinc pulse of the amplifier and respective drain current profile for BLF 573 is also shown [Fig. 4.3 (b-c)].



(a)



(b)

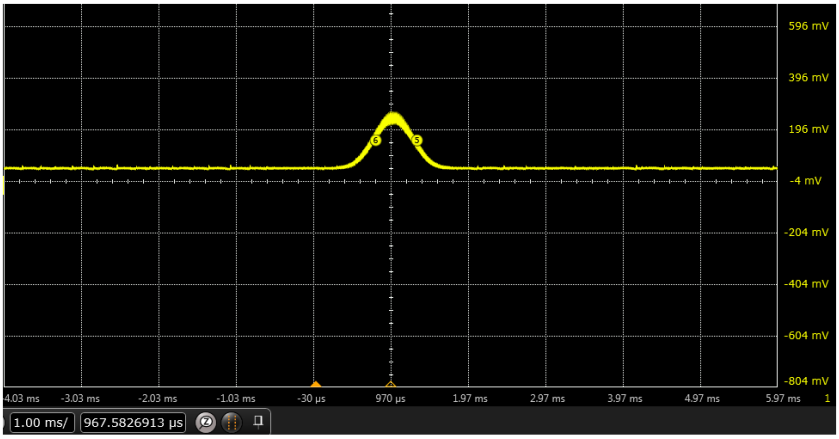


Fig. 4. 3: (a) The output of the supply modulation blocked when a 2 ms sinc pulse was generated (b) The modulated output sinc pulse of amplifier (c) The supply current profile.

4.3. Load Pull Analysis Results

From the simulation results of load pull analysis, drain efficiency and power delivered at different load impedances were calculated. It was observed that when the transmit coil impedance is 1.2-0.89j ohm, drain efficiency is 92% and output power is 54.8 dBm (302 W). The drain efficiency contours, power delivered contours and supply current contours are shown in Fig. 4.4. Drain efficiency contours (red) with decreasing efficiencies from inner-most to outer-most contours, with 99% and 75% drain efficiencies in the inner-most and outer-most contours respectively. Power delivered contours (blue) with decreasing power levels from inner-most to outer-most contours, with 55 dBm and 50 dBm power delivered in the inner-most and outer-most contours respectively. Supply current contours (pink) with decreasing current from inner-most to outer-most contours, with 5 A and 15 A current in the inner-most and outer-most contours respectively.

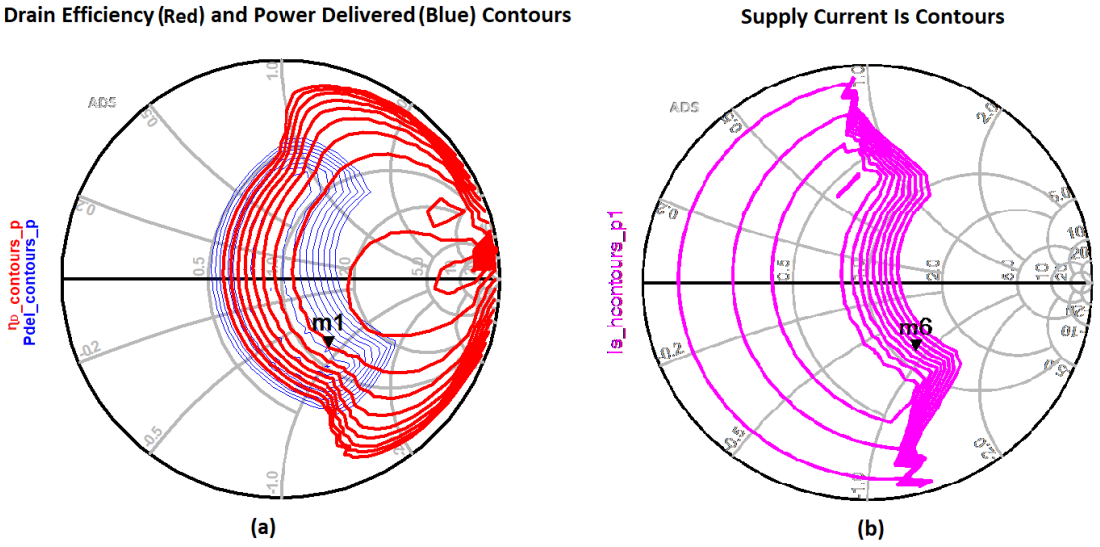


Fig. 4. 4: (a) Drain efficiency contours (red) and Power delivered contours (Blue). Marker m1 shows 1.21-j0.89 Ω load impedance point where 54.8 dBm (302 W) power is delivered at 92% efficiency (b) Supply Current Contours. Marker m6 shows 1.21-j0.89 Ω load impedance point where Is = 11.2 A

4.4. Output Power and Efficiency of Amplifier

The calculated efficiency of our amplifier from Eq. 2.13 is 93%. With the inclusion of supply modulation, the maximum drain efficiencies of 95% and 92% were achieved in simulations and in measurements respectively when output power is between 30W-80 W. At 300 W output power the drain efficiency is 93% in simulations and 84% in hardware. In Fig. 4.5a the simulated and measured drain efficiencies vs input power are shown while Fig. 4.5b shows the measured input and output powers of our amplifier. When input power is 360 W an output power of 302 W with 84% efficiency was achieved.

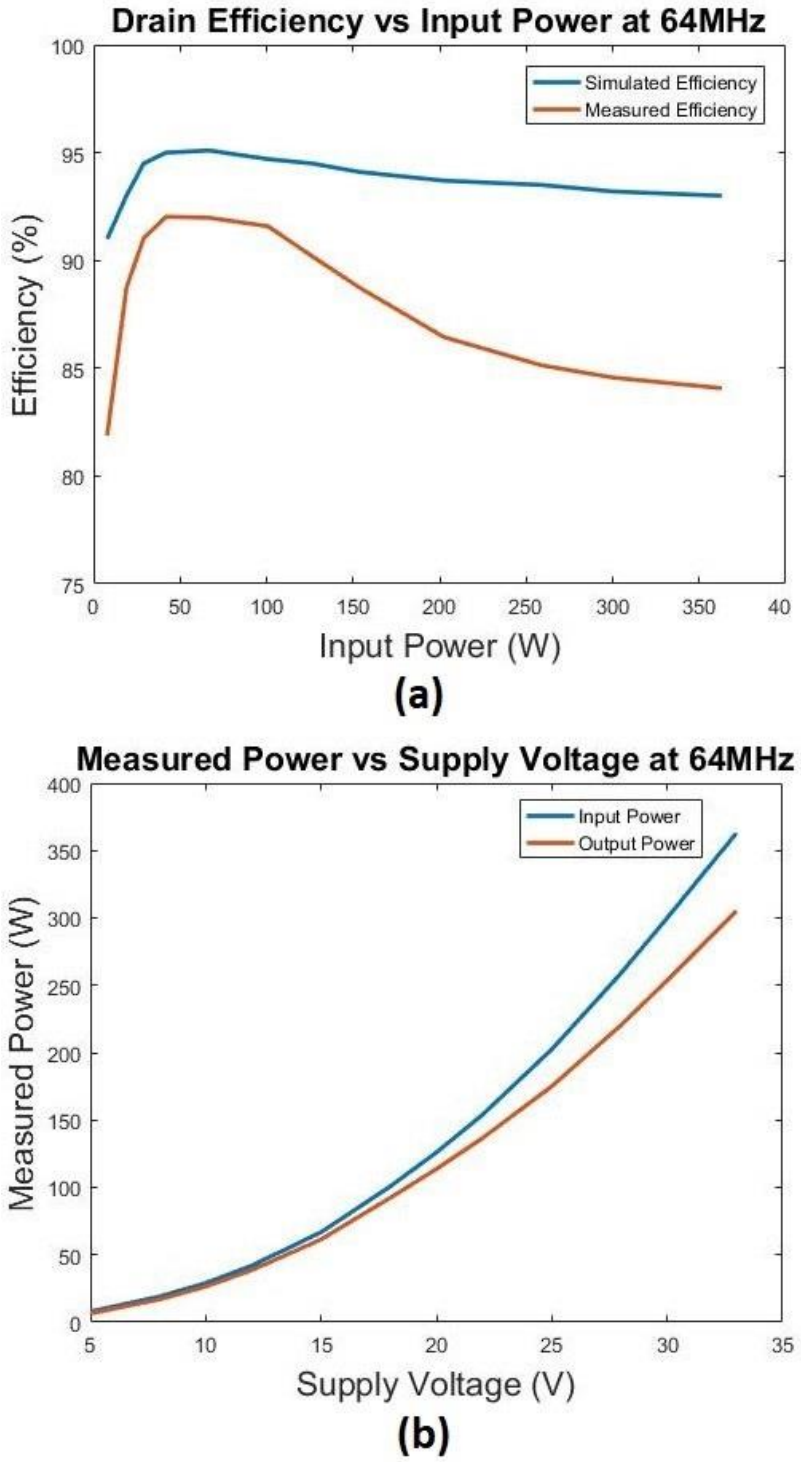


Fig. 4. 5: (a) Simulated and measured drain efficiencies vs input power (b) Measured input and output power vs supply voltage.

4.5. Class-E Amplifier's Performance in 1 MHz Bandwidth

The performance of the amplifier was investigated in 1 MHz bandwidth. The frequency was swept from 63.5 MHz to 64.5 MHz with the step size of 0.1 MHz. The drain efficiency was measured for each case at 300 W output in simulations as well as in hardware. It was observed that the maximum efficiency of 84% was achieved when the frequency was 64 MHz but in 1 MHz bandwidth, the frequency did not drop below 75%. The simulation and hardware results are in coherence with each other as can be seen from Fig. 4.6.

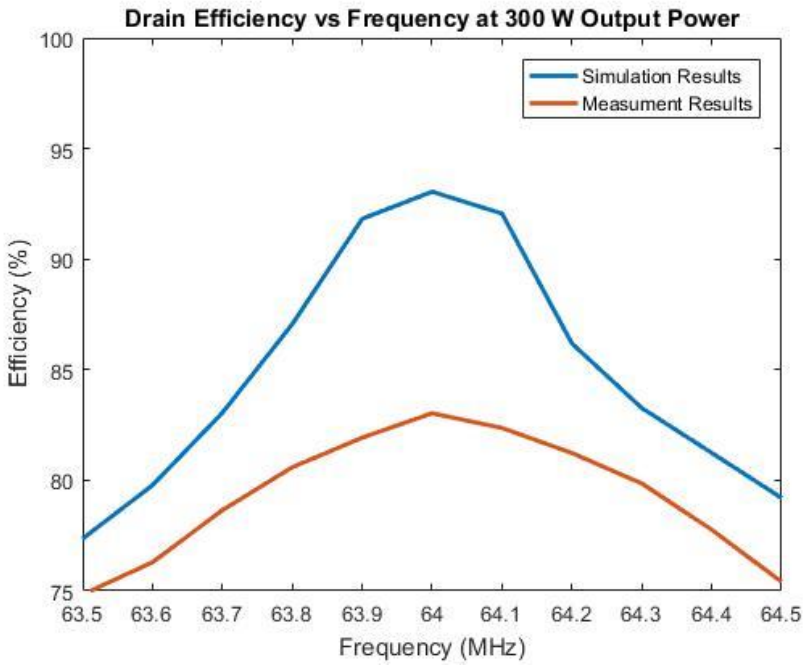
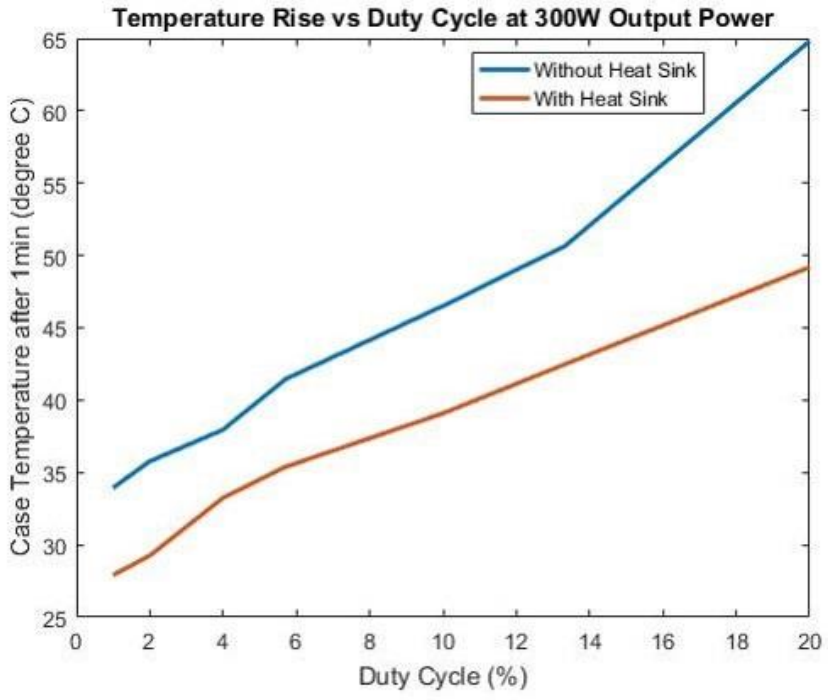


Fig. 4. 6: Simulated and measured drain efficiencies at 300 W output power in 1 MHz bandwidth.

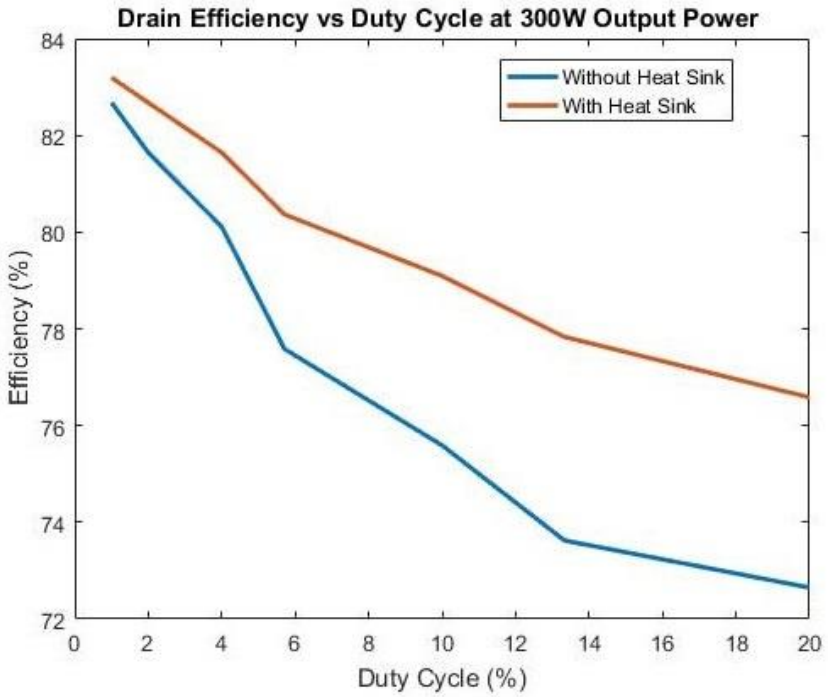
The good performance of amplifier in 1MHz bandwidth indicates that it could further be used to pre-distort the generated pulse in order to have a better slice selection. This is also a promising result for multi slice selection.

4.6. Performance in High Temperature

From our experiments, it was observed that the case-temperature of the transistor did not exceed 65℃ at 300W output power when 20% duty cycle was applied for 1 minute at 64 MHz without any heat sink. With heat sink attached on the top of MOSFET the maximum temperature when 20% duty cycle was applied for 1 minute was reached up to 50℃. The measured drain efficiency was also significantly improved with heat sink and did not drop below 76%. The case temperature of MOSFET vs duty cycle with and without heat sink is shown in Fig. 4.7a and the drain efficiency vs duty cycle is shown in Fig. 4.7b.



(a)



(b)

Fig. 4. 7: (a) Temperature measurements vs duty cycle of amplifier (b) Drain efficiency vs duty cycle of amplifier at 300 W output power.

4.7. Effect of Load Variation on Efficiency Results

It is observed that if the load is varied keeping the supply voltage fixed to 10 V, the input current changed so the input power also varied with the variation of load. When there is no phantom on the transmit coil then R=0.25 ohm and the current pulled from the supply is maximum. As the load is brought near the transmit coil R increases and hence the current pulled from the supply decreases. The effect of load variation is mainly on the input power of amplifier. The efficiency is not affected much as it can be seen from Fig. 4.8

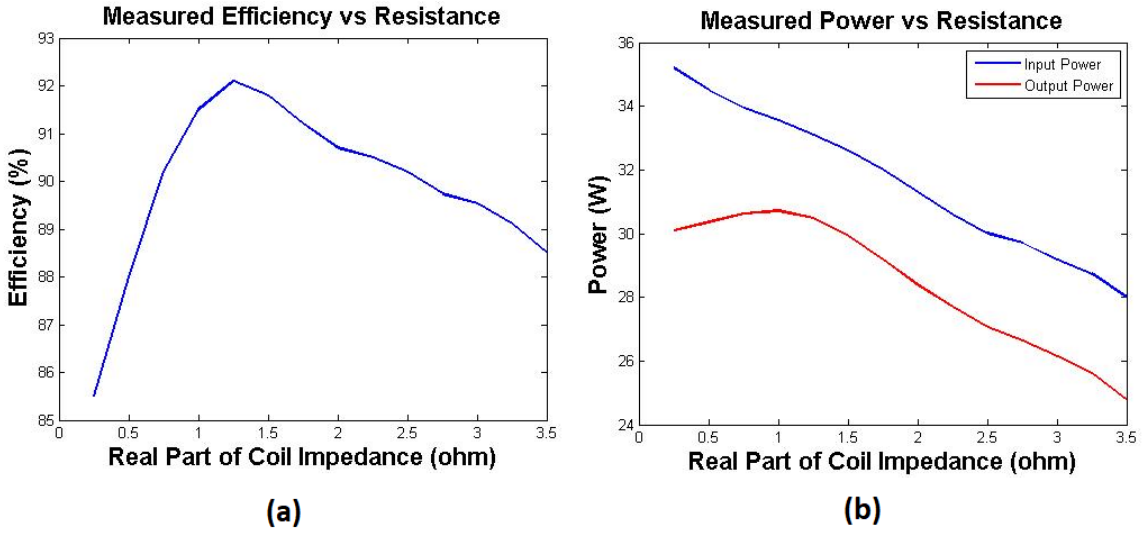


Fig. 4. 8: (a) Efficiency of the amplifier vs load resistance (b) Power vs load resistance

4.8. Dual Coil Amplifier

4.8.1. Coupling and Tuning Simulation Results

It was observed that even for the small values of coupling coefficient like K=0.1 the efficiency dropped to 35% from 93%. This implies that small change in the inductance of coil changed the tuning point of amplifier hence the efficiency dropped significantly. The capacitors in the series resonators of both class-E amplifiers were altered such that both

amplifiers are decoupled and tuned at 64 MHz and maximum efficiency can be achieved when they are working together simultaneously. The results before tuning and after tuning for one amplifier are shown in Fig. 4.9 and Fig. 4.10 respectively. The other amplifier has similar behavior before and after decoupling and tuning as this amplifier.

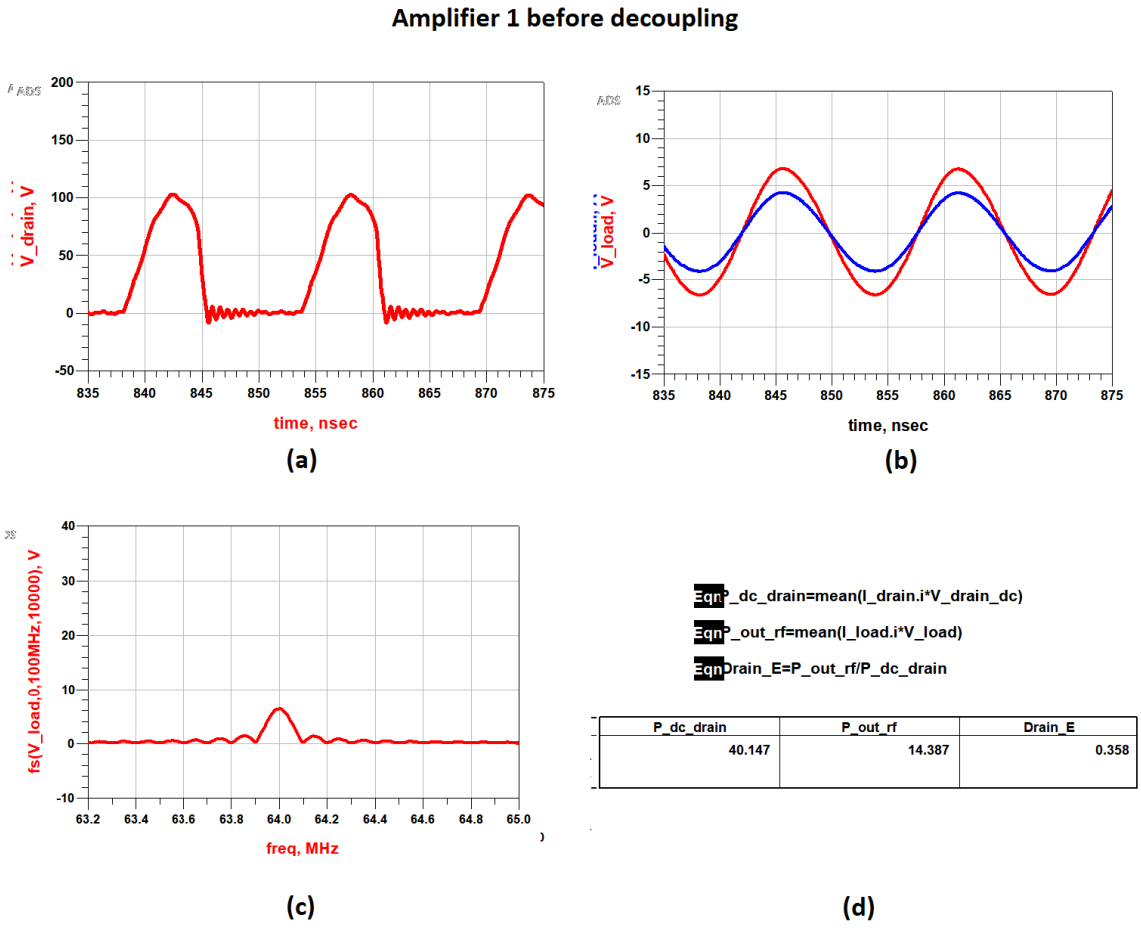


Fig. 4. 9: (a) The drain to source voltage (b) Load voltage and load current (c) The FFT of load voltage (d) Efficiency calculations

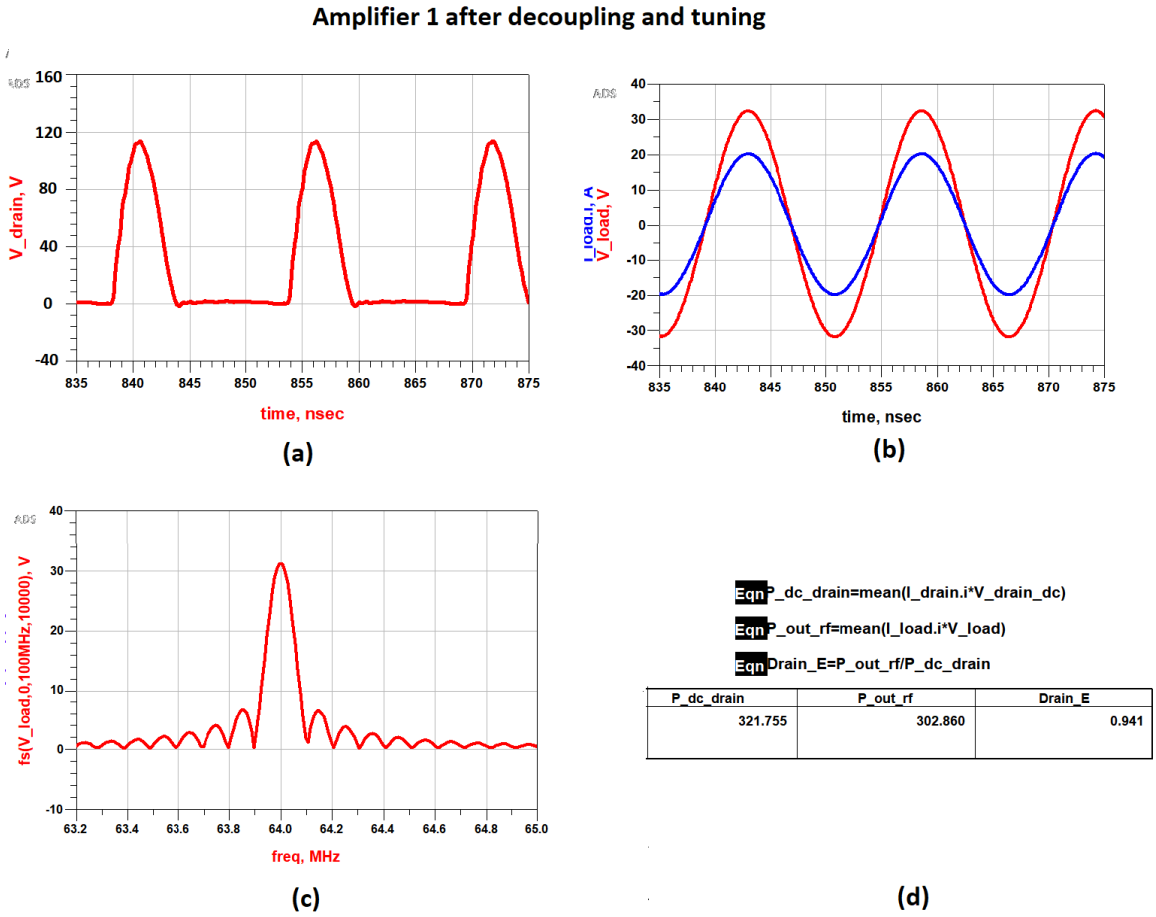


Fig. 4. 10: (a) The drain to source voltage (b) Load voltage and load current (c) The FFT of load voltage (d) Efficiency calculations

4.8.2. Coupling and Tuning Measurement Results

It was observed that the coupling between coils is inversely proportional to the distance between them. When two separately tuned amplifiers were placed together their maximum efficiency dropped to 44% at 7 cm distance. So the tuning capacitors on the transmit coil were altered to decouple and tune them to 64 MHz again at a distance of 7 cm. After decoupling and tuning the efficiency and output power of both amplifiers while working simultaneously at same input phase and frequency were measured. It was observed that amplifiers can work effectively simultaneously and their efficiency and

output power did not degraded in the presence of each other at same frequency and phase. Coupling between the transmit coils is measured to be 8% when 12 cm diameter coils are placed with a distance of 7 cm. The measured efficiency vs input power of both amplifiers after tuning is shown in Fig. 4.10.

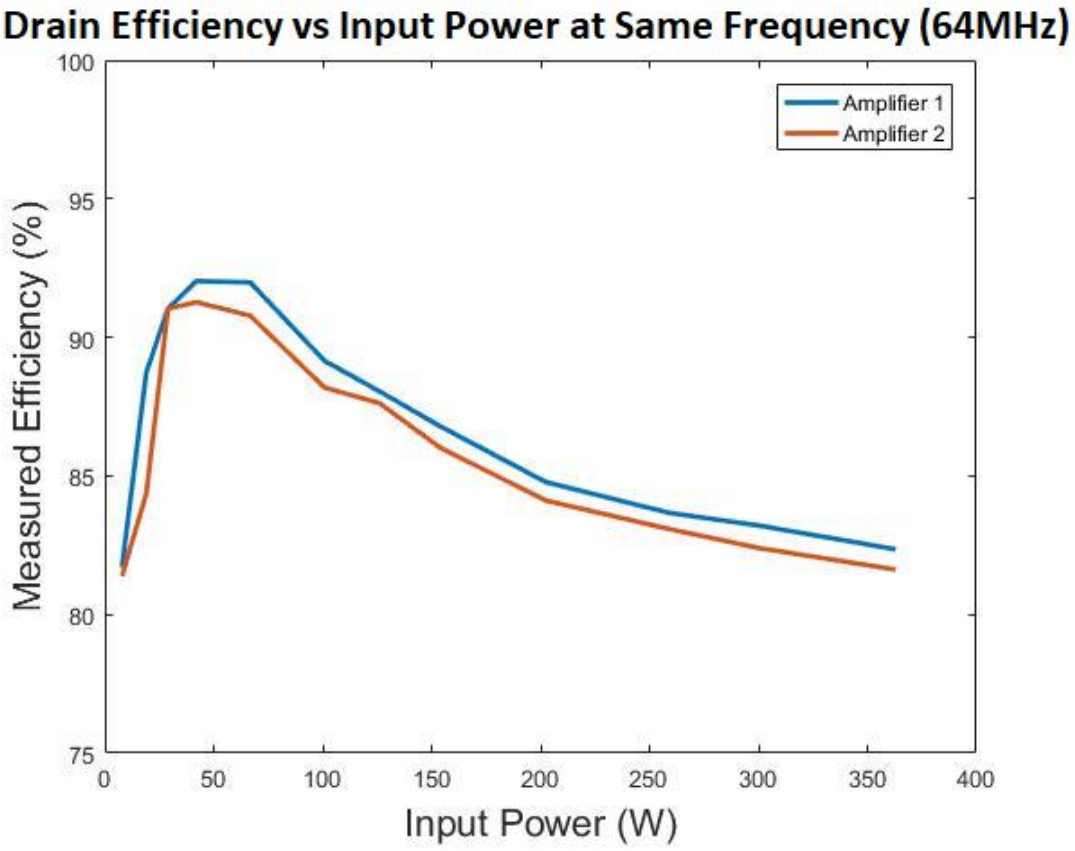


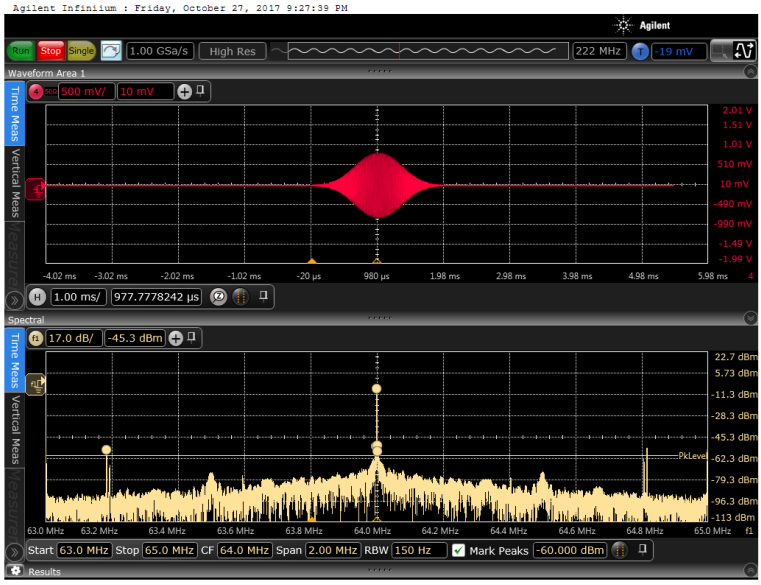
Fig. 4. 11: Measured drain efficiency when both amplifiers are operating at simultaneously at 64 MHz.

Maximum efficiency is observed around 30 W to 80 W output power but the system can operate with efficiency higher than 80 % in most power levels. Coupling between channels has an effect on the efficiency but it is also tolerable.

The behavior of both amplifiers working simultaneously at different frequencies is also observed. The modulated output pulse and its FFT for amplifier1, when both amplifiers

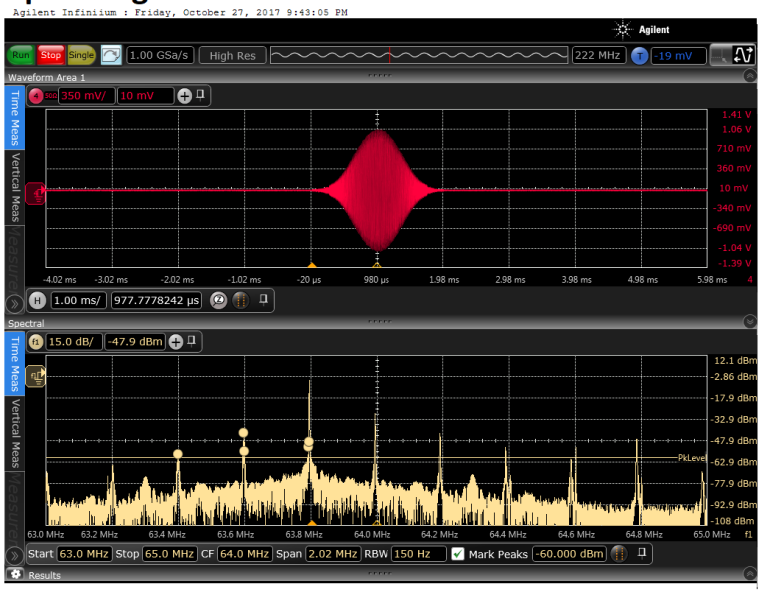
work simultaneously at same frequency and at different frequencies are shown in Fig. 4.11. It was also observed that when both amplifiers are simultaneously working at 64 MHz no harmonics were seen in the FFT of the output pulse in 1 MHz bandwidth, but when one amplifier is working at different frequency harmonics were seen. The behavior of the class-E amplifiers under coupled operations is being investigated. The initial results show that the effect is tolerable.

Both Amplifiers Operating at 64.0 MHz Simultaneously



(a)

Amplifier1 is operating at 64 MHz and Amplifier2 is operating at 63.8 MHz



(b)

Fig. 4. 12: (a)The modulated output pulse and its FFT for amplifier1 when both amplifiers are operating simultaneously at 64.0 MHz. (b) The modulated output pulse and its FFT for amplifier1 when amplifier1 is operating at 63.8MHz while amplifier2 is operating at at 64.0 MHz, both operating simultaneously.

The frequency component of the amplifier2 (operating at 64 MHz) as well as harmonics can be observed in the FFT of the amplifier1 shown in Fig. 4.9b. Harmonics are occurring at every 0.2 MHz (difference between 64 MHz and 63.8 MHz). Table 4.1 shows the effect of power on harmonics as the input power increases, output power increases and the effect of harmonics also increases.

Input Power of both Amplifiers **(W)**	The amplitude of the center frequency component (63.8MHz) **(dBm)**	The amplitude of the frequency component from the other amplifier (64MHz) **(dBm)**	The difference between the both frequency components. **(dB)**	The difference between Central frequency (63.8MHz) and the first harmonic **(dB)**
3	-11.2	-66	54.8	70
8	-7.4	-45	37.6	58.5
30	-3.8	-32	28.2	43.2
70	-1	-20	19	35.1
100	1.52	-13.5	15.02	27.4
150	2.01	-10.6	12.61	21.8
200	4.65	-5.4	10.05	17.3
250	6.4	-1.2	7.6	14
350	9	4.01	5	11.1

Table 4. 1: Relationship between the input power and the harmonics.

4.9. MRI Experiment Results

MRI results for class-E amplifier are very promising. It is observed that MR images show no artifact in the presence of amplifier near transmit coil inside the scanner. The results of MR experiments are shown in Fig. 4.12. . For the image in panel (a) an 8-channel Scimedix head coil and for the images in panels (b) and (c), body coil were used for reception so the images in panels (b) and (c) have noise. No visible artifact was observed in images due to the on-coil amplifiers. When one of the channel is off (panel c), induced current on the other coil resulted in tolerable B1+ field around the coil.

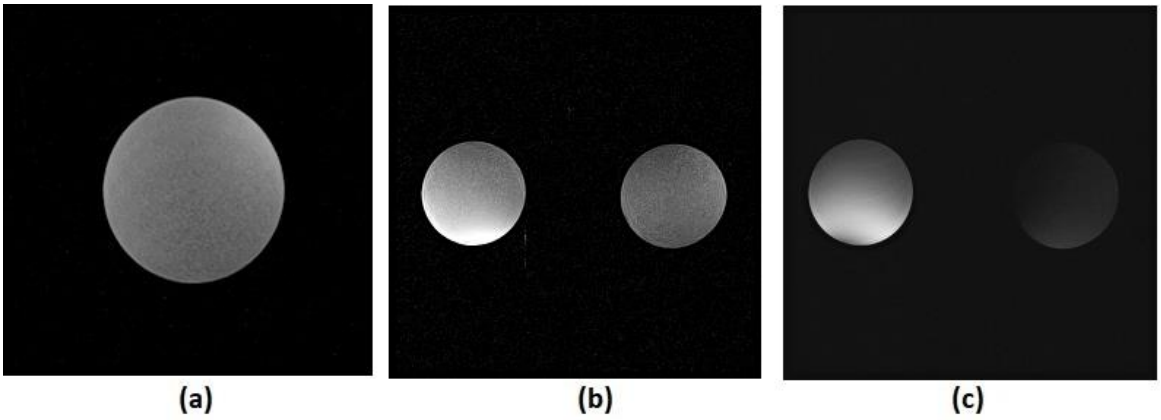


Fig. 4. 13: (a) MR image from single amplifier and transmit coil (b) MR image when both amplifiers are simultaneously on and are operating at 63.8 MHz (c) MR image when amplifier1 is on and amplifier2 is off.

CHAPTER 5

DISCUSSION AND CONCLUSION

In this thesis a highly efficient supply modulated class-E amplifier for RF excitation in MRI is presented. Class-E amplifier is verified to be a good candidate for on-coil application. It has the potential to replace the low efficiency conventional MRI RF amplifiers because of its high efficiency and small size. The decisive goal of this research is to design a 32-channel transmit array using on-coil amplifiers as an individual elements that will be able to deliver 300x32=9.6 KW power which should be adequate to run the body coil on a 1.5 T MR scanner. As each element on the coil would be controlled separately, it will provide more degree of freedom in slice selection and reduction of SAR. This amplifier was presented before with 100 W output power and with maximum efficiency of 88%. This amplifier was improved to deliver 250 W output power with maximum efficiency of 92% [36]. Now it can deliver 300 W output power. In order to maintain the operation of the class-E amplifier in the efficient region, there are some design constraints for the transmit coil. The tuning of coil is crucial for maximum output power and high efficiency as coil itself is used for matching and tuning network and a separate matching network is not required. The efficiency of amplifier is highly dependent on the tuning of transmit coil as small variations in tuning can change the input power and efficiency drastically.

The efficiency of amplifier in 1 MHz bandwidth does not drop below 75%. The good performance of amplifier in 1 MHz bandwidth designates that it could further be used to pre-distort the generated pulse in order to have an improved slice selection. The slight problem with this is that as the frequency changes between 63.5 MHz to 64.5 MHz the input power changes too as the input current changes. So the input power has to be adjusted by changing the supply voltage such that input power remains constant. The same problem occurs if the load resistance is varied. As the load resistance increases the current pulled by supply is decreases hence the input power decreases. To keep the input power constant we have to increase the supply voltage. The supply voltage cannot be increased too much as it is directly proportional to the V_{ds_max} so increasing it beyond the limiting V_{ds} of our MOSFET can burn it. So it will be better to design the current mode class-E amplifier similar to the one presented in [37] to make sure that the input current remains constant hence the input power remains constant for an uninterrupted and better operation. Also in current mode class-E amplifier the V_{ds_max} is lower as compare to voltage mode class-E amplifier. The initial step for this is done by doing the load pull analysis, the constant current contours for the amplifier are simulated for different impedance values but this has yet to be tested on hardware.

The driver of the amplifier is wide band and can be used for both 64 MHz and 123 MHz but the power transistor (BLF 573) used to deliver 300 W power could not be driven at 123 MHz by this driver. It was mainly because the frequency is so high that enough time was not available to charge and discharge the transistor's input capacitance. The same driver and supply modulation block can be used for some other transistor with have less input resistance and can deliver 300 W power. Another solution is to modify the driver design so that it is able to charge and discharge the input capacitance in small time so that even at 123 MHz BLF 573 can be used.

Due to the high efficiency this amplifier does not need separate cooling system when the duty cycle is low. The mechanisms for providing appropriate cooling are currently being investigated for an uninterrupted operation of the amplifier at low TR. It was observed

that if the duty cycle of amplifier is less than 20%, as the power is dissipated mostly in the main MOSFET, the junction temperature rose very quickly. Also at low duty cycle as the drain to source capacitance of our MOSFET is nonlinear; it caused the tuning point to get shift a little. This caused the drop in efficiency with in turn caused the amplifier to heat up. To minimize the effect of this nonlinear C_{ds} [38] [39] an external shunt capacitor is put in parallel with it such that at our tuning point C_p of class-E amplifier is equal to the sum of C_{sh} and C_{ds}. As C_{ds} is nonlinear so it changes as the supply voltage changes. The output power capability and efficiency of amplifier is greatly dependent on the grading coefficient of C_{ds}, It is explained in [39] that as the value of grading coefficient for C_{ds} increases the V_{ds_max} also increases so the output power capability decreases due to limiting V_{ds_max}. On the contrary efficiency increases. So the supply voltage was fixed such that the output power is 300 W and then the amplifier was tuned to get maximum efficiency at 300 W output power with appropriate C_p value. This strategy has minimized the heating of main MOSFET but has not eradicated this problem completely.

The behavior of the class-E amplifiers under coupled operations is being investigated. The initial results show that the effect is tolerable. The coupling between the transmit coils is inversely proportional to the distance between them. They were decoupled at 7 cm distance and it was observed that at 7cm more than 20 dB decoupling was achieved. When the amplifiers are working simultaneously at same frequency and phase there is no change in the efficiency after decoupling but when both amplifiers are operating simultaneously at different frequencies efficiency is time varying then. As the input frequency keeps on getting out of phase and in phase with respect to time, the efficiency also changes with time. Coupling is dependent on input power as well. The relationship between coupling and input power is nonlinear. When the input power increases coupling also increase but the relationship is nonlinear due to nonlinear C_{ds} , time varying phase of output pulse, the temperature change of transistor due to high power dissipation at high input power levels. The dependence of coupling of transmit coils and efficiency of amplifiers on various factors such as load variations, frequency variation, input power variation and output phase variation is currently being investigated. This will help us to

control the input parameters so that the efficiency can be controlled and amplifiers can be operated in such a way that they deliver maximum output with the highest efficiency possible.

The MR images show no artifacts in the presence of amplifier near the transmit coil inside the scanner. The developed 2 channel system can successfully select two separate slices at the same time. Better transmit coils are needed to conduct more MR experiments. Currently for 2-channel RF system body coil was used for reception so the images have low SNR. There is need to develop a 2 channel transmit coil that can fit on top of the 8 channel Scimedix head coil for signal reception. This will decrease the noise in the image and high SNR images will be acquired.

In future, It will be challenging to control all 32 channels together and to make sure there is no coupling between the transmit coils and other components to ensure the efficient and effective use of 32-channel transmit array with on coil amplifiers.

From the manufacturer point of view, this amplifier can be produced in our lab at $200. Its cost will be lower if it is mass-produced. In future, it is expected that the developed system will result in more efficient and flexible system than the current used system in MRI. It will also be highly controllable and will be useful in the future researches regarding improvement in SAR and reduction of implant heating etc.

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