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Selectively dry etched of p-GaN/InAlN heterostructures using BCI_3-based plasma for normally-off HEMT technology

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In this paper, an alternative selective dry etching of p-GaN over InAlN was studied as a function of the ICP source powers, RF chuck powers and process pressure by using inductively coupled plasma reactive ion etching (ICP RIE) system. A recipe using only BCI_3-based plasma with a resulting selectivity 13.5 for p-GaN in respect to InAlN was demonstrated. Surface roughness measurements depending on the etching time was performed by atomic force microscope (AFM) measurement and showed that a smooth etched surface with the root-mean-square roughness of 0.45 nm for p-GaN and 0.37 nm for InAlN were achieved. Normally-off p-GaN/InAlN HEMT device was fabricated and tested by using the BCI3-based plasma we developed.

1. Introduction

InAlN is a lattice-matched and strain free barier layer in InAlN/GaN high electron mobility transistors (HEMTs) that is enhanced the polarization and makes InAlN/GaN HEMTs more attractive than AlGaN/GaN devices in high frequency and high power applications [1-3].

InAlN/GaN HEMTs are normally depletion mode (D-mode) or “normally on” devices due to the nature of polarization charges. But p-GaN/InAlN/GaN heterostructure system are also used in HEMTs technology for enhancement-mode (E-mode) or “normally-off” operation. E-mode devices are mostly preferred for safety in power electronics and simple RF and Microwave circuits architecture in power switch applications [4-7]. In p-GaN/InAlN/GaN normally-off HEMTs devices, all the p-GaN layer must be etched except the area under the gate without etching 1-8 nm thick InAlN layer. III-N materials have high bond energies that makes wet chamical etching too diffucult. So that dry etching technique is mostly preferred for selective etching of GaN over InAlN.

Previously in the literature, various gases such as CCl_2F_2 [8], $SiCl_4$:Ar:SF_6 [9] and $SiCl_4$:SF_6 [10] are used for selective etching of GaN over InAlN. Sometimes depending on plasma conditions F ions formed by these gases are caused Al and AlF_3 non-volatile residuals on the InAlN surface. These by-products cannot be cleaned from the surface and cause a decrease in device performance by changing the structure of the surface. In this study, both to prevent this problem and to provide an alternative gas to the literature, BCI_3-based plasma was used for selective etching of p-GaN over InAlN with a good surface roughness. According to our research in the literature, as far as we know, this is the first time to used and characterized BCI_3-based plasma for selective etching of p-GaN over InAlN.

In this work, etch rate of p-GaN and InAlN were studied as a function of the ICP source powers, RF chuck powers and process pressure by using inductively coupled plasma reactive ion etching (ICP RIE) system. Surface roughness of p-GaN and InAlN depending the etching by the recipe obtained with the highest selectivity were performed by using atomic force microscope (AFM). Another group within NANOTAM tested the etching recipe by fabricating and DC characterizing of a p-GaN/InAlN normally off HEMT device [11].

2. Experimental procedure

The p-GaN, InAlN and p-GaN/InAlN HEMT structure were grown on a 2′′ Si substrate in a low-pressure metal-organic chemical vapor deposition reactor (Aixtron 200/4 RF-S). Trimethylgallium (TMGa), trimethylaluminum (TMAl), trimethylindium (TMIn), and ammonia (NH_3) were used as Ga, Al, In, and N precursors, respectively [12,13]. The growth of the all samples were initiated with a AlN nucleation layer and then an AlGaN buffer layer on it. After

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that, 60 nm Mg-doped GaN layer with the hole concentration of approximately $3.0x10^{17}$ cm^{-3} was grown for p-GaN etching rate studies. Consecutively 4 µm u-GaN and 60 nm $In_{0.17}Al_{0.83}N$ were grown for InAlN etching rate studies. p-GaN/InAlN HEMT structure was grown to consist of the following layers, consecutively AlGaN back-barrier, GaN channel, AlN spacer, 8 nm $In_{0.17}Al_{0.83}N$ and 20 nm p-GaN cap layer. The cross-section of the three grown samples is shown in figure 1. All 2" samples were cut into the 12x12 mm^2 pieces for etching studies.

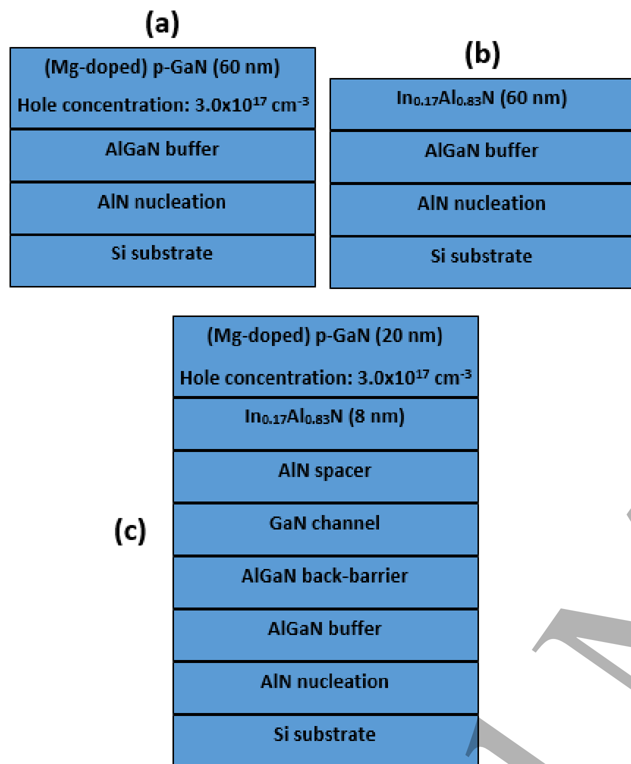

Figure 1. Cross sectional structure of the three samples grown by MOCVD. (a) Sample structure for p-GaN etching studies (b) Sample structure for InAlN etching studies (c) p-GaN/InAlN HEMT structure.

Previous to the fabrication process the samples were prepared by an organic cleaning procedure, using acetone, isopropanol and deionized water. Suss Microtec MA6 mask aligner was used for optical lithography and AZ5214E photoresist was used for masking. Dry etching processes was performed in SI-500 Sentech ICP RIE system and etching depth measurements were performed in Veeco Dektak 150 surface profilometer. Both InAlN and p-GaN samples were etched at the same time with various ICP source powers, RF chuck powers and process pressures under BCI_3-based plasma in order to maximize the selective etching of p-GaN over InAlN. It was tried to reach the maximum etching rate for p-GaN and the minimum etching rate for InAlN. In all etching processes, the BCI_3 gas flow was kept constant at 20 sccm. Surface roughness measurements of p-GaN and InAlN sample surfaces were performed in atomic force microscope (AFM) after the surfaces etching with the BCI_3-based plasma-etching recipe with the maximum selectivity (Selectivity = etch rate of p-GaN/etch rate of InAlN). After finding the etching recipe with the maximum selectivity, p-GaN/InAlN normally-off HEMT device was fabricated and DC characterized to test this recipe by another group within NANOTAM [11].

The fabrication process for p-GaN/InAlN normally-off HEMT device started with ohmic contact formation. At first all the p-GaN cap layer was etched until the top of the InAlN layer in the drain-source regions by using the BCI_3-based plasma-etching recipe and then a Ti/Al/Ni/Au metal stack was deposited. The metal stack was annealed in a nitrogen atmosphere at 875 °C for 30 s. Mesa etching was performed with the Sentech ICP RIE system by using Cl_2/BCl_3 plasma-based dry etch. Suss Microtec MA6 mask aligner and AZ5214E photoresist was used for optical patterning the gate foot region of the sample. The gate length, L_G, is 1.5 µm, and the gate width, W_G, is 100 µm. The source-to-gate, L_{SG}, and the gate-to-drain, L_{DG}, spacings are 1.75 µm. Gate feet regions were deposited with an Ni/Au metal stack by using using an electron beam evaporator system (EBE) with thicknesses of 50 and 300 nm, respectively. Then, a Ti/Au metal stack with a total thickness of 1.1 µm was deposited as an electrical contact pads. After this step, except for the p-GaN layer under the gate contact, all the p-GaN layer between drain-source was etched until the top of the InAlN layer with the BCI_3-based plasma-etching recipe. The use of a p-GaN layer under the gate contact causes the raising the conduction band and enables normally-off operation [11]. However, if the p-GaN layer between the drain-source is not etched, it also causes a decrease in the current and power density for the normally-off HEMT device due to the same effect. To prevent this, except for the p-GaN layer under the gate contact, all the p-GaN layer between the drain and the source was etched. Finally, a 200 nm SiN layer was deposited as a surface passivation layer using the plasma enhanced chemical vapor deposition (PECVD), and the fabrication process was completed with this last step. Figure 2 shows cross sectional representation and optical microscope image of the fabrication completed normally-off p-GaN/InAlN HEMT device [11].

DC characterization of normally-off p-GaN/InAlN HEMT device was performed using a Keysight B1500A Semiconductor Device Parameter Analyzer [11].

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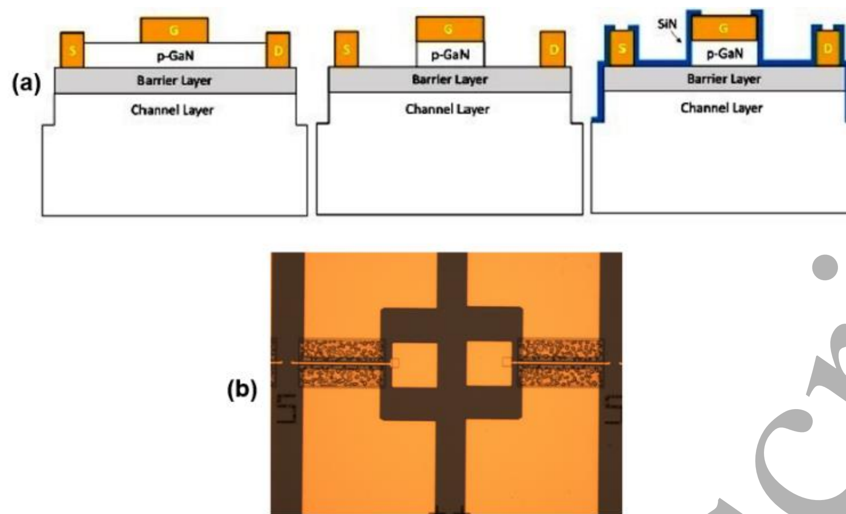

Figure 2. Cross sectional representation (a) and optical microscope image (b) of the fabrication completed HEMT device [11].

3. Results

p-GaN, and InAlN etch rates and selectivities are shown in Figure 3 as a function of process pressure in a BCl_3-based plasma. The process pressure was changed between 0.5-10 Pa while the other parameters were fixed to constant values. ICP source power and RF chuck power were fixed to 50W and 30W, respectively. The etching rate and selectivity were changed randomly due to the change in the types of radical species produced in the plasma depending on the different levels of applied pressure. The maximum selectivity value was obtained as 6.1 ± 1 at 7.5 Pa of process pressure value. At this pressure, the etching rate was found 4.7 ± 0.5 nm/min for p-GaN and 0.77 ± 0.08 nm/min for InAlN.

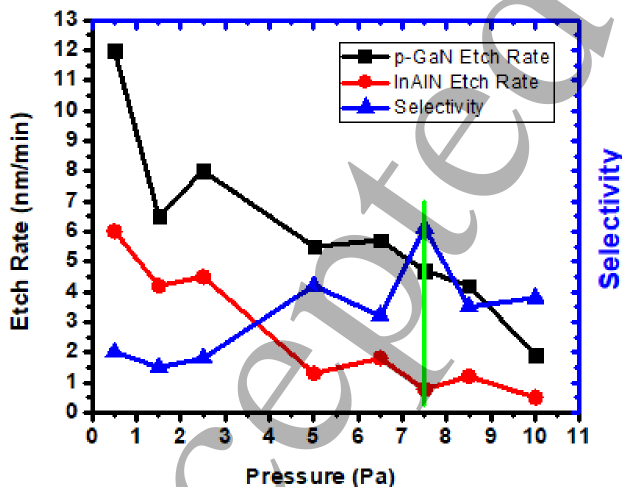

Figure 3. p-GaN, and InAlN etch rates and selectivities as a function of process pressure in a BCl_3-based plasma.

After obtaining the maximum selectivity value at 7.5 Pa, the process pressure and the RF chuck power values were fixed to 7.5 Pa and 30W, respectively, and the effect of the change in ICP source power value on the p-GaN, and InAlN etching rates and selectivity were investigated. The ICP source power was changed between 0-200 W. Figure 4 illustrates this situation.

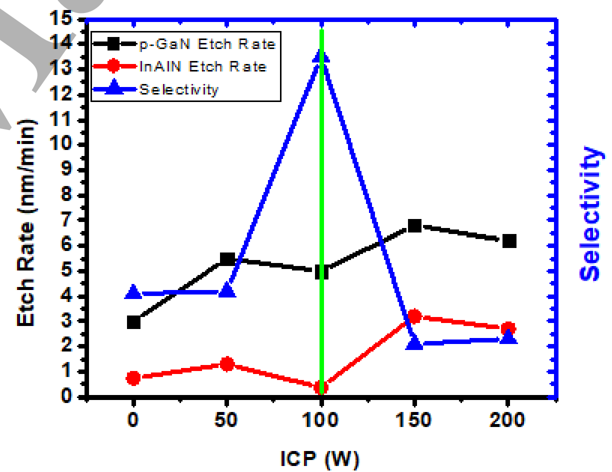

Figure 4. p-GaN, and InAlN etch rates and selectivities as a function of ICP source power in a BCl_3-based plasma.

As the ICP source power increases, the amount of ions produced increases. However, an increase in the amount of ions will affect the amount of collision of ions with each other and the physical and chemical interaction of these ions with the material surface. As seen in Figure 4, the etch rates of GaN and InAlN materials at different ICP source power values varied depending on the number of ions produced at different ICP source power values and the interactions of these ions with the surface. The selectivity increased with the

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increasing of the ICP source power and reached a maximum with a value of 13.5 ± 3 at 100 W but then decreased again after this power value. At this value, the etching rate was found 5 ± 0.5 nm/min for p-GaN and 0.37 ± 0.04 nm/min for InAlN.

Thereafter, the process pressure and the ICP source power values were fixed to 7.5 Pa and 100W, respectively, and the effect of the change in RF chuck power value on the p-GaN, and InAlN etching rates and selectivity were investigated. RF chuck power was changed between 30-200 W. This is seen in Figure 5. As the RF chuck power increases, the energy of the ions increases and types of radical species generated change. Chemical and physical response of p-GaN and InAlN materials to these radicals generated at different applied RF chuck power varies, which causes the etch rates of p-GaN and InAlN materials to change at different RF chuck power values. As seen from Figure 5, the selectivity decreased with the increasing of the RF chuck power. The maximum selectivity value was obtained as 13.5 ± 3 at 30 W of the RF chuck power value.

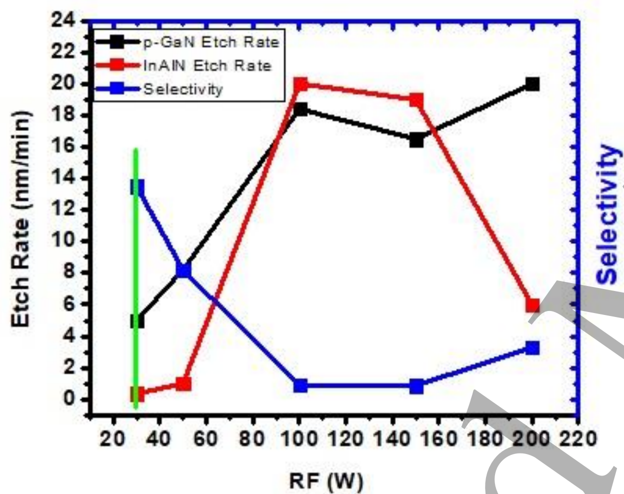

Figure 5. p-GaN, and InAlN etch rates and selectivities as a function of RF chuck power in a BCl_3-based plasma.

As can be seen from the figures above, the maximum selectivity with a value of 13.5 ± 3 while the p-GaN etching rate was 5 ± 0.5 nm/min and InAlN etching rate was 0.37 ± 0.04 nm/min could be obtained at the values where the process pressure, the ICP source power, the RF chuck power, and the flow of BCl_3 gase were 7.5 Pa, 100W, 30W, and 20 sccm, respectively. After obtaining the maximum selectivity value, the surface roughness variation of the p-GaN and InAlN layers depending on the etching time was investigated in the mentioned plasma parameters. Figure 6 shows the change in surface roughness depending on the etching time for p-GaN and InAlN surfaces was examined using tapping mode AFM for an area of 3.0 x 3.0 μm². Figure 7 shows the AFM images of the p-GaN surface for 5 minutes etched time and the InAlN surface for 1 minute etched time.

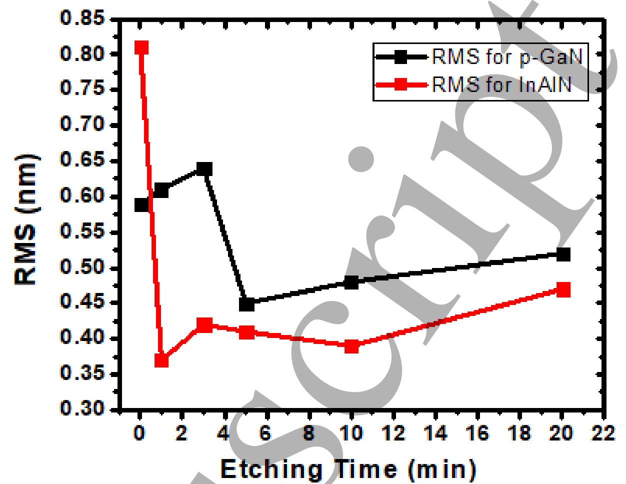

Figure 6. The surface roughness depending on the etching time for p-GaN and InAlN in tapping mode AFM for an area of 3.0 x 3.0 μm².

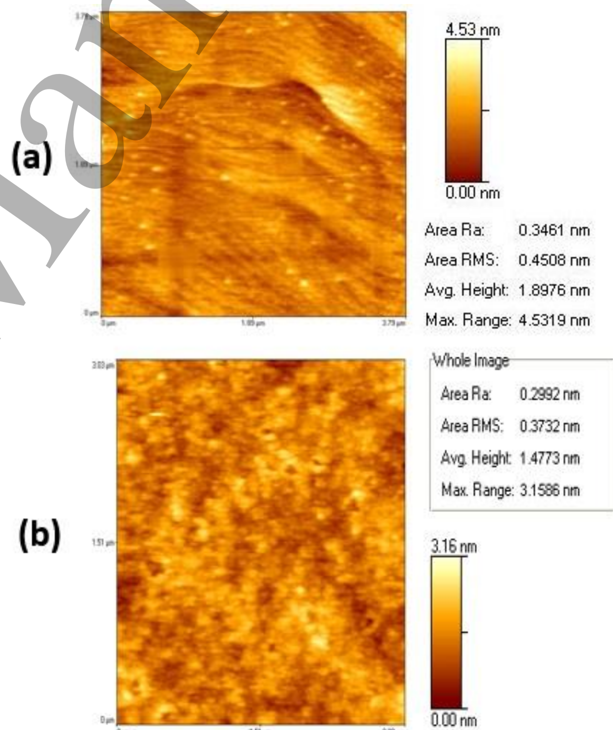

Figure 7. AFM images of (a) the p-GaN surface for 5 minutes etched time and (b) the InAlN surface for 1 minutes etched time.

Within the scope of p-GaN/InAlN normally-off HEMT device fabrication, the etching time for the 20 nm thick p-GaN layer is 5 minutes with the over etch time (4 min for etched 20 nm p-GaN and 1 min for over etched). During this period, the surface roughness value for the p-GaN layer

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etched with the mentioned process parameters was obtained 0.45 nm. For the InAlN layer, which is not required to be etched within the scope of normally-off HEMT fabrication, the surface roughness value was obtained 0.37 nm for 1 minute etching time (this time is over-etching time for the etching p-GaN layer over InAlN layer in the process) . When Figure 6 is examined, it is seen that the surface roughness decreases depending on the etching time. We think that this is due to induce the surface modification and also changed the particle size on the surface with respect to the etching time increases in our recipe, which is mostly chemical etching [14-27].

The use of a p-GaN layer under the gate contact causes the raising the conduction band and enables normally-off operation in p-GaN/InAlN HEMT devices. However, if the p-GaN layer between the drain-source is not etched, it also causes a decrease in the current and power density for the normally-off HEMT device due to the same effect. To prevent this, except for the p-GaN layer under the gate contact, all the p-GaN layer between the drain and the source must be etched without etching the very thin InAlN layer and without damaging the surface. p-GaN/InAlN normally-off HEMT device fabrication and DC characterization were done by another group within NANOTAM and showed that the developed BCl_3-based plasma etching recipe was worked well [11]. DC measurements were performed using a parametric semiconductor device analyzer. Figure 8 shows the I_d-V_g characteristics for HEMT device before and after the etching of p-GaN between the drain-source and after the SiN passivation coating. The pinch off-voltage (V_{th}), using the extrapolation of the current at the maximum linear slope, increased from 1.3 V to 2 V after the p-GaN layer etching.

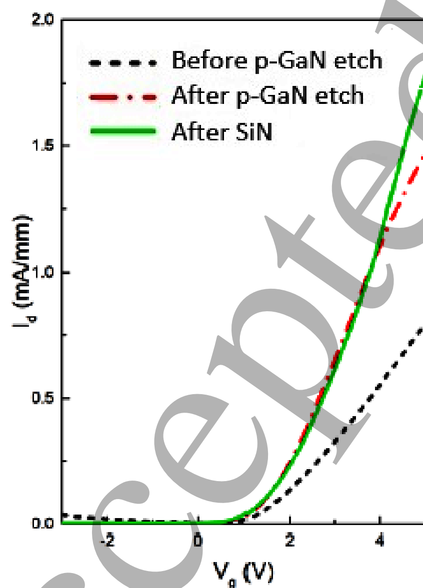

Figure 8. I_d-V_g characteristics of p-GaN/InAlN normally-off HEMT device. The drain bias (V_d) was 10 V [11].

Drain current-voltage (I_d–V_d) characteristics of HEMT device before and after the etching of p-GaN between the drain-source and after the SiN passivation coating of the device are shown in Figure 9. The gate bias (V_g) was swept from 1 to 4 V in a step of 1 V and drain current-voltage (I_d–V_d) characteristics was measured. As seen from Figure 8, the drain current (I_d) increases from 0.4 mA/mm to 1.0 mA/mm after the etching of p-GaN between the drain-source, and to 1.3 mA/mm after the SiN passivation coating. Figure 8 also shows that the selective etching of p-GaN over InAlN were done successfully with developed recipe.

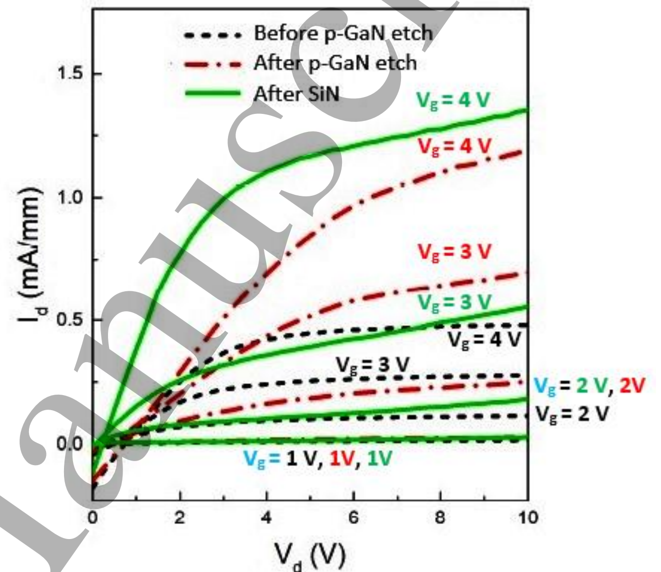

Figure 9. Drain current-voltage (I_d–V_d) characteristics of p-GaN/InAlN normally-off HEMT device. The gate bias (V_g) was swept from 1 to 4 V in a step of 1 V [11].

4. Conclusion

In summary, we developed a new selectively dry etching recipe for p-GaN/InAlN heterostructures using BCI3-based plasma for normally-off HEMT technology. The maximum selectivity, p-GaN etching rate and InAlN etching rate were obtained 13.5 ± 3, 5 ± 0.5 nm/min, and 0.37 ± 0.04 nm/min, respectively.

Using the developed recipe, the change in surface roughness depending on the etching time was investigated for p-GaN and InAlN surfaces depending on the etching time. The surface roughness values were measured as 0.45 and 0.37 nm, respectively, for p-GaN etched for 5 minutes and InAlN etched for 1 minute.

It has been shown that normally-off p-GaN gate HEMTs based on the p-GaN/InAlN heterostructure fabrication can be performed successfully using the BCI_3-based plasma recipe we developed [11].

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