BATCH-COMPATIBLE MICROMANUFACTURING OF A CMUT ARRAY FOR OPTOACOUSTIC IMAGING OF TISSUE-LIKE PHANTOMS

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By

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We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

BATCH-COMPATIBLE MICROMANUFACTURING OF A CMUT ARRAY FOR OPTOACOUSTIC IMAGING OF TISSUE-LIKE PHANTOMS

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Photoacoustic imaging (PAI), also named optoacoustic imaging, is a technology for medical imaging that relies on contrast data due to optical stimulation. Capacitive micromachined ultrasound transducers (CMUTs) are previously introduced for PAI applications.

In this thesis, the provided CMUT array design has been partially micromanufactured separately from electronics and a laser fiber light source while reserving the necessary chip space for integration with electronics and laser fiber light source. Batch compatible wafer-scale microfabrication of CMUT arrays was done by a combination of novel as well as traditional MEMS microfabrication processes. CMUT array gaps, bottom electrodes, and insulation layer were formed on the Pyrex wafer using three separate photolithography masks. Anodic wafer bonding method is used for the formation of the top electrodes and top side of the gap heights of CMUT arrays. Process development for anodic wafer bonding between Pyrex wafers and SOI wafers has been done, where the Pyrex wafers have been previously processed with plasma etching, wet etching, metal stack deposition, insulation layer deposition, and insulation layer patterning, while SOI wafers have been used as received. Pyrex wafers and SOI wafers were anodically bonded to each other with developed anodic wafer bonding processes. After full completion of the micromanufacturing of the CMUT array chips, these CMUT array chips will be integrated with ASIC chips. Then, CMUT array chips and ASIC chips will be combined with a traditional printed circuit board (PCB). These integrated CMUT array chips, ASIC chips, and PCB are going to be integrated with a fiber laser light source inside a mechanically robust hand-held probe that is planned to be used for optoacoustic imaging. The main goal of this CMUT

array micromanufacturing study is to significantly contribute to the development of one of the necessary components for imaging of a tissue like-phantom using a hand-held imaging probe.

Keywords: Capacitive Micromachined Ultrasonic Transducers, Microfabrication, CMUT, MEMS, Array, Optoacoustic Imaging, Photoacoustic Imaging, Anodic Wafer Bonding.

ÖZET

DOKU BENZERİ FANTOMLARN OPTOAKUSTİK GÖRÜNTÜLENMESİ İÇİN CMUT DİZİLERİNİN TOPLU MİKRO ÜRETİMİ

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Optoakustik görüntüleme olarak da adlandırılan fotoakustik görüntüleme (PAI), optik uyarılma sonucunda ortaya çıkan kontrast verilerine dayanan tıbbi görüntüleme teknolojisidir. PAI uygulamaları için kapasitif mikro-işlenmiş ultrason dönüştürücülerin (CMUT'lar) kullanılması daha önceden çalışılan bir alandır.

Bu tezde, elektronik ve lazer fiber ışık kaynağı ile entegrasyon için gerekli çip alanını koruyan, elektronik aksamdan ve bir lazer fiber ışık kaynağından ayrı olarak dizayn edilmiş CMUT dizi tasarımının mikro üretim süreci kısmen tamamlanmıştır. CMUT dizilerinin yonga ölçekli mikrofabrikasyonu, yeni ve geleneksel MEMS mikrofabrikasyon işlemlerini bir arada kullanarak tamamlanmıştır. Üç ayrı fotolitografi maskesi kullanılarak Pyrex wafer üzerinde CMUT dizi boşlukları, alt elektrotlar ve yalıtım katmanı oluşturulmuştur. CMUT dizilerinin üst elektrotlarının ve üst taraflarının boşluk yüksekliklerinin oluşturulması için anodik alttaş bağlama yöntemi kullanılmıştır. Pyrex alttaşlar ve SOI alttaşlar arasında anodik alttaş bağlama için süreç geliştirme deneyleri yapılmıştır. Pyrex alttaşlar, anodik alttaş bağlama işleminden önce plazma aşındırma, ıslak aşındırma, metal kaplama, yalıtım katmanı kaplama ve yalıtım katmanı desenleme ile işlenmiştir. SOI alttaşlar ise üzerlerinde herhangi bir işlem yapılmadan kullanılmıştır. Pyrex alttaşlar ve SOI alttaşlar, geliştirilmiş anodik alttaş bağlama işlemleri ile anodik olarak birbirine bağlanmıştır. CMUT dizisi yongalarının mikro üretiminin tam olarak tamamlanmasından sonra, bu CMUT dizisi yongaları ASIC yongaları ile entegre edilecektir. Ardından, CMUT dizi yongaları ve ASIC yongaları, geleneksel bir baskılı devre kartı (PCB) ile birleştirilecektir. Bu entegre CMUT dizi yongaları, ASIC yongaları ve PCB, optoakustik görüntüleme için kullanılması planlanan mekanik olarak sağlam, el ile tutulabilir bir probun içinde bir fiber lazer

ışık kaynağı ile entegre edilecektir. Bu CMUT dizisi mikro üretim çalışmasının ana amacı, el ile tutulabilen bir görüntüleme probu kullanılarak doku benzeri bir fantomun görüntülenmesi için gerekli bileşenlerden birinin geliştirilmesine önemli ölçüde katkıda bulunmaktır.

Anahtar sözcükler: Kapasitif Mikroişlenmiş Ultrasonik Dönüştürücüler, Mikrofabrikasyon, CMUT, MEMS, Dizin, Optoakustik Görüntüleme, Fotoakustik Görüntüleme, Anodik Yonga Bağlama.

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Chapter 1

Introduction

Photoacoustic imaging (PAI) is a non-invasive medical imaging method incorporating optical imaging contrast information and acoustic imaging spatial resolution. Capacitive micromachined ultrasound transducers (CMUTs) are previously introduced for PAI applications [1]. CMUTs are MEMS devices that can be fabricated via micromanufacturing methods. The research group at Stanford University firstly presented the CMUTs in 1994 [2]. Recent advances in microfabrication and further developments on CMUTs demonstrated that CMUTs could provide advantages such as larger bandwidth, ease of fabrication of large arrays with individual electrical connections, and integration with electronics in comparison to conventional piezoelectric transducers [3], [4].

A typical CMUT is a variable capacitor cell consisting of at least an electrically conductive movable plate, or membrane, suspended above a bottom electrode on a substrate. Typically, a vacuum gap is formed between a membrane (top electrode) and a silicon substrate (bottom electrode) [5]. A non-conductive material may either be deposited on the silicon substrate or below the conductive membrane to prevent a short circuit between the top electrode and bottom electrode. The gap height between the top electrode and bottom electrode changes due to the incident sound wave pressure. Thereby, the capacitance between the top electrode and bottom electrode changes, and that affects the produced current [6].

The "sacrificial layer release for the gap formation" and the "wafer bonding for the gap formation" integration process approaches are two standard integration processes for the microfabrication of CMUT arrays [5]. If not considered carefully, the sacrificial release process has some limitations due to long etch times, such as poor control over the uniformity, absolute thickness, and gap height [7]. On the other hand, if the substrate materials and electrode materials are considered carefully, the wafer bonding process simplifies the fabrication, reduces the number of process steps, provides uniformity and control over plate thickness [8]. Also, similar to the sacrificial layer release process, wafer bonding enables batch processing. Thus, numerous devices can be microfabricated on a single wafer using both approaches.

The sacrificial release approach was the first method developed for the manufacturing of CMUTs. In this approach, the vacuum gap is formed by etching a sacrificial layer between the top plate, and the substrate material [2].

A typical sacrificial release process includes the following materials. A top plate material, which has holes to give access to etchants to remove sacrificial material to form a gap, a substrate material that can be glass [9] or silicon [10], an electrical insulation layer, which can be grown on silicon wafer by thermal oxide growth method [11], or can be deposited by CVD methods [12], a sacrificial layer material, (Cr [9], Ni [13], polysilicon [14], or SiO_2 [11]), a utilizing sealing material (Si_3N_4 [12], undoped silicon glass [13], Al_2O_3 [11]) that fills the entrance or exit ports of the previously formed gaps under vacuum environment of the sealing material deposition process chamber. Lastly, a conductive material is deposited to form a top electrode. Furthermore, if the CMUT device is desired to work inside water or oxidative environment, it is necessary to deposit another insulating or passivating layer on top of the conductive electrode in order to prevent electrical shorts or undesired oxidation on the metal electrode.

The thickness of the sacrificial material determines the gap height, and the top plate thickness is determined by the deposited thickness of the top material in the sacrificial release process. In contrast to most of the wafer-bonding approaches, the sacrificial layer release approach makes non-uniform structures [3].

On the other hand, the sacrificial release process has several advantages. CMUT devices manufactured with sacrificial layer release process are convenient to use and durable. Furthermore, if manufactured carefully, yield issues that may be visible with wafer bonding technology approaches may not be visible with sacrificial layer release approaches. Furthermore, sacrificial release processes can be done with relatively low deposition temperatures (250 °C) [15]. The vacuum-sealing process in the sacrificial release approach makes devices suitable for immersion applications [16].

In the wafer bonding technique, the CMUT is made by using both silicon on insulator (SOI), and surface micromachining technologies [17]. The wafer bonding approach simplifies the micromanufacturing steps and introduces new levels of uniformity and control, particularly in terms of plate thickness, which is determined by the SOI wafer's device layer, instead of the thickness of deposited material [3].

Basic process steps of CMUT fabrication using wafer bonding technology starts with a substrate material which can be silicon [18], glass [19], or LTCC [20], [21]. Gap size and shape can be defined either on the bottom part (i.e. substrate) or top part (i.e. device layer of SOI wafer) and transferred to the wafers utilizing lithography processes followed by dry etch or wet etch. Here, it is important to emphasize that if there are features on both wafers before anodic wafer bonding, fine alignment will be required between two wafers to be bonded. On the other hand, if all the patterning is done only on one of the substrates (i.e. Pyrex), fine alignment will not be needed between the SOI wafer and Pyrex wafer for the wafer bonding process. In other words, if the features are only on one substrate up to the wafer bonding process, only course alignment would be sufficient between the patterned substrate and the unpatterned substrate. The conductive material can be deposited into the cavity and then passivated with an insulator to prevent shorting between the bottom of the gap and the conducting plate, which is going to be the device layer of the SOI wafer. Before the wafer bonding process, chemical-mechanical polishing (CMP) may be applied to the wafer's surface to be bonded to obtain a smooth and flat surface required for the wafer bonding process. Fundamentals of wafer bonding technology are reported by Cunningham et

al. (2016) [22]. After the wafer bonding process, it is possible to remove the bulk region of the SOI wafer by using mechanical polishing, dry etching, or wet etching processes. Finally, etchant solution, such as buffered oxide etchant (BOE), would be used to remove the BOX layer [23]. After these fabrication steps, bottom electrodes, gaps, suspended membranes, and top electrodes of CMUTs are formed. The rest of the process steps are related to the deposition of conductive contact pads and isolation (electrical isolation and under vacuum isolation of the gap) of the device. Metal contacts may be deposited by physical vapor deposition methods. In some cases, a thick layer of material may be deposited on top of the top electrode to produce higher output pressure during the operation of a CMUT device [24]. Finally, insulator material can be utilized to passivate the plate edge sidewall, to prevent shorting caused by surface conduction, and sealing the gaps for immersion applications [25].

The main disadvantage of the wafer bonding method is that the wafer bonding process is extremely sensitive to surface roughness [26] and cleanliness, and that may cause low yield [3]. There are several types of wafer bonding approaches that are used for CMUT device microfabrication. From these wafer bonding approaches, the anodic wafer bonding approach is a simple and effective approach [27], [28] while direct wafer bonding is more complex due to the strict surface quality constraints of the process [29]. From these bonding techniques, the suitable bonding technique should be selected concerning the substrate material's flatness, surface smoothness, and surface cleanliness. Furthermore, if anodic wafer bonding technique is selected for wafer bonding processing, there must be a glass substrate that has mobile alkali ions such as sodium or lithium [9] that allows chemical bonding between the glass substrate and Si wafer, or one of the silicon layers of an SOI wafer. When utilizing thermally oxidized wafers without a glass layer, the bonding is achieved by the migration of OH^- and H^+ ions instead of Na^+ ions [30]. The bonding approach also depends on the bonding environment, allowable bonding temperature, ambient pressure, applied force, and materials of the substrates.

Given the prior CMUT design parameters, membrane selection is mostly related

to the available fabrication method (i.e., wafer bonding or sacrificial layer approaches). Silicon nitride [10], polysilicon [31] and silicon [32] are commonly used materials for surface micromachining processes. As SOI wafers are used as the top wafer in the wafer bonding technology, Si device layers of SOI wafers have become one of the most used membrane materials for wafer bonding. Furthermore, investigation about various materials that are used as membrane materials (SiC, Si, diamond, Si_3N_4, and polysilicon) for CMUT devices has been done by Yasar et al. using a SIMULINK model [33].

The bottom electrode is a critical component of a fabricated CMUT device. The type of material or stack of thin-film materials combination of the bottom electrodes depends on the bottom substrate. Silicon is a commonly used material as the bottom electrode in the sacrificial release approach [34], and wafer bonding approach [24]. The bottom electrode material stack should be carefully selected in the case of a CMUT device that is fabricated with glass substrate using anodic wafer bonding technology, because gas could become trapped inside the cavities after the anodic wafer bonding process. One solution to this problem is titanium thin-film deposition in gap regions, which can be utilized as a getter to improve package pressure [35].

A through-silicon-via (TSV) is a direct vertical interconnection between different levels of a wafer. TSV is one of the most innovative and effective ways to use the third dimension of a wafer, in wafer and/or die level 3D integration techniques. TSV consists of a conducting via that connects the two sides of a wafer by crossing through the silicon substrate [36]. The TSV connection is usually etched through deep reactive ion etching (DRIE) and filled with metal using a conductive paste, electrodeposition, or PVD. Before the vias are filled in with a conductive material, the sidewalls of the formed via are passivated with a dielectric material. Then, if electrodeposition is going to be used for via filling, a metal seed layer is deposited before the actual electrodeposition process is performed. To provide electrical connectivity from the backside via through-silicon-via, additional steps can be added to the sacrificial release [37] or wafer bonding processes [38]. After etching through holes using DRIE, a conductive material is used to fill the vias, which serve as the fixed bottom electrode of a CMUT device [39].

Because of the significant mismatch in the coefficients of thermal expansion between the TSV filling conductor and the silicon wafer, significant thermo-mechanical stresses are created around the TSV when the structure is subjected to temperature loading during thermal processing [40]. The reliability of TSV-based 3D integration solutions can be affected by these stresses. Furthermore, due to constraints in the etching and metal deposition processes, the TSV has limited widths, and thicknesses [41].

Because of the unique and favorable material properties of glass, such as thermal expansion coefficient similar to Si, high electrical insulation, high corrosion resistance, low dielectric constant, optical transparency that allows visible inspection, and low parasitics, the through-glass-via (TGVs) approach is a promising solution to replace TSV [42]. Both of the sacrificial release and wafer bonding processes can be used to make CMUT devices with TGVs [9], [43]. Ultrasonic drilling [44], sandblasting [45], wet etching [46], dry etching [47], and laser drilling can all be used to build through-wafer channels [48]. In the vias, the use of conductive material with a matching thermal expansion coefficient to a glass substrate, reduces the potential for mechanical stress that may be induced by subsequent heating stages [49].

On the other hand, there are some challenges with TGV channel formation. In terms of hole formation speed and aspect ratio, laser drilling is the most efficient approach among the others [50]. However, residuals from laser drilling have an undesired effect on wafer bonding processes [51]. Furthermore, femtosecond lasers can produce smooth surfaces. However, although there are efforts to increase the material removal rates, up-to-date femtosecond lasers have low material removal rates and are expensive tools [52].

Low-Temperature Co-fired Ceramic (LTCC) substrates can be produced by aligned stacking of thin LTCC layers which have holes and lines filled with conductive materials [53]. Micromanufacturing of CMUT devices with LTCC substrates may be feasible since LTCC is an insulating substrate that contains 3D electrical conduction paths to carry the electrode connections to the other side of the substrate and due to the high-temperature resistance of the substrate. Furthermore,

based on the insulating property of the LTCC substrates, LTCC is advantageous to reduce parasitic capacitance and series resistance. For example, Yildiz et al. (2016) demonstrated a CMUT device that is made using LTCC substrates that have 3D conductive interconnections and utilized anodic wafer bonding technology [20].

In this batch-compatible CMUT array micromanufacturing thesis study, the CMUT array device is microfabricated using the anodic wafer bonding approach to form the gaps of the CMUT array between Pyrex and SOI wafers. The design of the CMUT array was done separately and was provided as input for the micromanufacturing study conducted in this thesis. When the CMUT design was being done, the limitations of the micro-manufacturing capabilities of the used cleanroom facilities were considered as carefully as possible. The designed input (i.e. given) properties of the CMUT device, which has 7.5 MHz operating frequency, 75 μm plate radius, 42 μm edge to edge distance, 5 μm line, and 6.75 μm space for wirings between the edge to edge distance, and 150 nm gap height, were determined by considering the experience from past projects and cleanroom process limitations. Furthermore, 256 CMUT element array is formed with reserved empty (i.e. no CMUT array) area in the center of CMUT chip for the laser fiber and dedicated areas for electronics connections.

After completing the batch-compatible wafer-scale microfabrication of CMUT array chips, it is planned that ASIC chips will be connected to CMUT array chips via flip-chip bonding processing. These CMUT-ASIC pairs will be integrated to a traditional printed circuit board (PCB) with a conductive paste using a stencil. These three major components (CMUT array chip, ASIC chips, and PCB) are going to be integrated into a hand-held probe.

Photoacoustic image formation from a tissue-like phantom using the fabricated CMUT arrays in the hand-held probe is the main goal and the last step of the entire project.

In Chapter 1, we did a detailed literature survey and analyzed the technologies that are available for CMUT array micromanufacturing. In Chapter 2, we are

going to be explaining our CMUT micromanufacturing approach in detail.

Chapter 2

Fabrication Process

2.1 Design Considerations of CMUT Array

Microfabrication capabilities of the cleanroom facility and the experience from past studies were some of the primary considerations while designing the CMUT array parameters. The designed CMUT array is constructed from 256 elements, where a reserved empty area of 12×12 elements (for the laser fiber) at the central region is subtracted from 20×20 elements to obtain the 256 elements.

Due to the needed electrical connections from each element, appropriate wiring of each of these CMUT elements is crucial. At least three wires need to be placed between two neighboring elements to make the best use of available wiring space. The experience that we obtained from recent studies, and considering the capabilities and limitations of our cleanroom facilities, the minimum width of the wires is set to 5 μm, and the spacing between wires is set to 6.75 μm. Thus, 42 μm becomes the edge-to-edge distance between two successive CMUT cells.

The given designed input parameters, which are operating frequency, plate radius, edge to edge distance, the thickness of the insulator, gap height, and the number of elements in the CMUT array, can be seen in Table 2.1.

Resonance Frequency (MHz)	7.5
Plate Radius (μm)	75
Plate Thickness (μm)	12
Edge to Edge Distance (μm)	42
Insulator Thickness (nm)	150
Gap Height (nm)	150
Array Elements	256

Table 2.1: Given structural design parameters for the microfabricated CMUT array.

2.1.1 Selection of Bottom Plate and Top Plate

In this batch-compatible CMUT array micromanufacturing study, anodic wafer bonding technology is used to form a gap between the top electrode and bottom electrode. The movable plate is constructed from single-crystal silicon device layer of an SOI wafer, which has favorable mechanical properties such as minimal internal defects, low internal mechanical loss, and very low internal stress [54]. A substantial thickness uniformity, process repeatability, and control over the stress can be achieved by using the device layer of an SOI wafer as the vibrating top plate [55].

Using an electrically insulating substrate to fabricate CMUTs can minimize device parasitics and improve the fabrication flow by avoiding the complex isolation procedures [56]. Thus, in this study, Pyrex 7740 glass is selected as a fixed bottom plate, where the bottom electrode is composed of Ti/Pt/Au metal stack for anodic wafer bonding processing requirements.

Furthermore, Pyrex 7740 glass has an optically transparent structure. Therefore, it can enable novel applications where optics and acoustics are combined [57].

However, micromachining glass for a cavity, hole, or microchannel formation is necessary for several MEMS devices. To be able to fabricate these MEMS devices, Pyrex can be structured by utilizing different techniques such as powder blasting [58], blade sawing [59], laser [60] and ultrasonic drilling [61], wet etching [62] or dry etching [63].

Selected materials for this study can be seen in Table 2.2.

Substrate Material	Pyrex 7740
Membrane Material	Silicon device layer of SOI
Insulator Material	Al_2O_3
Bottom Electrode	Ti/Pt/Au
Top Electrode	Si/Cr/Au

Table 2.2: Material selection for the microfabricated CMUT array.

2.2 Design Parameters for Main Components

Microfabrication of the CMUT array chips is the main objective of this study. However, other components such as laser fiber, ASIC chips, PCB, and their connections have to be taken into account while designing the masks which are going to be used in the microfabrication of the CMUT array chips. Design parameters for main components and their influence on the mask will be explained in the following sections.

2.2.1 Laser Fiber Hole

In photoacoustic imaging, imaging systems commonly use separate light sources, and transducers [64], [65]. In some cases, these devices can be inconvenient to use due to their bulky structure, since there may not be suitable surface area on the patient's body for a detector and a separate light source. Furthermore, it may be desirable to combine the laser fiber light source and the transducers to make the imaging system more compact.

In this work, a 12×12 CMUT array area is subtracted from a 20×20 CMUT array area to create a reserved area for a laser fiber hole that enables the integration of fiber light source and CMUTs in a compact unit. As a result of the arrangement between transducers and a light source, the total size of the probe can be minimized [66]. Furthermore, there is no need for alignment or co-registration between

the transducer and the light source during image formation due to pre-aligned configuration of the CMUT array and laser light source.

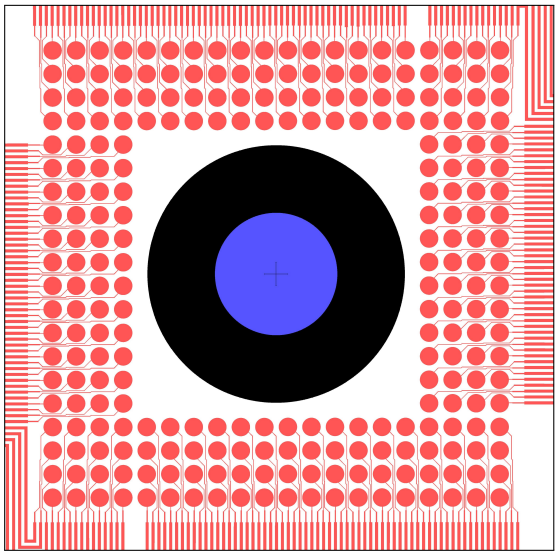


Figure 2.1: The blue region represents the actual laser fiber area, and the black region is the tolerable area for possible damage during and after hole opening. Possible destruction beyond the borders of the black region after hole opening is not acceptable.

Reserved space for laser fiber hole is demonstrated in Figure 2.1. The reserved space is placed exactly into the middle of the subtracted 12x12 CMUT array. The blue region indicates the laser fiber hole, which has a 0.5 mm radius. The black region is the region that does not have any CMUT circles inside and is kept broad on purpose to prevent CMUTs from residuals that may have come from laser drilling or mechanical drilling of Pyrex.

Formation of a hole though Pyrex can be done by using drilling, laser ablation, or etching. Furthermore, due to low light absorption and high transmittance of Pyrex, which can be seen in Figure 2.2, a laser fiber light source may be used without opening a hole through the Pyrex chip.

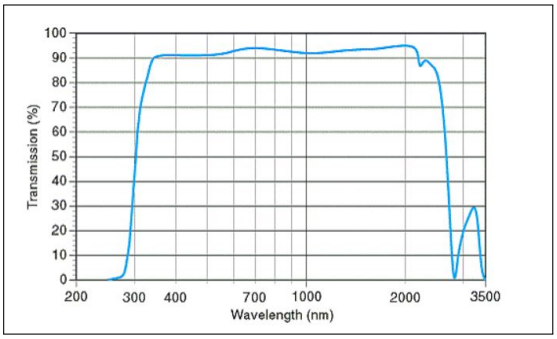


Figure 2.2: Transmission curve of Pyrex glass [67].

2.2.2 ASIC (Application Specific Integrated Circuit)

The CMUTs loose important signal-to-noise ratio (SNR) due to high input impedance caused by long cables that are used to connect CMUTs to hardware. Combining the transducer array with integrated circuits (ICs), which are low noise amplifiers, within the probe and enhance the signal before connecting to the cables, is one solution to this problem [3]. A close connection between an IC and a transducer array reduces parasitic capacitance and removes the need for a bulky cable [39].

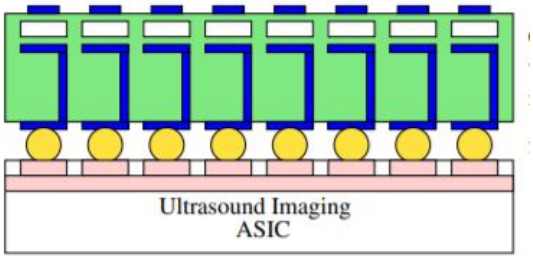


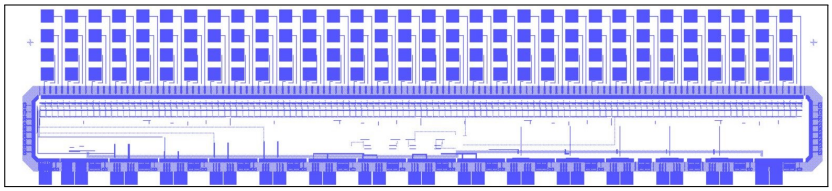
Figure 2.3: Illustration of Flip-Chip bonding process [3].

For a long time, multi-chip integration has been used to link CMUT arrays to electronics. The electronics and the CMUT array are designed separately and then connected using a range of integration techniques which can be seen in Figure 2.3, including flip-chip bonding with solder reflow [68], gold stud bumps [69], anisotropic conductive films (ACF) [70], and thermo-compression bonding [71].

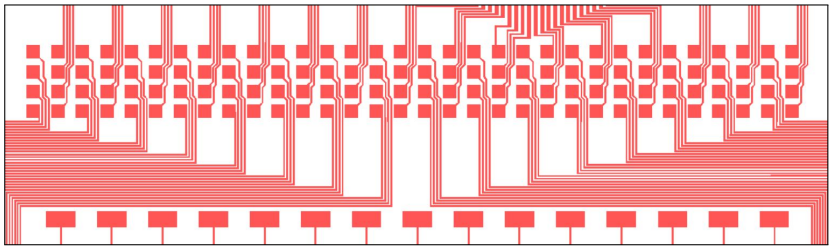
In this study, the bonding process is planned to be made using flip-chip bonding between CMUT arrays and ASICs. One ASIC has a total of 143 metal pads (128 CMUT input pads, and 15 output pads for ASIC to PCB connections on CMUT array chip), and our design needs at least 2 individual ASIC chips for best imaging performance. Wang et al. (2012) and many others suggest that 80 g/bump to 50 g/bump is the optimal force/bump in the flip-chip bonding processes. Furthermore, according to the literature this force range provides minimal bump deformation, and good bonding strength [72]. Assuming these force values per bump, for the bonding of 143 elements to the CMUT chip, the flip-chip bonding device should apply 11440 g/ASIC to 7150 g/ASIC force in total. However, that much force exceeds the capabilities of the flip-chip bonder tool in our fabrication facility.

To overcome the insufficient force/ASIC situation described in the earlier paragraph, CMUT pads that provide connections to ASICs are designed so that at most 4 ASIC chips may be used for flip-chip bonding connection of 64, 128, and 256 CMUT elements. This approach is expected to eliminate the total force/ASIC limitation of the flip-chip bonding device and allow bonding CMUT elements located in desired places. However, even if the force/bump requirement is satisfied, there are still challenges that needs to be overcome because a flip-chip bonding tool may use ultrasonic vibrations or thermo-compressive loading for bonding, which may decrease the strength of bonding between the first CMUT-ASIC pair while processing the second CMUT-ASIC pair.

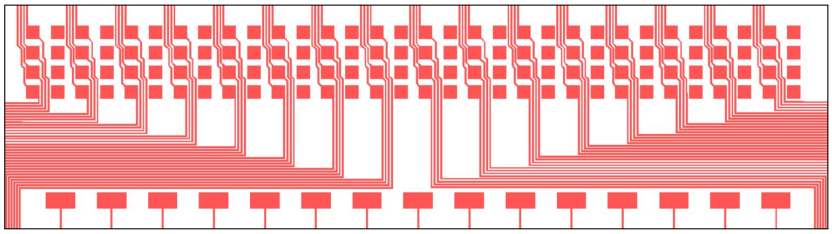
In the following sections, possible scenarios for CMUT-ASIC flip-chip bonding are explained. Figure 2.4a shows the ASIC chip layout drawing. Figure 2.4b and Figure 2.4c show the CMUT pads for CMUT-ASIC flip-chip bonding process. CMUT pads in Figure 2.4b are the main CMUT pads, and the CMUT pads in the 2.4c are the supplementary pads that are going to be used in the scenarios that need more than 2 ASICs (in other words, less force/ASIC). These pad areas are designed to be used as metal wirings if the bonding is accomplished using only 2 ASICs.



(a) Top view of ASICs.



(b) Main CMUT pads for ASICs to CMUT device connections.



(c) Supplementary CMUT pads for ASICs to CMUT device connections.

Figure 2.4: ASIC layout and electrical connection pad layout drawings for a CMUT device. Locations of these connection pads on the chip size CMUT array can be seen in Figure 2.5.

2.2.3 128×2 CMUT-ASIC Connections (2 ASIC chips with 128 connections per ASIC to 1 CMUT chip with 256 connections)

2 ASIC chips, with 128 pad connections on each ASIC chip, to 1 CMUT chip with 256 pads connection approach is the ideal scenario for our work in terms of imaging quality and resolution. In this scenario, all the 256 CMUT pads are connected to corresponding 2 ASIC chips with 128 pads on each ASIC chip. In

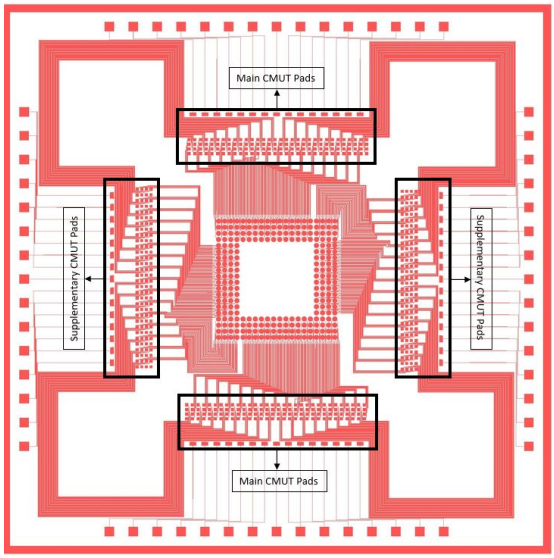


Figure 2.5: Locations of main CMUT pads and supplementary CMUT pads on chip size CMUT array.

this case, 2 ASICs are necessary for flip-chip bonding. However, all the CMUT-ASIC pads per flip-chip bonding process, which are 256 in total, must be in contact, which significantly challenges the force/bump capabilities of the flip-chip bonding tool. Figure 2.6 shows the used CMUT pads for flip-chip bonding process.

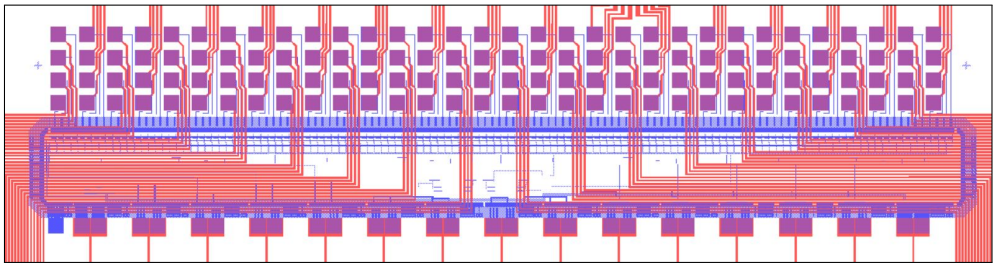


Figure 2.6: A view of a CMUT-ASIC pair with 128 pads for flip-chip bonding.

In this scenario, supplementary CMUT pads behave as metal wiring. Figure 2.7 and Figure 2.8 show the electrical conduction path of a specified CMUT cell.

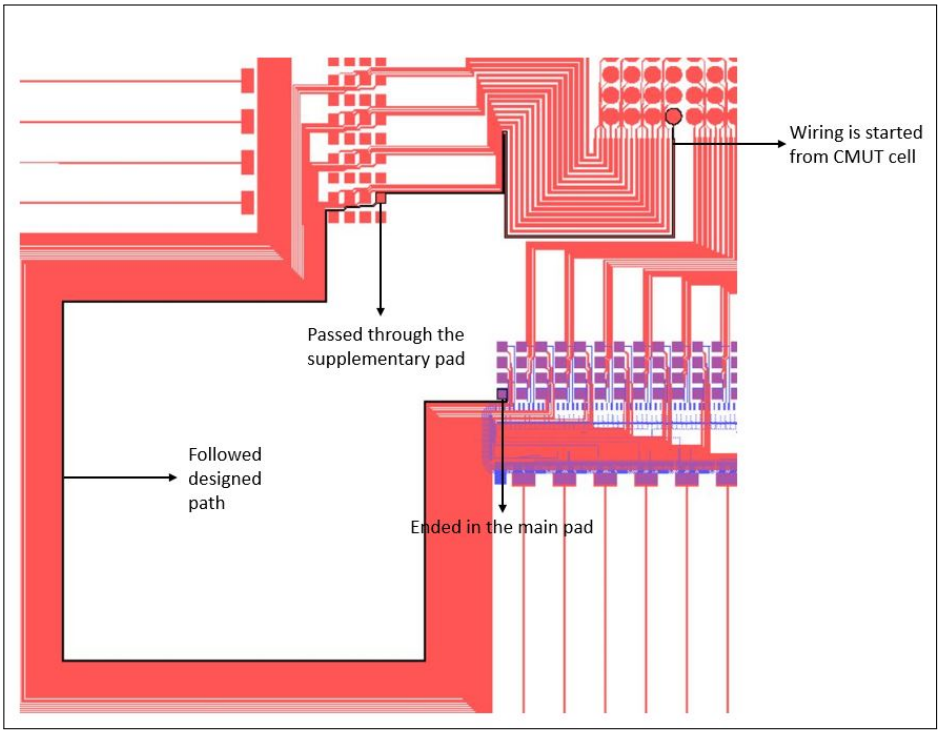


Figure 2.7: The path of wiring between CMUT cell and CMUT main pad using supplementary CMUT pad.

2.2.4 64×4 CMUT-ASIC Connections (4 ASIC chips with 64 connections per ASIC to 1 CMUT chip with 256 connections)

This is the second most desirable CMUT to ASIC connection scenario for our work. In this scenario, only half of the CMUT pads are connected to corresponding ASIC pads. The CMUT pads to be used must be selected manually in the ball bumping process before the flip-chip bonding process. In this case, 4 ASIC chips are necessary, and 64 pads from each ASIC should be in contact with a total of 256 CMUT pads after the completion of the 4 flip-chip bonding processes. In terms of image quality and resolution, this scenario is similar to the ideal case. Furthermore, there is an advantage in terms of the total force needed per flip-chip bonding of an ASIC chip to CMUT chip because the number of necessary pad connections per ASIC chip are reduced by half. Figure 2.10 and Figure 2.11 show the used CMUT pads for flip-chip bonding process.

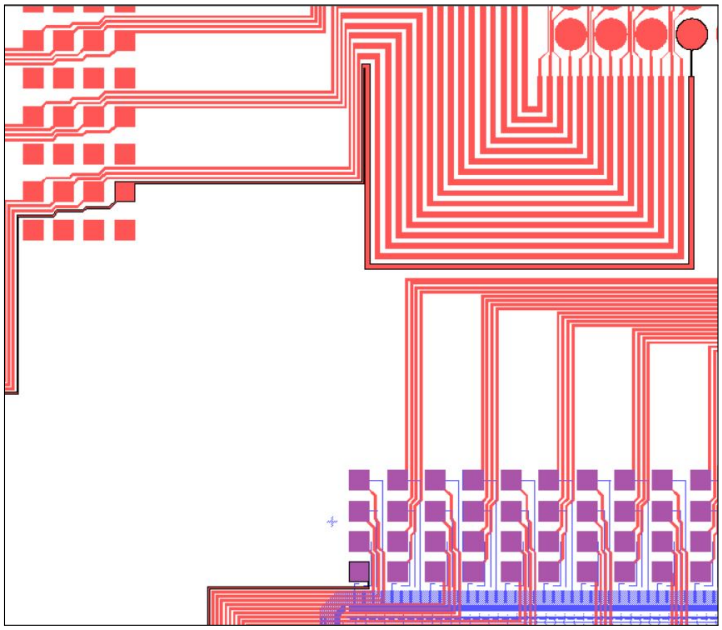


Figure 2.8: Magnified version of Figure 2.7.

2.2.5 64×2 and 32×4 CMUT-ASIC Connections

These are the scenarios that need the least amount of flip-chip bonding pad connections for each CMUT-ASIC pair. These are half of the 128×2 CMUT-ASIC connections and half of the 64×4 CMUT-ASIC connections which are explained in the previous sections, above. The essential matter in these approaches is that, half of the main CMUT pads and supplementary CMUT pads should be picked for the ball bump bonding process manually before doing flip-chip bonding. In these scenarios, while the possibility of successful flip-chip bonding processes is increasing due to reduced amount of total force per flip-chip bonding process, a compromise is done about the imaging quality and resolution.

2.2.6 Printed Circuit Board (PCB) Connections

Individual connections of inner CMUT elements to electronics pose a significant challenge. To overcome these connection challenges, ASICs are used. ASICs are used to reduce the number of bonding pads and enable the connection process

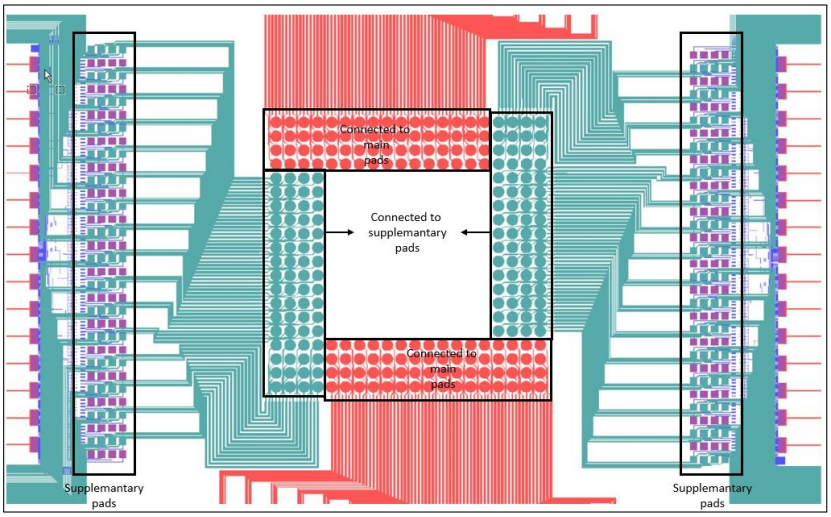


Figure 2.9: Half of the CMUT elements are connected to main CMUT metal pads, while the other half are connected to supplementary CMUT metal pads.

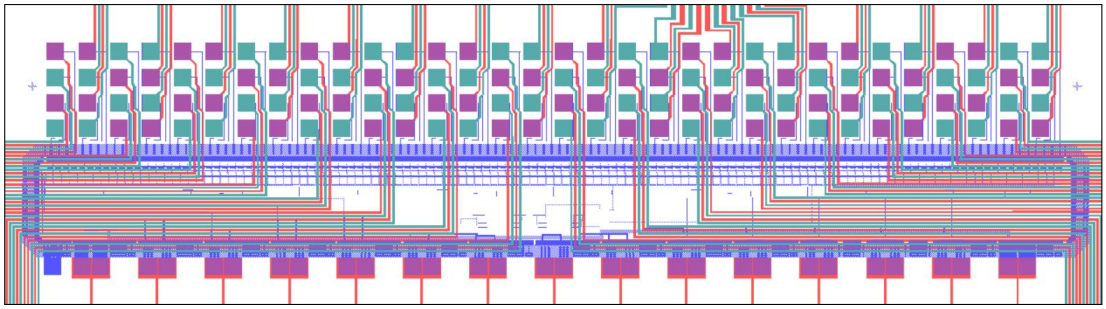


Figure 2.10: 128 pads are available for flip-chip bonding of CMUT-ASIC pairs. In the "reduced by half" pad connections scenario, half of the pads should be chosen manually for ball stud bumping before doing the flip-chip bonding with reduced number of pad connections.

between the PCBs and CMUT array device. PCB connections are located at the edges of our CMUT chip design, and PCB connections will be made by using a stencil and conductive paste. Due to the perforated structure of PCB design, which is shown in Figure 2.12, the PCB protects the CMUT chip from falling while allowing the laser fiber light to reach the phantom surface and ultrasonic signals reach back to the CMUT array.

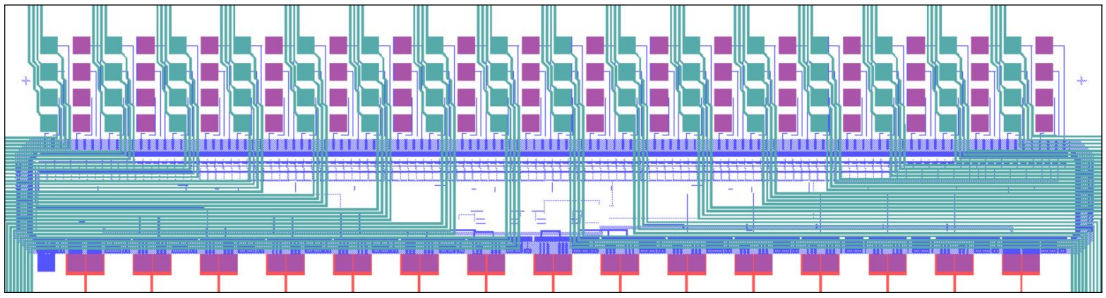


Figure 2.11: 64 pads are available for flip-chip bonding of CMUT-ASIC pairs in the supplementary pad area.

2.3 CMUT Fabrication Process Flow

2.3.1 Design Of Masks

In this study, 3 different main masks and one supportive mask were designed and manufactured for the photolithography and patterning processes. The first mask is used for cavity formation and bottom electrode metallization inside the Pyrex. The second mask is used for the alumina etching process from the intended areas only, such as metal contact pads on Pyrex substrate. The third mask is planned to be used for patterning the vibrating plate Si device layer in the silicon etching process. One supportive photolithography mask is used for simplified lift-off process after metal deposition. Initially, the first lithography mask is designed. After the first lithography mask, the second mask, and the third mask were built upon the first mask.

Also, a shadow mask that is cheaper than a soda lime chrome mask is to be used for the formation of top electrode wire bonding pads on Si device layer. These shadow mask deposited wire bonding pads will be responsible for the electrical connection between PCB and Si device layer of CMUT chip.

During the design of the first lithography mask, the 256 CMUT array elements, designed with the reserved space for laser fiber, are placed in the middle of the Pyrex chip. After that, wires between ASIC pads and CMUT pads are constructed. To ease the integration process of CMUT chip and PCB, pad electrodes

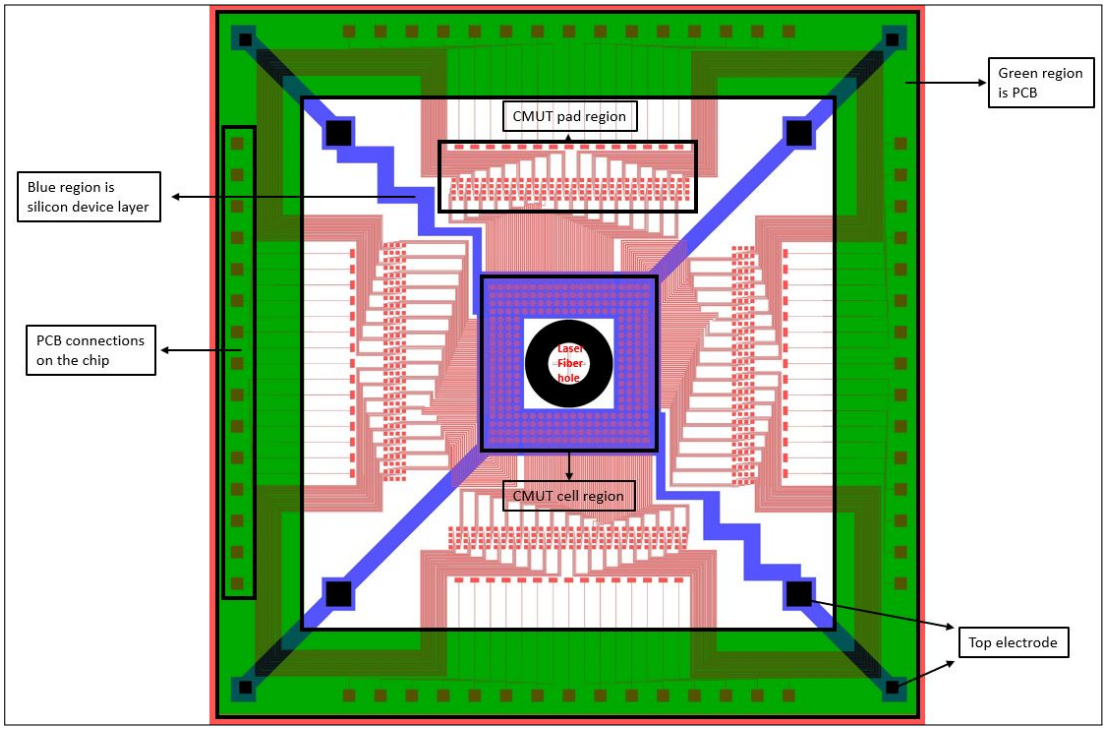


Figure 2.12: PCB-CMUT integration using a stencil and conductive paste.

on PCB and pad electrodes at the edges of CMUT chip are determined to be 0.5 mm x 0.5 mm. These pad electrodes on PCB and pad electrodes at the edges of CMUT chip are going to be connected using a stencil, conductive paste and flip-chip bonding approach with manual alignment.

Placement of CMUT array cells is followed by fanning out of wires that come from CMUT array cells to ASICs and from ASICs to electrical pads of PCB. Since the CMUTs are designed as 12×12 CMUT array subtracted from 20×20 CMUT array elements in a square manner (shown in Figure 2.13), connection wires of inner and outer cells on the CMUT array should be carefully designed for proper connections to ASIC chips.

In our design, there are four consecutive CMUT cells at one line, which means that the wiring line and space design may be composed of three wires between two neighboring CMUT cells, and that resulted in four spacings between two neighboring CMUT cells which can be seen in Figure 2.14. Here, the line and spacing design is not possible to have less than three wires and less than four

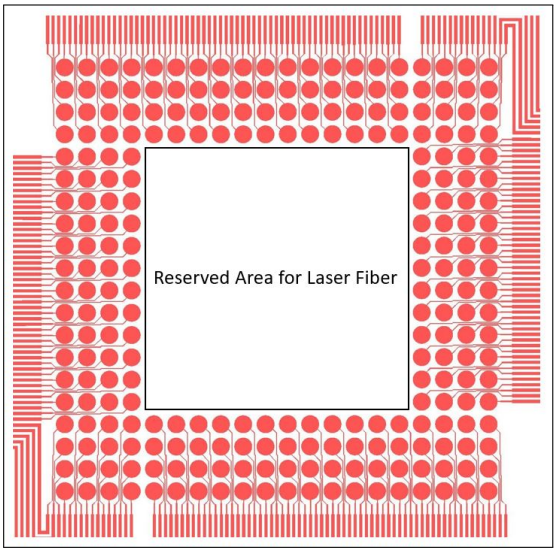


Figure 2.13: 12×12 CMUT subtracted from 20×20 CMUT elements in a square array pattern.

spacings. While it may be possible to have more lines and spacings, more lines and spacings brings manufacturing complexity for lithography and metallization as well as anodic wafer bonding of these dense line and space regions especially between the outermost two neighboring CMUT cells. Due to the line-width limitation for the wires inside the two consecutive cells, we decided to use 5 μm wires with 6.75 μm spacings. Hence, the separation between two consecutive cells is chosen to be 42 μm.

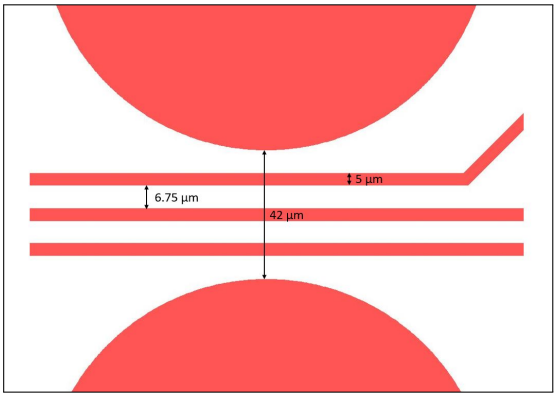


Figure 2.14: Dimensions of wires and spacings and separation between two consecutive cells.

2.3.2 CMUT Gap Formation

Surface cleaning of Pyrex wafer with acetone, isopropanol, and diluted water are the first steps of the entire fabrication process. Cleaning of the Pyrex wafer is followed by 50 nm chrome deposition by an e-beam evaporation. 50 nm thick chrome is used as a hard mask and adhesion layer, which is essential for further steps such as, isotropic BOE (Buffered Oxide Etch) etch on Pyrex, and platinum e-beam evaporation in the Ti/Pt/Au bottom electrode stack deposition. During BOE etching, BOE may penetrate faster from the photoresist and Pyrex wafer interface. Furthermore, platinum evaporates at very high temperatures, which causes deformation on the photoresist geometry and delamination of the photoresist from the Pyrex substrate. With the help of 50 nm thick chrome adhesion layer, we aimed to avoid these problems and preserved our defined structure during BOE wet etching and in high evaporation temperatures [73].

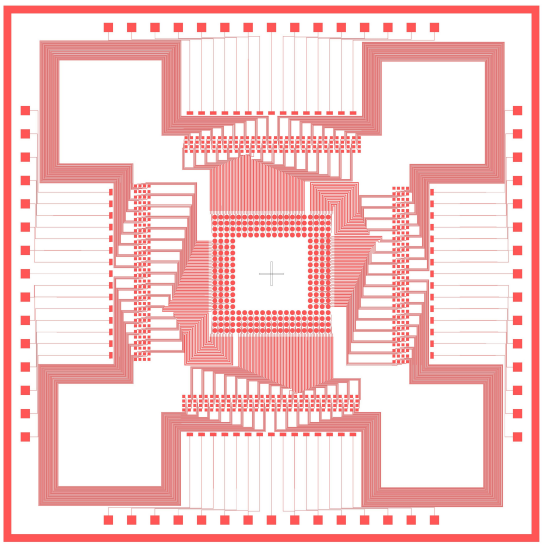


Figure 2.15: Chip size drawing of cavity formation mask.

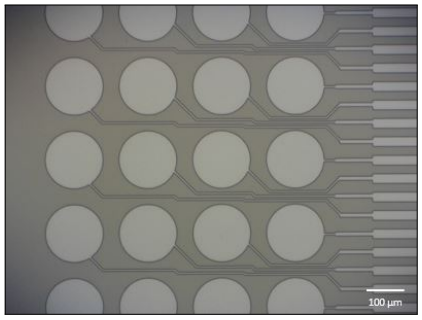
After 50 nm thick chrome deposition on Pyrex, photolithography is used for defining the structure. AZ4562 positive tone photoresist (Ulm, Germany) is spin-coated over 50 nm thick chrome surface at 6000 RPM, which gives close to 5 μm thick photoresist according to the technical datasheet of AZ4562. The thickness of the photoresist is decided by taking into account the thickness ratio between the smallest features in the mask and e-beam deposition of Ti/Pt/Au bottom

Figure 2.16: A photograph of the used cavity formation mask during microfabrication process.

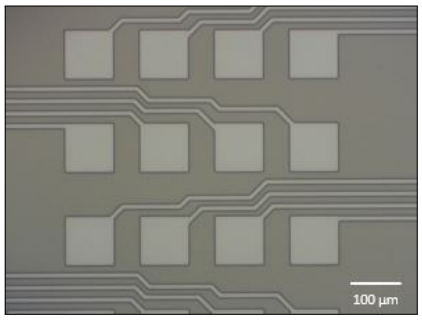
electrode metal stack. Photoresist should be thick enough to allow lift-off process after the deposition of Ti/Pt/Au bottom electrode metal stack. After spin-coating of the photoresist, UV exposure is the next step in the process. For UV exposure, 150 mJ/cm^2 is found to be the optimum exposure energy flux, while vacuum and hard contact modes are used because of the small feature sizes of the lines and spacings at the most dense line/space regions between two neighboring CMUT cells. UV exposure is done by EVG 620 mask aligner system (St. Florian, Austria) using the cavity formation mask shown in Figure 2.15, and Figure 2.16.

Development of UV exposed photoresist is completed in 3 minutes by using 1:4 diluted AZ400K developer from Microchemicals. Oxygen plasma by Inductively Coupled Plasma (ICP) equipment is done to ensure that all the unintentionally remaining photoresist residues are removed from the developed areas of the wafer.

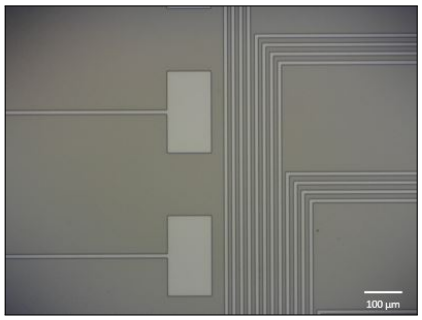
After the photoresist is completely removed from the developed areas, the cavity inside the Pyrex substrate will be formed for the deposition of the bottom electrodes. Before the cavity formation, chrome should be removed from intended regions. Argon plasma by ICP is used for the anisotropic etching of the chrome.



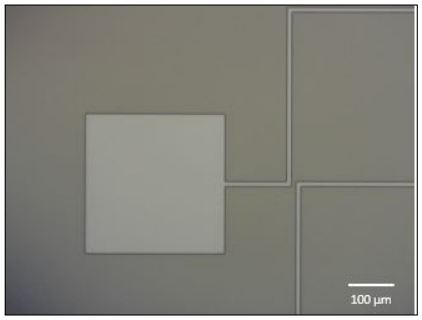
(a) CMUT cell region.



(b) Metal pad region.



(c) ASIC pad region.

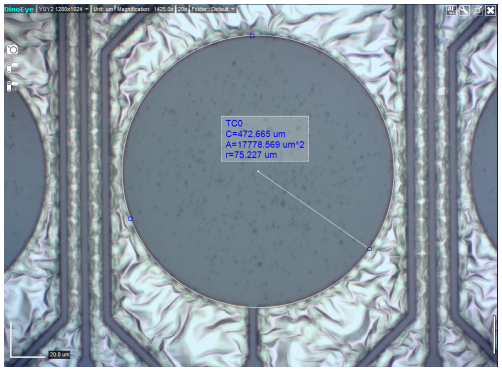


(d) PCB pad region.

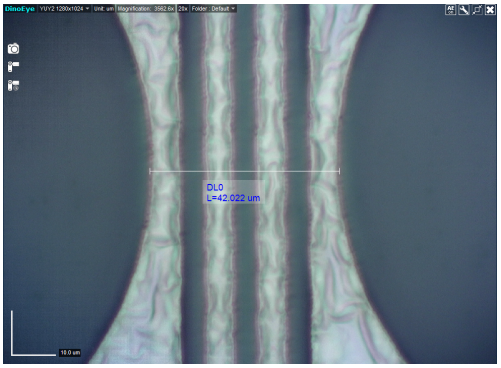
Figure 2.17: Microscope images from different regions of the CMUT chip after the lithography process is done.

Overetching and non-uniform Cr etching with Argon plasma in the ICP chamber causes further undesired etching in Pyrex. To compensate for this undesired etching, depth of cavity due to undesired argon plasma etching is measured by using a stylus profilometer on an expendable process test wafer. The depth caused by this additional undesired non-uniform etching in the ICP process chamber by argon plasma resulted in approximately 250 nm depth. This depth is taken into account in the final depth formation inside the Pyrex cavities.

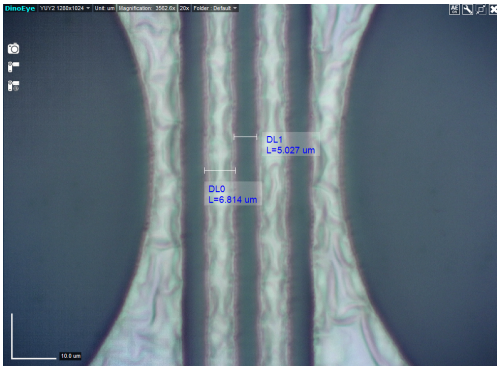
Maintaining low resistance on the wires that are connecting CMUT cells to ASIC electrical pads have a crucial role. To have low resistance wires, 500 nm gold, 100 nm platinum, and 100 nm titanium will be deposited in the Pyrex cavity. To have a 700 nm metal stack electrode and 150 nm gap, an 850 nm deep cavity should be formed into a Pyrex wafer before the metal stack is deposited. As stated before, the process test wafer had approximately 250 nm deep cavities in Pyrex due to non-uniform Cr etching. However, that gap height is not the same



(a) CMUT cell dimension after ICP argon plasma and hard baking.



(b) The separation between two consecutive CMUT cells after ICP argon plasma and hard baking.



(c) Dimensions of wires and spaces after ICP argon plasma and hard baking

Figure 2.18: Dimensions of wires and spaces after ICP argon plasma and hard baking.

all over the wafer. The cavity depth is changing from 210 to 290 nm between inner to outer devices. To get an additional 600 nm deeper gap formation, first, anisotropic plasma etching in ICP chamber (by using a plasma composed of SF_6 and argon) is used. After dry etching, isotropic wet etching (with buffered oxide etch (BOE)) is used to obtain clean and smooth Pyrex surface.

Isotropic wet etching feature of BOE and remaining residuals after ICP of Pyrex wafer are the main reasons for sequential usage of both BOE and ICP on Pyrex wafers. BOE can etch 600 nm deep cavities in Pyrex in approximately 30 minutes, however, due to its isotropic etching nature, BOE also etches (in other words, undercuts) the sidewalls of wires, and this undercut may result in undesired lifting off of the chrome adhesion layer (and hard mask) and the photoresist

sitting on this chrome thin-film, especially at the dense line and space regions between CMUT cells. As a result, BOE wet etching is done as short as possible (i.e., approximately 7 minutes) in this process. However, BOE wet etch is also required in this processing approach because following a plasma etch with ICP tool, undesired surface residues are formed on the plasma etched surfaces, and BOE wet etch is used to remove those undesired surface residues. Furthermore, timed BOE etch forms controlled deeper undercuts under the chrome hard mask, allowing more accessible and precise lift-off process after metallization.

Between Ar plasma chrome etching in ICP and BOE processes, the wafers were hard-baked for 1.5 hours at 110 °C and then for 3 hours at 150 °C. The reason for that hard baking procedure is to have a properly hardened photoresist profile during the e-beam evaporated metallization process that happens in high temperatures, especially during platinum evaporation. The leftover photoresist solvent is removed during the hard bake process, which enhances adhesion between the photoresist and the material in direct contact with the photoresist, enhances chemical stability of the photoresist, and makes the photoresist more selective during SF_6 ICP plasma processing and BOE wet etching. Furthermore, this had baking approach also protects the geometrical structure of CMUT cells in the e-beam evaporation process, especially at the high-temperature Pt evaporation step.

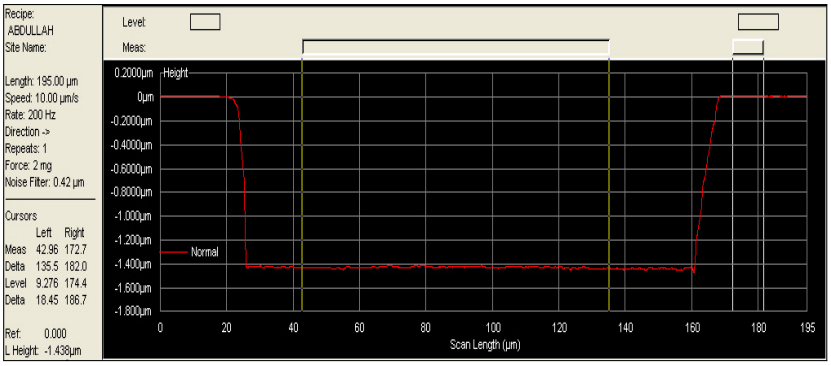


Figure 2.19: Stylus profilometer measurement of Pyrex chip after ICP argon and SF_6 plasma with the initial base recipe. Height difference is measured as 1438 nm

Firstly, a previously developed recipe from our research group is used for dry

etching. However, due to the unstable nature of the cleanroom environment and process equipment, the previously developed process recipe etched more than the aimed gap depth, which can be seen in Figure 2.19. After several trials with test wafers, the approximate material removal rate of the plasma etching recipe is measured to be 8.8 nm/min. Thus, for about 400 nm more deep etching, 45 minutes of processing is done with the same recipe, and 650 nm gap height is achieved after the processing as shown in Figure 2.20.

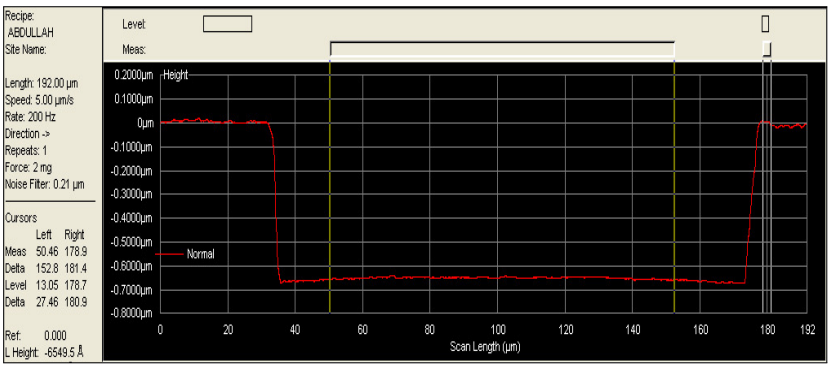


Figure 2.20: Stylus profilometer measurement of Pyrex chip after ICP argon and SF_6 plasma with the updated recipe. Height difference found as 654 nm.

Secondly, BOE wet etching is used for the remaining 200 nm etching step. Expendable wafer test pieces were dipped into BOE solution for 5, 10, and 15 minutes to calculate the BOE etch rate. From this etch rate calculation approach, wet etch rate of BOE is determined to be about 23 nm/min at the time of the etch rate calculation approach. After etching rate calculation, one of the expandable pieces is dipped into BOE, this time for the calculated amount of time. After stylus profilometer results confirmed that the calculated etch time is enough for the aimed gap depth, the process is continued with the BOE wet etching of real CMUT array device wafers. The gap height after timed BOE is shown in Figure 2.21.

It is important to note that, each BOE wet etch process is done by keeping concise time intervals between all the BOE processes due to the difficulty of controlling variations in BOE etching processes. This way, differences between fabricated devices and the etch rate differences between wafers are minimized as much as possible.

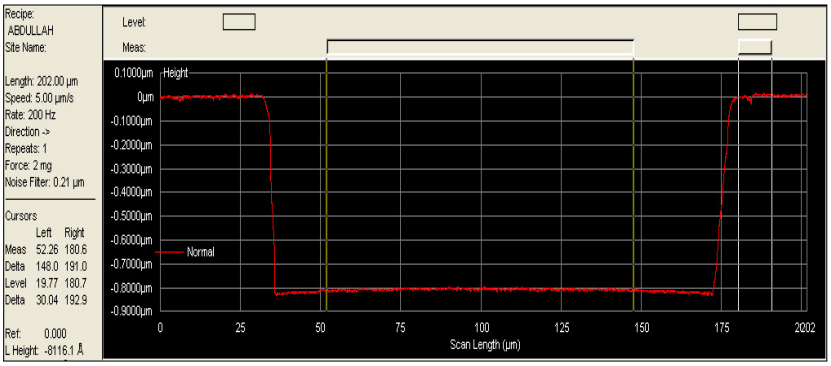


Figure 2.21: Stylus profilometer measurement of Pyrex chip after BOE etch. Height difference found as 811 nm.

2.3.3 Bottom Electrode

As mentioned before, 100 nm of Ti is used as an adhesion and getter layer, 100 nm of Pt is used as a barrier layer, and 500 nm of gold is used as a low electrical resistance layer. 500 nm of gold is also used to enhance the wire bonding and ball bumping processes, because the thicker the gold thin-film, the better the wire bonding and ball bumping processes are. 700 nm thick bottom electrode metal stacks are deposited into 850 nm cavity to achieve 150 nm gap height. This metal stack is deposited in MiDAS PVD e-beam evaporator tool (Ankara, Turkey).

Before deposition of the metal stack, the tooling factors for e-beam evaporation of each metal in the metal stack are calculated. First, initial thickness values for metals were intended to be 100 nm titanium, 100 nm platinum, and 500 nm gold. However, Focus Ion Beam (FIB) results showed that there are differences between the initial thicknesses of the metal films and the resulting thicknesses of the metal films. Secondly, new initial thickness values are calculated according to the resulting thicknesses of metal films measured by the FIB tool. Third, metals were coated on a test wafer to confirm the validity of thickness values by measuring the thickness values via FIB, which is shown in Figure 2.23. Finally, thin-film metals are deposited on actual wafers. During all these optimization, and batch-compatible micromanufactuting e-beam deposition processes, fresh (i.e. new, or not old) thin-film deposition monitoring crystals are used.

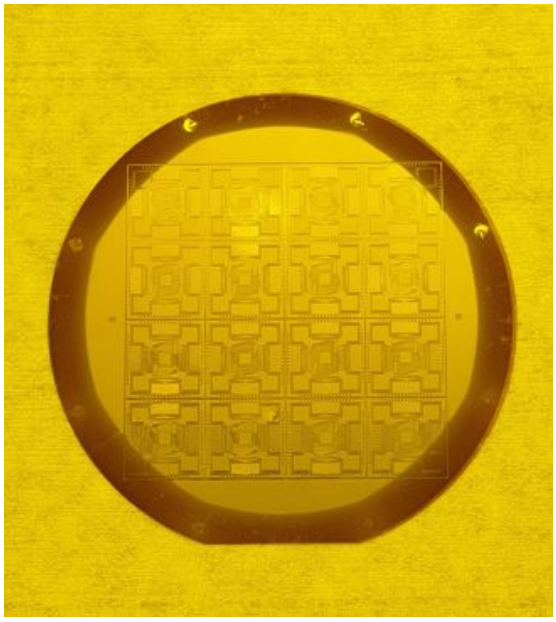


Figure 2.22: The image of manufactured wafer before the metallization step.

As mentioned above, the photoresist mask exists on the wafer surface during the e-beam evaporation process. To protect the photoresist from the high temperature that occurs while depositing platinum and gold, the vacuum chamber is left for cooling before and after depositing these metals.

Deposition is initiated after the chamber pressure reaches a minimum pressure of $2x10^{-}6$ Torr for each material. The adhesion between metal stack materials is also improved by not breaking the vacuum during the entire deposition process. Another concern for e-beam evaporation is deposition rates. High deposition rates cause residual stress in the films and interfaces between the films and substrate. Because of that, slow deposition rates are used. Titanium, platinum, and gold are deposited with deposition rates that did not exceed 1 Å/second for Ti, 1.5 Å/second for platinum, and 2.5 Å/second for gold. SEM images of the CMUT array and metal pad regions can be seen in Figure 2.25.

The lift-off process removes the sacrificial layer and the materials on top of the sacrificial layer to create metal stack patterns on the Pyrex wafer cavities. In our case, we used hardened AZ4562 photoresist as a sacrificial layer.

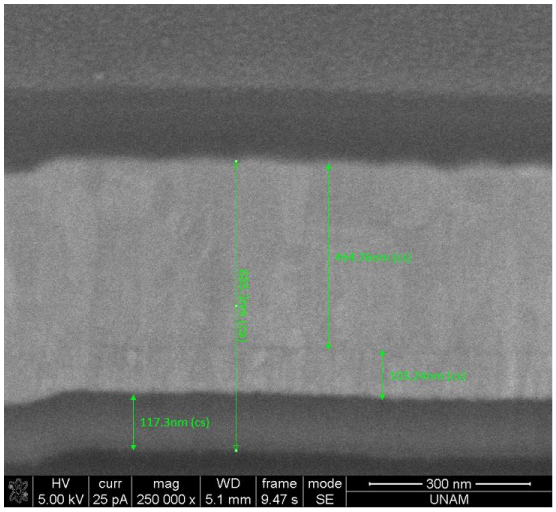
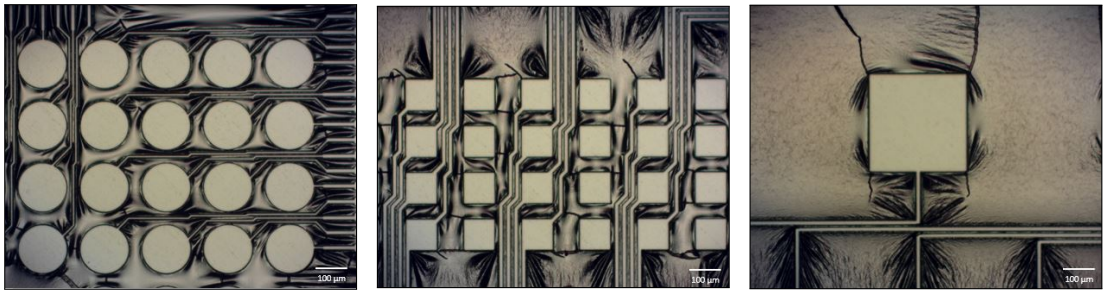


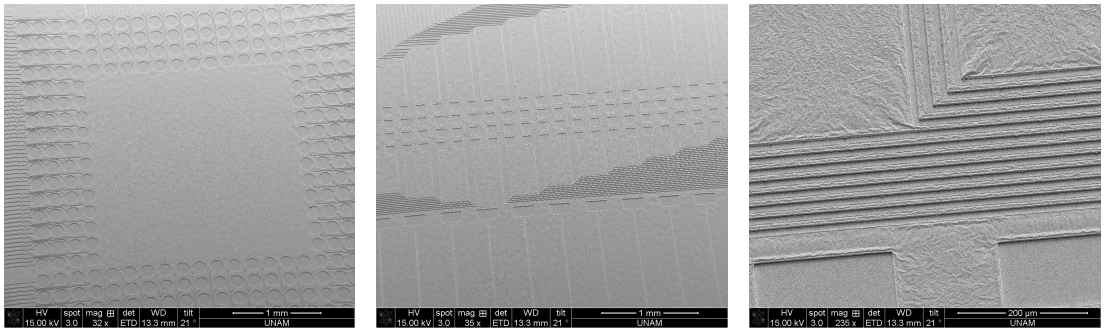
Figure 2.23: Focused Ion Beam (FIB) micrograph of the cross-section of the Ti/Pt/Au metal stack deposited on Pyrex wafer. Titanium thickness is measured as 117,30 nm, platinum thickness is measured as 103,24 nm, gold thickness is measured as 454,26 nm

Removal of the sacrificial layer hardened photoresist is done by piranha etchant because acetone alone is not sufficient to dissolve hardened photoresist. Furthermore, the initial lift-off trials showed that due to the very narrow entry regions for piranha etchant, removing sacrificial layer photoresists from these narrow entry regions requires long etch times. The image of these narrow entry regions is shown in Figure 2.26. Keeping the wafer in piranha etchant for an extended time etches the titanium, which is located under the Pt and Au stack. Undesired etching of Ti damages the integrity of the electrodes. To prevent bottom electrodes from



(a) CMUT cell region. (b) Small metal pad region. (c) Large metal pad region.

Figure 2.24: Microscope image of different regions on the wafer after deposition of Ti/Pt/Au metal stack.



(a) CMUT cell region. (b) Small metal pad region. (c) Connection wires.

Figure 2.25: SEM image of different regions on the wafer after deposition of Ti/Pt/Au metal stack.

extended time exposure to piranha etching, a large amount of Ti/Pt/Au stack is etched before the actual lift-off process by using an additional mask, which is shown in Figure 2.28. First and foremost, the lithography processes were applied to the Ti/Pt/Au deposited wafer. Aqua Regia solution, which is a mixture of one unit of nitric acid and three units of hydrochloric acid, diluted with two units of DI water, was used for gold and platinum etching while BOE was used in order to etch titanium [23].

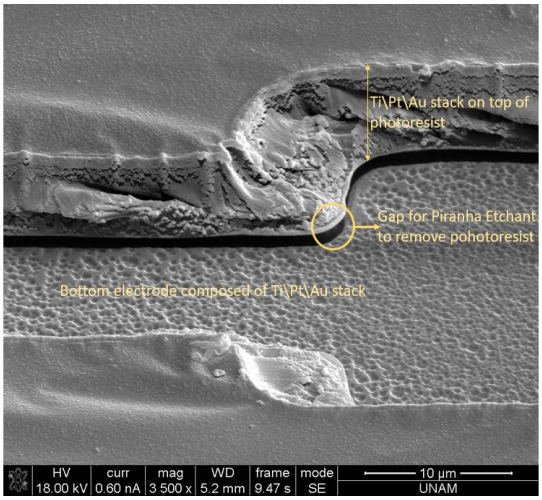


Figure 2.26: Entry regions for the piranha etchant to remove photoresist on top of the Pyrex surface to reveal bottom electrode.

The second stage of the lift-off process is the complete removal of the photoresist on the surface. As explained before, the photoresist is significantly hardened before the e-beam evaporation step. This hardening process made the photoresist

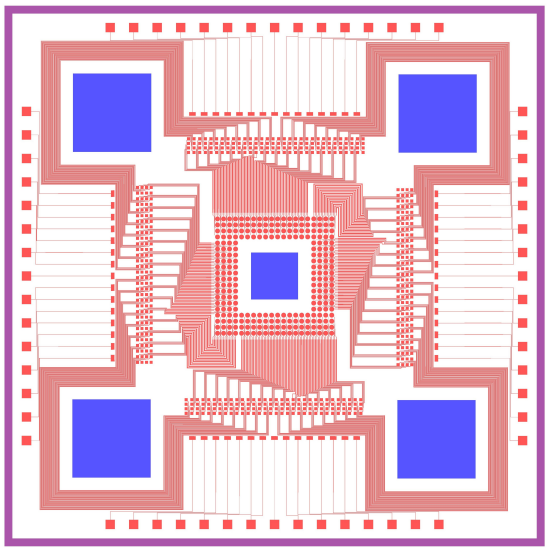


Figure 2.27: Chip size drawing of Metal Open mask on Cavity Formation mask (1st mask). Blue regions represent the metal openings and red regions represent the cavities.

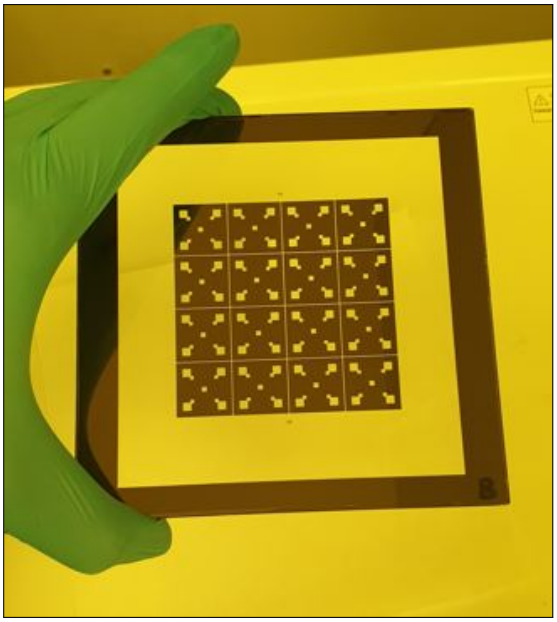


Figure 2.28: The image of used Metal Open mask during microfabrication process.

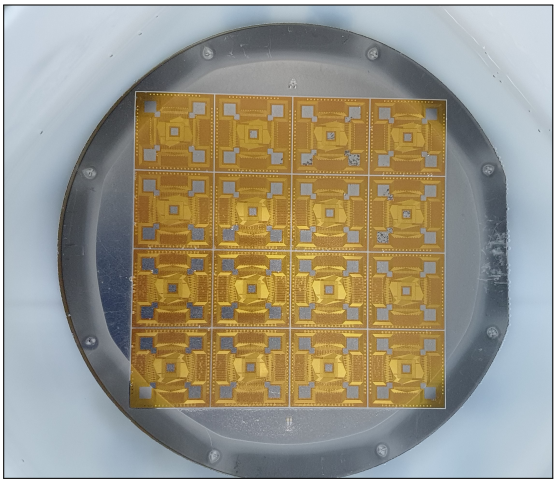


Figure 2.29: The image of the fabricated wafer using the Metal Open mask.

more resistant to acetone and prevented it from dissolving using acetone. Piranha is well known for etching organic materials and residues, including photoresists. For this reason, piranha wet etch was used to complete the lift-off process. But before the piranha process, acetone treatment of the wafer reduces the burden on piranha for the lift-off process. To prepare the piranha solution, three units of sulfuric acid (H_2SO_4) and one unit of hydrogen peroxide (H_2O_2) are used [23]. Putting the wafer into piranha solution results in lifting off the photoresist and Ti/Pt/Au stack on top of the photoresist. After lift-off process, the intended metal stack connections remain on the surface. Chrome wet etching is done after the complete removal of the photoresist from the wafer surface. Chrome wet etchant, CR-7 (Sigma-Aldrich, Taufkirchen, Germany), has high etching rates, and due to this property of CR-7, chrome removal from the wafer surface is done very rapidly. After chrome removal, gap height between the bottom electrode and the Pyrex surface is measured to confirm that the height difference is in the desired range.

2.3.4 Insulator Layer Deposition and Patterning

The undesired collapse of the silicon device layer (the top electrode of the CMUT array device) to the bottom electrode after the wafer bonding process may cause

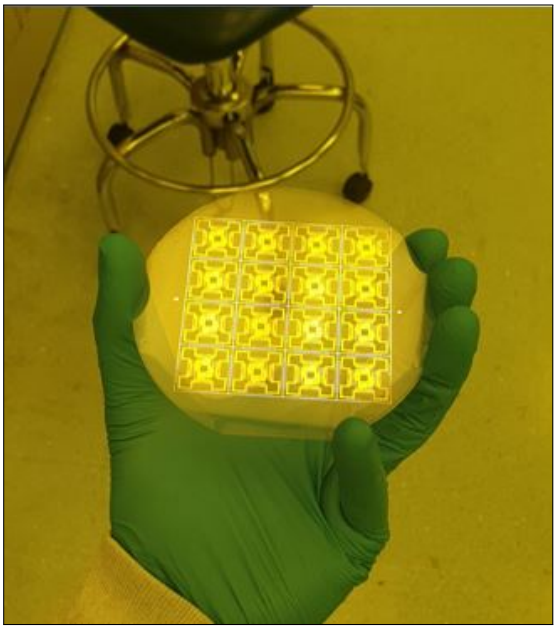


Figure 2.30: Image of the fabricated wafer after lift off process.

short-circuit during the operation of the CMUT array device. To prevent such short-circuit behavior, an insulator layer is conformally coated on the whole wafer and etched from the metal pad areas only. Alumina (Al_2O_3) is deposited by conformal thermal atomic layer deposition to make sure that the gap height between the bottom electrode, and the wafer bonded silicon device layer surface is kept as it is before the atomic layer deposition. ALD Savannah Thermal ALD equipment (Veeco, Plainview, NY) is utilized with an alumina deposition recipe. Each deposition cycle deposits 1.005 Angstrom of the alumina layer. The needed insulator thickness was given as 150 nm for this study. Thus, 1500 cycles of deposition were enough using the above method, which takes around 7 hours to complete. However, thickness measurements of the deposited alumina showed that the deposition rate is 20 percent less than the expected value. To compensate for this, the number of deposition cycles are increased by 25 percent from 1500 cycles to 1875 cycles.

Etching the alumina only from the desired locations on the substrate is the next step after alumina deposition. Alumina that is deposited on the metal stack pads should be removed to have electrical contact during the flip-chip bonding of ASIC to CMUT chips, and manual flip-chip bonding of CMUT chips to PCB

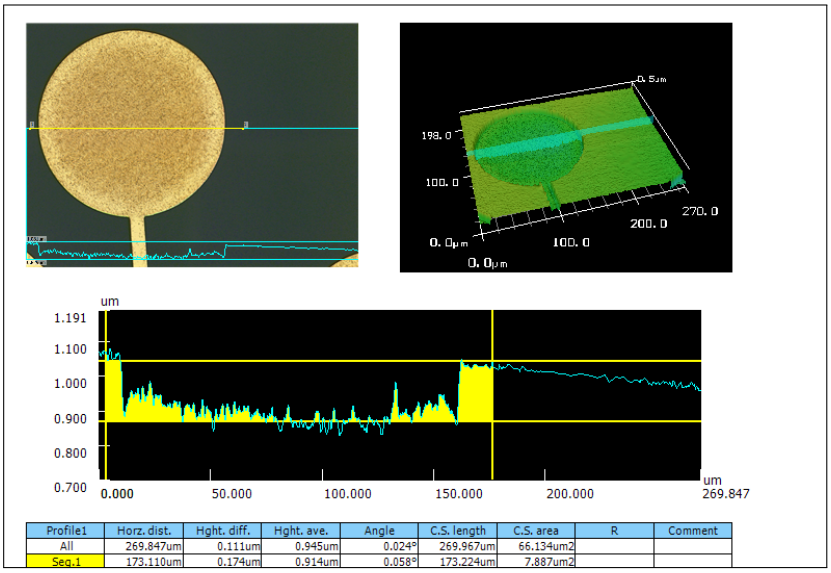


Figure 2.31: Keyence VK-X100 analysis of single CMUT cell. It shows that the gap height is approximately 150 *nm* as expected.

processes. In other words, the alumina insulator should be etched from these areas to maintain electrical connectivity between metal pads, ASICs and PCB. Alumina also should be etched from the fiber hole area for further processes. Alumina etch mask, which is the second main mask in this project, is used for this purpose. One unit of AZ400K developer that is diluted with four units of DI water that is regularly used for developing AZ4562 photoresists, was used to etch alumina. To make a precise etching, etch rate of diluted AZ400K is experimentally calculated. Calculations showed that this wet etching procedure takes about two hours for 150 *nm* thick alumina. Utilizing just a photoresist as a mask for this much long alumina etching process results in alumina etching over unintended areas. For this reason, before alumina wet etching, chromium is deposited on the surface of alumina and used as a hard mask. Chrome wet etch is used to remove the chrome from the electrical pad connecting sections after the photoresist have been developed. After the chrome wet etching and alumina wet etching processes are completed, metal pad conductivity is measured by using the resistance measurement function of a Keithley 4200A-SCS Parameter Analyzer. Results in Figure 2.36 have shown that alumina was removed from the metal pad areas.

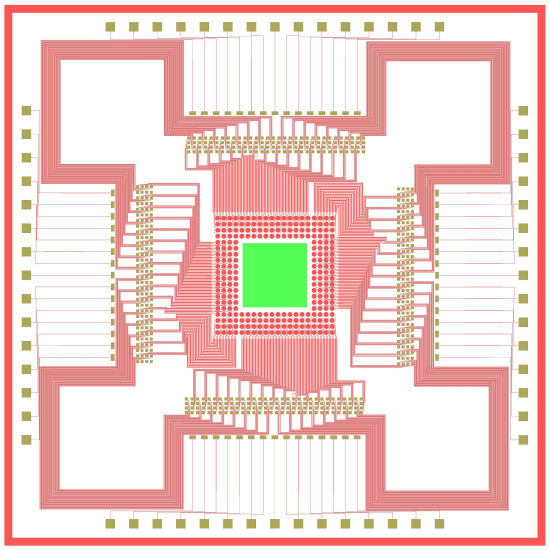


Figure 2.32: Chip size drawing of Alumina Etch mask (2nd mask) on Cavity Formation mask (1st mask) in Layout Editor. Green regions were etched to maintain electrical conductivity between metal pads.

It may be important to state that, any leftover photoresist is removed with acetone in the firstly developed process steps; however, due to the long interaction between AZ400K and the photoresist during the alumina etch process, acetone could not remove the photoresist on the dense electrical pad regions on the wafer surface. This observation is shown in Figure 2.34. The photoresist residues are not entirely removed from the surface after the cleaning with acetone. Because of this reason, to overcome the photoresist residue issues, we changed the integration process and removed the photoresist on the chrome layer before the alumina etch process. However, we found out that the very small amount of KOH inside the AZ400K solution that is used for alumina etch, also etches the chromium layer [23] very slowly, or AZ400K solution penetrates though the grain boundaries in the Cr hard mask layer resulting in damaging alumina surface below Cr hard mask. The AFM surface topography results showed that random holes on the alumina surface, that are already protected with Cr hard mask, are created during the alumina etching process. Because of that, we concluded that the photoresist should be hardened before the alumina etch process and must be on top of the chrome hard mask layer while etching the alumina from the intended areas. AFM surface topography measurement showing the roughness on the alumina surface

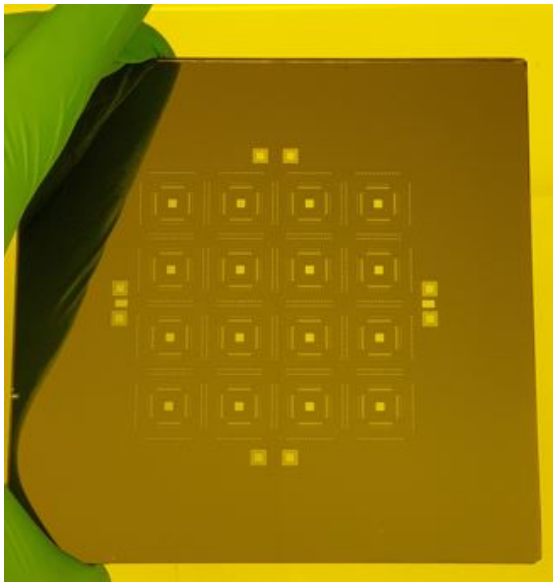


Figure 2.33: The image of used Alumina Etch mask during microfabrication process.

can be seen from Figure 2.35. To overcome these issues, we cleaned the wafer surface with AZ100 Remover instead of acetone in the following trials, and that procedure solved this problem. After completion of the alumina open, the chrome hard mask layer is etched using CR-7 chrome wet etch.

Finally, except for the electrical connection pad regions, the alumina insulator layer became the surface layer on the Pyrex wafer. The image of etched areas is shown in Figure 2.37. After microscopic inspection, alumina thickness is measured by the stylus profilometer. Results (Figure 2.38) showed that deposited alumina is 150 nm as expected. To ensure that alumina is fully etched from all over the metal pad areas, the resistance of the metal pads is measured by a Keithley 4200A-SCS Parameter Analyzer. Results showed that alumina fully etched from the metal pads and resistance is around 7.63 ohm between the probe tips. The current and resistance graph for this measurement is demonstrated in Figure 2.36.

At this stage of the integration process, wafer pairs are ready for anodic wafer bonding processing. Before the anodic wafer bonding process, an Atomic Force Microscope (AFM) device is used to measure the roughness of the alumina-coated

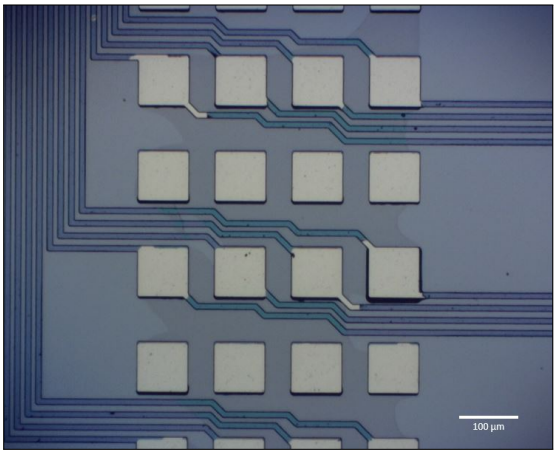


Figure 2.34: Optical microscope image of the photoresist residuals after acetone cleaning.

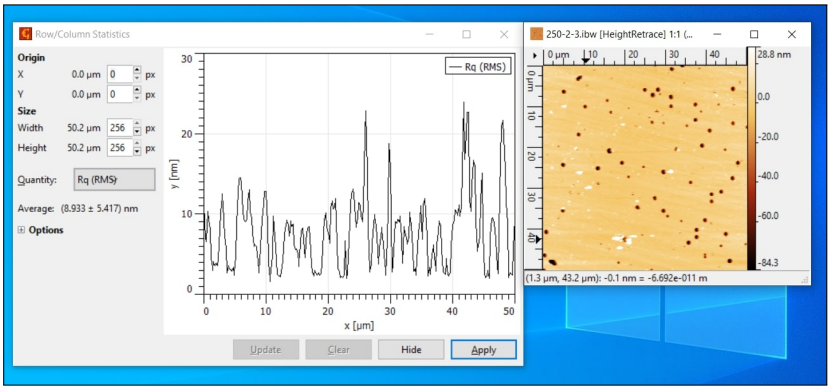


Figure 2.35: AFM surface topography measurement of alumina deposited chip. The photoresist is removed from the chip before the alumina etch process. Only a chrome layer exists on the surface during alumina etch.

surface. The required surface roughness value for successful anodic wafer bonding is about ten times lower than the necessary value for fusion bonding (i.e. 5 nm R_q max roughness for anodic wafer bonding as opposed to 0.5 nm R_q for fusion bonding) [28]. EVG, the wafer bonding company that did the anodic wafer bonding service for our wafers, suggested having lower than 10 nm R_q surface roughness value for the best results in anodic wafer bonding. Figure 2.39 shows a roughness measurement by AFM, and it can be observed from the measurement that the R_q value satisfies the requirement for the anodic wafer bonding process. Although there is an almost 6 nm spike in the graph, this is not common on the wafer surface, and these spikes will be eliminated during the

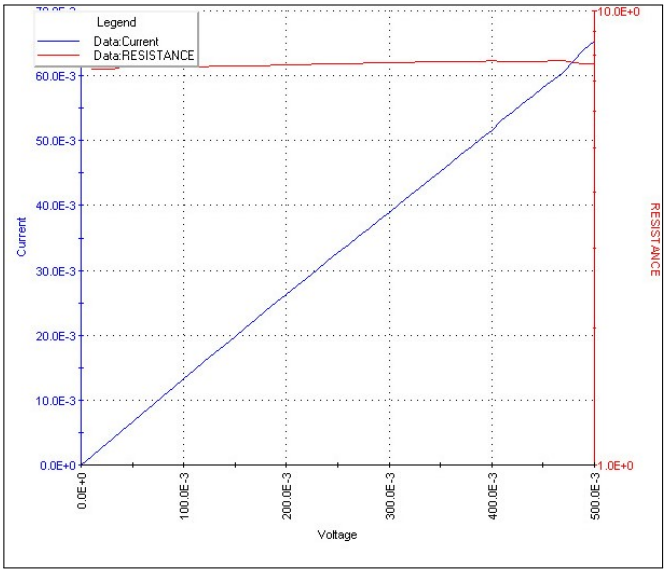
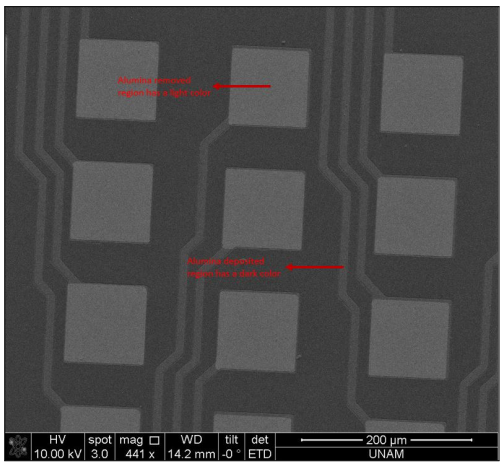


Figure 2.36: Current and resistance measurements are taken from the metal pad area after alumina etch.

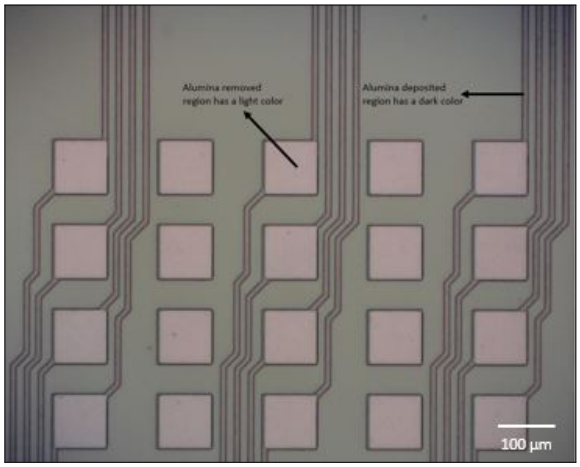
surface cleaning procedure before the anodic wafer bonding process. Before the anodic wafer bonding, the surface cleaning processes have a crucial role because surface cleaning processes provide low surface roughness both for SOI and Pyrex wafers. Influence of the cleaning processes on anodic wafer bonding process is investigated by Joyce et al. (2015). They suggested that RCA cleaning is the best approach for surface cleaning. However, in our study, alumina is coated on the prepared Pyrex substrates. Thus, diluted AZ400K is used as the cleaning solution before the anodic wafer bonding processes.

2.3.5 Wafer Bonding

Wafer-bonding technology allows for the fabrication of complex structures, including sealing and encapsulation of wafers or parts of a wafer. Also, wafer bonding enables transferring of layers of various materials from one wafer to another wafer [22]. During CMUT device microfabrication, if done properly, wafer bonding may enhance yield, uniformity, and process control by simplifying the integration process and minimizing the number of microfabrication steps. Wafer bonding also removes concerns related to sacrificial layer release procedures such as extended



(a) SEM image of metal pad region.



(b) Microscope image of metal pad region.

Figure 2.37: Metal pad regions after alumina etch, etched areas are brighter than other regions.

time wet (or dry) etch removal of sacrificial layer, or selectivity requirements between sacrificial layer and the other structural layers of CMUT devices on a substrate. With wafer bonding, it is possible to optimize both the cavity and the membrane, even though they may be designed on different wafers. Furthermore, wafer bonding gives a variety of design flexibility that improves device efficiency [74].

Anodic wafer bonding is a variation of wafer bonding. Ion drift within the glass leads to an adhesive contact in anodic wafer bonding, which is used to bond glass to silicon substrate. Time, temperature, and voltage are the main variables in this process [22]. This process can tolerate higher surface imperfections and surface roughness values compared to direct wafer bonding process, due to the strong electrostatic attraction pressure at the wafer pair interface during the anodic bonding process. In addition, anodic wafer bonding has excellent reliability compared to direct wafer bonding [28].

Bellaredj et al. published a study in 2014 [75] describing an innovative low temperature CMUT fabrication approach based on anodic bonding of an SOI wafer to a glass wafer. The study shows that it is possible to fabricate CMUTs with a precise membrane thickness based on the device layer thickness of the SOI wafer

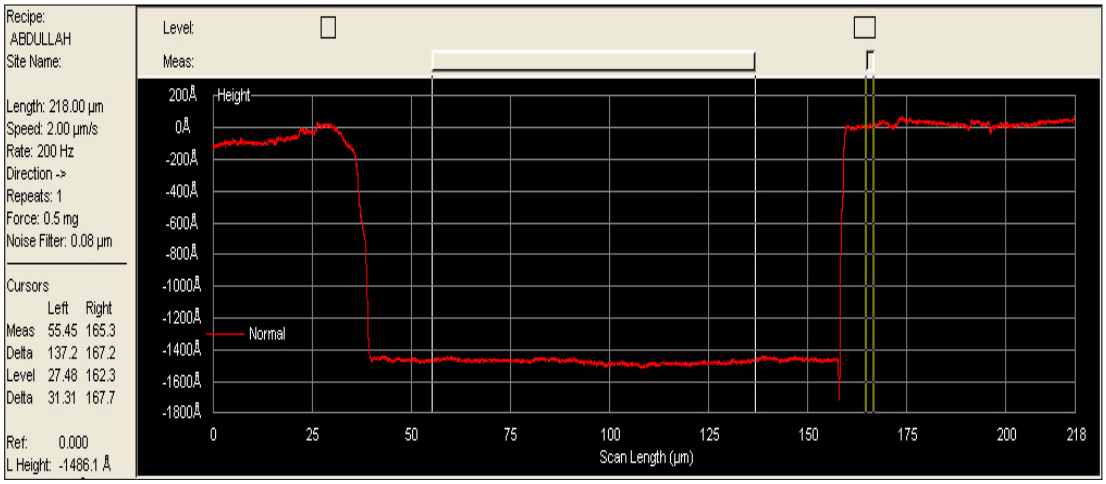


Figure 2.38: Using the stylus profilometer, alumina thickness is measured as nearly 150 nm as expected.

using the suggested manufacturing approach. The most significant disadvantage of the anodic wafer bonding method is the outgassing that occurs during the bonding process. Outgassing results in trapped gas in cavities in the bonding interface [56]. We tried to solve this problem by adding a titanium layer inside the cavity in our fabrication process. This solution is suggested by Torunbalci et al. [35].

Temperatures in anodic wafer bonding are typically in the 200 °C – 450 °C range [76]. Higher temperatures increase the mobility of positive ions in the glass. Increased mobility of ions leads to a faster bonding process [77]. However, the temperature should be less than the softening point of glass [78]. The typical anodic bonding voltage ranges from 200 V to 2000 V [79], [80]. High voltage helps with the transportation of positive ions in glass towards the cathode, resulting in a negatively charged area at the bonding interface. The electrostatic force at the interface brings silicon and glass into direct contact, enabling oxygen ions in the glass to oxidize the silicon and form strong chemical bonds. Irreversible Si-O-Si-bonds can be produced on the contact areas using this approach [30]. High voltage, helps in decreasing the temperature required for successful anodic wafer bonding. When temperature and voltage are decreased, the bonding or sealing time that is needed for successful anodic bonding typically increases [81].

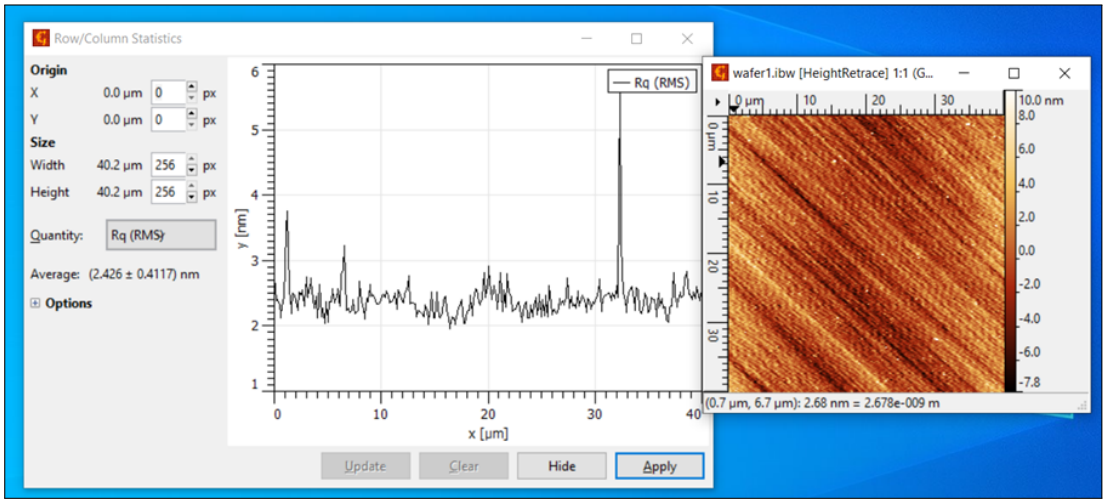


Figure 2.39: ALD alumina surface roughness measurements by AFM showed that R_q value is lower than 10 nm.

In this thesis study, the anodic wafer bonding process development studies are carried out in the cleanroom facilities of EVG in Austria. 150 nm alumina coated eight Pyrex wafers with approximately 150 nm gap height are used in these studies. The lack of knowledge in the so-far published literature for wafer bonding of alumina deposited Pyrex wafers with SOI wafers gave us the opportunity to do process development experiments. For process development purposes, 48 Pyrex wafer chips and 4 Pyrex wafer quarters, and 48 SOI wafer chips and 4 SOI wafer quarters were prepared. 16 Pyrex chips are coated with 150 nm alumina, another 16 Pyrex chips are coated with 250 nm alumina, and the remaining 16 Pyrex chips are coated with 300 nm alumina. Pyrex quarter wafers are coated with 150 nm alumina. The alumina film on these chips and quarter wafers was etched to form 150 nm deep features using the second alumina mask. The etching method was explained in the Insulator Layer Deposition section. 150 nm gap height was maintained in each Pyrex chip group. Pyrex and SOI wafer chips and wafer quarters were cleaned and carefully packed to prevent contamination.

Some process integration factors affect the bonding quality between Pyrex and SOI wafers. One of these factors is the dimensions of the gaps on the Pyrex surface. The second mask which has been used for the preparation of Pyrex chips and wafer quarters have 2000x2000 μm, 300x300 μm, 100×200 μm and

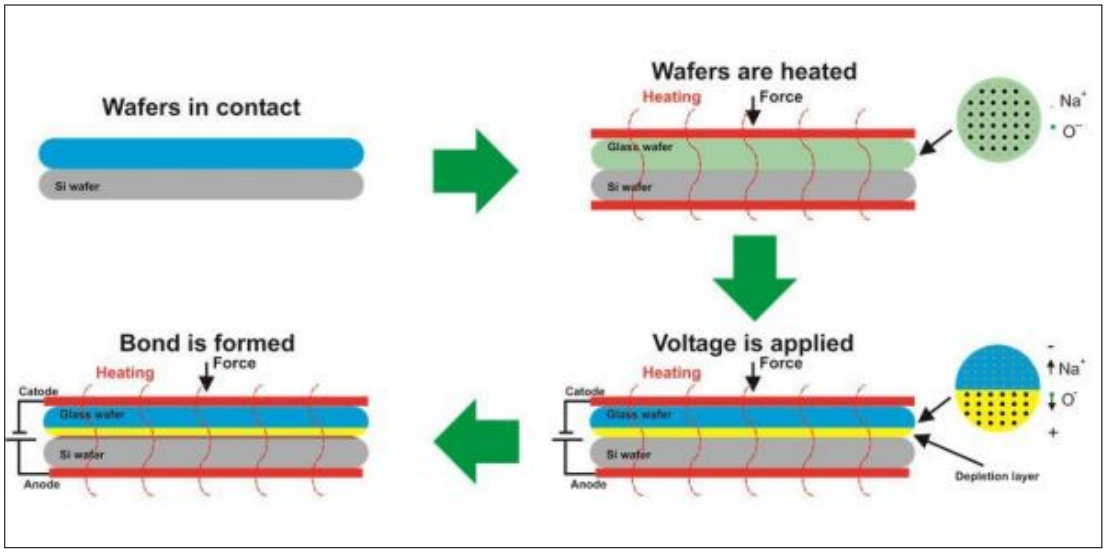
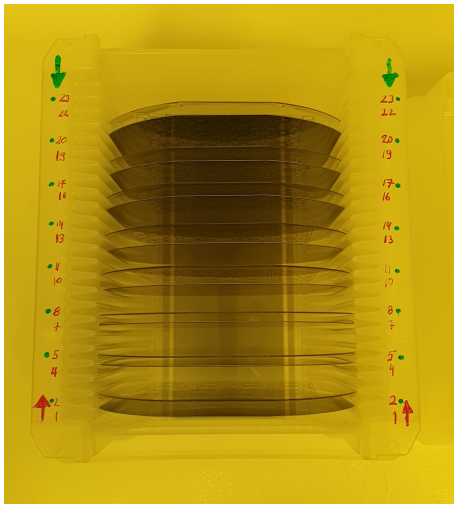


Figure 2.40: Diagram of anodic wafer bonding applied by EVG.

90×90 μm size squares and rectangles where alumina is patterned by wet etching. Anodic wafer bonding process behavior of these gap geometries is essential to understand how the gap geometry affects the wafer bonding process. Another factor that affects the wafer bonding process is the density of the features. Gaps that are placed densely, decrease the area of the bonding surface and might cause poor bonding. 90×90 μm size squares with 85 μm distance between them were arrayed as 4×32 arrays. This area has the highest gap density in this mask, and the density factor can be investigated from this area. The third factor is the thickness of the alumina. As we know from earlier experience from our group in wafer bonding of alumina coated Pyrex wafer with SOI wafer, deposited alumina thickness on Pyrex wafer influences the wafer bonding process. 150 nm, 250 nm, 300 nm alumina coated Pyrex chips helped to understand this effect.

In the anodic wafer bonding, at a specific temperature, oxygen ions dissociate from the glass by an electric field and form silicon dioxide at the interface of the wafers [82]. A diagram of anodic wafer bonding process is shown in Figure 2.40. Bond voltage and bond temperature are the two main characteristics of anodic wafer bonding. Bonding time commonly depends on the voltage and temperature, and mechanical pressure is applied to ensure that there is good electrical conduction across the substrates [83]. After several chip-scale bonding



(a) Fabricated Pyrex, and SOI wafer pairs.

(b) Manufactured alumina coated trial chips.

Figure 2.41: Fabricated Pyrex wafers and trial chips, and SOI wafers.

trials, the bonding recipe that fulfills the wafer bonding requirements of 150 nm alumina coated Pyrex wafer, and SOI wafer, is found.

Surface defects such as residues, particles, and scratches were visible on both Pyrex and SOI wafers before the bonding, which could be reasons for local bonding faults. The EVG 520IS 200 mm semi-automated wafer bonding machine is used for wafer bonding processes. After cleaning the wafer pairs with DI water and a megasonic nozzle, mechanical edge alignment is performed, followed by wafer bonding.

In Figure 2.42 anodically bonded Pyrex - SOI chip pair can be seen. Three different areas are indicated based on their density and gap size. There are 90x90 μm, 100×200 μm, and 300×300 μm rectangles located in Region 1, Region 2, and Region 3, respectively. In Figure 2.43 and Figure 2.44 three different Pyrex - SOI chip pairs that were bonded with different recipes are compared side by side. It should be noted that, in these process trials, the Pyrex surface was coated with 250 nm alumina. The holes in Region 1 and Region 2 are not bonded to the SOI chip for the 3 different recipes. However, in Region 3, the first and second recipes caused contact between the Pyrex - SOI chip pairs. Grey regions in Figure 2.44

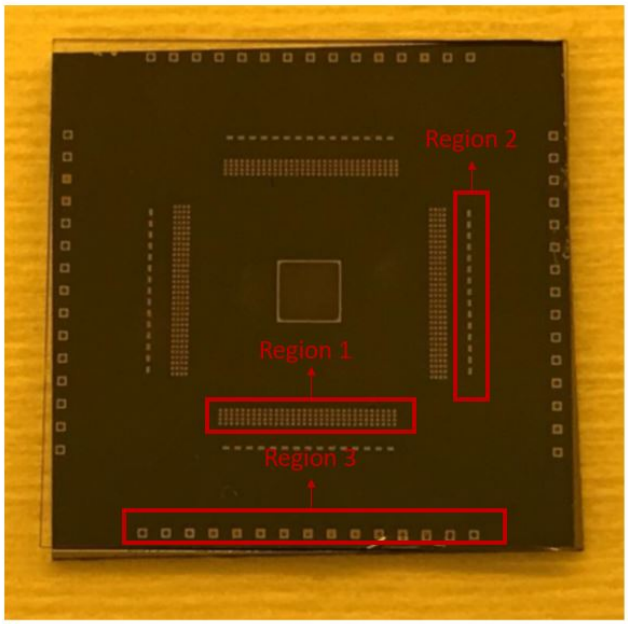
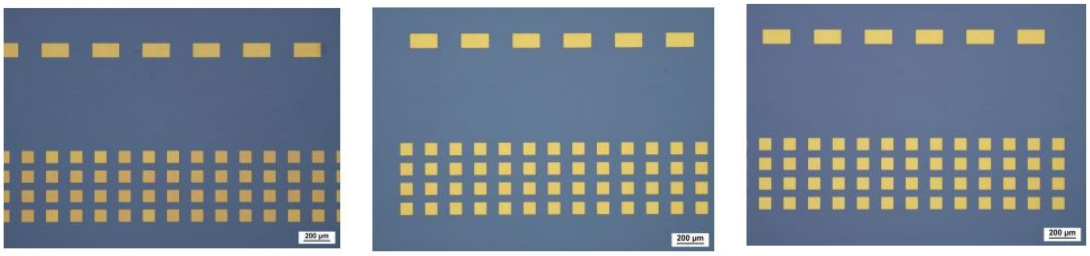


Figure 2.42: Regions in the Pyrex- SOI chip pairs after wafer bonding process. Region 1 has 90×90 μm gaps, Region 2 has 100×200 μm gaps and Region 3 has 300×300 μm gaps.

show that Pyrex and SOI are in contact. On the other hand, trials of the third recipe showed that with decreased voltage and temperature, the touching issue for relatively large pads such as in Region 3 are preventable.

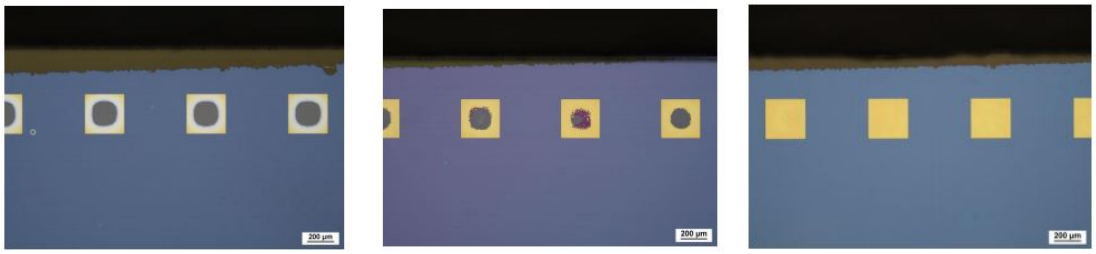
After these trials were done successfully on a chip scale, the same recipe (Recipe 3) was applied to the 4-inch full-size real wafers. However, the results were not satisfactory, and only 3 of the 16 chips had a good bonding. The root cause of this difference is that the bonding area of the 4-inch wafer is much higher than chip size Pyrex and SOI pairs. Voltage, temperature, bonding time, and applied force should be revised and arranged again according to full-size wafers. The bonding trial of the full-size wafer with Recipe 3 is shown in Figure 2.45a. White regions imply that bonding is not successfully done in these regions. Unbonded regions and bonded regions can be seen more clearly under the microscope.

After the unsatisfactory results of Recipe 3, the second bond is done to the wafer pair, which has a 175 nm cavity depth and 183 nm alumina thickness. 1000 V, 450 °C, 2000 N mechanical force and extended waiting time are applied



(a) Trial with Recipe 1. (b) Trial with Recipe 2. (c) Trial with Recipe 3.

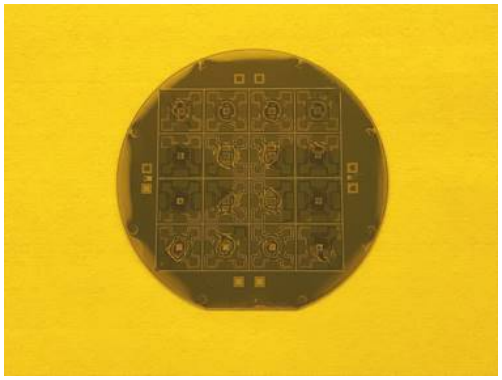
Figure 2.43: Wafer bonding results of Region 1 and 2 after 3 different recipe trials.



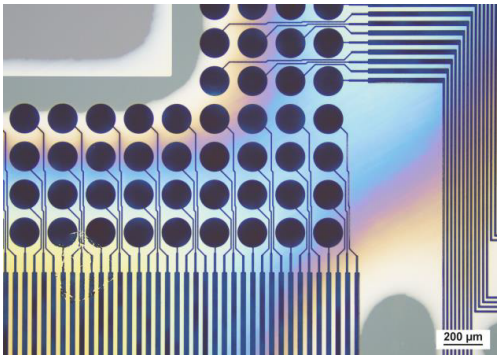
(a) Trial with Recipe 1. (b) Trial with Recipe 2. (c) Trial with Recipe 3.

Figure 2.44: Wafer bonding results of Region 3 after 3 different recipe trials.

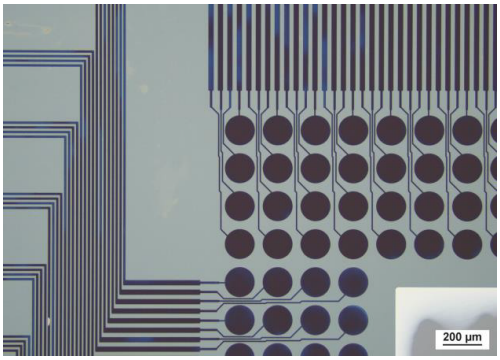
during the bonding process. Pyrex wafer was dipped into diluted AZ400K before the bonding process to eliminate residuals on the surface. Good bonding was achieved between wafer pairs after the anodic wafer bonding process with this recipe. However, 363 °C is the eutectic temperature of gold-silicon elements that can be seen in the gold-silicon phase diagram in Figure 2.47. We believe that Au diffused into Si at this temperature, and as a result, a significant amount of golden patches occurred. Bonding of the second 4-inch Pyrex - SOI wafer pair and golden patches can be seen in Figure 2.46. Another indicator for good bonding is the test structures on the wafer. Test structures are created during the alumina etch process. Because of the bottom electrode on the real CMUT devices, there is no way to see bonding in these regions. We took advantage of the close thickness values of the CMUT gap and alumina thickness and formed these structures to imitate bonding in the CMUT devices. In that way, bonding in the test structures shows the bonding in the CMUT devices, and the good bonding can be verified using these test structures.



(a) 4-inch wafer bonded wafer with Recipe 3.



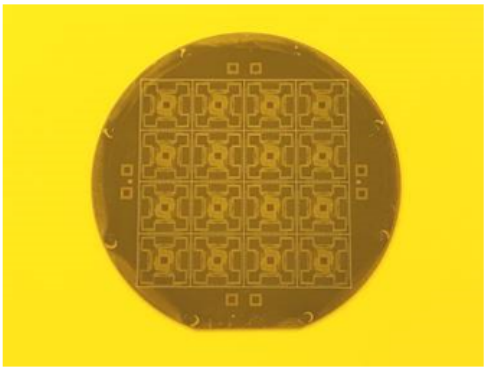
(b) Unbonded areas on the wafer.



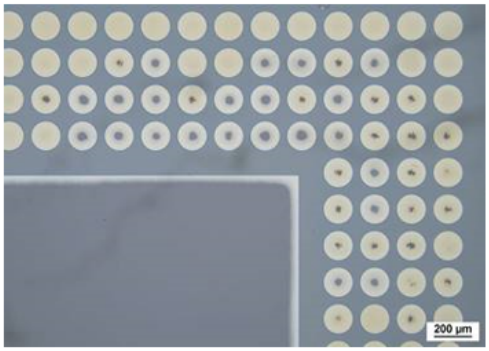
(c) Bonded areas on the wafer.

Figure 2.45: The first anodic wafer bonding of the 4-inch Pyrex - SOI wafer pair. Recipe 3 was used for this bonding process.

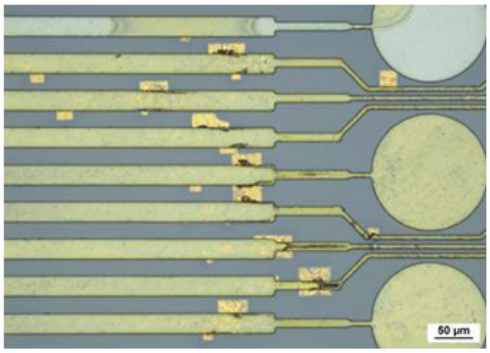
To prevent the occurrence of golden patches near to structures, bonding temperature is decreased to under 363 °C in the third trial. However, as we know from the studies we accomplished before, the temperature significantly impacts wafer bonding quality. Therefore, bonding time is increased to compensate for the reduced temperature in the third bonding trial. The third trial was done with 1000 V, 350 °C temperature, 60 minutes waiting time in each voltage step, 2000 N mechanical force, and surface treatment with diluted AZ400K is done before wafer bonding. The wafer in the third trial has 160 nm cavity depth and 160 nm alumina thickness. Results of the third bonding trial showed that golden patches are remarkably decreased, and it can be seen in Figure 2.48c. However, some parts on the wafer surface remained unbonded. These unbonded regions are the areas that have the densest line and space structures on the Pyrex wafers. Out of 16 CMUT array chips on a full-scale Pyrex wafer, only 5 or 6 CMUT array chips



(a) 4-inch wafers are bonded with the new recipe.



(b) Test structures on the wafer.



(c) Golden patches near to structures.

Figure 2.46: The second anodic wafer bonding of the 4-inch Pyrex - SOI wafer pair. New recipe was used for this bonding process.

were successfully bonded in these densest line and space regions with this recipe. Furthermore, test structures in the Pyrex wafer did not have contact with the SOI wafer, which indicates good bonding between Pyrex and SOI wafers at the gap regions of CMUT arrays.

The last 3 trials showed that temperature is a necessary but not the only factor for successful wafer bonding of our wafer pairs. In addition to that, our earlier experience showed that increasing the voltage higher than 1000 V causes arcing and harms the wafer. According to trial third, Pyrex which has 130 nm cavity depth and 150 nm alumina thickness and SOI pairs, are bonded reasonably well despite the low temperature. However, there aere still unbonded areas that needed to be improved. To increase bonded areas, mechanical force is increased 4 times in the fourth trial, while the other parameters are not changed. Results of the fourth

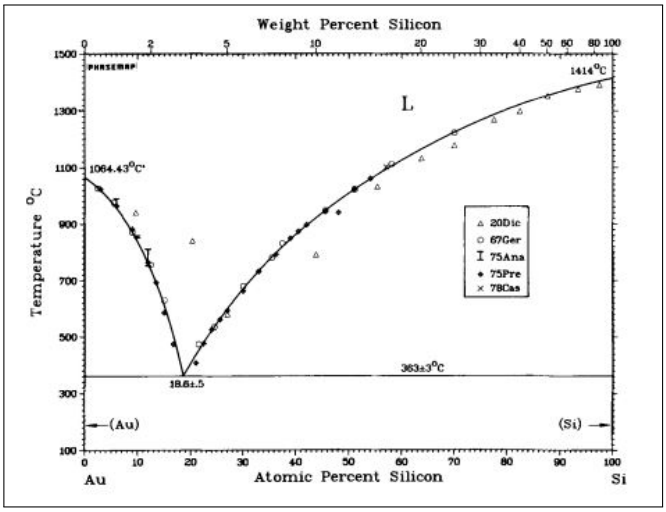
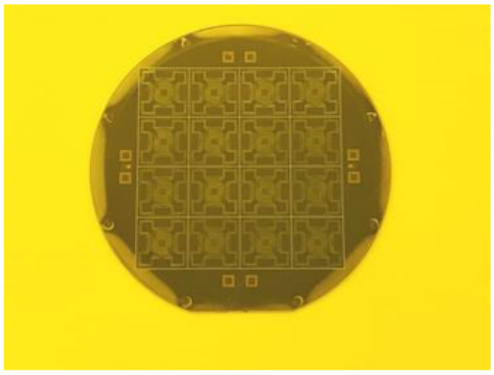


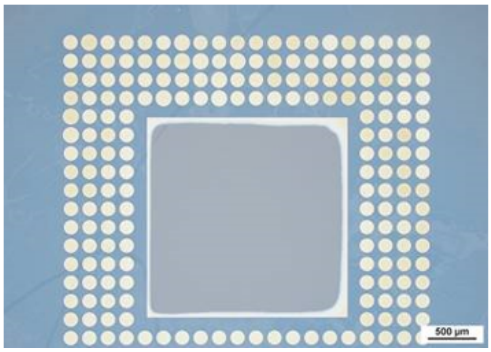
Figure 2.47: Phase diagram of Au-Si [84].

trial showed that increasing mechanical force does not significantly improve the anodic bonding quality, more than needed mechanical force may have a negative impact on test structures and real CMUT devices. Out of 16 CMUT array chips on a full-scale Pyrex wafer, only 6 or 7 CMUT array chips were successfully bonded in these densest line and space regions with this recipe. Furthermore, test structures in the Pyrex wafer had some contact with the SOI wafer, which indicates more than the needed force for bonding between Pyrex and SOI wafers at the gap regions of CMUT arrays.

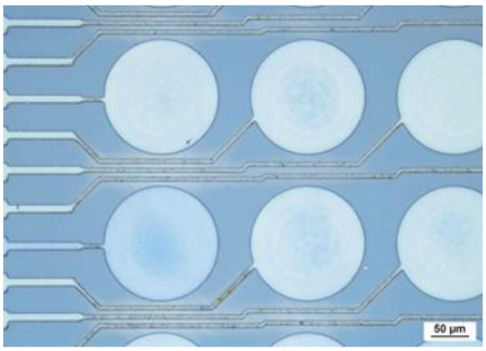
In the fifth trial, mechanical force was decreased back to 2000 N, last voltage step remained at 1000 V and waiting time remained 60 minutes in each voltage step. On the other hand, the temperature is increased to 355 °C, and the surface cleaning process with diluted AZ400K in the ultrasonic bath is increased to 30 seconds. Results showed that all the dense line-and-space regions on the wafer, which has 120 *nm* cavity depth, and 148 *nm* alumina thickness, appear to be bonded. However, some metal lines has a noticeable yellowish color. Finally, undesired bonding between Pyrex and SOI wafers was observed only in a small percentage of the circular test structures. Although all the devices are appropriately bonded, there is a color change in most of the CMUT structures. Out of 16 CMUT array chips on a full-scale Pyrex wafer, only 3 CMUT array chips were successfully bonded in these densest line and space regions with this recipe. At



(a) 4-inch wafers are bonded with reduced temperature recipe.



(b) Test structures on the wafer.

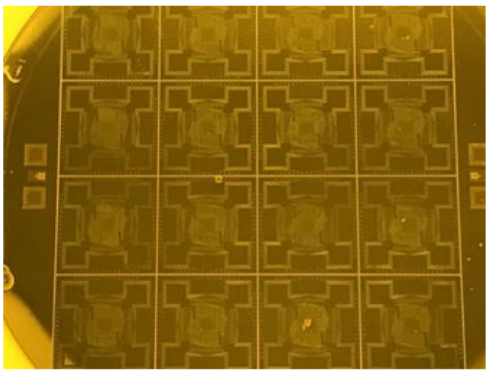


(c) CMUT device structures.

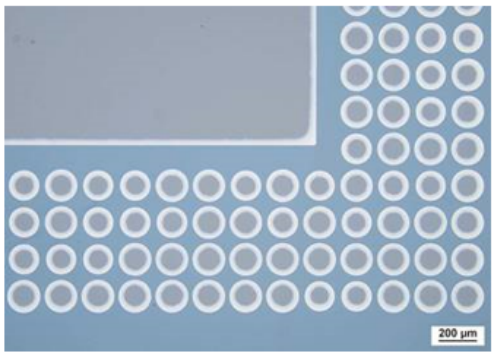
Figure 2.48: The third anodic wafer bonding of the 4-inch Pyrex - SOI wafer pair. Reduced temperature recipe was used for this bonding process.

the same time, the rest of the 13 devices showed a color change in the metal stack regions, including the wiring regions and the CMUT bottom electrode regions. Further analysis for the yield calculations should be done for these wafer pairs in the following process steps after the electrical pads on Pyrex substrates are revealed.

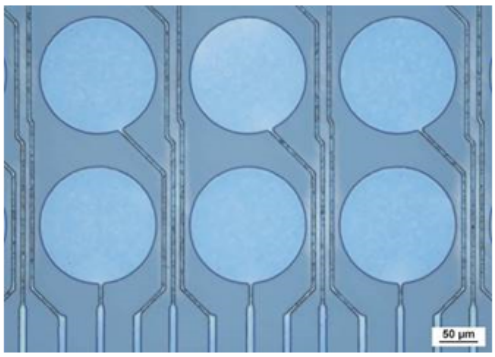
In the sixth Pyrex and SOI anodic wafer bonding trial, to prevent color change inside the wiring and bottom electrode structures, anodic bonding temperature and waiting time in each voltage step are decreased. Temperature is reduced to 350 °C and 30 minutes waiting time in each voltage step is applied for this trial. The Pyrex wafer in this trial has 180 nm cavity depth and 147 nm alumina thickness. Ultrasonic bath cleaning time is also decreased to 15 seconds which was 30 seconds in the previous trial, but the total cleaning time was kept as 5



(a) 4-inch wafers are bonded with reduced temperature and increased mechanical force recipe.



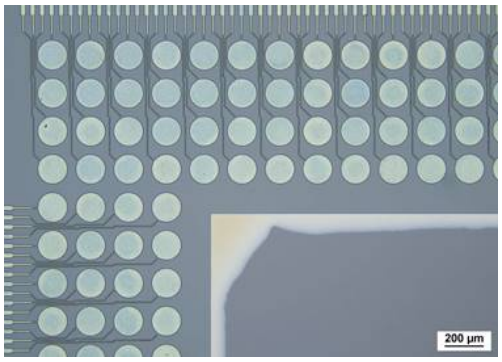
(b) Test structures on the Pyrex wafer have contact with SOI wafer.



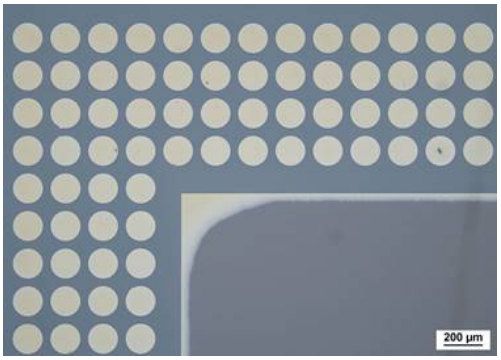
(c) CMUT device structures.

Figure 2.49: The fourth anodic wafer bonding of the 4-inch Pyrex - SOI wafer pair. Reduced temperature and increased mechanical force recipe was used for this bonding process.

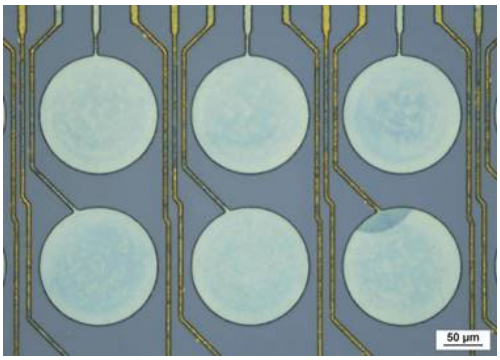
minutes. Voltage and mechanical force parameters have remained unchanged. Results showed that the majority of line-and-space structures on the wafer are bonded. There is some color variation inside the structures, but a color change to yellow can only be seen in rare cases and with a low number. Out of 16 CMUT array chips on a full-scale Pyrex wafer, 12 CMUT array chips were successfully bonded in these densest line and space regions with this recipe. At the same time, the rest of the 4 devices showed unbonded features only at the densest line and space regions between two CMUT cells of a CMUT array. However, in comparison to the fifth bonding process, a more significant number of test structures appear to be in contact, even though bonding duration and temperature were lowered while cavity depth was increased. These results from the test structure region



(a) Wafers are bonded with increased surface cleaning process.



(b) Significant amount of test structures on the Pyrex wafer do not have contact with SOI wafer.

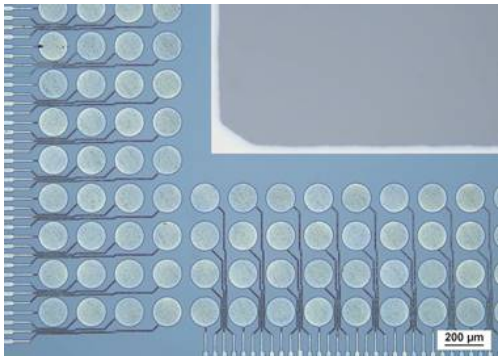


(c) CMUT device structures have a color change to yellow.

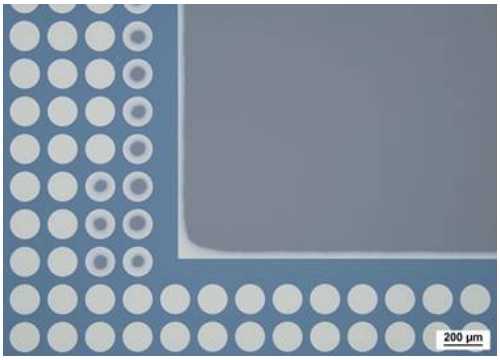
Figure 2.50: The fifth anodic wafer bonding of the 4-inch Pyrex - SOI wafer pair. Temperature is increased to 355 °C and surface cleaning time is increased to 5 minutes.

imply that the local quality of the wafers plays a significant role in the obtained results.

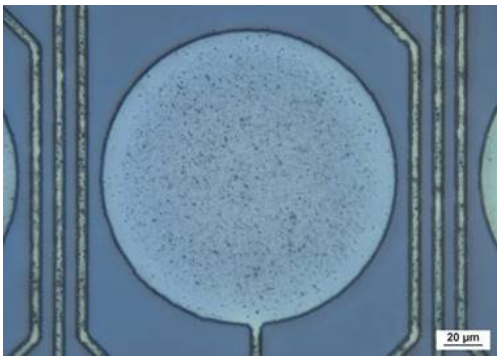
In the seventh process trial, except for the waiting time in each voltage step, the recipe was kept the same compared to the previous sixth rpcess trial. The Pyrex wafer in this trial has 100 nm cavity depth and 160 nm alumina thickness. 30 minutes waiting time is increased to 45 minutes in the seventh trial. None of the test structures had undesired contact with the SOI wafer, which indicates not excessive, not insufficient, but enough bonding quality at these test regions. In addition to that, most of the dense line-and-space regions were bonded. However, there was a distinctive color change inside the metal structures. Although the



(a) 4-inch wafers are bonded with decreased temperature, waiting time and ultrasonic cleaning.



(b) Compared to fifth bond, significant amount of test structures on the Pyrex wafer have contact with SOI wafer.

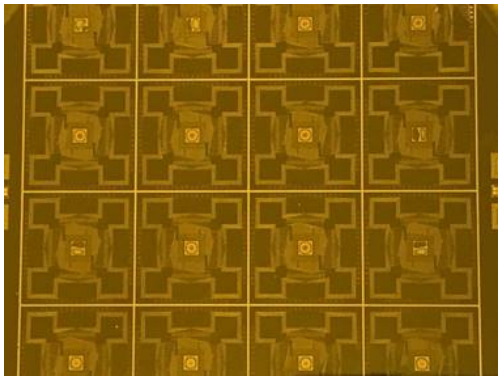


(c) Most of the CMUT structures do not have a color change to yellow.

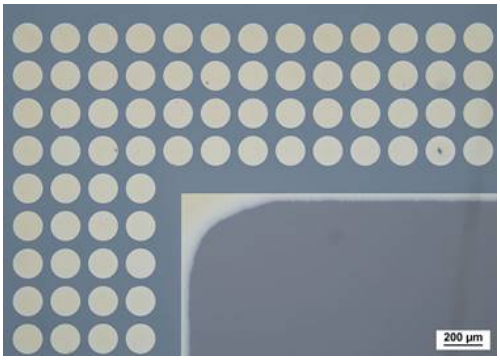
Figure 2.51: The sixth anodic wafer bonding of the 4-inch Pyrex - SOI wafer pair. Temperature is reduced to 350 °C, waiting time is decreased to 30 minutes and surface cleaning with the ultrasonic bath is decreased to 15 seconds.

exact reason for the color change is unknown, we believe that the main reason is different from the previous color changes where the strong yellow color was visible.

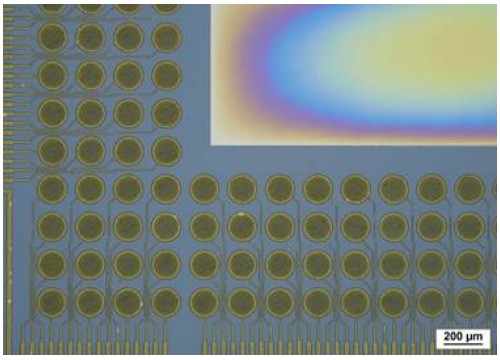
In the eighth anodic wafer bonding trial, the recipe was kept the same as the previous seventh trial recipe. The Pyrex wafer in this trial has 200 nm cavity depth and 140 nm alumina thickness. Results showed that the dense line-and-space structures on the entire wafer were bonded successfully. None of the test structures have contact with the SOI wafer. Furthermore, we applied the same recipe to the seventh and eighth trials, and the color change to yellow is rarely seen in the locations where there are defects inside the structures in the eighth



(a) 4-inch wafers are bonded with 45 minutes waiting time in each voltage step.



(b) None of test structures on the Pyrex wafer have contact with SOI wafer.

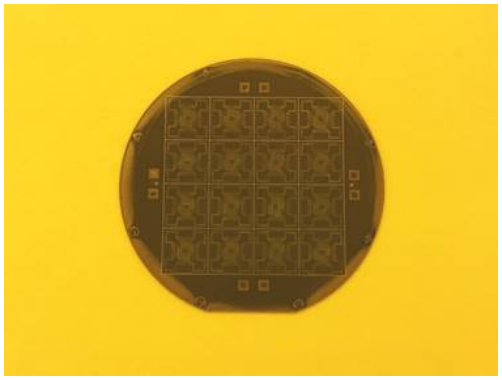


(c) CMUT structures have yellow/brown color.

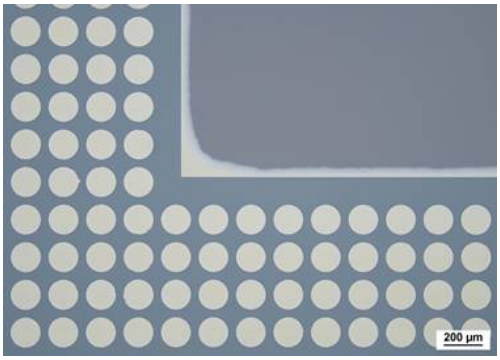
Figure 2.52: The seventh anodic wafer bonding of the 4-inch Pyrex - SOI wafer pair. Waiting time is raised to 45 minutes, other parameters remained same as trial number six.

trial. Hence, results show that the root cause for color change in the seventh trial is most likely because of the metal layers inside the structures, not the temperature, such as in the second bond.

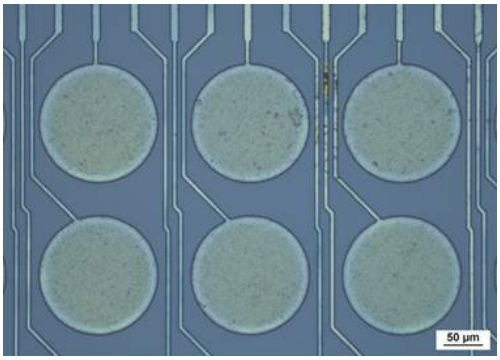
For the detailed investigation and the qualitative results of the unbonded and bonded regions on the wafer pairs, infrared (IR) transmission microscopy, acoustic microscopy, and white light interferometry can be done. Also, the strength measurements of the wafers can be done by pull testing and shear testing. However, these pulling test and shear tests are destructive and may harm the bonded wafers. These strength tests are only applicable to trial chips in our studies.



(a) 4-inch wafers are bonded with 45 minutes waiting time in each voltage step.



(b) None of test structures on the Pyrex wafer have contact with SOI wafer.



(c) Color change to yellow is very rare and located at the defected regions.

Figure 2.53: The eighth anodic wafer bonding of the 4-inch Pyrex - SOI wafer pair. Parameters were kept same as trial number seven.

2.3.6 Removing Silicon Layers and Top Electrode Formation

SOI stands for Silicon on Insulator and consists of three layers. These are the handle layer, BOX layer, and device layer. For the designed CMUT fabrication process, the handle layer and BOX layer must be entirely removed from the surface after anodic wafer bonding is completed. In addition, the device layer also will be removed from the desired regions only. First and foremost, the Si handle layer with 350 μm thickness will be removed using the RIE capability of the ICP tool. RIE etching will be done using continuous plasma processing. The thickness of the handle layer of the wafer will be regularly checked to probe the

remaining RIE processing. After the handle layer is completely etched from the BOX surface, the second layer to be etched is the BOX layer. BOE can easily etch BOX layer. The silicon device layer of 12 μm thickness, which will be the vibrating CMUT plate, will be reached after thoroughly etching the BOX layer.

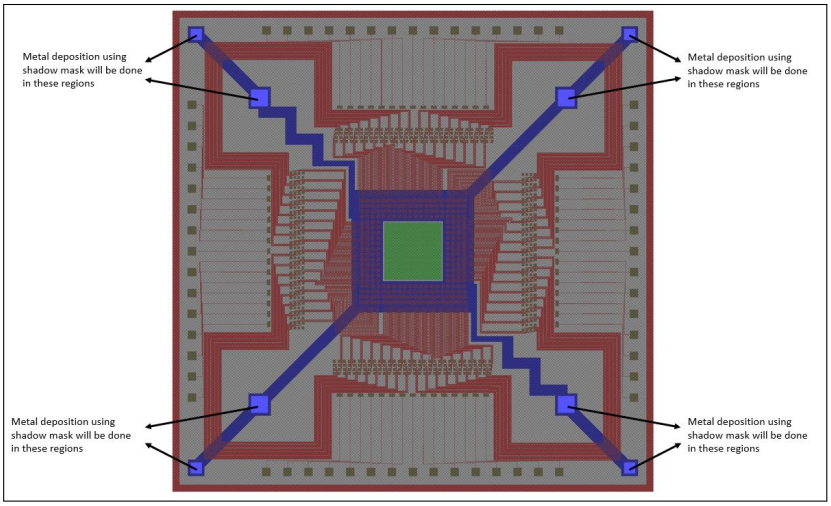


Figure 2.54: Chip size drawing of Shadow mask on Cavity Formation mask. Red color represents Cavity Formation mask (1st mask), alumina etched from green regions (2nd mask), the top metal electrode will be deposited on the blue region on top of the silicon by e-beam evaporator using a shadow mask.

Before the silicon device layer is etched from the desired regions, 30 nm Cr, 40 nm Au, and 30 nm Cr film stack will be deposited on top of the silicon device layer to lower the resistance across the Si device layer. Due to the possibility of a poor conductivity silicon device layer, the current that will go towards the ground pads will encounter a high resistance if there is not highly conductive metal deposition on top of the silicon layer. The ground pads which are located in the corners of the chip are designed as 1 mm squares, and there is a certain distance between pads and the nearest features that can be seen in Figure 2.54. Shadow mask, which will be used for the ground pad metal deposition, is cost-effective and less time-consuming than chrome on glass UV lithography masks. However, it can only be applied to less alignment demanding process steps. In this way, 30 nm Cr and 500 nm Au stack will be deposited on the silicon plate by using a shadow mask without doing UV lithography related process steps.

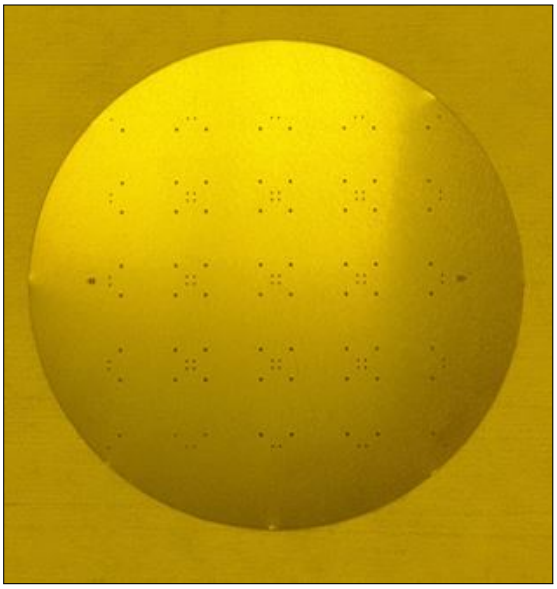


Figure 2.55: The image of produced and planned to use Shadow Mask.

The next step after deposition of 30 nm Cr and 500 nm Au stack, is doing the necessary UV lithography steps for etching the previously deposited Cr/Au/Cr metal stack, and device layer silicon to reveal the bottom electrodes, separate the vibrating CMUT plate layer from bottom electrodes and open the fiber region area. The third lithography mask will be used for these etching steps. Microchemical's AZ4562 (Ulm, Germany) photoresist, which was used in previous photolithography steps, will be replaced by Microchemicals AZ5214E (Ulm, Germany), which is a thinner positive photoresist and can be etched in a shorter time using oxygen plasma processing. After HMDS spinning on the wafer, 2 μm of AZ5214E will be spin-coated, UV exposed. After the photoresist is successfully developed with diluted AZ400K, the Cr-Au-Cr metal stack in the patterned areas will be etched with wet etchants. Both of the Cr thin-films will be wet etched with CR-7, and Au thin-film that is sandwiched between Cr thin-films will be removed with diluted Aqua Regia solution (3:1:2 hydrochloric acid, nitric acid, and DI water). The wafer will be rinsed with DI water after each wet etching process. After the metal layers in the stack are removed by wet etching, using the same photoresist mask, Si device layer will be patterned to form the vibrating CMUT plate layer. To prevent liquid penetration to CMUT cells from the open channels during the photoresist removal process after silicon device layer patterning, the photoresist

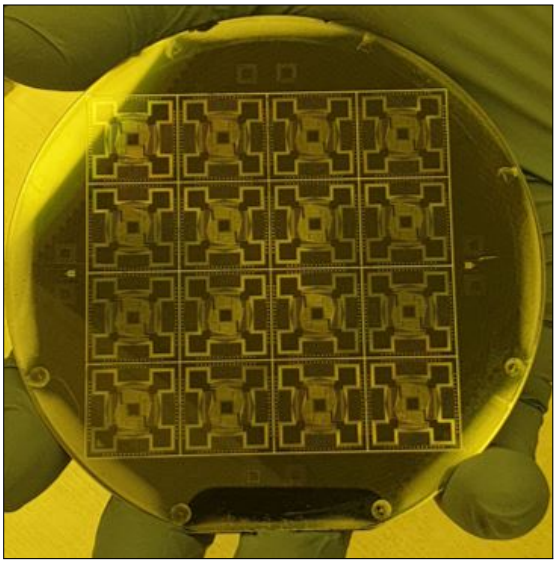


Figure 2.56: The back side image of fabricated wafer after wafer bonding process.

will be etched by oxygen plasma using the ICP tool.

As explained above, after patterning of the Cr-Au-Cr metal stack on the Si device layer surface is completed, the next step is to remove (i.e. pattern) the silicon device layer from desired regions that are shown in Figure 2.57. Etching the silicon device layer by using a wet etchant will fill (and damage) the gap regions in the CMUT cells because the Si etched areas are connected to CMUTs cells via the channels above bottom electrode metal stack wires. For this reason, the dry etch process by ICP is going to be utilized. The Bosch process will be chosen as the best option for maximizing anisotropic etching [85]. The silicon device layer on the electrical pad connecting sections will entirely be etched after applying the Bosch process for sufficient etching time. Before finalizing the silicon patterning process, the last step will be removing the photoresist from the patterned Si device layer surface. As explained before, wet etching for photoresist removal will not be an option because the channels that are directly reaching the CMUT gaps are accessible by wet processing approaches. Hence, O_2 plasma will be employed to etch the photoresist. Oxygen plasma will etch the photoresist across the entire patterned wafer surface. Furthermore, O_2 plasma will also target the chrome layer underneath the photoresist. As a result, the 500 nm thick gold top electrodes for wire bonded ground connections, and the 40 nm thick gold resistance reduction

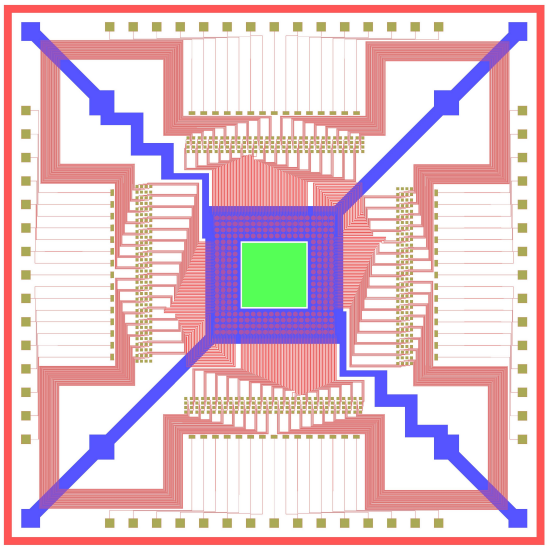


Figure 2.57: Chip size drawing of Silicon Etch mask (3rd mask) on Cavity Formation mask (1st mask). Red color represents Cavity Formation mask, and alumina etched from green regions (2nd mask), the black region is a top metal electrode (shadow mask). The blue region is the silicon region that is aimed to stay on the surface.

layer will remain as the final top surface layers on the wafer.

After all the fabrication steps stated above, the overlapped version of the used masks for the CMUT array devices in the 4-inch wafer can be seen in Figure 2.59.

2.3.7 CMUT-MEMS Fabrication Overview

Manufacturing simulation for large arrays, such as CMUT arrays, requires high-capacity hardware. Due to lack of high-capacity hardware, simulations and drawings are kept as simple as possible. In the 2D CMUT Manufacturing Process Flow section, all process details are shown as much as possible for one CMUT cell, ASIC metal pad, and PCB metal pad. ASIC and PCB connections and Parylene C coating are also shown, although these processes are not included in this thesis timeline of the manufacturing project. In the 3D CMUT Manufacturing Process Flow section, 4 CMUT cells and corresponding metal pads are shown. ASIC and PCB connections, Parylene C coating, and fiber hole drilling process are shown

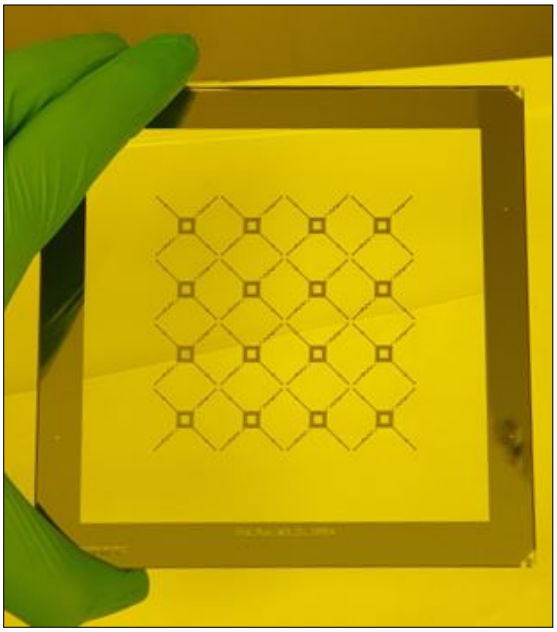


Figure 2.58: The image of produced and planned to use Silicon Etch mask.

in this process flow. As mentioned above, these processes are not included in this part of the manufacturing project.

2.3.8 2D and 3D CMUT Micromanufacturing Integration Process Flow

In Figure 2.60 all process details for simple design are shown in 2D.

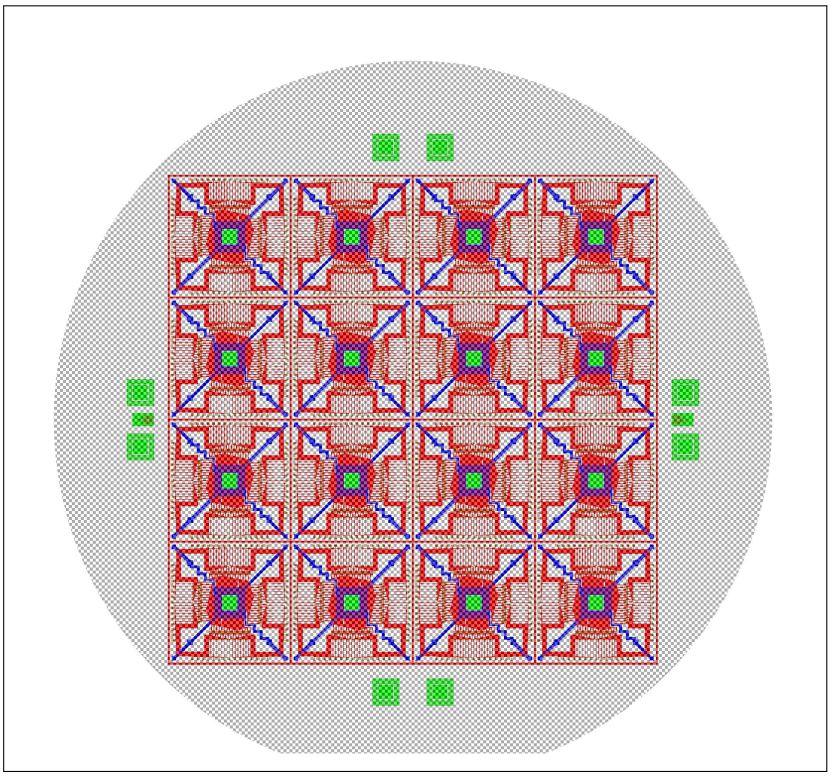


Figure 2.59: Wafer size drawing of all main masks. The red color represents the Cavity Formation mask (1st mask), alumina etched from green regions (2nd mask), the blue region is the silicon region that is intended to stay on the surface (3rd mask).

1)

- Start with blank Pyrex wafer.

2)

- Chrome deposition as hard mask.

3)

- Photolithography with first chrome mask for cavity definiton on Pyrex substrate.

4)

- Argon Reactive Ion Etching (RIE) by Inductively Coupled Plasma (ICP) for ething chrome.

5)

- SF_6 Reactive Ion Etching (RIE) by Inductively Coupled Plasma (ICP) for etching Pyrex.

6)

- Buffered Oxide Etch (BOE) process for etching Pyrex.

7)

- Ti/Pt/Au metal deposition by e-beam evaporator for bottom electrodes and wirings.

8)

- Lift-off process by using Piranha etchant.

9)

- Chrome etching by using chrome etchant.

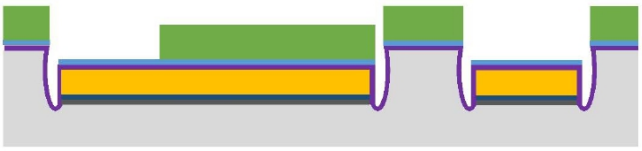
10)

- Alumina deposition for insulator layer by Atomic Layer Deposition.

11)

- Chrome deposition as hard mask.

12)



- Second lithography for etching Alumina on the connection pads.

13)

- Chrome Etch over the connection pad areas pads.

14)

- Etching Alumina over the connection pad areas by using AZ400K developer.

15)

- Photoresist removed from the surface by using acetone and piranha.

16)

- Chrome etching by using chrome etchant.

17)

- Wafer bonding with Silicon on Insulator wafer (SOI).

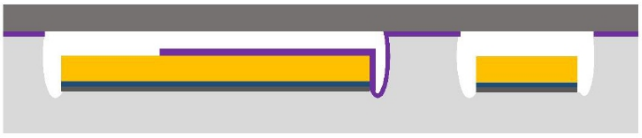
18)

- Wafer bonding with Silicon on Insulator wafer (SOI).

19)

- Removing Handle Layer with SF_6 plasma. (Due to time constraints, not performed in this study. These remaining steps will be performed by the next graduate student who will be working on microfabrication of the remaining process steps.)

20)



- Removing Buried Oxide (BOX) Layer by using BOE. (Due to time constraints, not performed in this study. These remaining steps will be performed by the next graduate student who will be working on microfabrication of the remaining process steps.)

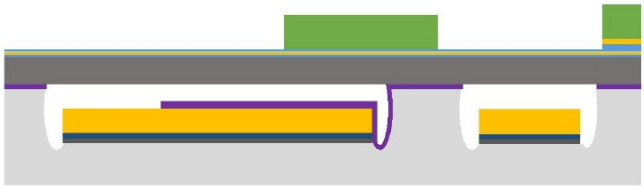
21)

- Cr-Au-Cr resistance reduction layer deposited by E-beam evaporator. (Due to time constraints, not performed in this study. These remaining steps will be performed by the next graduate student who will be working on microfabrication of the remaining process steps.)

22)

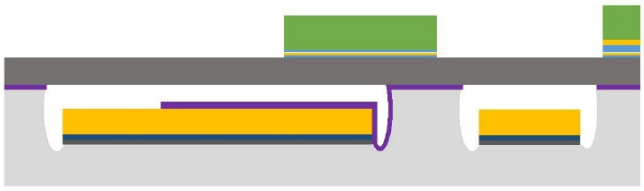
- Top electrode deposited using shadow mask by E-beam evaporator. (Due to time constraints, not performed in this study. These remaining steps will be performed by the next graduate student who will be working on microfabrication of the remaining process steps.)

23)



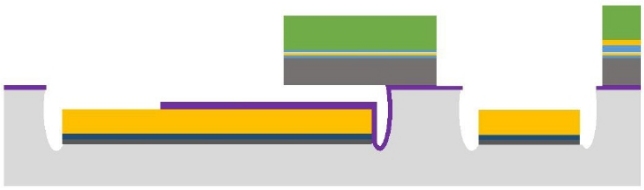
- Third lithography done to open connection pad areas. (Due to time constraints, not performed in this study. These remaining steps will be performed by the next graduate student who will be working on microfabrication of the remaining process steps.)

24)



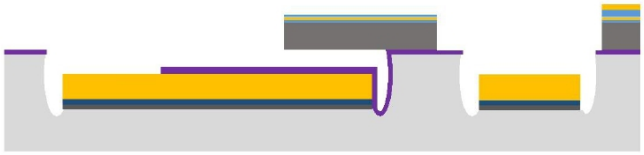
- Cr/Au/Cr wet etch. Cr etched by chrome wet etch and Au etched by aqua regia solution. (Due to time constraints, not performed in this study. These remaining steps will be performed by the next graduate student who will be working on microfabrication of the remaining process steps.)

25)



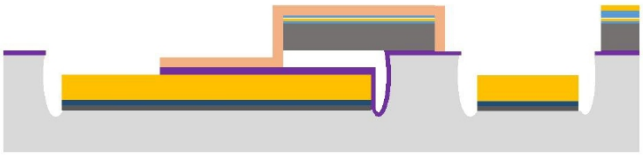
- Silicon device layer etched by Bosch process. (Due to time constraints, not performed in this study. These remaining steps will be performed by the next graduate student who will be working on microfabrication of the remaining process steps.)

26)



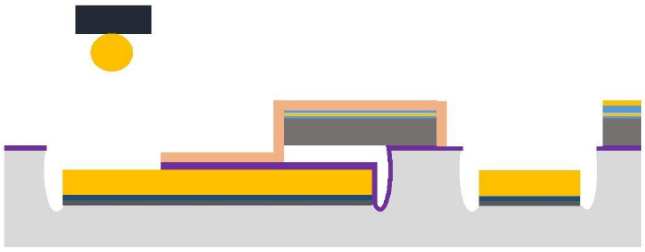
- Photoresist removed from the surface. (Due to time constraints, not performed in this study. These remaining steps will be performed by the next graduate student who will be working on microfabrication of the remaining process steps.)

27)



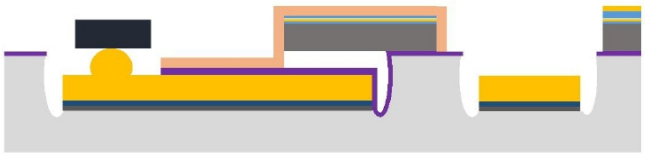
- Parylene-C coating. (Due to time constraints, not performed in this study. These remaining steps will be performed by the next graduate student who will be working on microfabrication of the remaining process steps.)

28)



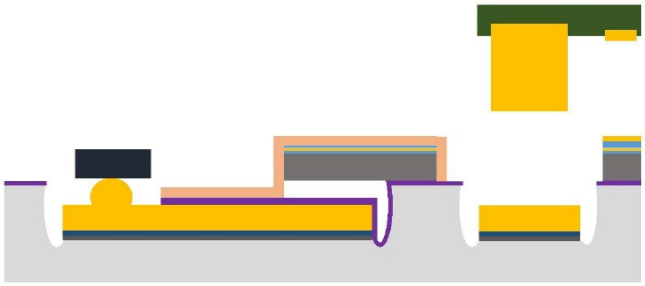
- ASIC preparation for flip-chip bonding. (Due to time constraints, not performed in this study. These remaining steps will be performed by the next graduate student who will be working on microfabrication of the remaining process steps.)

29)



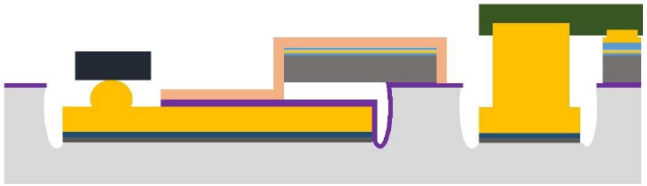
- Flip-chip bonding of CMUT chip to designed ASICs. (Due to time constraints, not performed in this study. These remaining steps will be performed by the next graduate student who will be working on microfabrication of the remaining process steps.)

30)



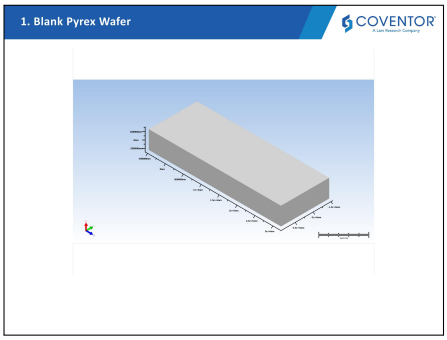
- PCB preparation for bonding process. (Due to time constraints, not performed in this study. These remaining steps will be performed by the next graduate student who will be working on microfabrication of the remaining process steps.)

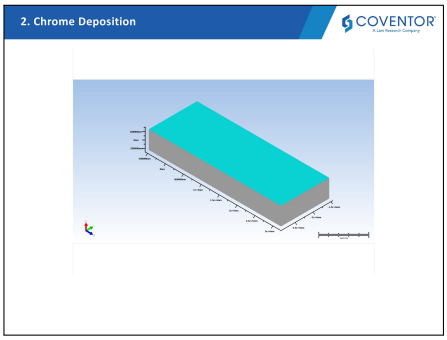
31)

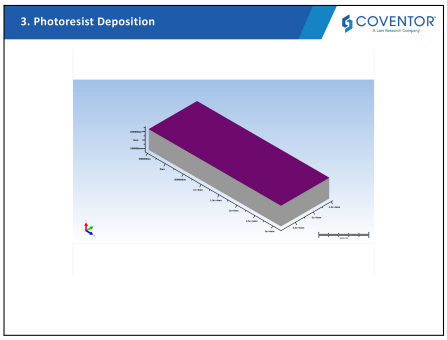


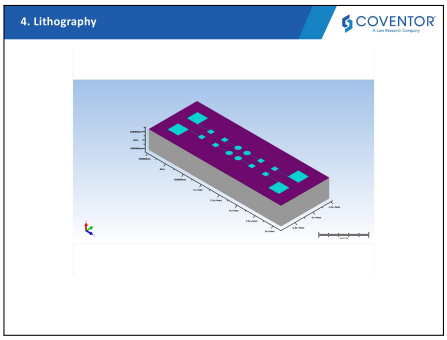
- Bonding of CMUT chip to designed PCB and wire bonding of ground pads on PCB. (Due to time constraints, not performed in this study. These remaining steps will be performed by the next graduate student who will be working on microfabrication of the remaining process steps.)

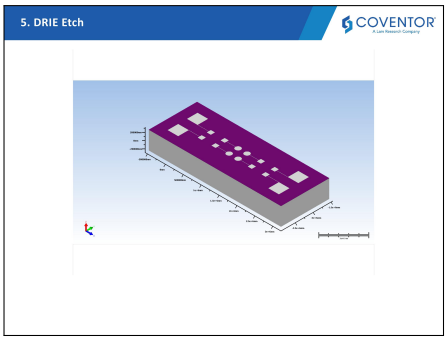
Figure 2.60: 2D Fabrication flow of CMUT arrays that are manufactured at Bilkent University UNAM and will continue to be manufactured at Bilkent University UNAM for the remaining process steps.

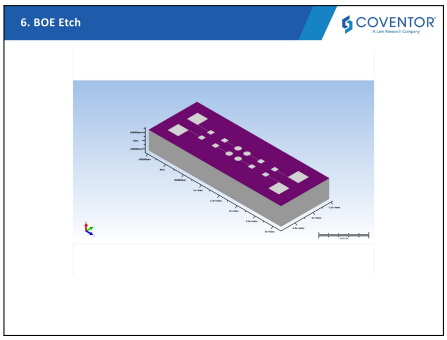

1. Blank Pyrex Wafer
COVENTOR

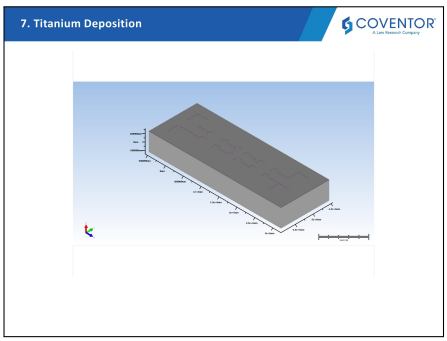

2. Chrome Deposition
COVENTOR

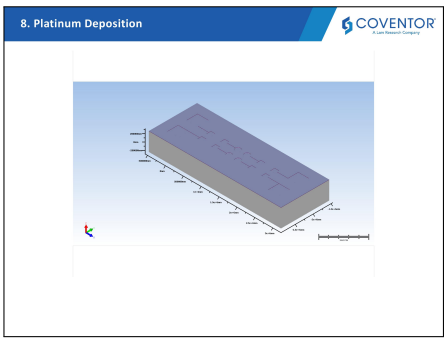

3. Photoresist Deposition
COVENTOR

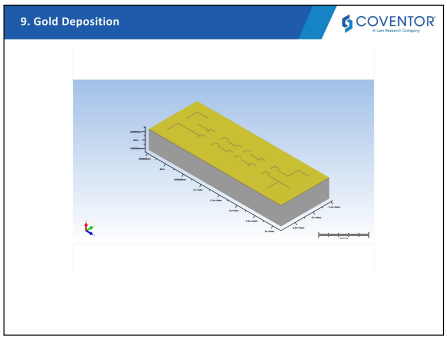

4. Lithography
COVENTOR

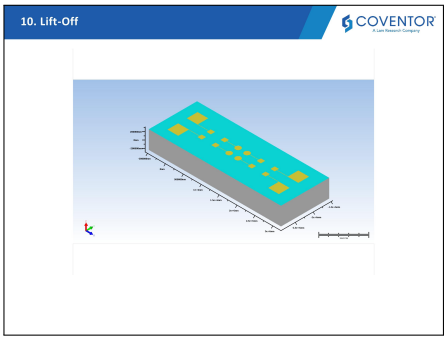

5. DRIE Etch
COVENTOR

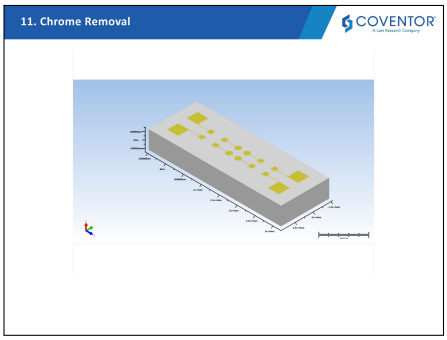

6. BOE Etch
COVENTOR

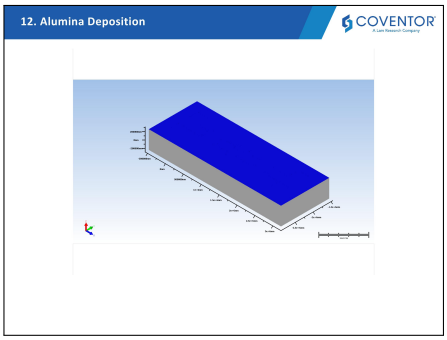

7. Titanium Deposition
COVENTOR

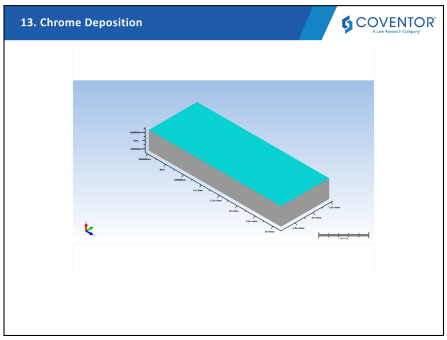

8. Platinum Deposition
COVENTOR

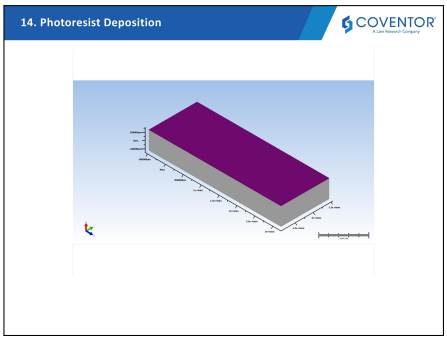

9. Gold Deposition
COVENTOR

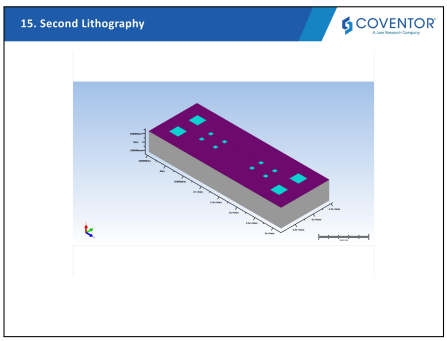

10. Lift-Off
COVENTOR

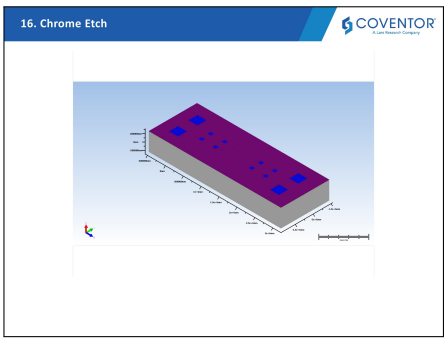

11. Chrome Removal
COVENTOR

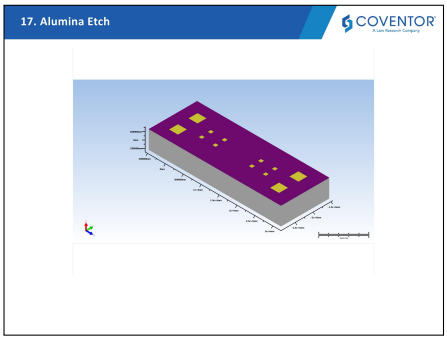

12. Alumina Deposition
COVENTOR

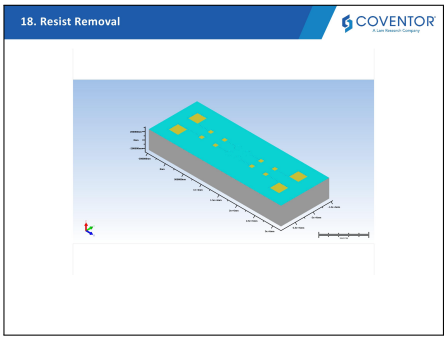

13. Chrome Deposition
COVENTOR

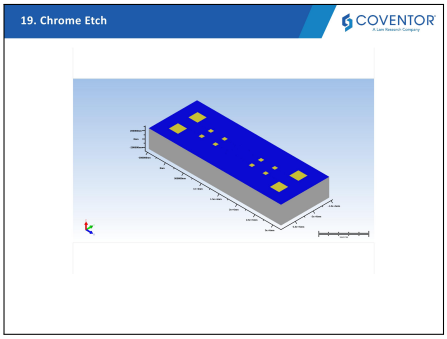

14. Photoresist Deposition
COVENTOR

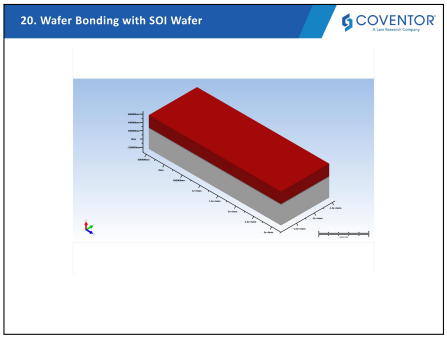

15. Second Lithography
COVENTOR

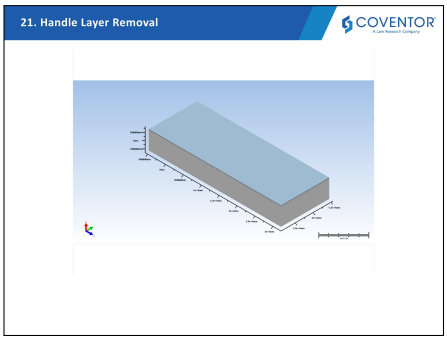

16. Chrome Etch
COVENTOR

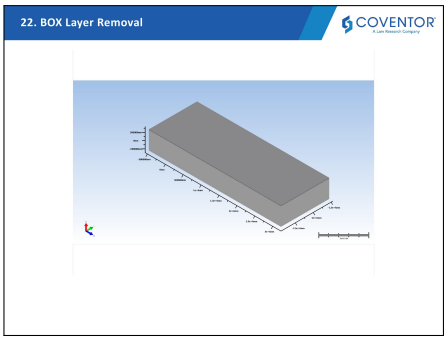

17. Alumina Etch
COVENTOR

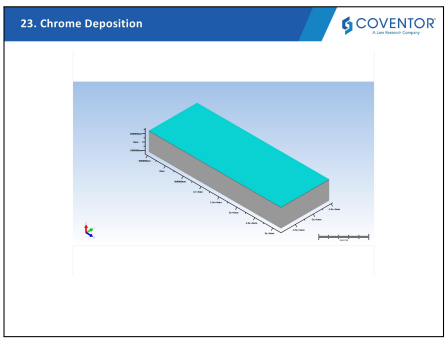

18. Resist Removal
COVENTOR

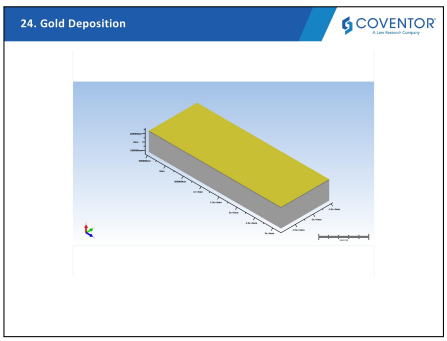

19. Chrome Etch
COVENTOR

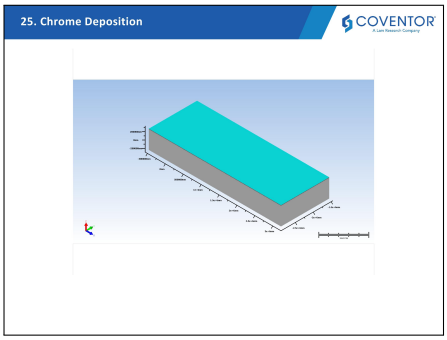

20. Wafer Bonding with SOI Wafer
COVENTOR

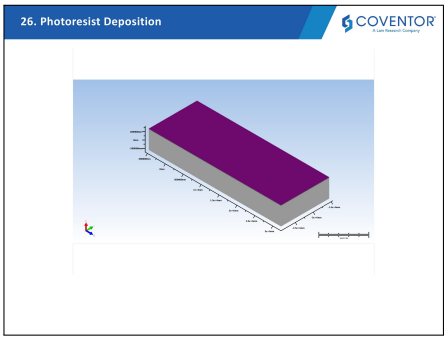

21. Handle Layer Removal
COVENTOR

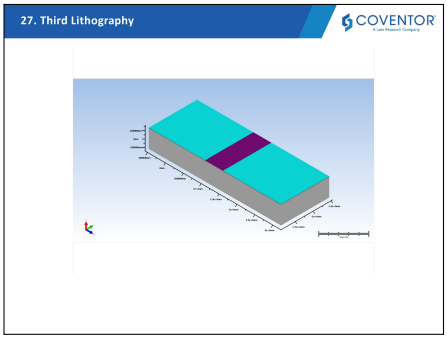

22. BOX Layer Removal
COVENTOR

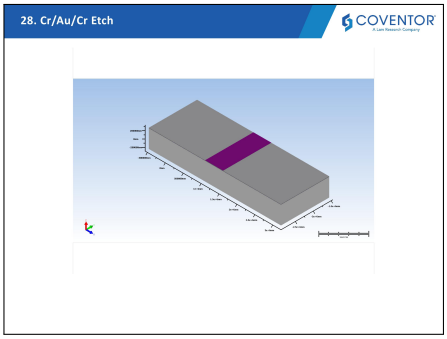

23. Chrome Deposition
COVENTOR

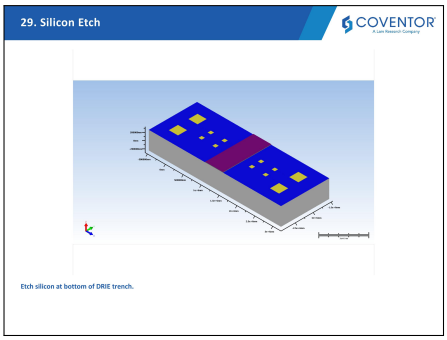

24. Gold Deposition
COVENTOR

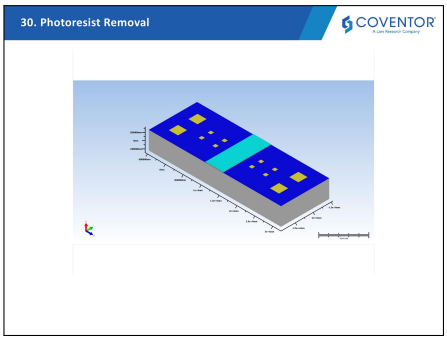

25. Chrome Deposition
COVENTOR

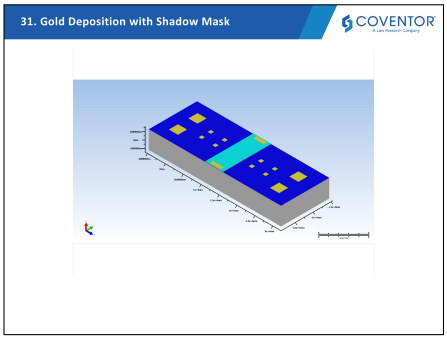

26. Photoresist Deposition
COVENTOR

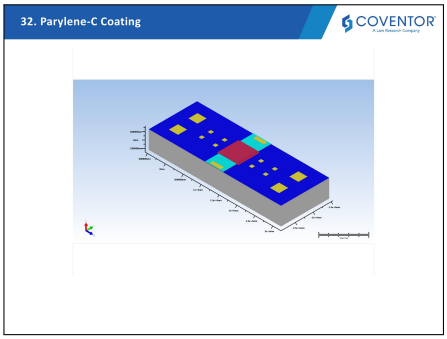

27. Third Lithography
COVENTOR


28. Cr/Au/Cr Etch
COVENTOR


29. Silicon Etch
COVENTOR
Etch silicon at bottom of DRIE trench.


30. Photoresist Removal
COVENTOR


31. Gold Deposition with Shadow Mask
COVENTOR


32. Parylene-C Coating
COVENTOR

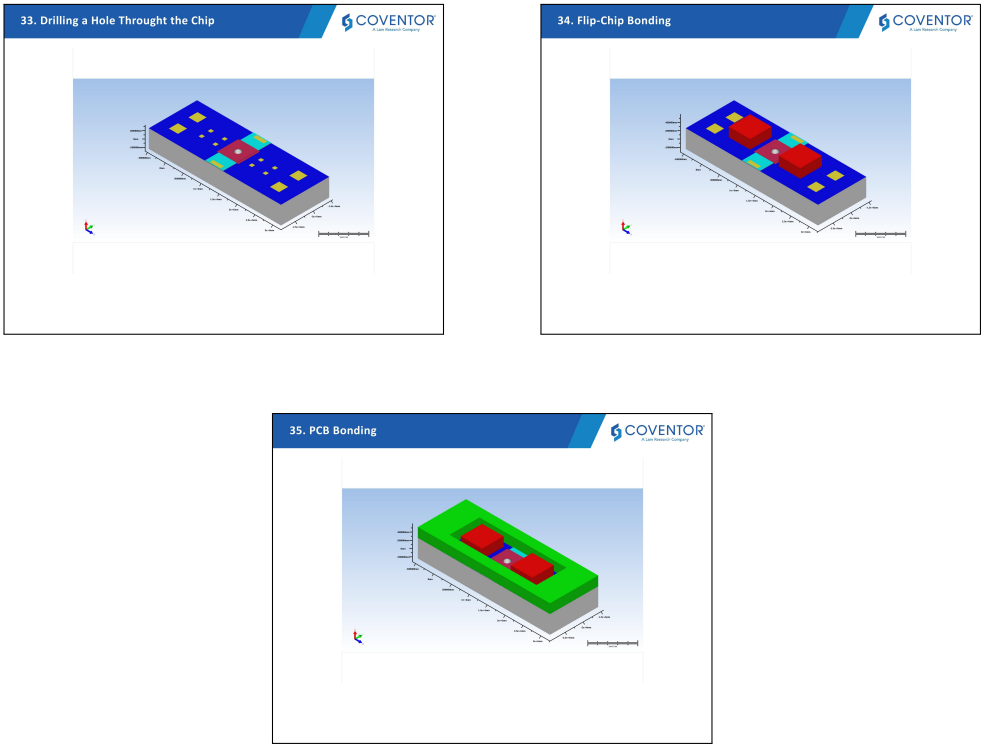


Figure 2.61: 3D process flow drawn by Coventor SEMulator 3D software when the software license was given free of charge due to the COVID-19 pandemic constraints.

Chapter 3

Conclusion

This thesis is about batch-compatible micromanufacturing of CMUT arrays for optoacoustic imaging. On 8 pairs of Pyrex and SOI wafers, the batch-compatible micromanufacturing of CMUT arrays is partially completed till the end of the anodic wafer bonding process. To be able to obtain these 8 pairs of Pyrex wafers and SOI wafers in approximately 30 months of time, approximately 40 Pyrex wafers, and 15 SOI wafers are consumed for process execution, and building sufficient microfabrication process experience. To reduce process expenses, 4-inch SOI wafers, and SOI wafer chips are used only for anodic wafer process development. The rest of all the process learning, and experience building up, have been done on Pyrex wafers or silicon wafers.

CMUT devices are fabricated using micromanufacturing techniques and process equipment in a cleanroom environment (either at Bilkent University UNAM cleanroom, or cleanroom at EVG facilities in Austria) using batch-compatible wafer-scale microfabrication processes. A cavity (i.e. CMUT gap) is defined on the Pyrex wafer using dry and wet etch techniques. The bottom electrode metal stack composed of Ti/Pt/Au is deposited on the cavities by e-beam evaporation physical vapor deposition. The alumina insulator layer is conformally deposited on the entire Pyrex wafer surface for the electrical isolation of the CMUT array gaps. Then, only the relevant electrical connection pad regions are patterned

to remove the insulator material from the electrical pad regions. The patterned Pyrex wafer is bonded to an SOI wafer by anodic wafer bonding approach. The development and optimization of the anodic wafer bonding process is done on trial test chips and 8 pairs of real 4-inch wafers with different anodic bonding process recipes. For the designed entire microfabrication process, three separate photolithography masks and one shadow mask are planned for usage. 3 of these masks are used for processes on Pyrex substrate, while the remaining masks are intended to be used after anodic wafer bonding.

From the available CMUT array microfabrication approaches, conventional anodic wafer bonding is used for CMUT gap formation and fixing the silicon vibrating plate to the Pyrex substrate. To achieve a relatively high yield at the wafer bonding unit process, our research group collaborated with EVG, a major provider of high-volume production equipment for packaging and MEMS/NEMS device micromanufacturing. The anodic wafer bonding process is done at the process facilities of EVG in Austria by developing a suitable bonding recipe with process trials on test chips and 4-inch full-size wafers. Effect of voltage, temperature, waiting time at each voltage step, mechanical force, and surface cleaning process are investigated. According to the information provided by EVG, optical inspection of the test structures and the CMUT array devices at the Pyrex and SOI wafer interface (after anodic wafer bonding) suggests that the anodic wafer bonding process is done successfully with a relatively high yield.

After successful anodic wafer bonding between the real Pyrex wafers and the real SOI wafers, handle layers of the SOI wafers, and BOX layers of the SOI wafers will be etched to reveal the device layers of the SOI wafers. To enhance the conductivity of the silicon device layers, top electrode metal stack (50 nm Cr/ 50 nm Au/ 50 nm Cr) is going to be deposited on top of the entire silicon device layer by blanket e-beam evaporation deposition. Using a shadow mask, the electrical pad wire bonding connection regions (50 nm Cr / 500 nm Au) on top of the top electrode metal stack will be deposited. Then, the blanket deposited Cr/Au/Cr metal stack and Si device layer will be patterned with another photolithography mask. With the defined photoresist mask, Cr wet etch, Au wet etch, and Cr wet etch will be performed to reach the Si device layer surface. Once the Si device

layer surface is revealed, the DRIE process will be used to define the geometry of the Si device layer. At this phase (i.e. after patterning the Si device layer) of the designed integration process flow, the CMUT arrays are fully microfabricated with only three remaining major steps, which are oxygen plasma dry removal of the photoresist mask, sealing of the gap channel openings of CMUT cells by Parylene C deposition, and obtaining individual CMUT array chips that are microfabricated on the 4-inch Pyrex substrates.

In this study, a scanning electron microscopy (SEM) is used for surface inspection and cross-section inspection, a focused ion beam (FIB) is used to obtain fine cross-section information, a mechanical profilometer is used for surface topography inspection, atomic force microscopy is used for fine surface roughness inspection, and resistance measurement module of a semiconductor parameter analyzer is used for electrical inspection to inspect the quality (i.e. resistance) of the metal stack (Ti/Pt/Au) on the Pyrex substrates after the patterning of the insulator layer from the top of the electrical connection pad regions.

As future work, the remaining steps after anodic wafer bonding (which are explained in Chapter 2) will be completed in another Master of Science degree study, by another graduate student.

Bibliography

[1] IO Wygant et al. "Photoacoustic imaging using a two-dimensional CMUT array". In: *Proceedings of the IEEE Ultrasonics Symposium, Rotterdam, The Netherlands*. 2005, pp. 18–21.

[2] MI Haller and BT Khuri-Yakub. "A surface micromachined electrostatic ultrasonic air transducer". In: *1994 Proceedings of IEEE Ultrasonics Symposium*. Vol. 2. IEEE, pp. 1241–1244.

[3] Kevin Brenner et al. "Advances in capacitive micromachined ultrasonic transducers". In: *Micromachines* 10.2 (2019), p. 152.

[4] B. T. Khuri-Yakub et al. "Silicon micromachined ultrasonic transducers". In: *1998 IEEE Ultrasonics Symposium. Proceedings (Cat. No. 98CH36102)*. Vol. 2. 1998, 985–991 vol.2.

[5] Butrus T Khuri-Yakub and Ömer Oralkan. "Capacitive micromachined ultrasonic transducers for medical imaging and therapy". In: *Journal of Micromechanics and Microengineering* 21.5 (Apr. 2011), p. 054004.

[6] Arif S. Ergun, Goksen G. Yaralioglu, and Butrus T. Khuri-Yakub. "Capacitive Micromachined Ultrasonic Transducers: Theory and Technology". In: *Journal of Aerospace Engineering* 16.2 (2003), pp. 76–84.

[7] D.Lin et al. "6F-5 Characterization of Fabrication Related Gap-Height Variations in Capacitive Micromachined Ultrasonic Transducers". In: *2007 IEEE Ultrasonics Symposium Proceedings*. 2007, pp. 523–526.

[8] Arif S Ergun et al. "Capacitive micromachined ultrasonic transducer technology for medical ultrasound imaging". In: *Medical Imaging 2005: Ultrasonic Imaging and Signal Processing*. Vol. 5750. International Society for Optics and Photonics. 2005, pp. 58–68.

[9] Oluwafemi J Adelegan et al. "Fabrication of 2D capacitive micromachined ultrasonic transducer (CMUT) arrays on insulating substrates with through-wafer interconnects using sacrificial release process". In: *Journal of Microelectromechanical Systems* 29.4 (2020), pp. 553–561.

[10] G Caliano et al. "cMUT echographic probes: Design and fabrication process". In: *2002 IEEE Ultrasonics Symposium, 2002. Proceedings.* Vol. 2. IEEE. 2002, pp. 1067–1070.

[11] Linus Elsaesser et al. "Stress controlled CMUT fabrication based on a CMOS compatible sacrificial release process". In: *2015 Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP)*. IEEE. 2015, pp. 1–4.

[12] G Caliano et al. "A cMUT linear array used as echographic probe: Fabrication, characterization, and images". In: *IEEE Ultrasonics Symposium, 2004*. Vol. 1. IEEE. 2004, pp. 395–398.

[13] Emilie Bahette et al. "Progresses in cMUT device fabrication using low temperature processes". In: *Journal of Micromechanics and Microengineering* 24.4 (2014), p. 045020.

[14] A Buhrdorf et al. "Fabrication and characterization of a new capacitive micromachined ultrasonic transducer (cMUT) using polysilicon as membrane and sacrificial layer material". In: *IEEE Symposium on Ultrasonics, 2003*. Vol. 2. IEEE. 2003, pp. 1951–1954.

[15] Joshua Knight, Jeff McLean, and F Levent Degertekin. "Low temperature fabrication of immersion capacitive micromachined ultrasonic transducers on silicon and dielectric substrates". In: *IEEE transactions on ultrasonics, ferroelectrics, and frequency control* 51.10 (2004), pp. 1324–1333.

[16] HT Soh et al. "Silicon micromachined ultrasonic immersion transducers". In: *Applied physics letters* 69.24 (1996), pp. 3674–3676.

[17] Y Huang et al. "Fabrication of Capacitive Micromachined Ultrasonic Transducers (CMUTs) using wafer bonding technology for low frequency (10 kHz-150 kHz) sonar applications". In: *OCEANS'02 MTS/IEEE*. Vol. 4. IEEE. 2002, pp. 2322–2327.

[18] Hui Zhang et al. "Fabrication and Characterization of a wideband low-frequency CMUT array for air-coupled imaging". In: *IEEE Sensors Journal* 20.23 (2020), pp. 14090–14100.

[19] Oluwafemi J Adelegan et al. "Design and fabrication of high-frequency ultra-wideband 1D CMUT arrays for acoustic angiography applications-preliminary results". In: *2018 IEEE International Ultrasonics Symposium (IUS)*. IEEE. 2018, pp. 1–4.

[20] Fikret Yildiz, Tadao Matsunaga, and Yoichi Haga. "CMUT arrays incorporating anodically bondable LTCC for small diameter ultrasonic endoscope". In: *2016 IEEE 11th Annual International Conference on Nano/Micro Engineered and Molecular Systems (NEMS)*. IEEE. 2016, pp. 50–53.

[21] Fikret Yildiz, Tadao Matsunaga, and Yoichi Haga. "Fabrication and packaging of CMUT using low temperature co-fired ceramic". In: *Micromachines* 9.11 (2018), p. 553.

[22] Shawn J Cunningham and Mario Kupnik. "Wafer bonding". In: *MEMS Materials and Processes Handbook*. Springer, 2011, pp. 817–877.

[23] K.R. Williams, K. Gupta, and M. Wasilik. "Etch rates for micromachining processing-Part II". In: *Journal of Microelectromechanical Systems* 12.6 (2003), pp. 761–778.

[24] Hyo-Seon Yoon et al. "Fabrication of CMUT cells with gold center mass for higher output pressure". In: *AIP conference proceedings*. Vol. 1359. 1. American Institute of Physics. 2011, pp. 183–188.

[25] Zhou Zheng et al. "Development of a novel CMUT-based concentric dual-element ultrasonic transducer: Design, fabrication, and characterization". In: *Journal of Microelectromechanical Systems* 27.3 (2018), pp. 538–546.

[26] Norihisa Miki and SM Spearing. "Effect of nanoscale surface roughness on the bonding energy of direct-bonded silicon wafers". In: *Journal of Applied Physics* 94.10 (2003), pp. 6800–6806.

[27] Ravindra Mukhiya et al. "Fabrication of Capacitive Micromachined Ultrasonic Transducer Arrays With Isolation Trenches Using Anodic Wafer Bonding". In: *IEEE Sensors Journal* 15.9 (2015), pp. 5177–5184.

[28] F. Yalcın Yamaner, Xiao Zhang, and Ömer Oralkan. "A three-mask process for fabricating vacuum-sealed capacitive micromachined ultrasonic transducers using anodic bonding". In: *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control* 62.5 (2015), pp. 972–982.

[29] Albert IH Chen et al. "Practical CMUT fabrication with a nitride-to-oxide-based wafer bonding process". In: *Journal of Microelectromechanical Systems* 26.4 (2017), pp. 829–836.

[30] Gerald Gerlach and Wolfram Dotzel. *Introduction to microsystem technology: a guide for students*. John Wiley & Sons, 2008.

[31] Tahereh Arezoo Emadi and Douglas A Buchanan. "Design and Fabrication of a Novel MEMS Capacitive Transducer With Multiple Moving Membrane". In: *IEEE Transactions on Electron Devices* 61.3 (2014), pp. 890–896.

[32] Wook Lee et al. "Fabrication and characterization of a micromachined acoustic sensor with integrated optical readout". In: *IEEE Journal of Selected Topics in Quantum Electronics* 10.3 (2004), pp. 643–651.

[33] Abdullah İrfan YAŞAR and Fikret YILDIZ. "Investigation of different membrane materials effects in CMUT membrane behaviour". In: *2019 3rd international symposium on multidisciplinary studies and innovative technologies (ISMSIT)*. IEEE. 2019, pp. 1–4.

[34] Mengli Wang et al. "Fabrication and characterization of surface micromachined CMUT with a bossed membrane". In: *2008 IEEE Ultrasonics Symposium*. IEEE. 2008, pp. 394–397.

[35] Mustafa Mert Torunbalci, Said Emre Alper, and Tayfun Akin. "Wafer level hermetic sealing of MEMS devices with vertical feedthroughs using anodic bonding". In: *Sensors and Actuators A: Physical* 224 (2015), pp. 169–176.

[36] Vasilis F Pavlidis, Ioannis Savidis, and Eby G Friedman. *Three-dimensional integrated circuit design*. Newnes, 2017.

[37] Azadeh Moini et al. "Fabrication, Packaging, and Catheter Assembly of 2D CMUT Arrays for Endoscopic Ultrasound and Cardiac Imaging". In: *International Electronic Packaging Technical Conference and Exhibition*. Vol. 56901. American Society of Mechanical Engineers. 2015, V003T07A008.

[38] J Due-Hansen et al. "Fabrication process for CMUT arrays with polysilicon electrodes, nanometre precision cavity gaps and through-silicon vias". In: *Journal of Micromechanics and Microengineering* 22.7 (2012), p. 074009.

[39] Ira O Wygant et al. "Integration of 2D CMUT arrays with front-end electronics for volumetric ultrasound imaging". In: *IEEE transactions on ultrasonics, ferroelectrics, and frequency control* 55.2 (2008), pp. 327–342.

[40] EJ Cheng and Y-L Shen. "Thermal expansion behavior of through-silicon-via structures in three-dimensional microelectronic packaging". In: *Microelectronics Reliability* 52.3 (2012), pp. 534–540.

[41] Simon J Bleiker et al. "High-aspect-ratio through silicon vias for high-frequency application fabricated by magnetic assembly of gold-coated nickel wires". In: *IEEE Transactions on components, packaging and Manufacturing technology* 5.1 (2014), pp. 21–27.

[42] Jong-Min Yook, Dongsu Kim, and Jun Chul Kim. "High performance IPDs (Integrated passive devices) and TGV (Through glass via) interposer technology using the photosensitive glass". In: *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)*. Ieee. 2014, pp. 41–46.

[43] Fu-rong Yao et al. "Ultra-low temperature anodic bonding of silicon and glass based on nano-gap dielectric barrier discharge". In: *Journal of Central South University* 28.2 (2021), pp. 351–360.

[44] A Schorderet, E Deghilage, and K Agbeviade. "Tool type and hole diameter influence in deep ultrasonic drilling of micro-holes in glass". In: *Procedia CIRP* 6 (2013), pp. 565–570.

[45] H Nouraei et al. "Surface evolution models for abrasive slurry jet micromachining of channels and holes in glass". In: *Wear* 309.1-2 (2014), pp. 65–73.

[46] Ciprian Iliescu, Bangtao Chen, and Jianmin Miao. "Deep wet etching-through 1mm pyrex glass wafer for microfluidic applications". In: *2007 IEEE 20th International Conference on Micro Electro Mechanical Systems (MEMS)*. IEEE. 2007, pp. 393–396.

[47] JH Park et al. "Deep dry etching of borosilicate glass using SF6 and SF6/Ar inductively coupled plasmas". In: *Microelectronic engineering* 82.2 (2005), pp. 119–128.

[48] H Schröder et al. "glassPack—A 3D glass based interposer concept for SiP with integrated optical interconnects". In: *2010 Proceedings 60th Electronic Components and Technology Conference (ECTC)*. IEEE. 2010, pp. 1647–1652.

[49] Aric B Shorey and Rachel Lu. "Progress and application of through glass via (TGV) technology". In: *2016 Pan Pacific Microelectronics Symposium (Pan Pacific)*. IEEE. 2016, pp. 1–6.

[50] Fan Yang et al. "Research on wafer-level mems packaging with through-glass vias". In: *Micromachines* 10.1 (2019), p. 15.

[51] Chen-Kuei Chung and SL Lin. "CO2 laser micromachined crackless through holes of Pyrex 7740 glass". In: *International Journal of Machine Tools and Manufacture* 50.11 (2010), pp. 961–968.

[52] R Böhme, K Zimmer, and B Rauschenbach. "Laser backside etching of fused silica due to carbon layer ablation". In: *Applied Physics A* 82.2 (2006), pp. 325–328.

[53] Norio Chujo et al. "LTCC package for high-bandwidth logic to memory interconnection". In: *2015 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS)*. IEEE. 2015, pp. 5–8.

[54] AY Usenko and WN Carr. "Silicon-on-insulator technology for microelectromechanical applications". In: *Semiconductor Physics Quantum Electronics & Optoelectronics* (1999).

[55] Yongli Huang et al. "Fabricating capacitive micromachined ultrasonic transducers with wafer-bonding technology". In: *Journal of Microelectromechanical Systems* 12.2 (2003), pp. 128–137.

[56] F Yalcin Yamaner, Xiao Zhang, and Ömer Oralkan. "Fabrication of anodically bonded capacitive micromachined ultrasonic transducers with vacuum-sealed cavities". In: *2014 IEEE International Ultrasonics Symposium*. IEEE. 2014, pp. 604–607.

[57] Afshin Kashani Ilkhechi et al. "Transparent capacitive micromachined ultrasonic transducer (CMUT) arrays for real-time photoacoustic applications". In: *Optics express* 28.9 (2020), pp. 13750–13760.

[58] E Belloy et al. "The introduction of powder blasting for sensor and microsystem applications". In: *Sensors and Actuators A: Physical* 84.3 (2000), pp. 330–337.

[59] J.A. Plaza et al. "Definition of high aspect ratio glass columns". In: *Sensors and Actuators A: Physical* 105.3 (2003), pp. 305–310.

[60] S. Nikumb et al. "Precision glass machining, drilling and profile cutting by short pulse lasers". In: *Thin Solid Films* 477.1 (2005). ICMAT 03, pp. 216–221.

[61] Chantal Khan Malek et al. "Deep microstructuring in glass for microfluidic applications". en. In: *Microsystem Technologies* 13.5-6 (Jan. 2007), pp. 447–453.

[62] Thierry Corman, Peter Enoksson, and Göran Stemme. "Deep wet etching of borosilicate glass using an anodically bonded silicon substrate as mask". In: *Journal of Micromechanics and Microengineering* 8.2 (June 1998), pp. 84–87.

[63] Junting Liu et al. "Etch rate and surface morphology of plasma etched glass and glass-ceramic substrates". In: *Journal of Non-Crystalline Solids* 342.1 (2004), pp. 110–115.

[64] Alexander A. Oraevsky et al. "Optoacoustic imaging of blood for visualization and diagnostics of breast cancer". In: *Biomedical Optoacoustics III*. Ed. by Alexander A. Oraevsky. Vol. 4618. International Society for Optics and Photonics. SPIE, 2002, pp. 81–94.

[65] A. C. Tam and G. Ayers. "Ultrasonic imaging of layered structures utilizing nondestructive subnanosecond photoacoustic pulse generation". In: *Applied Physics Letters* 49.21 (1986), pp. 1420–1422.

[66] Jingkuang Chen et al. "A photoacoustic imager with light illumination through an infrared-transparent silicon CMUT array". In: *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control* 59.4 (2012), pp. 766–775.

[67] *Optical Transmission – American Scientific Glassblowers Society*. en-US. URL: `https://asgs-glass.org/optical-transmission/` (visited on 06/21/2021).

[68] Sarveshvaran Suppiah et al. "A review on solder reflow and flux application for flip chip". In: *AIP Conference Proceedings* 1885.1 (2017), p. 020264.

[69] J. Jordan. "Gold stud bump in flip-chip applications". In: *27th Annual IEEE/SEMI International Electronics Manufacturing Technology Symposium*. 2002, pp. 110–114.

[70] Sun-Chul Kim and Young-Ho Kim. "Review paper: Flip chip bonding with anisotropic conductive film (ACF) and nonconductive adhesive (NCA)". In: *Current Applied Physics* 13 (2013). Special Issue: ENGE 2012, S14–S25.

[71] Horst Clauberg et al. "Advanced thermocompression flip chip bonding". In: *2014 IEEE 16th Electronics Packaging Technology Conference (EPTC)*. 2014, pp. 492–495.

[72] Fuliang Wang and Yun Chen. "Modeling study of thermosonic flip chip bonding process". In: *Microelectronics Reliability* 52.11 (2012), pp. 2749–2755.

[73] Yasuyuki Kushida et al. "Practical use of hard mask process to fabricate fine photomasks for 45nm node and beyond". In: *24th European Mask and Lithography Conference*. 2008, pp. 1–10.

[74] AS Erguri et al. "Capacitive micromachined ultrasonic transducers: Fabrication technology". In: *IEEE transactions on ultrasonics, ferroelectrics, and frequency control* 52.12 (2005), pp. 2242–2258.

[75] Mohamed Bellaredj et al. "Anodic bonding using SOI wafer for fabrication of capacitive micromachined ultrasonic transducers". In: *Journal of Micromechanics and Microengineering* 24.2 (2014), p. 025009.

[76] J Wei et al. "Low temperature wafer anodic bonding". In: *Journal of Micromechanics and Microengineering* 13.2 (2003), p. 217.

[77] Petra Nitzsche et al. "Ion drift processes in Pyrex-type alkali-borosilicate glass during anodic bonding". In: *Journal of the Electrochemical Society* 145.5 (1998), p. 1755.

[78] Dongqing Li. *Encyclopedia of microfluidics and nanofluidics*. Springer Science & Business Media, 2008.

[79] J Wei et al. "Role of bonding temperature and voltage in silicon-to-glass anodic bonding". In: *4th Electronics Packaging Technology Conference, 2002.* IEEE. 2002, pp. 85–90.

[80] Ram Gopal et al. "Fabrication of MEMS xylophone magnetometer by anodic bonding technique using SOI wafer". In: *Microsystem Technologies* 23.1 (2017), pp. 81–90.

[81] George Wallis and Daniel I. Pomerantz. "Field Assisted Glass-Metal Sealing". en. In: *Journal of Applied Physics* 40.10 (Sept. 1969), pp. 3946–3949.

[82] Yohei Yuda et al. "Anodic Bonding of Transparent Conductive Oxide Coated Silicon Wafer to Glass Substrate for Solar Cell Applications". In: *Applied Physics Express* 6.1 (Jan. 2013), p. 012302.

[83] Shari Farrens, S Sood, and SUSS MicroTec. "Wafer level packaging: Balancing device requirements and materials properties". In: *Proc. Pan Pacific Microelectron. Symp.* 2014, pp. 22–24.

[84] H. Okamoto and T. B. Massalski. "The AuSi (Gold-Silicon) system". en. In: *Bulletin of Alloy Phase Diagrams* 4.2 (Sept. 1983), pp. 190–198.

[85] Banqiu Wu, Ajay Kumar, and Sharma Pamarthy. "High aspect ratio silicon etch: A review". In: *Journal of applied physics* 108.5 (2010), p. 9.