

Accurate and Process-Tolerant Resistive Load

Batuhan Sutbas¹, Ekmel Ozbay, *Member, IEEE*, and Abdullah Atalar, *Fellow, IEEE*

Abstract—Resistive terminations cannot preserve high-quality matching at high frequencies due to the parasitic effects of the nonideal resistor. Moreover, resistance values of the termination resistors in integrated circuits are subject to process variations. Therefore, it is difficult to obtain accurate and process-tolerant terminations that are crucial for high performance in microwave circuits. We propose a new resistive network that compensates for the high-frequency parasitic effects of the resistors to improve the bandwidth of the termination. In addition to maintaining accuracy, the presented network provides tolerance to variation in the resistor values. The accuracy and tolerance of the proposed structure is analytically shown and experimentally verified by three test structures at the X-band fabricated on a GaN technology. The experimental results show that a small size and wideband 50- Ω load with a return loss better than 25 dB can be obtained, while the resistor value changes $\pm 30\%$.

Index Terms—Accurate, integrated circuit, parasitic effect, process-temperature variation, resistor, sheet resistance, termination, tolerance, via inductance, wideband.

I. INTRODUCTION

RESISTORS are used in the load termination networks of microwave circuits, such as couplers, dividers, and balanced and distributed amplifiers. Bandwidth and performance of the circuits are significantly dependent on the load accuracy. However, parasitic effects associated with the resistor and changes in the resistor value due to process variations limit the accuracy of the load.

A real resistor exhibits parasitic capacitive or inductive effects limiting the useful bandwidth. Early efforts focused on avoiding a direct ground connection to reduce inductive effects and achieve broadband characteristics [1]. Researchers used nongrounded loads with open [2] and radial [3] stubs along with branched [4], compensated [5], and ellipse-shaped [6] terminations. With known resistor characteristics at high frequencies, it is also possible to design an additional circuitry

that cancels the parasitic effects and increases the highest operating frequency [7]–[9]. However, these approaches require an accurate model for the parasitics of the resistive elements and they do not compensate for the manufacturing variations in the value of the intrinsic resistor, limiting their usefulness. More recently, the emerging use of carbon nanotubes [10] and 2-D inkjet printing [11] have also facilitated unconventional methods to fabricate wideband loads.

The resistance value of the intrinsic resistor is somewhat variable since the fabrication processes have tolerance and repeatability limits. For instance, the thickness of the thin-film resistors may be different in successive processes or even in wafers from the same fabrication batch which changes the sheet resistance value. For higher yield and better circuit performance, this variation has to be considered at the design step and the tolerance of the load network needs to be increased. This procedure is vital, especially in the case of integrated circuits, as it is difficult to have a tuning mechanism after the fabrication.

Resistance variances of discrete resistors in a discrete circuit are independent of each other. On the contrary, the resistances of resistors in an integrated circuit or in a thick-film circuit are related to each other by the fabrication process itself and change in the same direction. Resistors in close proximity have almost identical sheet resistance regardless of the deviation from the nominal value. When the process has a higher sheet resistance than its nominal value, all resistors in the same integrated circuit have higher resistance values. Similarly, high-frequency parasitic capacitors of the resistors are dependent on the substrate that they share, hence, resistors in the same area show a similar parasitic capacitance. Also, when the resistors are identical in size, they exhibit an equal parasitic inductance.

In this article, we use this correlated behavior of resistors in integrated and thick-film circuits to realize a novel accurate resistive load with parasitic effect cancellation, which does not require previous knowledge of the resistor parasitics. Although our proposed technique is not as useful for providing tolerance to variations in discrete circuits, it can still achieve parasitic effect cancellation and can be utilized in discrete load networks. The presented load network can easily be integrated with RF components, such as couplers and balanced amplifiers for performance, bandwidth, and tolerance improvement.

Our proposed structure consists of two resistors in parallel where one of the resistors is transformed by a quarter-wave length transmission line. The idea is that the change in the resistances of the two parallel resistors is in the opposite direction after quarter-wave transformation, providing tolerance to variations in resistor values in a wide bandwidth.

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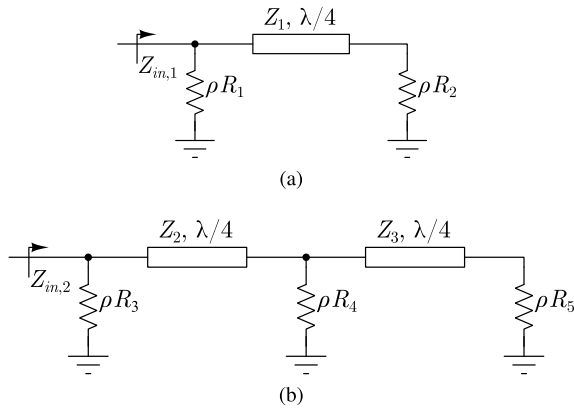


Fig. 1. Schematic of the proposed accurate and process tolerant resistive load network. (a) First-order ($N = 1$). (b) Second-order ($N = 2$).

Moreover, our proposed topology compensates for the parasitic effects of the resistor including via inductance, improving the high-frequency response and enabling higher bandwidth. As the integrated circuit frequency moves toward the millimeter-wave region, it becomes a necessity to use such a structure since parasitic components dominate the intrinsic resistor. One drawback of the presented approach is that the circuit occupies more area because it requires a quarter-wave length transmission line. Nevertheless, the additional high-impedance transmission line can be meandered for a smaller size without bandwidth degradation. We demonstrate that the miniaturized structure also achieves high performance in a wideband with high sheet resistance tolerance.

The relation between sheet resistance tolerance, return loss, and bandwidth is shown analytically. We derive an equation for the improvement in return loss compared with a single resistor when the resistor model with parasitic effects is incorporated. Three test structures are fabricated with a GaN on SiC microstrip monolithic microwave integrated circuit (MMIC) technology and demonstrate that our proposed technique is applicable at the X-band. Studies have shown that the reliability and accuracy of sheet resistance in a fabrication process can be improved to implement accurate loads [12], [13]. However, to the best of our knowledge, this is the first work that obtains a sheet resistance tolerance using an improved design.

II. ANALYSIS AND DESIGN

A. Analysis for Sheet Resistance Variance

Our proposed network for the resistive termination is shown in Fig. 1(a). R_1 and R_2 are two shunt resistors without parasitics separated by a quarter-wavelength transmission line with a characteristic impedance of Z_1 . We should have

$$Z_1 = R_1 = R_2 = 2Z_0 \quad (1)$$

with perfect matching. In our analysis, ρ represents the normalized sheet resistance that is ideally equal to 1 but is defined by the manufacturing process. For $\rho < 1$, both ρR_1 and ρR_2 have a resistance value below the nominal design resistance values. However, the impedance seen into the network, $Z_{in,1}$, does not drop by the same ratio because the quarter-wave

transformed impedance $Z_1^2/(\rho R_2)$ increases and compensates for the decrease in ρR_1 . Similarly, for $\rho > 1$, the deviations from nominal values are in opposite direction and the overall impedance changes by a much smaller amount. The presence of a quarter-wavelength line does not cause a bandwidth reduction since the load and the characteristic impedance have nearly the same values. The proposed structure uses the fact that the variation in Z_1 is considerably less than that in ρ .

Sheet resistance tolerance and bandwidth of the circuit can be improved further by adding another shunt resistor and quarter-wavelength transmission line, as shown in Fig. 1(b). Here, R_4 , Z_3 , and R_5 form a network similar to the first-order load. The additional quarter-wavelength line Z_2 transforms the impedance seen into this network to compensate for the change in ρR_3 , greatly reducing the overall deviation in $Z_{in,2}$.

To obtain a first-order load network with reflection coefficient smaller than a limit level of δ , the following inequality has to hold:

$$|\Gamma_{in,1}| = \left| \frac{Z_{in,1} - Z_0}{Z_{in,1} + Z_0} \right| < \delta \quad (2)$$

where the impedance seen into the network for (1) is

$$Z_{in,1} = 2Z_0 \frac{\rho^2 + jT\rho}{2\rho + jT(1 + \rho^2)}. \quad (3)$$

Here, Z_0 is the reference characteristic impedance and $T = \tan(\pi \hat{f}/2)$ with $\hat{f} = f/f_0$, where f_0 is the design center frequency. Then, the reflection coefficient simplifies to

$$|\Gamma_{in,1}| = \sqrt{\frac{(\rho - 1)^2 4\rho^2 + T^2(\rho - 1)^2}{(\rho + 1)^2 4\rho^2 + T^2(\rho + 1)^2}} < \delta \quad (4)$$

and the fractional bandwidth (FBW = BW/ f_0) in terms of ρ and δ becomes

$$\text{FBW} = \left| 2 - \frac{4}{\pi} \arctan \sqrt{\frac{4\rho^2(\rho - 1)^2 - \delta^2(\rho + 1)^2}{\delta^2(\rho + 1)^4 - (\rho - 1)^4}} \right|. \quad (5)$$

Although a single ideal termination resistor with resistance Z_0 does not have bandwidth limitation, for $\rho \neq 1$, it can only achieve a reflection coefficient of Γ_0 given by

$$|\Gamma_0| = \frac{|\rho Z_0 - Z_0|}{\rho Z_0 + Z_0} = \frac{|\rho - 1|}{\rho + 1} < \delta. \quad (6)$$

For a desired matching level of $\delta = 0.056$ (25 dB return loss), the sheet resistance tolerance should be less than 12%.

The resistor and the line impedance values given in (1) can be optimized to achieve a wider bandwidth, by sacrificing the perfect match condition at the center frequency. In the general case, the impedance seen into the first-order network is

$$Z_{in,1} = \frac{Z_1 \rho^2 R_1 R_2 + jT Z_1^2 \rho R_1}{Z_1 \rho (R_1 + R_2) + jT (Z_1^2 + \rho^2 R_1 R_2)}. \quad (7)$$

For instance, a first-order load of Fig. 1(a) with $Z_1 = 1.9Z_0$, $R_1 = 2.4Z_0$, and $R_2 = 1.8Z_0$ achieves a 25-dB return loss in a 30% FBW despite a 48% variation in sheet resistance, while a circuit using (1) could tolerate up to 34% variation within the same bandwidth.

In Fig. 2, we plot the 25-dB FBW of the first-order network based on (5) along with optimized¹ first- and second-order

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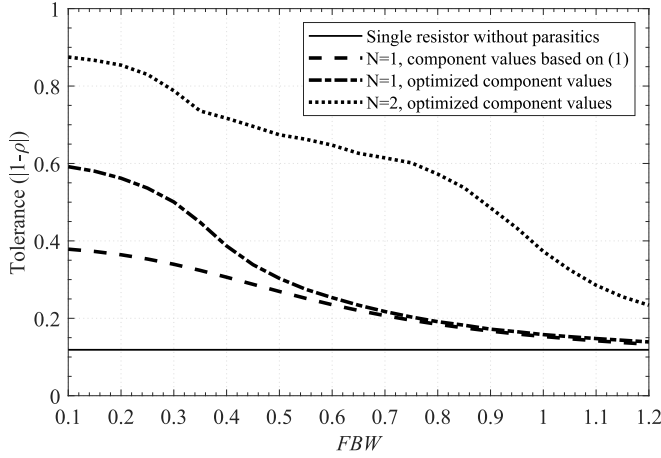


Fig. 2. Achievable sheet resistance tolerance level versus FBW for 25-dB ($\delta = 0.056$) return loss using a single resistor without parasitics and using our proposed network.

networks. The proposed networks always provide better sheet resistance tolerance levels than a single resistor, but the improvement gradually decreases as the bandwidth of operation is increased. For narrowband applications, the proposed first-order network can provide sheet resistance tolerances higher than 60% for a 25-dB load compared with 12% of a single resistor without parasitics.

It is possible to add more sections and increase the order of the network N for further improvement in tolerance and matching levels. However, we note that the improvement diminishes and becomes insignificant after $N = 3$. The additional degrees of freedom in higher order networks can be used to find the component values that are more suitable or easily realizable. For example, a second-order load of Fig. 1(b) with $Z_2 = 1.3Z_0$, $Z_3 = 2.5Z_0$, $R_3 = 4.6Z_0$, $R_4 = 2.8Z_0$, and $R_5 = 2Z_0$ achieves a 25-dB return loss in an FBW of 80% despite more than 50% variation in sheet resistance.

The very high sheet resistance tolerance obtained by the network not only increases the accuracy but also enables the proposed circuits to be placed inside the normally unusable area in wafers with high variation in process parameters, essentially increasing the number of devices fabricated per wafer. Furthermore, the high tolerance enables the load circuit to work with high temperature variations.

In addition to the increase in sheet resistance tolerance, the proposed network has an increased power-handling capability due to the higher number of resistors connected to the ground.

B. Analysis for Parasitic Effect Cancellation

The lumped element model of a shunt resistor is shown in Fig. 3: R_i represents the intrinsic resistance, L_i is the intrinsic inductance to account for the finite electrical length of the resistor, C_g is the capacitance, and L_v is the via inductance.

We replace R_1 and R_2 in our first-order network with a resistor model with unknown parameters to analyze the parasitic effect cancellation, assuming that the real part of the impedance seen looking into the resistor is only dependent

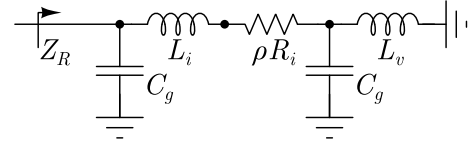


Fig. 3. Lumped element model of a shunt thin-film resistor.

on the intrinsic resistance, $\text{Re}\{Z_R\} = \rho R_i$. The reflection coefficient of a single resistor with respect to Z_0 becomes

$$|\Gamma_1| = \left| \frac{\bar{Z} - 1}{\bar{Z} + 1} \right| \quad (8)$$

where $\bar{Z} = \rho + j\bar{X}$ is the normalized impedance and $\bar{X} = \text{Im}\{Z_R/Z_0\}$ is the normalized parasitic reactance. For a comparison with our proposed structure, we use two of such resistors with an intrinsic resistance of $2\rho Z_0$, both of which have a normalized parasitic reactance of $2\bar{X}$, separated by a quarter-wavelength transmission line with $Z_1 = 2\alpha Z_0$ as in (1). Here, we further consider a variation in the characteristic impedance of the transmission line by a factor of α . We find the reflection coefficient with respect to Z_0 as

$$|\Gamma_2| = \left| \frac{\frac{\bar{Z}_T}{2\bar{Z}} - 1}{\frac{\bar{Z}_T}{2\bar{Z}} + 1} \right| \quad (9)$$

where the normalized quarter-wave transformed impedance is

$$\bar{Z}_T = 2\alpha \frac{\bar{Z} + jaT}{\alpha - jT\bar{Z}}. \quad (10)$$

Then, the reflection coefficient in terms of α , \bar{Z} , and T is

$$|\Gamma_2| = \left| \frac{\alpha^2 T (2\bar{Z} - 1) - T\bar{Z}^2 - j2\alpha(\bar{Z}^2 - \bar{Z})}{\alpha^2 T (2\bar{Z} + 1) + T\bar{Z}^2 - j2\alpha(\bar{Z}^2 + \bar{Z})} \right|. \quad (11)$$

The characteristic impedance of a line is a more stable parameter since it changes more slowly with deviations in the physical parameters, such as the height and dielectric constant of the substrate and the width of the transmission line. Hence, the sheet resistance variance and parasitic effects are more dominant. The reflection coefficients for $0.95 \leq \alpha \leq 1.05$ are calculated using the resistor model parameters for our substrate and plotted in Fig. 4 for a center frequency of 10 GHz along with the reflection coefficient of a single resistor.

The proposed network achieves better matching than a single resistor at all frequencies even in the case of an unlikely deviation from the desired line impedance. With $\alpha = 1$, the improvement in return loss can be simplified as

$$\left| \frac{\Gamma_2}{\Gamma_1} \right| = \left| \frac{T(\bar{Z} - 1) + j2\bar{Z}}{T(\bar{Z} + 1) + j2\bar{Z}} \right| \quad (12)$$

and is 0 dB at the worst case (for $T = 0$), which shows that our proposed network never performs worse than a single resistor

$$\lim_{T \rightarrow \infty} \left| \frac{\Gamma_2}{\Gamma_1} \right| = \left| \frac{\bar{Z} - 1}{\bar{Z} + 1} \right| = |\Gamma_1|. \quad (13)$$

For odd multiples of the center frequency (when $T \rightarrow \infty$), (13) shows that the proposed structure doubles the return loss

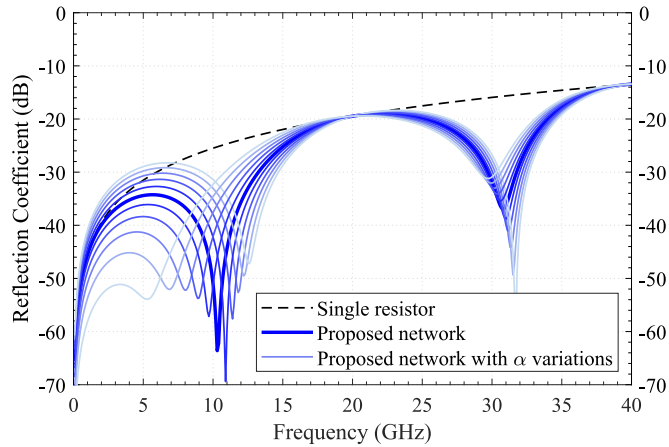


Fig. 4. Reflection coefficients of a single resistor and the proposed network ($N = 1$) with variations in the transmission-line characteristic impedance as a function of frequency using the extracted model parameters ($L_i = 77$ pH, $C_g = 11$ fF, and $L_v = 35$ pH) of a 53- μm -wide high power 50- Ω resistor.

(in dB-scale) of a single resistor, irrespective of the sheet resistance variance and the parasitic values.

The proposed method can be combined with other parasitic cancellation techniques given in the literature to achieve even higher performance levels with an additional benefit of sheet resistance tolerance and higher power-handling capability. For instance, $N + 1$ of the matched loads with radial stubs described in [3] can be separated by N quarter-wavelength lines in the form of an N order accurate and process-tolerant resistive load network to obtain superior performance than the original matched loads with the additional benefit of having tolerance to variation in process and operating conditions. We note that the bandwidth of the original parasitic cancellation technique will not be reduced because our analysis treats the single resistor as a black box, and thus, (12) and its implications apply to any type of termination network. On a separate note, the parasitic effect cancellation of the presented technique can be utilized in discrete circuits by selecting the resistor parts from the same supplier, as they show a similar parasitic behavior.

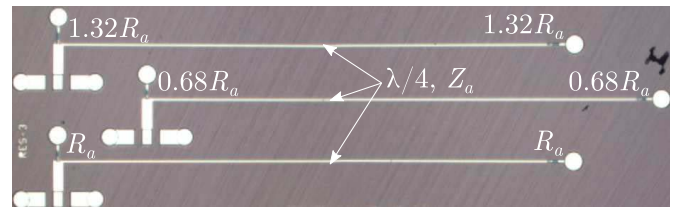
III. EXPERIMENTAL RESULTS

Three test structures (TS-A, TS-B, and TS-C) at 10 GHz are fabricated to demonstrate the proposed technique that provides sheet resistance tolerance and parasitic effect cancellation. Each test structure is composed of an $N = 1$ termination network with three variants. The first variant uses the nominal resistor, whereas the other two variants have deliberately changed resistor values to simulate the manufacturing variance.

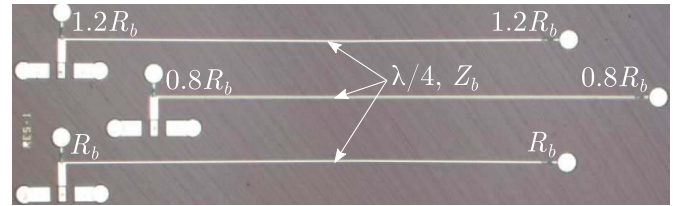
In TS-A, shown in Fig. 5(a), the nominal resistor value is $R_a = 105 \Omega$. The quarter-wave length line widths are 10 μm ($Z_a = 102 \Omega$). SEM image of R_a is shown in Fig. 6 with the measured length and width of 35 and 10 μm , respectively.

In TS-B, shown in Fig. 5(b), we have $R_b = 100 \Omega$. The quarter-wave length line widths are 12 μm ($Z_b = 99 \Omega$).

The compact loads in test structure TS-C, shown in Fig. 7, use meandered lines for smaller footprints compared with the



(a)



(b)

Fig. 5. Microscope photograph of (a) TS-A with $\pm 32\%$ resistance variation and (b) TS-B with $\pm 20\%$ resistance variation.

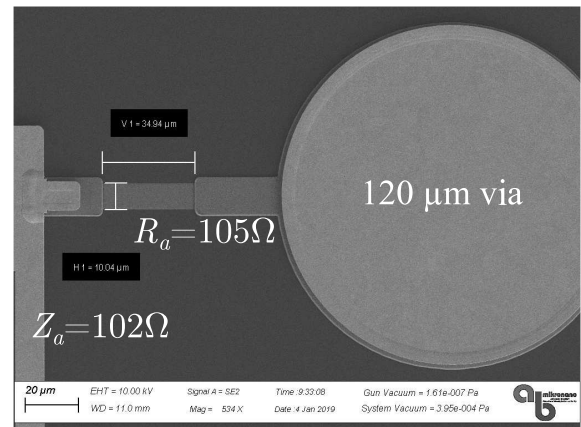


Fig. 6. SEM image of the nominal resistor in the first variant of TS-A.

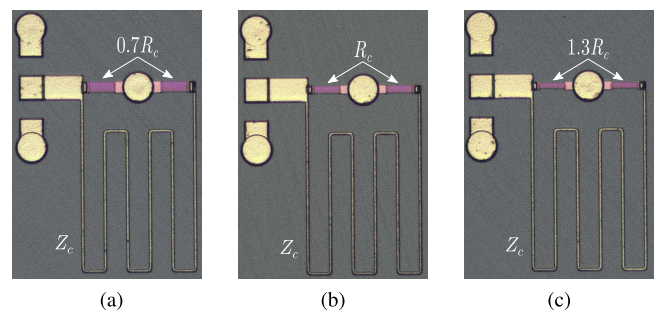


Fig. 7. Microscope photograph of TS-C with (a) smaller resistances ($\rho = 0.7$), (b) nominal resistances ($\rho = 1$), and (c) larger resistances ($\rho = 1.3$).

loads in TS-A and TS-B. The resistors are oriented in the same direction next to each other and connected to the ground using the same via hole. We use $R_c = 101 \Omega$ and $Z_c = 102 \Omega$. The sizes of the termination networks in TS-C without the measurement pads are less than 0.47 mm \times 0.82 mm.

All the test structures with their variations are fabricated using our in-house GaN monolithic microwave integrated circuit (MMIC) process with two metal (Au) layers and a

TABLE I
MEASURED BANDWIDTH FOR 25-dB RETURN LOSS

Type	TS-A			TS-B			TS-C		
	ρ								
ρ	0.68	1	1.32	0.8	1	1.2	0.7	1	1.3
f_L (GHz)	8.1	dc	8.7	5.7	dc	6.9	8.2	dc	9.0
f_H (GHz)	12.3	25+	12.4	12.8	25+	13.4	11.1	34.4	11.4
FBW	0.41	1	0.35	0.77	1	0.64	0.30	1	0.24

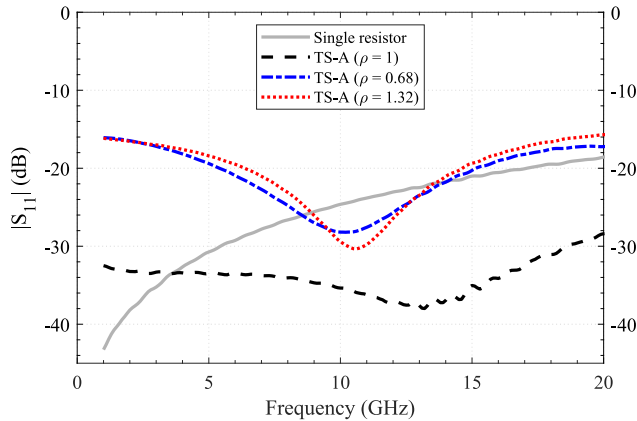


Fig. 8. Measured reflection coefficients of TS-A as a function of frequency.

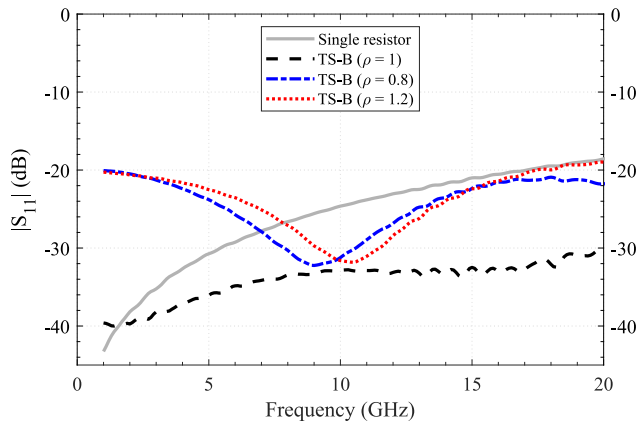


Fig. 9. Measured reflection coefficients of TS-B as a function of frequency.

backside via-hole process. SiC substrate is 100- μm -thick with a dielectric constant of 9.7. Thin-film resistors are formed using TaN sputtering with a thickness of 90 nm. The nominal sheet resistance of the process technology is 30 Ω/\square . Quarter-wave length at 10 GHz is approximately 3.3 mm.

Calibration and measurements are performed using Cascade² RF wafer probe station, GGB³ GSG150 picoprobes, and R&S⁴ ZVA40 vector network analyzer. A summary of the experimental results is presented in Table I.

Fig. 8 shows the measured S-parameters of TS-A with different resistor values achieving return losses better than 25 dB from 8.7 to 12.3 GHz (an FBW of 34%) with a sheet resistance tolerance of 32%. Fig. 9 shows that TS-B achieves

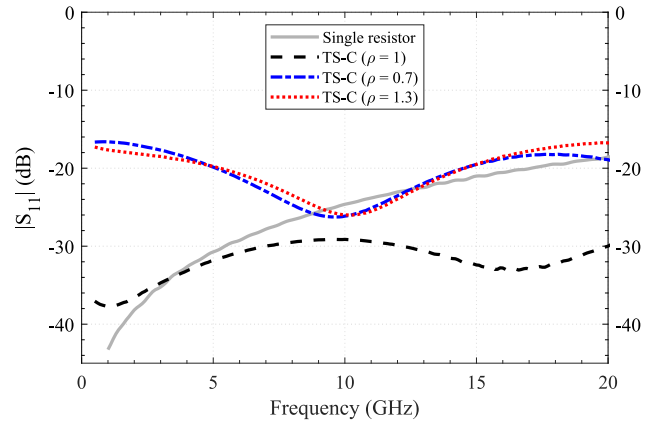


Fig. 10. Measured reflection coefficients of TS-C as a function of frequency.

the return losses better than 25 dB from 6.9 to 12.8 GHz (an FBW of 60%) with a sheet resistance tolerance of 20%. Fig. 10 shows the measured reflection coefficients of TS-C, demonstrating 20-dB matching from 5.5 to 14.6 GHz (an FBW of 91%), even though the resistor values are changed by $\pm 30\%$.

For comparison, the measured reflection coefficient of a single nominal 50- Ω resistor placed next to the test structures is also provided on each figure. Due to its high-frequency parasitic effects, the single resistor cannot present a 25-dB load at frequencies higher than 9.6 GHz. All proposed test structures with nominal resistors achieve almost 30-dB return loss from dc to 20 GHz.

IV. CONCLUSION

A novel resistive load network, which provides high accuracy and sheet resistance tolerance, is introduced. The presented technique is useful for adding process tolerance to balanced and distributed amplifiers, as well as couplers and dividers while improving their high-frequency performance. Parasitic effect cancellation of the method is independent of the fabrication technology and the underlying resistor model, which makes the load circuit suitable for high-frequency RF components in both discrete and integrated circuits.

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