Mic-in-CMOS:
CMUT as a Sealed-Gap Capacitive Microphone

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***Abstract*— The design and production of a CMOS compatible, watertight and ingress-proof CMUT (capacitive micromachined ultrasonic transducer) microphone, mic-in-CMOS, with vacuum-gap is described. We present an analytical model-based approach for the design of mic-in-CMOS, where a basis for quantitative comparison of performance trade-offs is provided. The sealed vacuum gap of the mic-in-CMOS is basically a lossless sensor, free of mechanical noise. Its SNR is determined by the noise of the pre-amplification electronics (the noise contributor in a CMUT with vacuum gap is essentially the radiation resistance, which is less than 0 dBA for audio band for a 1 mm^2 device). The design of mic-in-CMOS involves many multilateral trade-offs such as gap height vs membrane thickness vs sensitivity vs need for linear operation vs bias voltage and atmospheric depression, to name few. The mic-in-CMOS design can be mass produced using CMOS film stacks only, as such the fabrication process can be carried out entirely in a CMOS processes production line complemented with CMOS compatible post-processing approaches. Mic-in-CMOS has the advantage of low production cost with minimal packaging requirement and on-die EMI / EMC.**

Keywords—Capacitive microphone. Sealed gap, MEMS, CMUT, CMOS

I. Introduction

The state-of-the-art capacitive MEMS Microphones incorporate very compliant (perforated silicon) membranes and pressure compensated gap. These membranes resonate at 25−30 kHz, slightly over the audio frequency band. The sensor noise level is about 27−30 dBA, which is dominated by the air friction at the perforations of the membrane. The sensitivity achieved at this noise level is such that the required biasing and pre-amplification electronics can be designed with the same level of noise contribution.

The noise contributor in a CMUT with vacuum gap is essentially the radiation resistance, which is less than 0 dBA for audio band for a 1 mm^2 device. Also, such a CMUT is waterproof since the gap is sealed. The sensitivity of this microphone is lower due to less compliant membrane, because there is a need for maintaining an elastically linear operation under atmospheric pressure. The SNR is determined by the noise of the pre-amplification electronics.

In this paper, an analytical model-based approach for the design of these microphones is presented [1]. An analytical basis is provided for quantitative comparison of performance trade-offs. The three critical dimensions: the gap radius, the effective gap height and the membrane thickness are determined uniquely for a given performance.

This design method exploits the standard CMOS materials and process thicknesses to construct a microphone in CMOS, *mic-in-CMOS*. This production process requires some extra post processing steps. CMOS processes have been utilized to produce sealed gap CMUT devices by post-processing fabricated CMOS chips [2-8]. In such studies, depending on the design, metal, alloy, polysilicon, or SiO_2 layers are designated as sacrificial layers. Similarly, SiO_2, metal, alloy or polysilicon films could be used as structural layers. Once the sacrificial layers are etched from the CMOS chip, the microphone gap entrances/exits are sealed under low pressure. The gaps can be sealed with thin films of either SiO_2 or Si_3N_4, or conformal coating materials according to the design needs.

It is important to note that through the design method employed in this work, the mic-in-CMOS is fabricated on the same die as the pre-amplification and other electronic stages.

II. Design Theory

In the presented method, it is shown that the performance of sealed vacuum gap capacitive microphones can be expressed using only three independent parameters [1]: (i) V_{DC}: dc bias voltage; (ii) F_b/F_g (<1): The ratio of ambient pressure to the pressure necessary to depress the microphone plate by effective gap height; (iii) V_{DC}/V_C (<1): the ratio of the dc bias voltage to the collapse voltage at the ambient pressure. All of the properties of the microphone, including performance related ones like sensitivity (open circuit received voltage or short circuit received current) and the input impedance are uniquely specified once these three parameters are specified. The dimensions of the microphone, depicted in Fig.1, are also determined using only these three parameters and the plate material properties.

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A. Gap and plate dimensions

The device is analytically described in terms of variables such as dimensions and relevant voltage values in detail in [1]. To summarize the main points, the effective gap height t_{ge} is expressed as:

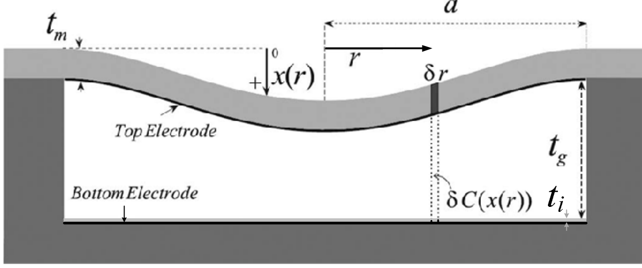


Fig. 1. Cross sectional view of the circular mic-in-CMOS geometry. Top electrode is placed on the bottom of the microphone plate and the insulating dielectric layer is on the bottom electrode.

$$t_{ge} = t_g + t_i/\varepsilon_r \tag{1}$$

where t_g is the physical gap height, t_i is insulator thickness and ε_r is the relative permittivity of the insulating layer, can be expressed as:

$$t_{ge} = V_{DC_n}\left(\frac{V_{DC}}{V_C}\right)^{-1} t_{ge_n} \tag{2}$$

where V_C is the collapse voltage,

$$t_{ge_n} = \left(\frac{V_C}{V_r}\right)^{-1}\sqrt{\frac{F_b}{F_g}} \tag{3}$$

is the reference voltage (collapse voltage in vacuum), and V_{DC_n} is related to the bias voltage as expressed in:

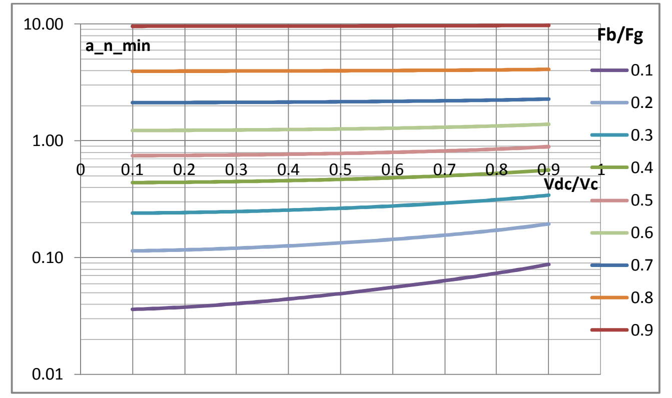
$$V_{DC_n} = \frac{3}{2}\sqrt{\frac{\varepsilon_0}{P_0}}V_{DC} \tag{4}$$

which is $1.4 \times 10^{-8}\,V_{DC}(m)$ for a vacuum sealed gap at Standard Atmospheric Pressure (SAP). P_0 and ε_0 are ambient static pressure and permittivity of free space. The normalized effective gap height, t_{ge_n}, depends only on F_b/F_g, since as described in [9]. This can be expressed as:

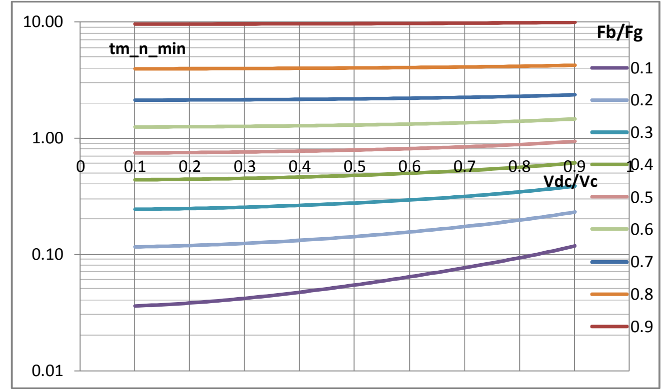
$$\frac{\mathrm{V_C}}{\mathrm{V_r}} \approx 0.9961\text{-}1.0468\frac{\mathrm{F_b}}{\mathrm{F_g}} + 0.06972\left(\frac{\mathrm{F_b}}{\mathrm{F_g}}\text{-}0.25\right)^2 + 0.01148\left(\frac{\mathrm{F_b}}{\mathrm{F_g}}\right)^6 \tag{5}$$

The optimum effective gap height is uniquely determined by the bias voltage and the atmospheric depression and it is independent of plate material properties.

For a given set of operational parameters, (V_{DC}, V_{DC}/V_C, F_b/F_g), there is a minimum value for the microphone radius. This minimum value can be expressed as follows:



(a) a_n



(b) t_{m_n}

Fig. 2. Normalized dimensions $\boldsymbol{a_n}$ a_n and $\boldsymbol{t_{m_n}}$ versus $\boldsymbol{V_{DC}/V_C}$ for different values of $\boldsymbol{F_b/F_g}$

$$a_{min} = \left(10\sqrt[4]{\frac{Y_0}{15(1-\sigma^2)P_0}}\right)V_{DC_n}\left(\frac{V_{DC}}{V_C}\right)^{-1} a_n \tag{6}$$

where P_0 is the ambient static pressure, Y_0 and σ are the Young's modulus and Poisson's ratio of the plate material, respectively, and normalized radius, a_n, is given as:

$$a_n = \left(\frac{a}{t_m}\right)^{-3}_{N_max}\left[\left(\frac{V_C}{V_r}\right)^{-1}\left(\frac{F_b}{F_g}\right)^{3/2}\right] \tag{7}$$

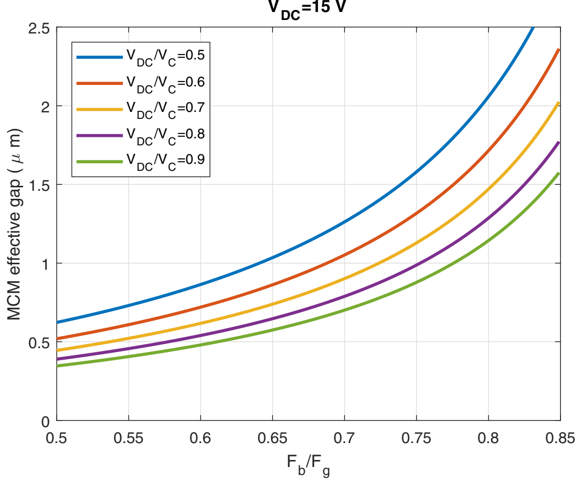
For a silicon plate, the material dependent term is found as:

$$10\sqrt[4]{\frac{Y_0}{15(1-\sigma^2)P_0}} = 178 \tag{8}$$

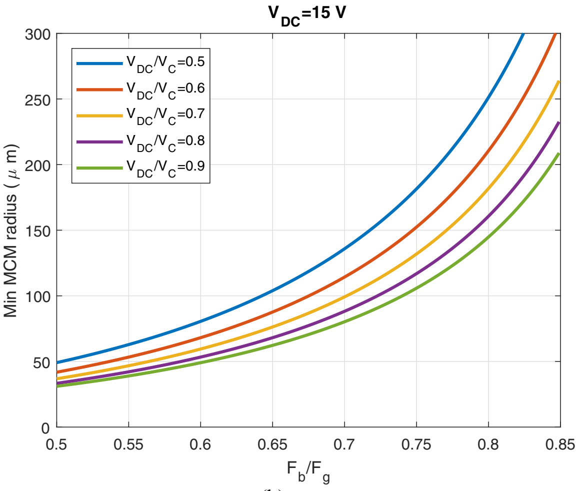
when P_0 is equal to SAP. If the plate is made of few layers of different materials, equivalent Y_0 and σ are employed in the calculation [10]. The plate is a composite of aluminum and oxide layers if fabricated in CMOS processes, in which case this term becomes 150. This normalization parameter for the radius is non-dimensional and contains only the elastic constants of the plate material and the differential static pressure.

The normalized radius, a_n, is independent of material properties and the bias voltage, but it is a function of only the

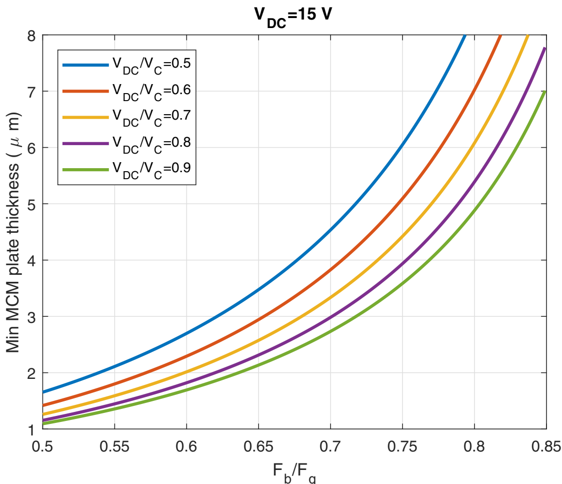
operational parameters F_b/F_g, and V_{DC}/V_C. In order that the microphone plate remains elastically linear, its radius-to-thickness ratio must be less than a maximum, $(a/t_m)_{_max}$ [1]. This limit is also a function of same operational parameters. The variation of a_n with respect to F_b/F_g and V_{DC}/V_C depicted in 2(a).



(a) t_{ge}



(b) a



(c) t_m

Fig. 2. The gap height, radius and the thickness of a silicon membrane designed for 15 V bias as a function of $\boldsymbol{V_{DC}/V_C}$ and $\boldsymbol{F_b/F_g}$

The plate thickness for this radius is similarly obtained as [1],

$$t_{m_min} = 5V_{DC_n}\left(\frac{V_{DC}}{V_C}\right)^{-1} t_{m_n} \tag{9}$$

where;

$$t_{m_n} = a_n\left(\frac{a}{t_m}\right)^{-1}_{N_max} \tag{10}$$

The variation of t_{m_n} with respect to F_b/F_g and V_{DC}/V_C is depicted in 2(b).

B. Scaling

It is possible to increase the microphone gap radius beyond a_{min} such that same performance is maintained at the same effective gap height and operating parameters (V_{DC}, V_{DC}/V_C, F_b/F_g). The new radius and the plate thickness are determined as:

$$a = K^3 a_{min} \tag{11}$$

and

$$t_m = K^4 t_{m_min} \tag{12}$$

where K>1. This property is referred to as *scaling*.

C. Microphone design for 15V bias

The variation of the dimensions of a silicon microphone, designed for 15 V bias, with respect to atmospheric depression is depicted in Fig. 2(a) for various values of V_{DC}/V_C. For example, if the microphone is intended to be used at F_b/F_g =0.7 and V_{DC}/V_C =0.7, the effective gap height must be set at t_{ge}= 0.90 µm.

The radius and the membrane thickness for this bias voltage is also given in Fig. 2 when the membrane is made of silicon. The thickness is t_m=3.2 µm and radius is a=100 µm. The radius also depends on the plate material properties but this dependence is rather weak. The radius varies by the fourth root of the material stiffness so that, for example, if silicon oxide plate is used instead of silicon, a minimum radius of 83 µm is necessary instead of 100 µm, although the Young's modulus of silicon is more than twice as large as that of silicon oxide. The effective gap height and the thickness remains the same.

The approach presented in this paper can also be extended to cover elliptic gaps and plates and convex polygons and elliptic polygons [11]. Same methodology is applicable to square and rectangular microphones, although circular geometry is always more sensitive for a given area.

The required gap heights and plate thicknesses are suitable for designing microphones to be fabricated in standard CMOS fabrication processes. The octagonal gaps and plates are particularly convenient for this purpose.

Sealed gap microphone open-circuit-receive-voltage (OCRV) sensitivity is significantly less compared to MEMS microphones with pressure compensated gap. This is because of the need for relatively thick plates. For example, radius-to-thickness ratio for silicon plates must be less than 35 in order to maintain elastically linear operation under SAP. The lower

microphone output voltage places more demand on low noise pre-amplification. Nevertheless, when the microphone is implemented in a CMOS process integrated with the preamplifier, it was possible to obtain 62 dB SNR.

III. Integrated Electronics

The amplifying electronics is a simple nMOS common source stage with a resistive load, providing a voltage gain of about 10. To reduce the noise of the stage, the gate bias resistance should be very large. To realize a large resistance we use two transistors, one nMOS and the other pMOS both with a gate to source voltage below the threshold voltage. To have a low noise transistor, the amplifying transistor should normally be chosen with a W/L ratio as large as possible. The input gate capacitance of the transistor will generate a voltage divider, reducing the effective input voltage since our input source is purely capacitive. Consequently, there is an optimum value of W/L ratio that gives the highest output signal-to-noise ratio.

IV. Post Processing

After the CMOS processing of a wafer is completed using standard approaches, post-processing of the mics-in-CMOS is initiated and completed using CMOS compatible, wafer-scale adaptable, and batch-compatible unit processes and integration processes. The mic-in-CMOS devices are suitable for mass production using "CMOS film stack only", entire in-CMOS processes production line and CMOS compatible post-processing approaches.

"CMOS compatible post-processing approaches" are composed of etching and deposition steps that may need one or at most two simple (i.e. not technology challenging) lithography levels for the formation of a sealed vacuum gap microphone that becomes watertight and ingress-proof".

V. Conclusion

Mic-in-CMOS, a sealed gap microphone, which is suitable for production in CMOS manufacturing processes is presented in this paper. The analysis and design methodology is fully disclosed. It is possible to get optimum designs for different CMOS manufacturing processes using this approach. The preamplifier and other sensor electronics is readily integrated on the same CMOS die. Presented results are applicable to variety of gap geometries.

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