GaN HEMT BASED MMIC DESIGN AND FABRICATION FOR *Ka*-BAND APPLICATIONS

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We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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Gallium Nitride (GaN) technology has recently dominated the high power applications in the mm-wave frequencies, and its commercial use is emerging with the upcoming 5G technology. High Electron Mobility Transistors (HEMTs) based on GaN show superior material properties and high power densities, which makes them promising candidates to utilize for Monolithic Microwave Integrated Circuits (MMICs) in high frequency applications.

NANOTAM's 0.15 µm/0.2 µm GaN HEMT on Silicon Carbide (SiC) microfabrication process is used to fabricate the transistors and passive components. Process steps are explained, as well as in-house epitaxial growth. Fabricated transistors are characterized for their direct current (DC), small-signal, and large-signal performances. T-gate structure of the transistors is optimized for the highest gain performance at 35 GHz. A three-stage MMIC amplifier is designed, fabricated in two process cycles, and measurements are performed on-wafer at room temperature. The best performing MMIC shows a small-signal gain higher than 23.1 dB with an output power of 31.9 dBm and a power-added efficiency (PAE) of 26.5% at 35 GHz.

Keywords: Gallium Nitride, HEMT, *Ka*-band, MMIC, amplifier.

ÖZET

Ka-BANT UYGULAMALARI İÇİN GaN HEMT TABANLI MMIC TASARIMI VE ÜRETİMİ

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Galyum Nitrür (GaN) teknolojisi son zamanlarda mm-dalga frekanslarındaki yüksek güç uygulamalarına yön vermektedir ve geliştirilmekte olan 5G teknolojisi ile bu teknolojinin ticari kullanımı artmaktadır. GaN Tabanlı Yüksek Elektron Hareketlilikli Transistörler (HEMT'ler) üstün malzeme özellikleri ve yüksek güç yoğunlukları gösterdiklerden, yüksek frekans uygulamalarında Monolitik Mikrodalga Entegre Devrelerinin (MMIC'lerinin) tasarımında kullanılmak için potansiyel barındırmaktadır.

Transistörler ve pasif devre elemanları, NANOTAM'da geliştirilen Silisyum Karbür (SiC) tabanlı 0.15 µm/0.2 µm AlGaN/GaN HEMT mikrofabrikasyon süreci ile üretilmiştir. Mikrofabrikasyon sürecinin aşamaları ve epitaksiyel büyütme aşamaları anlatılmıştır. Üretilen transistörlerin doğrusal akım (DC), küçük işaret ve büyük işaret performansı karakterize edilmiştir. Transistörlerin T şeklindeki kapı geometrisi 35 GHz frekansında en iyi kazancı elde etmek için uygun hale getirilmiştir. Üç kademeli bir yükselteç MMIC tasarımı yapılmış, üretimi iki fabrikasyon döngüsünde gerçekleştirilmiş ve ölçümleri on-wafer olarak oda sıcaklığında yapılmıştır. En iyi sonucu veren devreden, 35 GHz frekansında 23.1 dB küçük işaret kazancı ile 31.9 dBm çıkış gücü ve %26.5 güç eklenmiş verimlilik (PAE) elde edilmiştir.

Anahtar sözcükler: Galyum Nitrür, HEMT, *Ka*-bant, MMIC, yükselteç.

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Chapter 1

Introduction

1.1 General Introduction

Gallium Nitride (GaN) technology has been used for commercial and military applications for several years with its high output power and efficiency performance [1]. Moreover, it has recently dominated the mm-wave frequencies of the electromagnetic (EM) spectrum for high power applications, such as phased-array radars, wireless communication systems, and transmitters. These systems use power amplifiers, switches, and low-noise amplifiers. GaN-based High Electron Mobility Transistors (HEMTs) are preferable for all these usages in terms of their material qualities. For compactness, lower cost, and reliable production, Monolithic Microwave Integrated Circuits (MMICs) are the choice to produce RF amplifiers based on GaN HEMTs [2].

Nowadays, the commercial use of GaN at *Ka*-band, with the approved frequencies 28 GHz, 37 GHz, and 39 GHz, is popular thanks to the upcoming 5G technology with the necessity of low-latency and high-speed transmission for cellular applications [3]. These systems, e.g., massive MIMO which consists of many transmitters and receivers, require high output power and efficiency with small chip dimensions [4].

1.2 GaN HEMT for RF and mm-wave Applications

The research on wide band-gap semiconductors has been going on for many years, and has shown a considerable performance improvement for RF applications. Wide band-gap devices are able to work at high voltages, high temperatures, and high frequencies, providing better performance. Besides the most-widely used Silicon (Si) transistors, new devices using wide band-gap semiconductors are developed after the 1970s, including MESFET, HBT, pHEMT based on Gallium Arsenide (GaAs), Indium Phosphide (InP), and Silicon Carbide (SiC). HEMTs are introduced in 1979, showing high output power and efficiency with high breakdown voltage and the ability to work at high frequencies [5, 6]. HEMTs have become superior to other devices, thanks to two-dimensional electron gas (2DEG) formed between the heterojunction (Aluminium Gallium Arsenide (AlGaAs)/GaAs or Aluminium Gallium Nitride (AlGaN)/GaN) on the epitaxial structure. This heterojunction with different band-gap materials results in a quantum well consisting of free electrons with high mobility. The separation of free electrons and donor atoms reduces the impurity scattering along 2DEG and increases the drift velocity of the electrons and the carrier mobility [6]. Thanks to well-confined channel, HEMTs also show higher saturated velocity.

HEMT based on GaN is first introduced in 1994 and has been under development ever since [7]. The comparison of GaN with more mature semiconductor materials are given in Table 1.1 together with two figures of merit (FOMs) [8, 9]. GaN HEMTs are superior in terms of high output power thanks to the high breakdown field and high saturated velocity. Johnson's FOM (JFOM) shows the material's performance for high power and high frequency applications, where GaN is exceptional. Baliga's FOM (BFOM) indicates the performance for power switching applications, and GaN is better than the other semiconductor materials. It can also be seen that the maximum operation temperature of GaN is very high even though the thermal conductivity is comparable to Si, which allows GaN devices to work at higher channel temperatures for high output powers.

Table 1.1: Comparison of material properties and two FOMs of Si, GaAs, SiC, and GaN.
[a] Electron mobility of 2DEG formed in the heterostructure, others in bulk.
[b] Normalized to Si.

Material Property / FOM	**Si**	**GaAs**	**4H-SiC**	**GaN**
Band-gap Energy, W_g (eV)	1.12	1.43	3.26	3.39
Brekdown Field, E_{crit} (MV/cm)	0.3	0.4	2.5	3.3
Electron Mobility, μ ($\mathrm{cm^2/(V\,s)}$)	1300	5000[a]	260	2000[a]
Saturated Velocity, v_{sat} (10^7 cm/s)	1	1	2	2.5
Thermal Conductivity, k (W/(K cm))	1.5	0.46	4.9	1.3
Max. Operation Temperature, T_{max} (°C)	200	300	500	700
JFOM[b], $v_{sat}E_{crit}/2$	1	11	410	790
BFOM[b], $\epsilon_n \mu_c (E_{crit})^3$	1	28	290	910

The choice of the substrate for GaN epitaxial growth is also crucial since the homeepitaxy, growing GaN on a GaN substrate, is not practical to form GaN HEMTs due to small wafer sizes and high costs of bulk GaN substrates [9]. Epitaxial structure of AlGaN/GaN can be grown on Si with low cost, facing the drawbacks of higher lattice mismatch and lower thermal performance. The heat dissipation of GaN devices is improved by growing the structure on good thermal conductors, such as SiC or diamond. AlGaN/GaN structures can be grown on SiC substrates, having low lattice mismatch and low thermal expansion mismatch, which are ideal conditions for high power applications.

The achieved performance of GaN HEMTs and the mentioned FOMs show that these devices are in a well-deserved place in RF and microwave applications. With the developing performance of GaN HEMTs for mm-wave frequencies, many MMICs are realized at *Ka*-band with HEMTs based on AlGaN/GaN and InAlGaN/GaN structures, aiming satellite, cellular, or radar applications [10–17]. At 35 GHz, a saturated power density of 4 W/mm is achieved for an AlGaN/GaN device in [10]. Another AlGaN/GaN device is reported in [11] with 5 W/mm power density at 35 GHz. In [13], a 40 W MMIC is realized using a process with 4 W/mm output power at 30 GHz with 28 V operating voltage. The MMICs in recent works [16] and [17] show good output power densities of 4.5 W/mm with 28 V supply voltage at 30 GHz. Using an InAlGaN/GaN structure, a power density of 2.7 W/mm at 30 GHz is achieved [14]. For high efficiency performance,

a Doherty power amplifier is also realized with a peak power-added efficiency (PAE) of 25% at 28.5 GHz in [18].

1.3 Thesis Outline

In this thesis, NANOTAM's AlGaN/GaN HEMT on SiC process aiming mm-wave applications is introduced. Design and measurement results of a three-stage amplifier MMIC are presented. Fabricated MMIC shows a small-signal gain of 23.1 dB, an output power of 31.9 dBm, and a PAE of 26.5% at 35 GHz. High efficiency result is achieved using 20 V drain voltage of 30% duty cycle in the large-signal measurement, which is a challenging condition considering other works around the same frequencies [11, 12, 15].

The in-house fabrication process is explained in Chapter 2. Characterization steps for HEMTs are given in Chapter 3, including direct current (DC), small-signal, and large-signal measurement setups. Layout details and the optimization of the T-gate structure of HEMTs for better small-signal performance at 35 GHz are described in Chapter 4. Design of the three-stage MMIC is detailed in Chapter 5, considering the topology, matching network designs, and stability analysis. Chapter 6 shows the measurement results from two different processes. Thesis is completed with discussion and conclusion in Chapter 7.

Chapter 2

GaN HEMT Fabrication Technology

Fabrication for GaN HEMTs and MMICs starts with epitaxial growth, which is followed by the front-side process as for co-planar devices, and the back-side process as for microstrip devices.

2.1 Epitaxial Growth

The growth of GaN material is performed on top of a carrier substrate together with nucleation, buffer, transition, and channel layers to create the epitaxial structure for HEMTs to operate on. This deposition method is called Metal Organic Chemical Vapor Deposition (MOCVD), in which thin layers of GaN materials are deposited using metal-organic compounds, Trimethyl Gallium (TMGa) or Trimethyl Aluminum (TMAl) and ammonia (NH_3) as group-III and group-V elements. Deposition takes place at around 1000 °C temperatures. Sapphire, Si, or SiC can be chosen as the carrier substrate for GaN, depending on the technology and usage. The bulk GaN crystal is not being used as a carrier substrate, in the shape of wafers, due to difficulty and immaturity of its growth process. Si is the

cheapest alternative and can be produced as large wafers. However, it has a high lattice mismatch to GaN and has poor thermal conductivity [19]. On the other hand, SiC substrate has a better lattice match to GaN, and shows a good thermal conductivity compared to Si and Sapphire [9]. The comparison of common substrate materials for the GaN-epitaxy is given in Table 2.1.

Table 2.1: Comparison of substrate materials for the GaN-epitaxy.
[a] Relative to GaN.

Substrate	**k (W/(K cm))**	**Lattice Mismatch[a]**	**Wafer Size**	**Price (€/cm²)**
Si	1.5	−17%	any	0.1
Sapphire	0.35	−16%	up to 8-inch	1
SiC	4.9	+3.5%	up to 6-inch	10
Bulk GaN	1.3	none	2/3-inch	10

Epitaxial structure that is grown by the MOCVD process is given in Fig. 2.1. Growth for the GaN-epitaxy starts with the deposition of the nucleation layer over a 3-inch diameter, 300 µm thick 4H-SiC substrate. The nucleation layer is used between the substrate and GaN material to reduce the effect of their lattice mismatch and to lower the strain on the following GaN buffer layer. Low-temperature AlN of 100 nm is used as the nucleation layer.

The growth continues with buffer layer deposition, which consists of intentionally doped or undoped GaN. This layer should be very high quality, resulting in low defect density to prevent buffer leakage and traps. The pinch-off performance of a device and drain current collapse mechanism are directly affected by the trapping of 2DEG electrons due to the low quality buffer layer. The quality of this layer also impacts interface roughness, which is essential to achieve a high performance 2DEG layer with good confinement and high electron mobility. Moreover, the resistivity of the GaN buffer layer should be high, therefore nucleation layer should be deposited considering this property. The thickness of this layer can be increased to obtain an interface with lower dislocations, which also contributes to the 2DEG quality. To minimize the buffer-induced current collapse (i.e., degradation in drain current due to defects and traps), a highly-resistive GaN layer is achieved by C-doping, Fe-doping, or intrinsic growth defects with proper doping

Figure 2.1: Epitaxial structure showing the layers grown by MOCVD.

concentrations which also affect the current collapse [20–22]. The buffer layer is grown with Fe-doping in the structure, with prior knowledge of the effects of the buffer layer's doping properties on the buffer leakages and the trapping mechanism. The existence of deep-acceptor traps in the C-doped buffer results in a high voltage-dependent current collapse, whereas Fe-doping only causes mild current collapse thanks to the lack of these deep-acceptor traps [20]. Moreover, buffer leakage current is smaller in the Fe-doped structures due to the higher energy barrier between the channel and the buffer layer [23]. The thickness of this buffer layer is 1100 nm.

660 nm thick transition GaN layer is grown after the buffer layer, providing a transition from highly Fe-doped region to undoped channel region since Fe-doping has around 700 nm diffusion tail. To serve as the layer where 2DEG occurs, a high quality, 130 nm thick GaN layer is deposited after the transition GaN. This layer should have low defect density with high surface smoothness. Between the GaN channel and AlGaN barrier layer, a spike layer, composed of AlN, is deposited. The spike layer has a significant effect on the 2DEG characteristics, which is

determined by its thickness, such as lower alloy scattering, higher confinement, and higher gate Schottky barrier.

AlGaN barrier layer is grown after the spike layer to form 2DEG and to source electrons. With this layer, spontaneous and piezoelectric polarization in GaN/AlGaN heterojunction induces positive polarization charge at the interface and negative charge at the AlGaN layer, creating an electric field. Hence, the thickness and Al concentration of this layer affect the carrier concentration of 2DEG. The Al concentration should be set to increase the 2DEG density as much as possible without any relaxation [8]. The thickness of this layer is 22 nm and its Al concentration is 28.4% in the grown structure.

As the final step of MOCVD, a thin GaN cap layer (2 nm to 3 nm) is deposited in order to eliminate the oxidation of Al in the barrier layer, resulting in lower surface defects and higher reliability. This layer eases the Schottky gate formation and prevents the gate leakages.

The grown wafers are characterized for various parameters, such as 2DEG sheet carrier concentration, electron mobility, sheet resistance, surface roughness, and crystal quality. These specifications give an idea about the quality of the growth, as well as the possible outcomes of the device fabrication using the wafer. For the wafers grown for Ka-band applications, surface roughness is measured using Atomic Force Microscopy, and is below 1 nm in root mean square. Hall Effect measurement is performed to determine the sheet carrier concentration and electron mobility of 2DEG, which are higher than $1.0 \times 10^{13}\,\mathrm{cm}^{-2}$ and $2000\,\mathrm{cm}^2/(\mathrm{V\,s})$, respectively. Sheet resistance is measured as lower than $350\,\Omega/\square$.

2.2 Photomask Design

In order to form active and passive devices, lithography patterns should be developed for each layer of the fabrication process. Various HEMT layouts are designed for a $10\,\mathrm{mm}^2 \times 10\,\mathrm{mm}^2$ sized reticle, which is distributed over a 3-inch

photomask. The photomask may also include MMIC layouts and passive components besides the Process Control Monitoring (PCM) regions throughout the whole wafer. PCMs consist of control transistors, patterns to check lithography steps, Transfer Length Method (TLM) patterns to determine ohmic contact resistance, and passive elements to monitor the uniformity across the wafer, such as resistors and capacitors. The 3-inch photomask that is used for the fabrication is shown in Fig. 2.2.

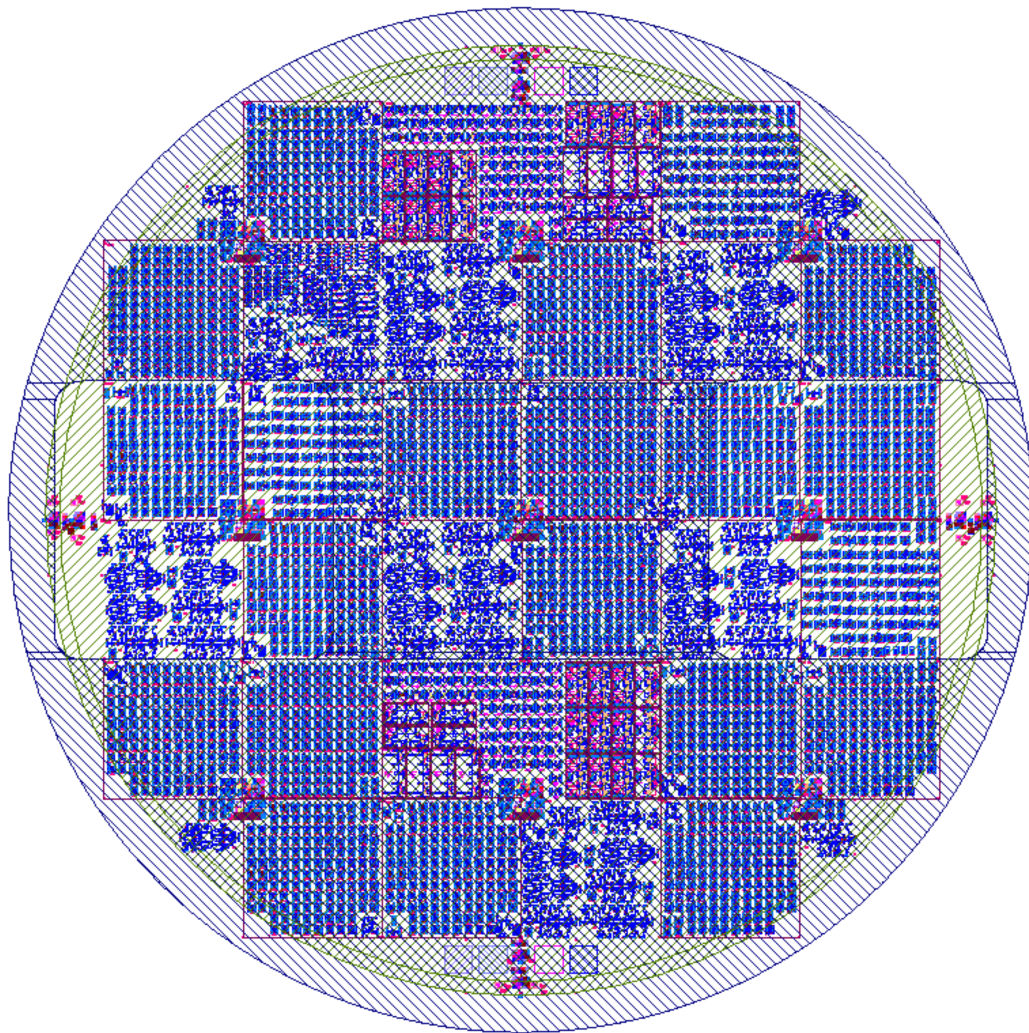


Figure 2.2: 3-inch photomask, including transistor reticles, MMICs, passive components, and PCM regions.

2.3 Front-Side Process

The main steps of active device fabrication are ohmic contact formation, mesa isolation, gate lithography, passivation, and metallization. For passive devices, thin-film resistor (TFR) and capacitor formation steps are also performed besides metallization.

2.3.1 Ohmic Contacts

Ohmic contacts are formed to enable the electrical connection from the upper surface of the wafer through the channel. Ohmic contacts need to have low resistance at the metal-semiconductor interface since their resistance directly affects the device performance. To form ohmic contacts, a stack of Ti/Al/Ni/Au is deposited on the wafer using an electron beam evaporator, which is followed by annealing at high temperatures around 850 °C, resulting alloying and diffusion. The total thickness of the ohmic metal stack is 200 nm in this fabrication. Fig. 2.3 shows the cross-section of the structure with the ohmic contacts.

Figure 2.3: The cross-section of the structure after the alloyed ohmic contact process.

2.3.2 Mesa Isolation

Isolation of active devices is provided by mesa etching, in which AlGaN layer and part of the GaN layers are etched to remove 2DEG for whole wafer surface apart from the active areas. The mesa isolation islands are defined by photolithography, and the etching is performed using a plasma-based dry etch process in an inductively coupled plasma reactive ion etching (ICP-RIE) system. An approximate etching thickness for mesa isolation is 80 nm. Fig. 2.4 shows the cross-sectional view of the sample after the mesa isolation.

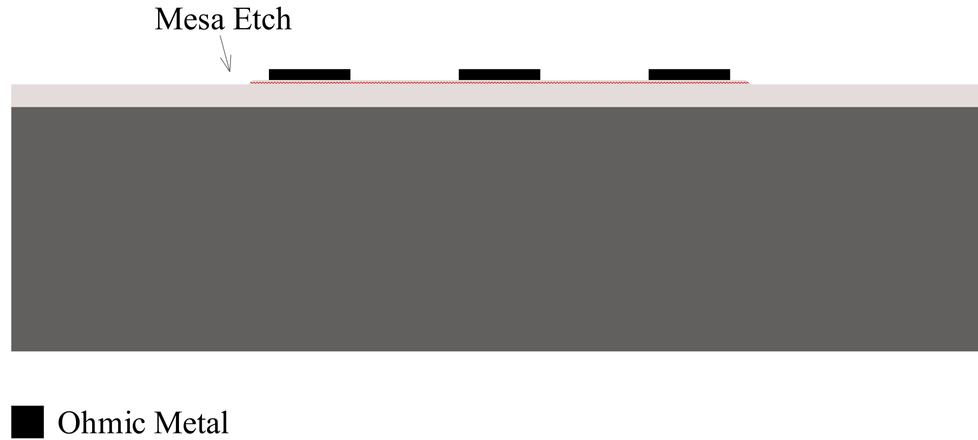


Figure 2.4: The cross-section of the wafer after the mesa isolation.

TLM Measurements

The quality of ohmic contacts are analyzed after the ohmic contact and mesa isolation steps in the fabrication flow. The contact resistances of the ohmic contacts are measured using the four-point probe technique. Four probes are used for this measurement to eliminate the resistances of the probes. TLM pattern includes same size ohmic contacts placed side-by-side with different spacing as shown in Fig. 2.5.

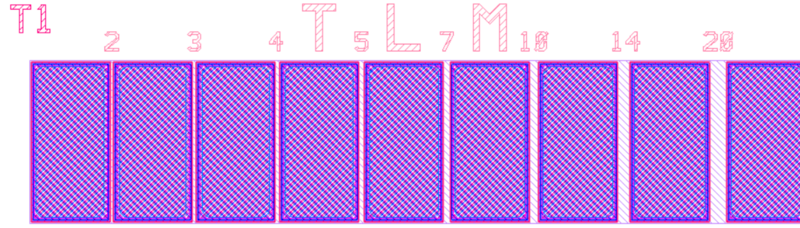


Figure 2.5: TLM pattern in the PCM regions across the wafer.

When the resistance between each two of these ohmic contact patterns is measured, the ohmic contact resistance can be found using the following formula,

$$R = 2\frac{R_c}{w} + R_s\frac{d}{w}, \tag{2.1}$$

where R is the measured resistance, R_c is the ohmic contact resistance, R_s is the sheet resistance of the structure ($350\,\Omega/\square$), w is the width of the ohmic contact patterns ($2\,\mu m$ to $20\,\mu m$), and d is the distance between two contacts ($200\,\mu m$). The fitting of the measured resistance data gives R_c of the ohmic patterns. In our process, the ohmic contact resistance values are around $0.3\,\Omega\,mm$.

2.3.3 Passivation

Passivation is a significant step in the process flow, since it affects the leakage currents and the neutralization of the surface states. The defects on the surface and the surface states may result in electron trapping and virtual gate formation, which degrades the device performance. A dielectric passivation layer is coated on the wafer surface after the mesa isolation and before the gate formation. This passivation layer is composed of Si_3N_4, deposited using a plasma-enhanced chemical vapor deposition (PECVD) system, and is dry-etched by ICP-RIE for contact openings. The thicknesss of this layer is 100 nm, which also determines the thickness of the gate foot. The cross-sectional view of the sample after passivation dielectric deposition and etching is given in Fig. 2.6.

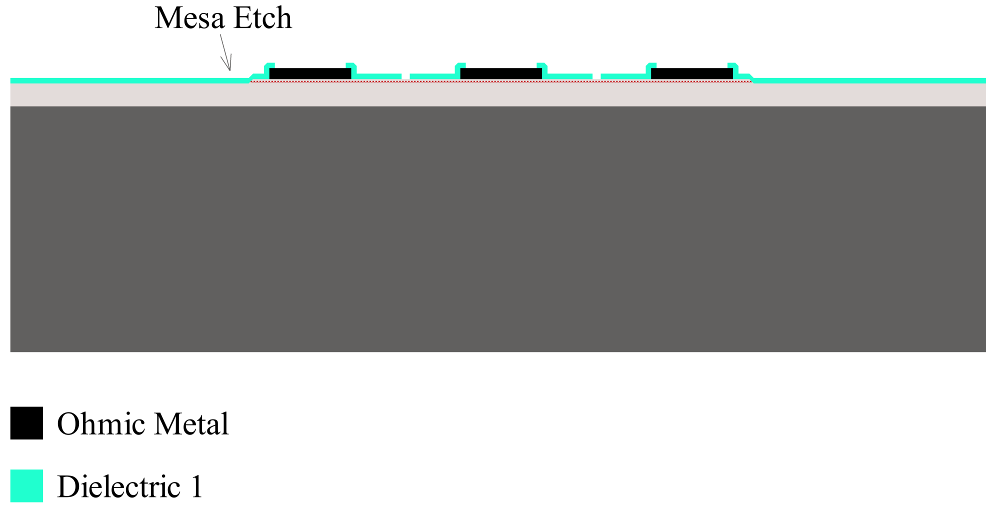


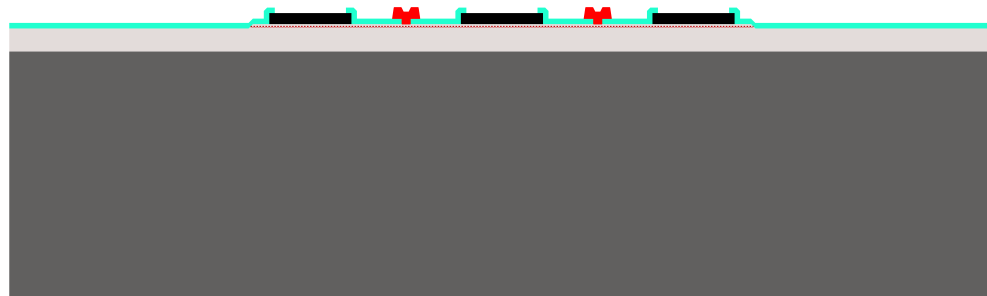
Figure 2.6: The cross-section of the wafer after mesa isolation and the first dielectric deposition.

2.3.4 Gate Formation

The gates are formed as Schottky contacts between the semiconductor surface and the gate metal, which is significant to create high barrier height energy. The adhesion of gate metal to the semiconductor surface is crucial as well as its thermal stability. The resistance of Schottky contact metal depends on these properties, which directly affects the input gate resistance of the devices. Ni is used to form the Schottky gate in our process, and Au is used on top of Ni for better conductivity and to prevent oxidation. Gates are formed as T-gate, a gate foot with a field-plate (head) connected to itself, to increase the breakdown voltages by changing the electric field distribution under the gate and reducing the gate resistance. The gate foot length of transistors determines their performance with respect to frequency. In our process, the minimum gate length is 150 nm due to the limitation of the process.

Gate foot regions are patterned by E-beam lithography using a proper resist. Gate head regions are also defined using E-beam lithography. Ni/Au metal stack is deposited on the patterned gate foot and head regions using an E-beam evaporator with thicknesses of 100 nm and 400 nm, respectively. Fig. 2.7 shows the cross-sectional view of the wafer after the gate formation. The SEM image of

one of the gates are given in Fig. 2.8. This type of nitride-based T-gates are supported with the dielectric covering the gate metal foot and the head, which is a disadvantage in terms of the parasitic capacitances of the gate.



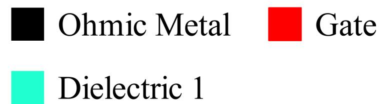


Figure 2.7: The cross-sectional view of the wafer after the gate formation.

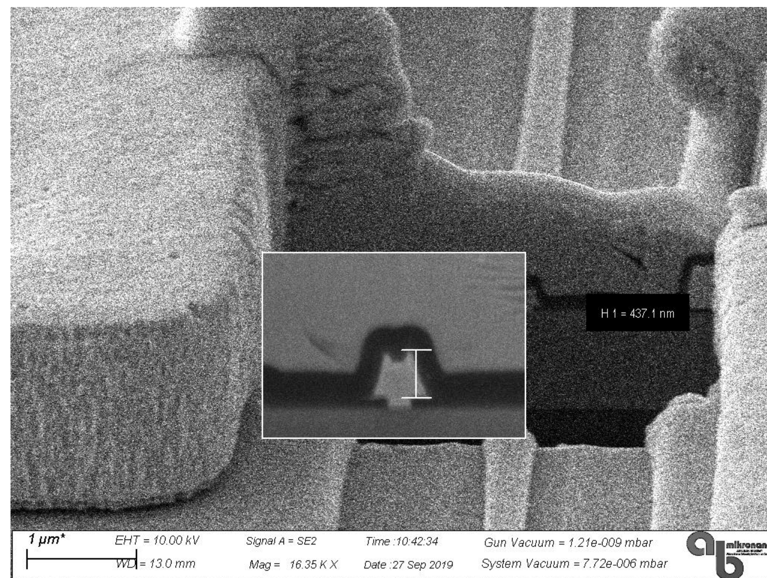


Figure 2.8: The SEM image of the fabricated nitride-based T-gate.

Mushroom-Shaped Gates

Another gate process is implemented in the fabrication for high frequency devices, in order to decrease the capacitance to achieve higher gains and faster devices.

Mushroom-shaped gates are like T-gates without the dielectric support, having no nitride layer surrounding the structure. The foot and the head of this type of gate are also defined by E-beam lithography using proper resists. They are harder to fabricate due to the very small foot length of gates compared to their height and head length. Therefore, a gate length of 200 nm is used for this process. However, better RF performance can be achieved with this gate type thanks to smaller parasitic gate capacitances. Fig. 2.9 shows the SEM image of one of the fabricated mushroom-shaped gates.

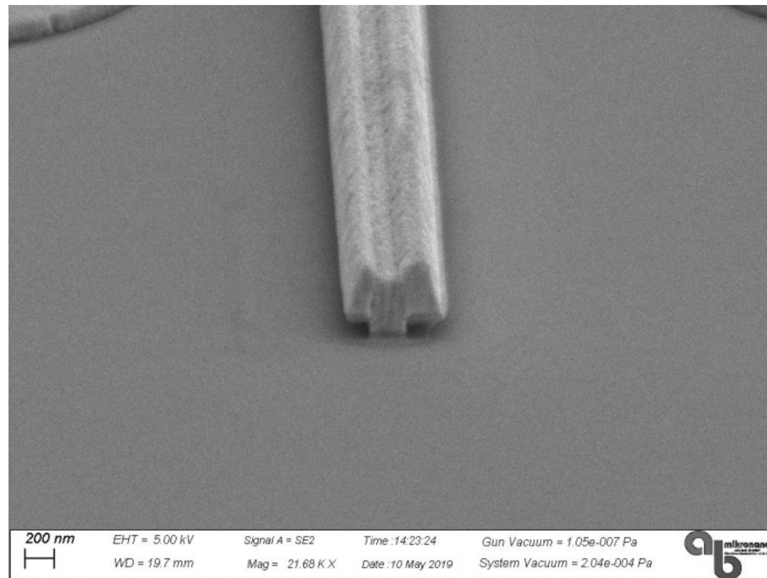


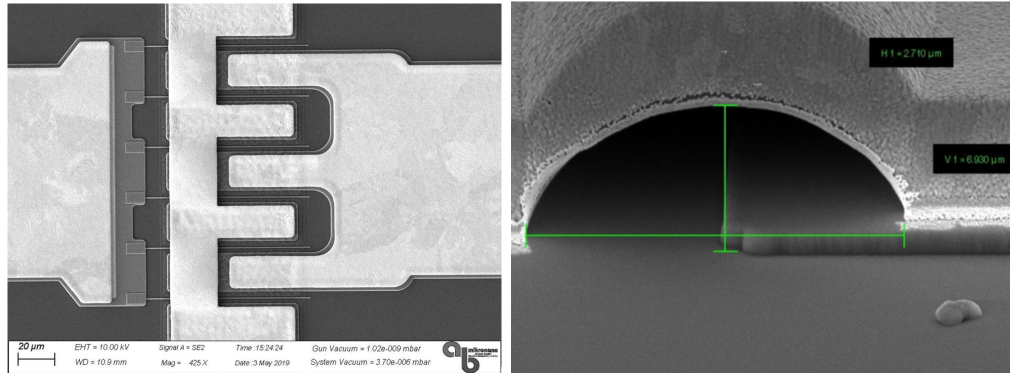
Figure 2.9: The SEM image of the fabricated mushroom-shaped gate.

2.3.5 Metallization

There are two metallization steps in the process. The first metal layer is patterned using photolithography and it is coated using the E-beam evaporator system as the first interconnection metal after the passivation and gate formation. Ti/Au metal stack is used in this step with 50 nm and 1000 nm thicknesses. This metal layer shapes the drain and source contacts of the transistors, and it is the first metal of metal-insulator-metal (MIM) capacitors.

Air-bridges are formed before the second metal layer for metal-metal crossovers

without short circuits. Air-bridge structures are patterned by photolithography and resist reflow is performed. A seed layer of 10 nm of Ti and 100 nm of Au are evaporated over the surface before the electroplating step of the second metal layer, and this layer is patterned by the appropriate photolithography mask. The second metal layer of 4 µm of Au is deposited using electroplating. The active device process is finalized by removing the air-bridge post and seed layer after the second metal layer deposition. SEM images of a transistor are given in Fig. 2.10a and Fig. 2.10b, showing the metal layers and air-bridge structures, respectively. The cross-sectional view of the finalized active device is shown in Fig. 2.11 together with the passive devices.



(a) SEM image of a transistor after metallization and air-bridge processes.

(b) A close-up SEM image of an air-bridge structure.

Figure 2.10: SEM images of a transistor during process flow.

2.3.6 Thin Film Resistors and MIM Capacitors

TFRs and MIM capacitors are formed in our process to have on-chip resistors and capacitors to be used in the MMIC design. Resistors are deposited with TaN in a sputtering system. The resistance density of the TFR layer is set to 30 Ω/□ using 90 nm TaN thickness. For on-chip capacitors, MIM structures are formed with a dielectric layer of Si_3N_4 in between two metal layers of the process. This layer is deposited by PECVD with a thickness of 350 nm to achieve a capacitance density of 175 pF/mm^2. This density depends on the dielectric constant of Si_3N_4 as well as the thickness. Its dielectric constant is set to 7 in the deposition

process, hence the capacitance density can be changed by changing the dielectric thickness. Inductors can also be fabricated using the same process with two metal layers and the air-bridge structures. However, they are not demonstrated here as only capacitors, resistors, and transmission lines are used in the MMIC design. Fig. 2.11 shows the cross-sectional view of a TFR and a MIM capacitor, as well as the active device, at the end of the front-side process.

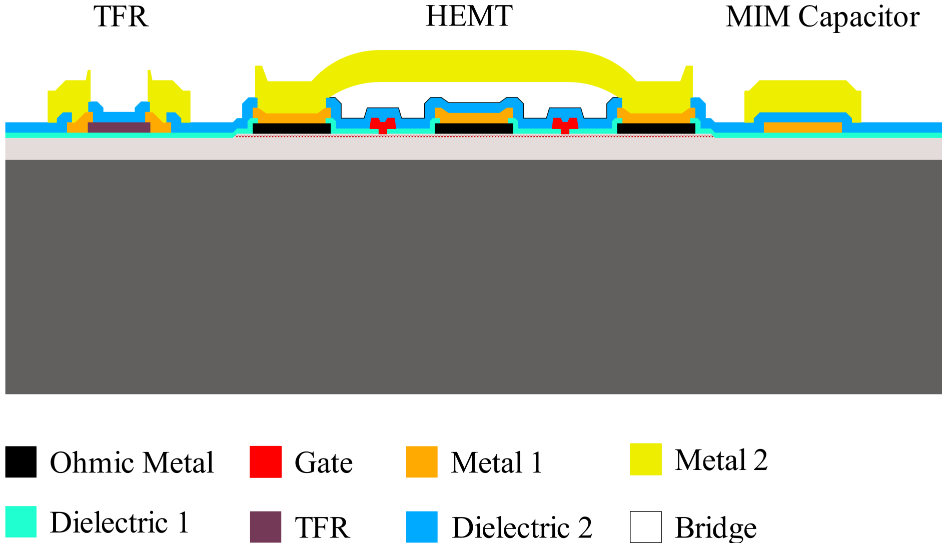


Figure 2.11: The cross-section of the structure showing the active device, MIM capacitor, and TFR.

2.4 Back-Side Process

To enable microstrip structures, the grounds of the active and passive devices are connected to the bottom of the wafer in the back-side process. Firstly, the wafer is thinned to 100 µm from its back-side. SiC material is protected by forming a Ni mask with appropriate via hole patterns before back-via hole opening step. Back-via holes are opened using a three-step etching process. SiC material is etched using a two-step (fast and slow) F-based plasma etching process, and Cl-based plasma etching is performed to etch the other layers of the structure. The walls of opened via holes and the back-side of the wafer are coated with 5 µm thick Au by electroplating, forming the ground connection from the top

to the bottom of the wafer. The microstrip active and passive device process is completed with this step. The cross-sectional view of the wafer after the back-side process, demonstrating the active device, TFR, and MIM capacitor, is shown in Fig. 2.12.

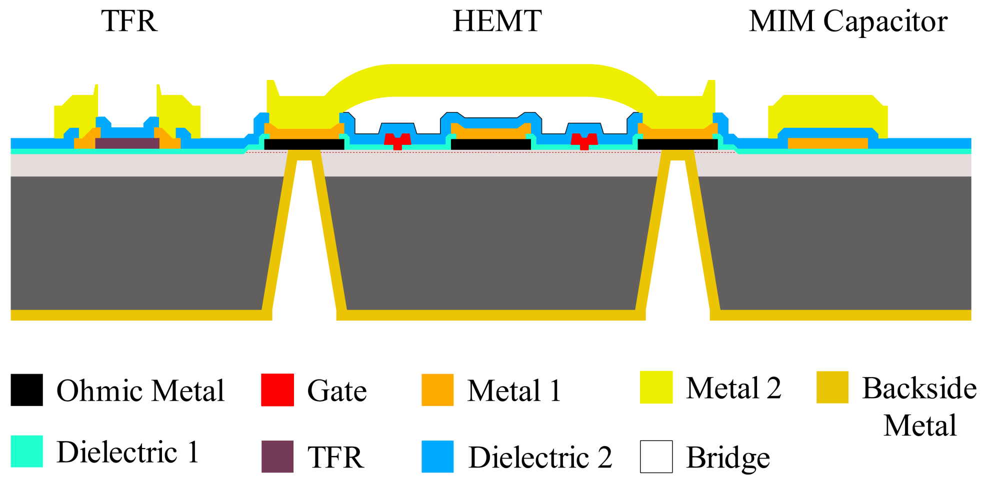


Figure 2.12: The cross-sectional view of the wafer after the back-side process.

Chapter 3

HEMT Characterization and Measurements

After the fabrication, active devices are characterized to see the performance across the wafer. DC, small-signal, and large-signal characterizations are performed in this order.

3.1 DC Characterization

DC measurement is the first step to characterize HEMTs in terms of their maximum saturated drain current (I_{dss}), transconductance (g_m), and DC breakdown voltage. The measurements are performed using a power device analyzer (B1505) from Keysight Technologies. Fig. 3.1 shows the DC measurement setup. On-wafer DC measurements are performed for each transistor before further RF and large-signal characterization.

I-V curves of a device give a solid idea about its RF and large-signal performance by indicating the maximum voltage and current swings which determine the maximum RF power that can be drawn from the device. Knee-voltages of

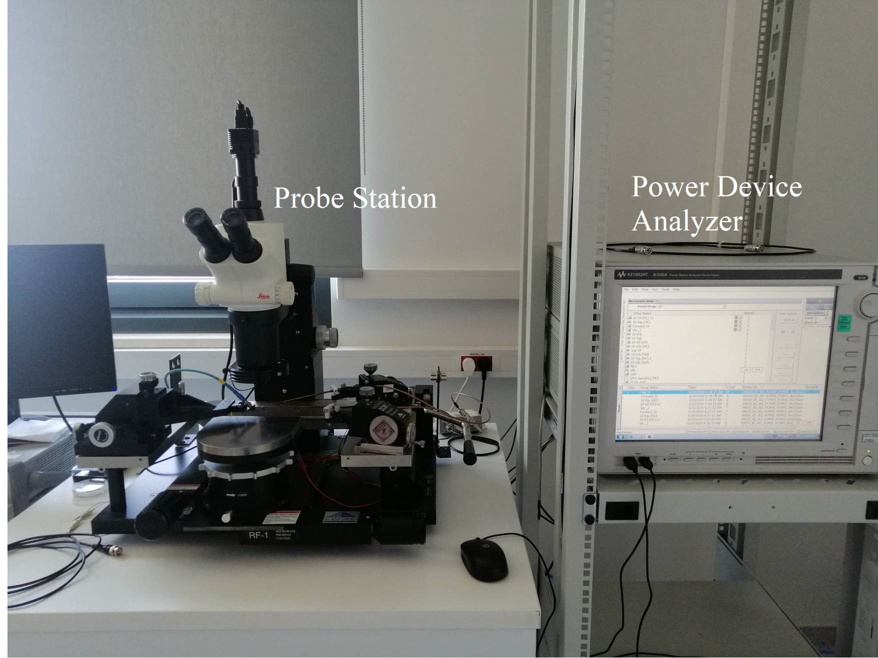


Figure 3.1: DC measurement setup used for HEMT characterization, including power device analyzer.

transistors are also determined from the I-V measurements. A typical I-V measurement of a 4×75 µm HEMT is shown in Fig. 3.2. I_{dss} of this device is measured as 306.65 mA which results in 1.02 A/mm. The knee-voltage is 4 V. This graph is also an indicator for gate and drain leakages, which might degrade the device performance if they are significant.

DC transconductance of a transistor is the change in its drain current caused by small changes in the gate to source voltage, which is given by the formula

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}. \tag{3.1}$$

Fig. 3.3 shows transistor's drain current while sweeping the gate voltage for the drain voltages from 6 V to 10 V, and the derivatives of these curves for 4×75 µm device. The highest transconductance is measured as 108.25 mS for 10 V drain voltage, which gives 360.83 mS/mm. The pinch-off voltage is also recorded in this measurement as −3.5 V, which is a valuable data for the following characterization steps and the MMIC design.

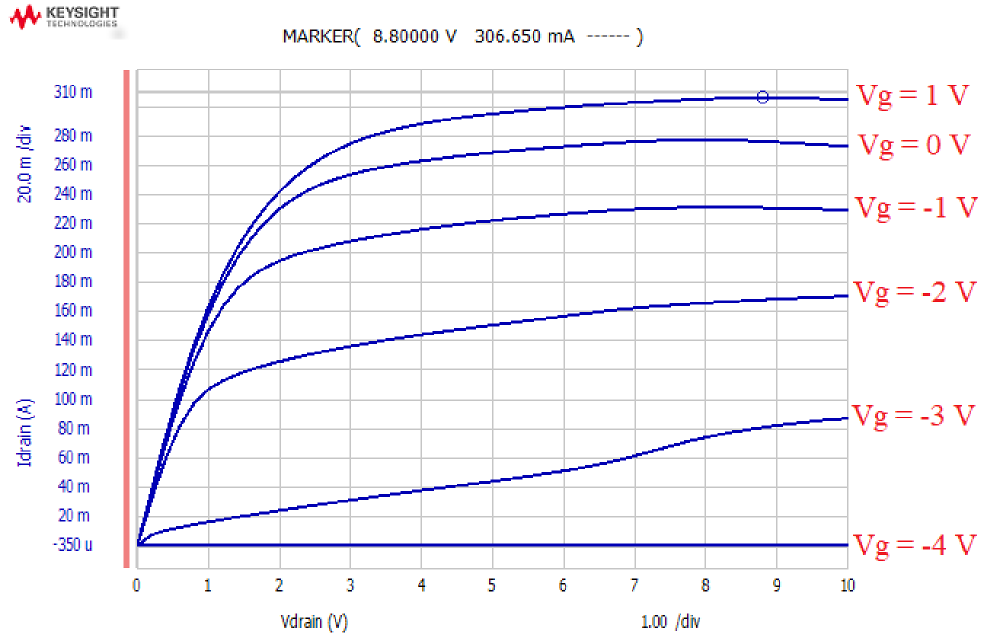


Figure 3.2: I_d-V_d curves of a 4×75 µm device for $V_g = -6\,\mathrm{V}$ to $V_g = 1\,\mathrm{V}$ (top) in 1 V steps.

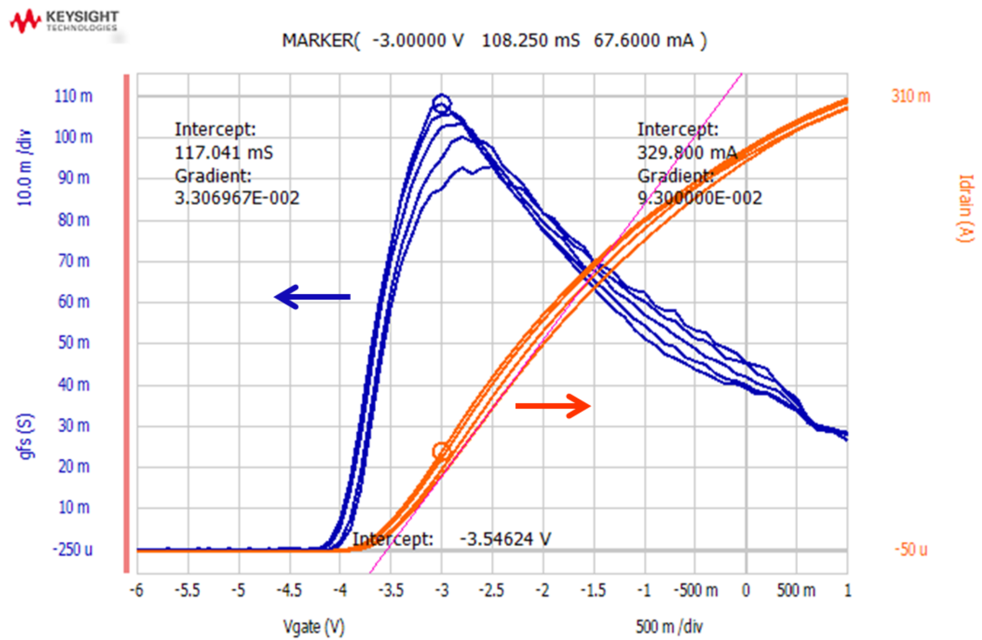


Figure 3.3: Transconductance and I_{ds}-V_{gs} curves of a 4×75 µm device.

To observe the gate and drain leakages, DC breakdown measurement is performed. Fig. 3.4 shows the breakdown characteristics of a typical device. The drain voltage is swept up to 45 V while the gate is pinched-off with −6 V. For the highest drain voltage level, the drain and gate leakage currents are measured as around 235 µA and 1 µA, respectively.

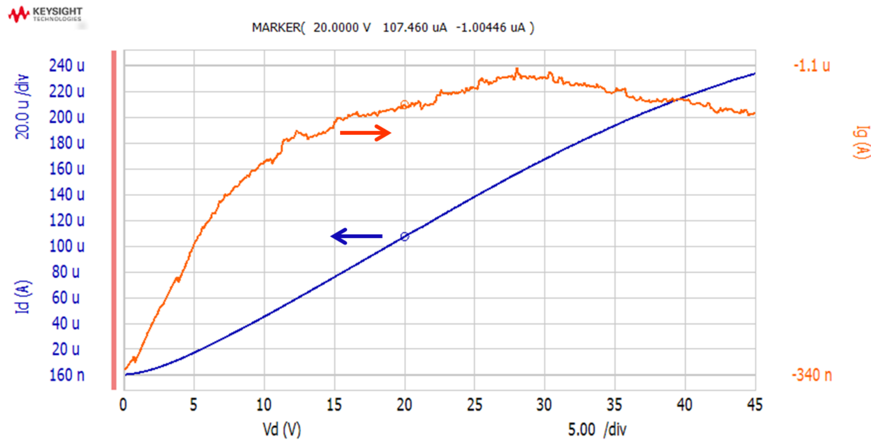


Figure 3.4: Drain and gate leakage currents of a 4×75 µm device.

3.2 Small-Signal HEMT Measurements

RF small-signal measurements are performed to characterize the frequency-dependent behavior of the transistors. A network analyzer is used to measure S-parameters of the device, which is performed on-wafer using the setup given in Fig. 3.5. Small-signal measurements can be done at different bias voltages with various chuck temperatures. The bias voltages can be supplied via bias-tees using DC power supplies for continuous wave (CW) measurements or pulsers for pulsed S-parameter measurements. With thermally controllable chucks, chuck temperatures can be set to different values to observe high or low temperature response of the devices.

Small-signal measurement of a device gives S-parameter data, i.e., input reflection coefficient (IRC) and output reflection coefficient (ORC) with forward and reverse transmissions. S-parameter measurement results of 4×75 µm and

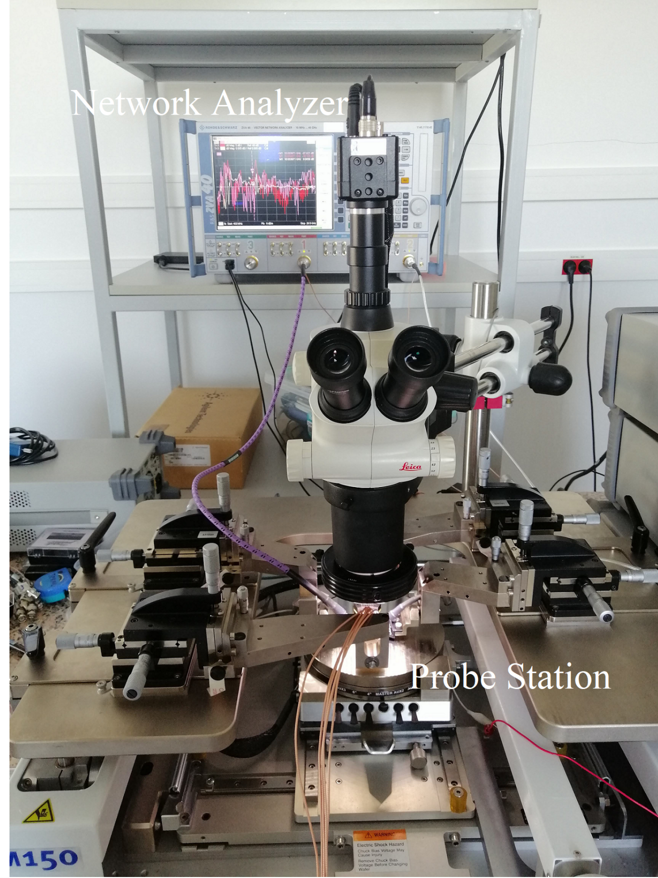


Figure 3.5: Small-signal measurement setup.

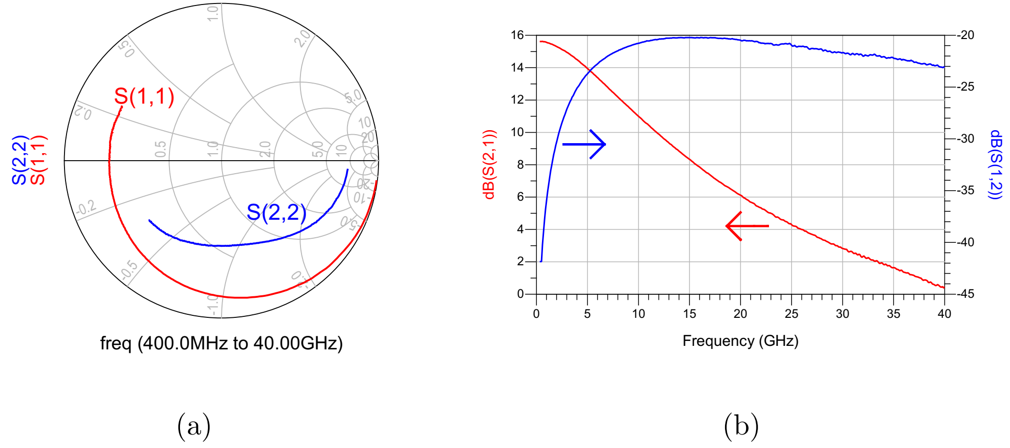
6×75 µm devices with 20 V drain voltage and 100 mA/mm drain current can be seen in Fig. 3.6 and Fig. 3.7, respectively.

These parameters also lead to many parameters that are used to characterize the transistors. Maximum available gain (MAG), cut-off frequency (f_T), and maximum oscillation frequency (f_{max}) can be calculated and the stability of the transistors can be checked using S-parameter data. Stability factor (K factor) of the transistor shows the probability of having a reflection coefficient greater than one under all possible terminations, and is defined as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|}, \tag{3.2}$$

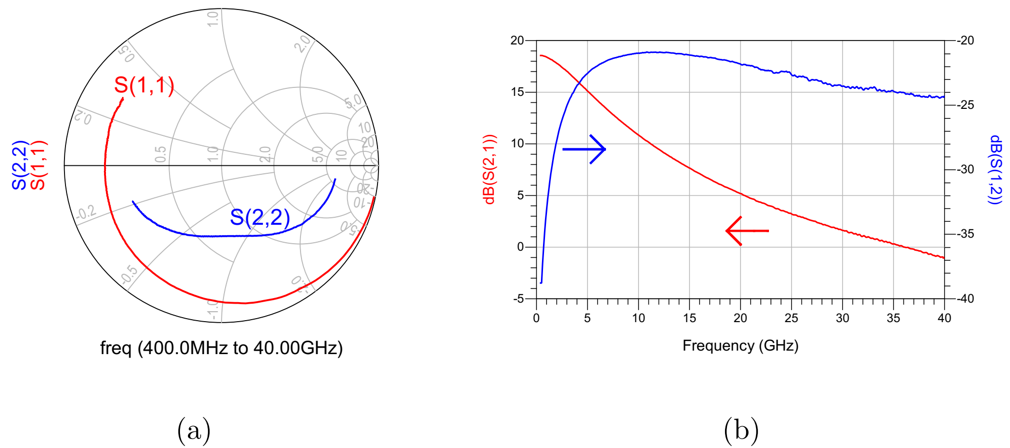
where Δ is given as:

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}|. \tag{3.3}$$



(a) (b)

Figure 3.6: S-parameters of a 4×75 µm HEMT; a) IRC (S_{11}) and ORC (S_{22}), b) Forward transmission (S_{21}) and reverse transmission (S_{12}).



(a) (b)

Figure 3.7: S-parameters of a 6×75 µm HEMT; a) IRC (S_{11}) and ORC (S_{22}), b) Forward transmission (S_{21}) and reverse transmission (S_{12}).

MAG is the gain value that can be achieved with a perfect match at the input and output sides of the device. MAG is dependent on the stability factor, and is calculated as:

$$\text{MAG} = \begin{cases} \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{(K^2-1)}\right), & \text{if } K > 1 \\ \frac{|S_{21}|}{|S_{12}|}, & \text{if } K \leqslant 1. \end{cases} \tag{3.4}$$

MAG decreases with larger device peripheries due to higher parasitic effects and mismatch losses between device fingers. Fig. 3.8 shows MAG values of typical 4×75 µm and 6×75 µm transistors from our fabrication, which have 7.5 dB and 7 dB MAG values at 35 GHz, respectively.

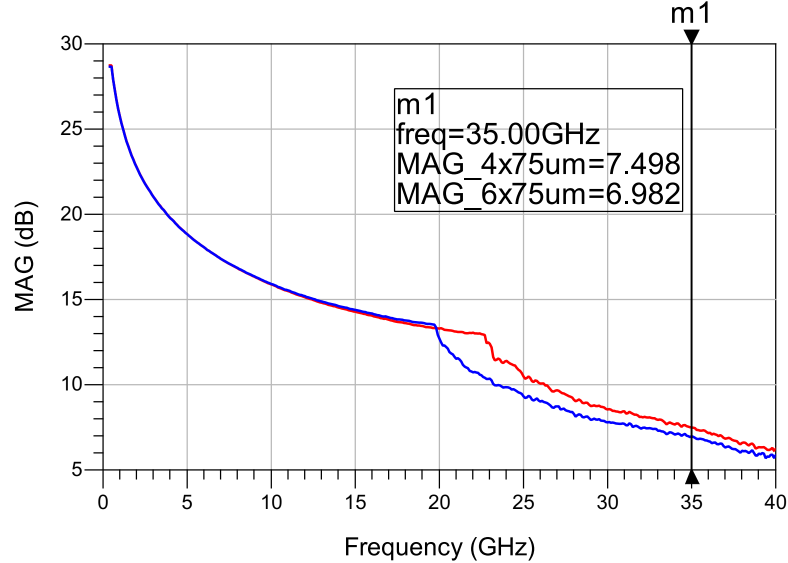


Figure 3.8: MAG plots of 4×75 µm and 6×75 µm devices.

f_T is the frequency where transistor's current gain (H_{21}) crosses 1, and is defined as:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}, \tag{3.5}$$

where g_m is the transconductance of the device, C_{gs} is the gate-to-source capacitance, and C_{gd} is the gate-to-drain capacitance.

f_{max} is the frequency at which unilateral power gain (G_U) (or the stable region

of MAG) of the device becomes unity, i.e., 0 dB, and is calculated as:

$$f_{max} = \frac{f_T}{2\sqrt{\pi f_T C_{gd}(R_s + R_g + R_{gs} + 2\pi L_s) + G_{ds}(R_s + R_g + R_{gs} + \pi f_T L_s)}}, \tag{3.6}$$

where R_s is the source resistance, R_g is the gate resistance, R_{gs} is the gate-to-source resistance, L_s is the source inductance, and G_{ds} is the output conductance.

f_T and f_{max} of a transistor can be easily determined using the S-parameter measurement data by calculating its current gain and MAG, and finding their zero-crossing points. Fig. 3.9a shows an example for a 4×75 µm device, where its current gain and MAG parameters are extrapolated to achieve zero-crossings by fitting these parameters with 20 dB/dec. For this transistor, f_T is calculated as 35.8 GHz and f_{max} is calculated as 82.6 GHz. For a 6×75 µm device, f_T and f_{max} are calculated as 37.3 GHz and 76 GHz, respectively, which is shown in Fig. 3.9b.

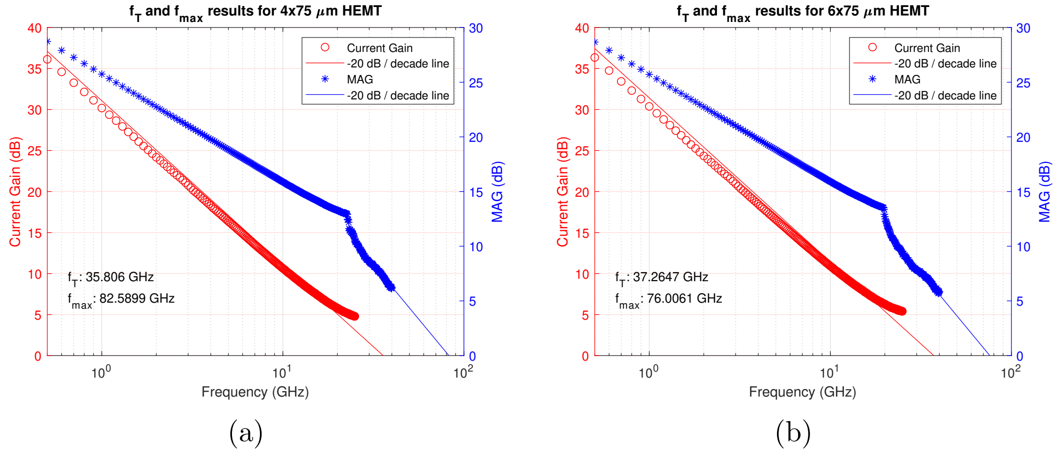


Figure 3.9: Current gain and MAG graphs and extrapolation fits for f_T and f_{max} calculations of a 4×75 µm HEMT (a) and a 6×75 µm HEMT (b).

3.3 Large-Signal HEMT Characterization and Hybrid Load-Pull Measurement Setup

Power amplifier design requires large-signal characterization of HEMT devices, as the input and output impedances of transistors vary with source power level,

and become different than the impedances that are extracted from the small-signal measurements. While the source power level of the transistor increases, the gain starts compressing, the output power becomes saturated, and the optimum impedance points for the gain and the output power, as well as efficiency, start to differentiate. The input and output impedance values at the gain compression are used to match a transistor for the highest output power or efficiency. These impedance points are determined via vector-based load-pull measurements, where the output power, efficiency, and gain of the device are measured.

Vector-based load-pull measurement system is based on a network analyzer with source and load tuners. A network analyzer can be used as a signal generator as well as a vector-receiver. With the calibration at the device-under-test (DUT) plane for on-wafer measurements, reflected and forward-traveling waves sampled from low-loss couplers are analyzed by the measurement software, AMCAD Engineering's IVCAD, to determine the desired parameters for each frequency point of the calibration. For instance, delivered input power, output power of DUT, and the impedances presented by the tuners are constantly being measured in vector-based load-pull measurements.

Tuners and the other components in the setup, such as cables, might create a significant amount of loss depending on the frequency of interest. The load impedance seen by DUT, that is the ratio of the reflected wave by the forward-traveling wave, is limited by the losses in the system. The optimum load impedance of the transistor changes according to the bias condition as well as the parasitic components, which make it also dependent on the frequency of interest. For higher frequencies, it becomes impossible to determine the optimum load impedances of transistors using passive load-pull systems for small devices. To overcome this issue, a hybrid load-pull system is used to determine the optimum load and source impedances of the transistors at 35 GHz. Fig. 3.10 illustrates the schematic of a hybrid load-pull measurement setup. In this setup, an external signal is amplified and injected to the output of DUT to boost the reflected wave which is no longer limited by the original reflected signal as in a passive load-pull measurement [24]. For a hybrid system, a smaller active injection signal with a smaller amplifier is used to overcome the losses. The hybrid load-pull

measurement system, consisting of Keysight PNA and Maury tuners, is shown in Fig. 3.11.

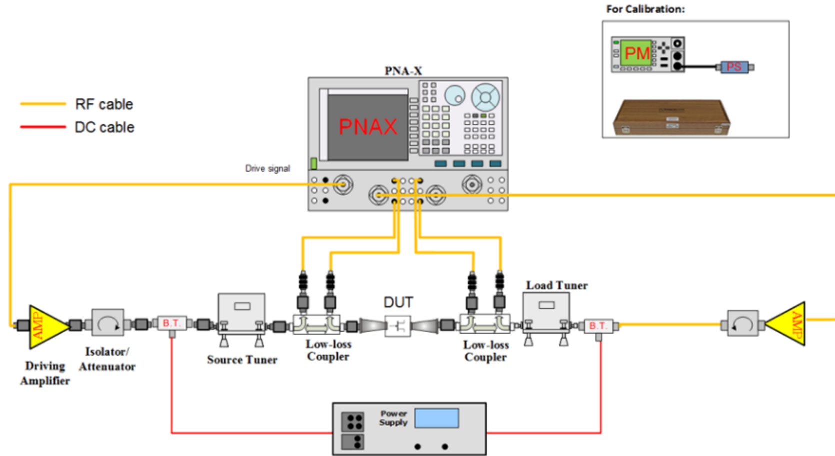


Figure 3.10: Schematic of the hybrid load-pull measurement setup.

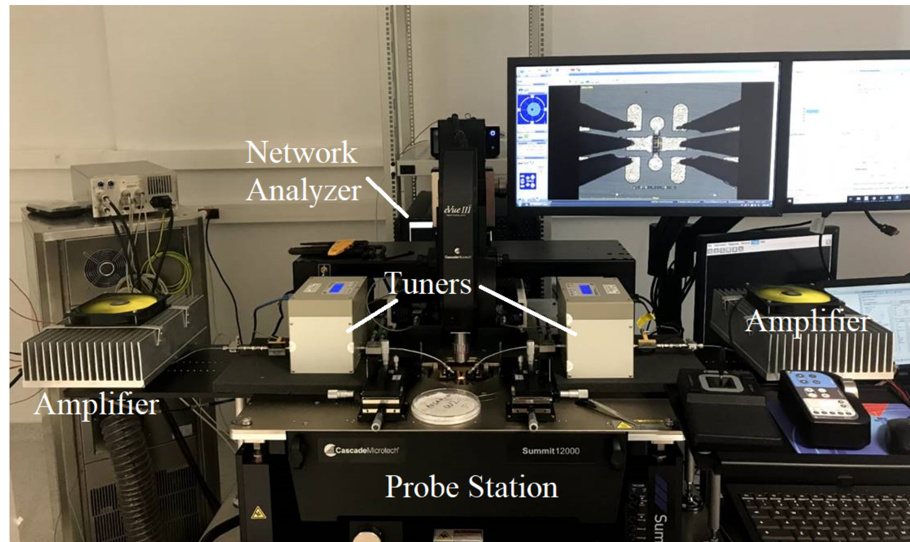
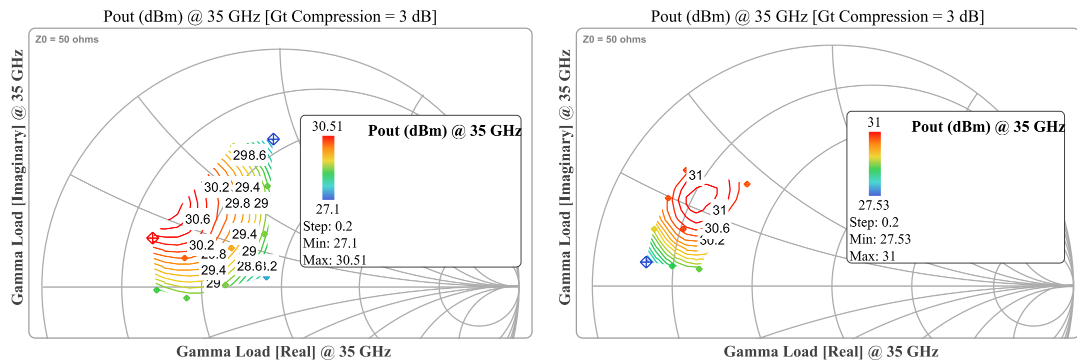


Figure 3.11: The hybrid load-pull measurement setup.

The load impedance points that are scanned by passive load-pull configuration at 35 GHz can be seen in Fig. 3.12a. The drain voltage is 20 V and the drain current is 100 mA/mm for these large-signal measurements. As the impedance points that are shown to DUT by tuners are limited by the losses in the system for the passive load-pull measurement, the contour for output power or efficiency

can not be completed for a 6×75 µm HEMT. With the injection of an external signal, further impedance points in the Smith's Chart can be achieved in the hybrid load-pull measurement, which is shown in Fig. 3.12b for the same 6×75 µm device. These data are analyzed together to see the completed contours for the output power, efficiency, and gain contours of the device, which can be seen in Fig. 3.13. As an example, the source impedance of the 6×75 µm device is set to (11−13i) Ω, which is matched for the highest gain by source-pull tool of the software for 3 dB gain compression point. The highest output power of 31 dBm is achieved at the optimum load impedance of (16+14i) Ω with this transistor data. The optimum load impedance points for maximum drain efficiency and maximum gain can also be analyzed using this data.



(a) Load impedance points scanned in the passive load-pull measurement.

(b) Load impedance points scanned in the hybrid load-pull configuration.

Figure 3.12: Comparison of passive and hybrid load-pull measurements for a 6×75 µm HEMT.

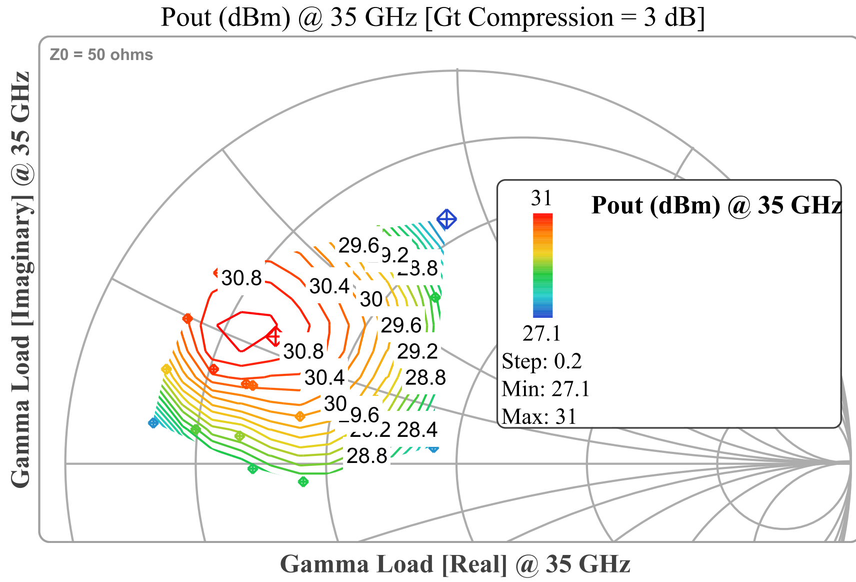


Figure 3.13: Combined load impedance points scanned in the hybrid load-pull measurement, showing output power contours.

Chapter 4

HEMT Layout Design and Gate Optimization

4.1 HEMT Layout Design

HEMT layouts are designed according to fabrication limitations and the frequency of interest. MAG of a transistor decreases with an increasing number of gate fingers due to the mismatch losses and higher parasitic effects. On the other hand, the output power of a transistor increases with larger peripheries (gate width of a finger times gate finger number), which is controllable via HEMT layout design. Moreover, the frequency where the transistor stops to provide gain (f_{max}) gets higher as the gate length gets smaller. Therefore, smaller gate lengths are necessary to work at mm-wave frequencies. Smallest possible gate length is 150 nm for our fabrication with the standard gate process according to the capabilities of the E-beam lithography equipment.

The layout of the transistor, the gate structure, passivation layer, and metal thicknesses affect the intrinsic parameters of the transistors. A basic small-signal equivalent circuit for a HEMT is given in Fig. 4.1, showing the intrinsic device [25].

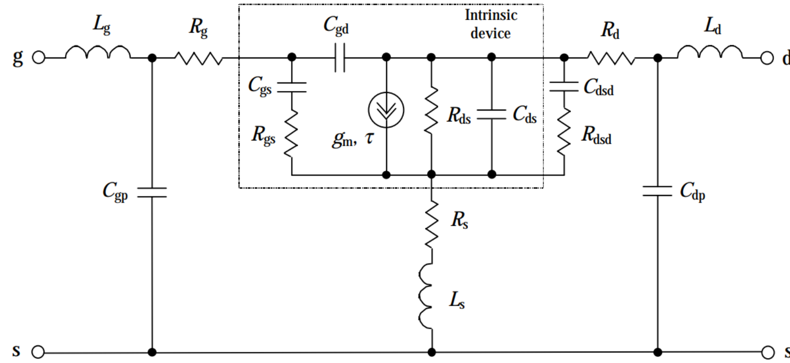
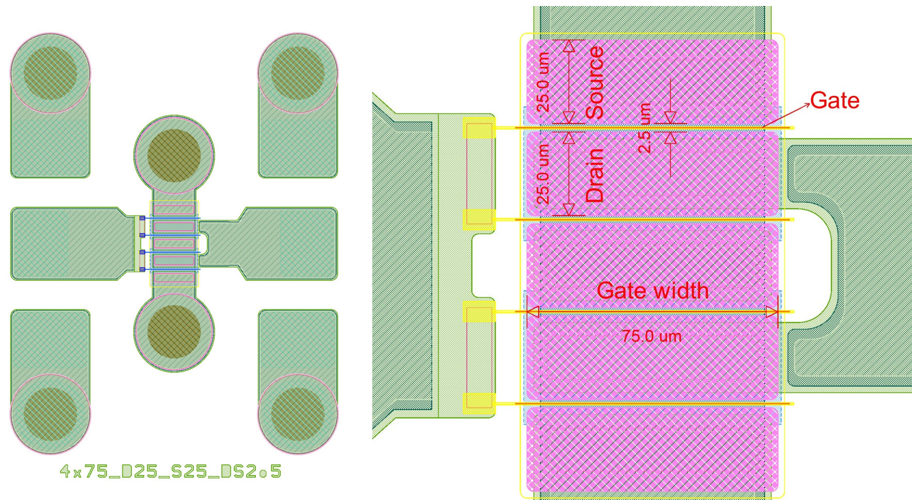


Figure 4.1: Small-signal equivalent circuit for a HEMT, showing its intrinsic parameters.

Fig. 4.2a shows the layout of a 4×75 µm HEMT, including the gate lithography patterns, sources contacts, drain contacts, via holes, and pads for the gate and drain contacts. This HEMT has four fingers, each being 75 µm width, which results in a total gate periphery of 300 µm. The contact region length of a source contact is 25 µm, as well as a drain contact. The distance between a source and a drain contact is 2.5 µm, which determines the channel length of the device. These dimensions are shown in Fig. 4.2b.



(a) HEMT layout showing four fingers, gate and drain pads, and via-holes.

(b) The drain contact length, source contact length, drain-to-source distance, gate width parameters of HEMT.

Figure 4.2: The layout of a 4×75 µm HEMT.

To create a variety for HEMT layouts, gate periphery, drain width, source width, and drain-to-source spacing parameters are swept for several chosen values. Fig. 4.3 shows an example of the designed HEMT reticle, which includes devices of 4, 6, and 8 fingers with 50 µm and 75 µm gate widths, 18 µm, 25 µm, and 32 µm drain or source length, and 2 µm, 2.5 µm, and 3 µm drain-to-source distances. These transistors are characterized after the fabrication for small-signal and large-signal, and the appropriate sizes are chosen for the MMIC design.

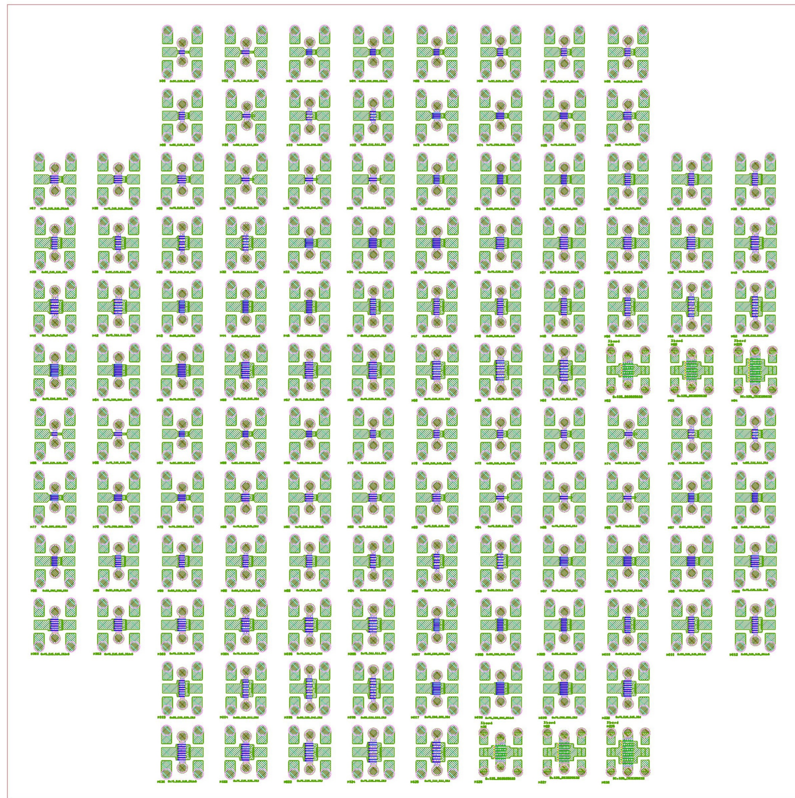


Figure 4.3: Photomask design for various HEMT structures.

A parametric study is carried out to see the device performance depending on the gate foot and head (gate-coupled field-plate) lengths for the T-gate structure. f_T and f_{max} of the transistors depend on its intrinsic parameters. They do not monotonously increase while the gate length decreases due to parasitic capacitances and resistances of the device, hence there is room for optimization when the active device fabrication process is set.

4.2 Optimum T-Gate Design

As the gate length affects the performance of the device directly, its structure is also significant and can be altered to obtain better performance. The smaller gate lengths are necessary to work at high frequencies, and 150 nm is common for HEMTs aiming *Ka*-band in the industry [26–28]. However, the gate resistance becomes dominant and limits the gain of the device as the gate length decreases. Therefore, it is common to use a gate-coupled field-plate, i.e., T-gate, to elevate the device performance by modulating the electric field in the channel and minimizing the parasitic effects [29, 30]. The structure and the position of the gate, gate-to-source distance, and the passivation process affect the intrinsic parameters of the device, such as C_{gs}, C_{gd}, and R_g. These effects change small- signal and large-signal characteristics, as well as the DC performance of the transistors.

I-gate is the easiest structure to fabricate, and presents high saturated drain current levels. However, the devices with I-gate structure tend to have higher leakages, and experience the current collapse phenomena [31]. T-shaped gate structure reduces the gate resistance, which helps to increase f_{max} [8]. Moreover, transistors with I-gate structures have lower breakdown voltages, due to the large electric field confinement around the same spot in the channel. T-gate decreases the peak electric field and spreads the electric field by creating another peak near the drain side of the gate foot, as shown in Fig. 4.4. Therefore, transistors with T-gate structures have lower leakages and higher breakdown voltages, yielding to higher output power densities.

At *Ka*-band frequencies, the most significant parameter for our process is the available gain of the transistor, since the results do not achieve proper values compared to the industry [26, 27]. Therefore, for the T-gate structure, a parametric study is carried out to determine the best gate structure fit for the highest possible gain, i.e., highest f_{max}. The frequency performance of the transistors depends on the parasitic capacitance and resistance values as seen in (3.5) and (3.6), and these parasitic components change according to the device layout, especially with the gate-to-source distance (L_{gs}) and the gate structure (gate head

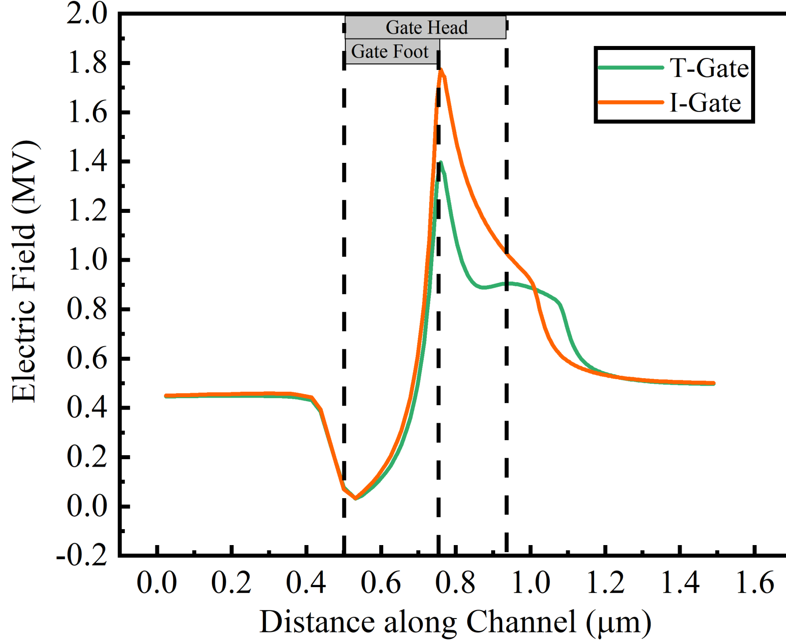


Figure 4.4: Electric field under the gate foot with respect to gate-to-drain distance.

length (L_{head}) or gate foot length (L_{foot})). These independent variables impact C_{gs}, R_s, and R_g of the transistor.

The change in R_s, i.e., access resistance, increases with higher L_{gs} values, having a larger area between gate and source regions. Access resistances of HEMTs have a significant effect on the total delays of the devices, resulting in lower f_T and f_{max} values [30, 32].

Gate-to-drain distance (L_{ds}) is another parameter that affects the device performance. f_{max} can be improved by decreasing L_{ds}, since R_g is also decreased while the variation in C_{gd} is negligible [30]. On the other hand, f_T is not dependent on L_{ds} since the transconductance and the parasitic capacitance values are not affected by this parameter. There is a compromise between f_{max} and the breakdown voltage in terms of L_{ds}, as the breakdown voltage can be improved by increasing L_{ds}.

With a T-gate structure, R_g is smaller compared to I-gate with the same length, yet the parasitic capacitances are needed to be observed. C_{gs} and C_{ds} values increase with increasing L_{head} and the height of the gate foot and head metals. Therefore, there is an optimum value for L_{head} for a fixed L_{foot} for the highest f_{max}, since it is dependent on R_g, as well as C_{gs} and C_{ds} [30].

In this study, small-signal performances of different L_{foot} and L_{head} combinations are analyzed. Small-signal measurements are performed with CW at room temperature up to 40 GHz, and f_T and f_{max} values are found by fitting the MAG and H_{21} data with 20 dB/dec. L_{gs} is kept constant, while different L_{head} and L_{foot} values are studied for the highest gain for two different total gate peripheries. For this purpose, 4×75 µm and 6×75 µm HEMTs with 2.5 µm L_{ds} are used. Gate foot and head lengths are swept to have 10 variations for both transistors. Small-signal characterization of the transistors from three different reticles are performed, and the average results of 12 measurements for each gate type are given in Table 4.1.

The effect of L_{foot} on f_T, f_{max}, and MAG can be seen in Fig. 4.5 for 4×75 µm HEMT with 500 nm L_{head}. The frequency performance of the device is improved with smaller L_{foot} values, as expected.

The results for f_T, f_{max}, and MAG are shown in Fig. 4.6, for the same device with 150 nm L_{foot} with respect to different L_{head}. As explained, there is an optimum value for L_{head} for the definite L_{foot} and L_{gs} values, keeping the parasitic components ideal to enable a higher gain.

This study shows that a T-gate with 150 nm gate foot and 500 nm gate head gives the highest f_{max}, i.e., highest MAG, at 35 GHz, for both transistor sizes. This optimization will only hold for the selected device layout and the mentioned fabrication, since the dielectric properties of the process also affect the device performance, relating to the parasitic capacitance values and the surface trap mechanism.

Table 4.1: Small-signal characterization results for different T-gate structures of 4×75 µm and 6×75 µm HEMTs.

Transistor	L_{foot} **(nm)**	L_{head} **(nm)**	**MAG at 35 GHz (dB)**	f_T **(GHz)**	f_{max} **(GHz)**
4×75 µm	150	400	7.0	42.9	80.6
	150	500	7.6	44.2	84.9
	150	600	7.3	42.7	83.4
	150	700	7.4	41.3	83.2
	200	400	7.1	41.8	79.8
	200	500	7.2	40.8	81.3
	200	600	7.2	39.6	81.1
	200	700	7.1	38.4	80.0
	250	500	7.0	38.0	78.3
	250	600	7.0	36.9	78.4
6×75 µm	150	400	6.6	48.2	75.0
	150	500	6.7	46.6	76.0
	150	600	6.6	45.7	75.1
	150	700	6.6	44.1	74.8
	200	400	6.4	44.7	72.8
	200	500	6.6	43.9	74.3
	200	600	6.5	42.4	73.7
	200	700	6.4	41.1	72.6
	250	500	6.4	40.9	72.3
	250	600	6.4	39.7	71.9

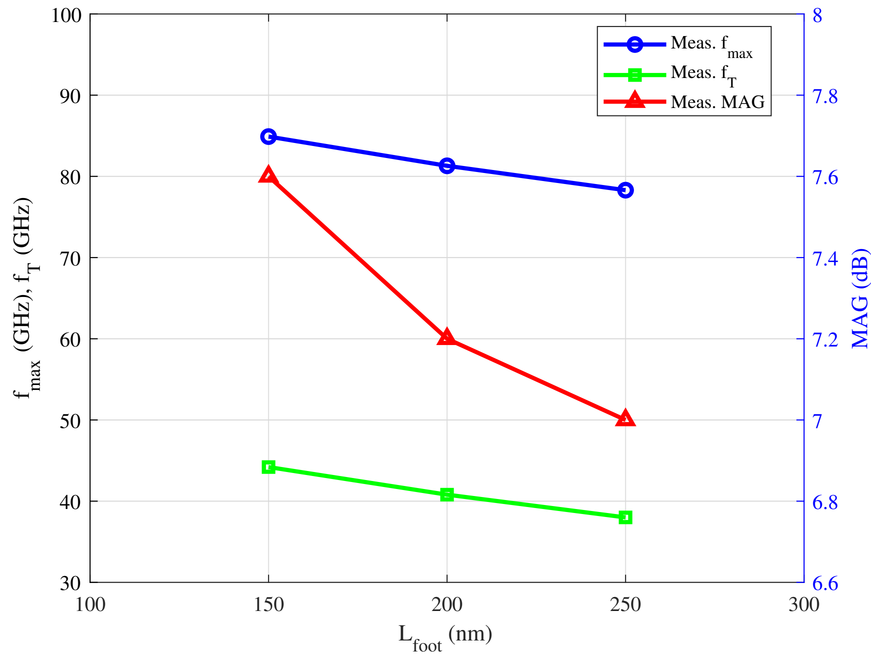


Figure 4.5: Measurement results of f_{max}, f_T, and MAG at 35 GHz of a 4×75 µm HEMT with 500 nm L_{head} with different L_{foot} values.

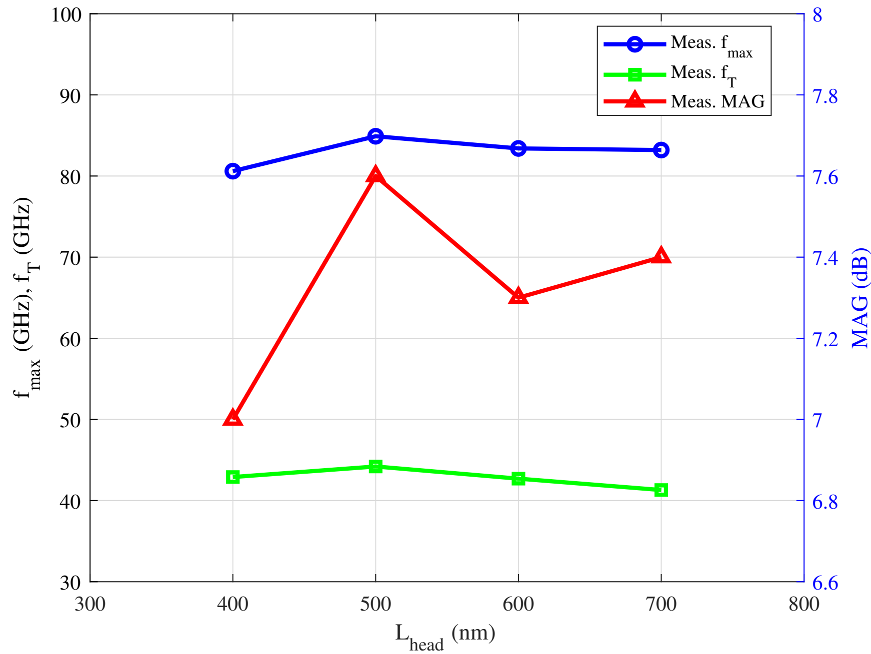


Figure 4.6: Measurement results of f_{max}, f_T, and MAG at 35 GHz of a 4×75 µm HEMT with 150 nm L_{foot} with different L_{head} values.

Chapter 5

Three-stage Amplifier MMIC Design

In this chapter, a three-stage amplifier MMIC, designed using the aforementioned fabrication process, is described. This design is based on the small-signal and large-signal measurements of the fabricated transistors. Large-signal measurement data is analyzed using the measurement software, AMCAD Engineering's IVCAD. The small-signal simulations are performed using Advanced Design System (ADS) software from Keysight. The layout design and EM simulations are also carried out in ADS, using the developed EM substrate based on our fabrication as described in [33]. The dielectric constant and the thickness of dielectric layer of MIM capacitors are set according to the fabrication process. As mentioned in Chapter 2, the capacitance density of MIM capacitors is $175\,\mathrm{pF/mm^2}$, and the density of TFR layer is $30\,\Omega/\square$. The design is carried out using the transistor measurements from the first 3-inch *Ka*-band fabrication of NANOTAM.

This design aims 16 dB small-signal gain with more than 31 dBm output power. The first step of the design process is to choose the device size for the desired specifications. Then, even-mode stability is achieved using a parallel *RC* circuit at the transistor's input side. The output matching network is designed considering the optimum impedance points of the transistor for the maximum output

power and the maximum efficiency. Interstage and input matching networks are designed aiming the maximum gain from the overall design. Bias networks are embedded in the matching while having enough in-band RF isolation. Matching network designs are finalized with positioning proper RF and DC pads for on-wafer measurements. Even-mode stability of three-stage design is checked at the final layout stage, as well as odd-mode stability, which is ensured with the additional elements.

5.1 Transistor Layout and Stability Circuit Design

Different transistor layouts are analyzed regarding their small-signal performance, and a 4×75 µm device with 2.5 µm drain-to-source distance is selected for the design. The small-signal and large-signal measurement data of the transistor include RF pads and the transmission lines between the device and these pads. Therefore, a device reference plane is obtained by de-embedding the transmission line and RF pads, as shown in Fig. 5.1. This de-embedding is done using the de-embedding component of ADS with the EM simulation data of the structures.

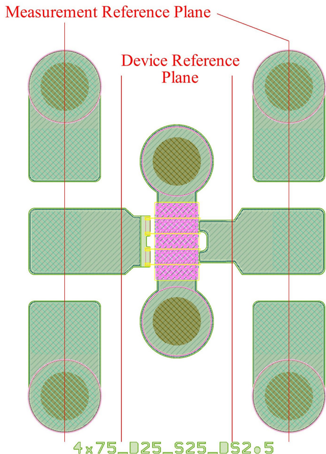


Figure 5.1: Layout of 4×75 µm HEMT showing the measurement and device reference planes.

The stability of an MMIC should be considered via different approaches to ensure both even-mode and odd-mode stability, and will be discussed in this chapter. On the other hand, the transistor's stability should be taken into interest before designing the MMIC. To measure the likelihood of oscillations, stability parameters of a transistor can be investigated by analyzing its reflection coefficients. If the magnitude of the input or output reflection coefficient is greater than one while the output or input is terminated with a load, the transistor could oscillate under this condition due to the reflection gain. The stability factor (K factor) is calculated using S-parameter data of the two-port network, and described in (3.2) in Chapter 3. When the K factor of a two-port network is greater than one, it is unconditionally stable, i.e., any load can be used to terminate the network's input and output. There are also two other parameters that show the stability of a network, μ and μ', which are defined as:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta(S_{11}^*)| + |S_{21}S_{12}|} > 1, \tag{5.1}$$

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta(S_{22}^*)| + |S_{21}S_{12}|} > 1. \tag{5.2}$$

μ and μ' measure the radius from the center of the Smith's Chart to the nearest unstable impedance point in the output plane and the input plane, respectively [34]. These parameters also need to be greater than one to move the nearest unstable impedance off the Smith's Chart. The higher values of these parameters mean a broader stabilization, unlike the K factor whose value does not matter as long as it is greater than one. Therefore, all of these parameters can be used to analyze the even-mode stability of a transistor.

Even-mode stability of the selected transistor is checked after de-embedding for a frequency range of 400 MHz to 40 GHz, which is the frequency coverage of the measurement setup. A parallel RC stability network is designed to ensure unconditional stability over a large frequency range. RC network introduces additional loss to the circuit to decrease the gain, hence there is a trade-off between the K factor and the available gain. The values of the resistor and capacitor are tuned so that the gain at higher frequencies is not dramatically affected. The stability circuit decreases the available gain of the transistor from 6.8 dB to 6.5 dB

at 35 GHz while stabilizing it unconditionally down to 1.7 GHz. Fig. 5.2 gives the available gain and the K factor of the $4 \times 75\,\mu\text{m}$ HEMT with and without the designed stability network.

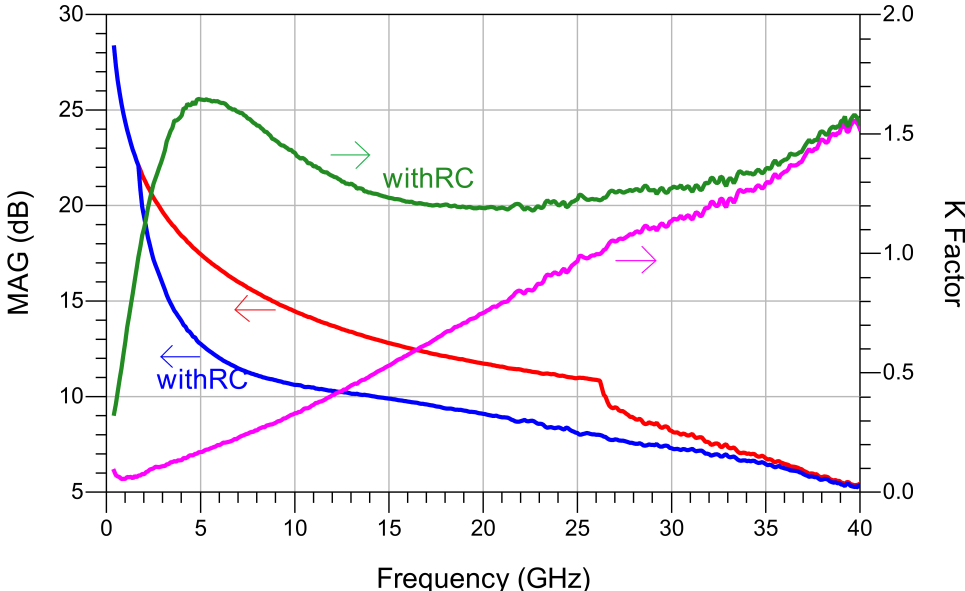


Figure 5.2: MAG and K factor of the selected HEMT with and without stability network.

The layout of the designed RC circuit is shown in Fig. 5.3. This circuit is formed with two resistors and a capacitor to create symmetry for RF signal. The value of one resistor is $240\,\Omega$ and the value of the capacitor is 0.25 pF.

The transistor is not unconditionally stabilized with this circuit at the frequencies below 1.7 GHz, in order to keep the transistor's gain as high as possible at high frequencies. However, the MMIC will be unconditionally stable after designing the matching circuits with stability components which will add losses, and these stability parameters will be analyzed again for the MMIC later in this chapter.

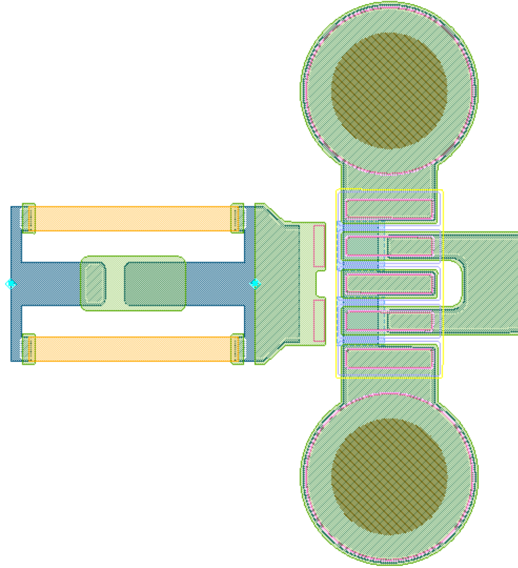
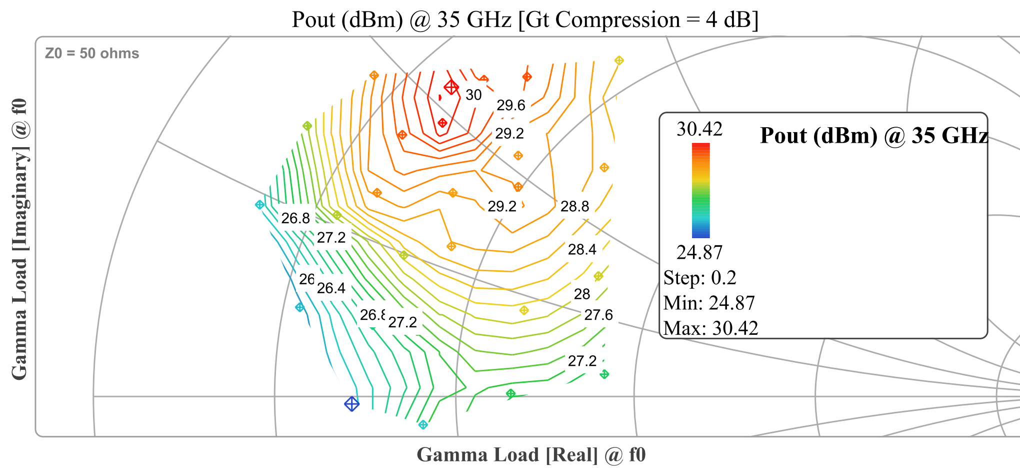


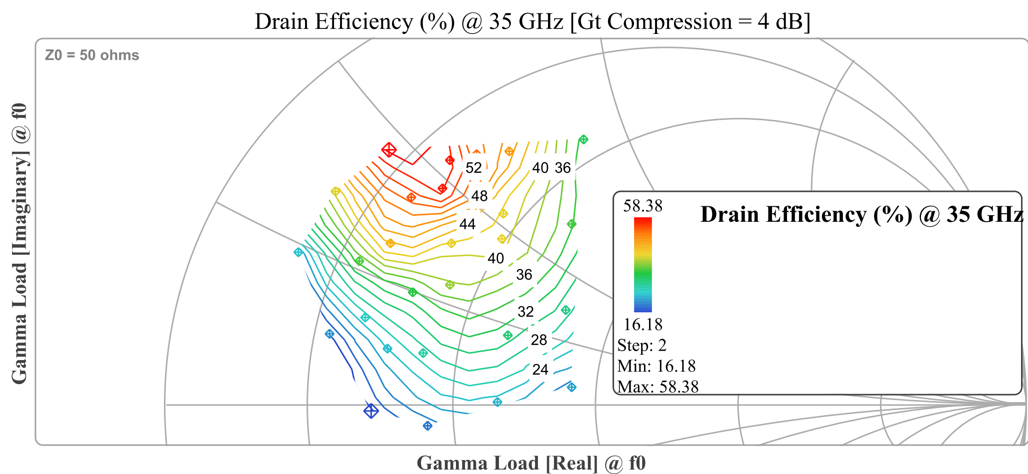
Figure 5.3: Layout of the RC stability network and the transistor with the de-embedded pads.

5.2 Topology Selection

This MMIC is aimed for 16 dB small-signal gain with 31 dBm output power. The selected $4\times75\,\mu$m transistor with the RC stability circuit gives a MAG greater than 6.5 dB at 35 GHz. Therefore, the design will be a three-stage MMIC to achieve the desired gain. The large-signal measurements of the selected device is also investigated to see the load and source impedances for the maximum output power, especially for the output matching. The load-pull measurements are performed using the hybrid load-pull setup, as described in Chapter 3.3. Even with this setup, the centers of output power and drain efficiency contours are at the edge of the measurement plane, due to limited area of possible load impedances. The transistor's output power contours are given in Fig. 5.4a, showing the optimum load impedance as (13+27i) Ω at 35 GHz, with a source impedance of (8−17i) Ω. Besides, Fig. 5.4b shows the optimum load impedance for drain efficiency as (8+23i) Ω, giving a maximum value of 58%, for the same source impedance. This source impedance is set for the highest possible gain of the transistor. The transistor has a maximum output power of 30.4 dBm at 4 dB gain compression at 35 GHz.



(a)



(b)

Figure 5.4: Output power (a) and drain efficiency (b) contours of the selected 4×75 µm transistor at 35 GHz.

Considering the possible highest output power of the transistor, two transistors will be used at the output stage, to achieve 31 dBm output power around 5 dB gain compression point for the whole MMIC. There will also be two transistors in the second stage, since the driving capability of one transistor is not enough for two output stage transistors at low compression levels. The input stage will have one transistor as a pre-driver, resulting in 1:2:2 ratio for the design. The overall design will be optimized for the highest gain at 35 GHz with the maximum possible output power.

5.3 Output Matching Network

The design procedure of the introduced MMIC starts with the output matching network (OMN), which directly affects the output power and efficiency performance of the MMIC. The load impedances that are presented to the output stage transistors should be close to the optimum load impedance points for maximum output power and maximum efficiency to satisfy the design goals. OMN is carefully designed to achieve optimum load impedances for each output stage transistor, with a good symmetry and low loss.

The impedance of a transistor changes while the input power increases, i.e., the small-signal impedance is not the same as its large-signal impedance. Since power amplifiers would work at saturation, the input power level is very high compared to the small-signal measurements. Therefore, the load impedance of the transistor is optimized to be the optimum load impedance determined from the large-signal measurements to ensure the maximum output power and efficiency at higher input powers. Moreover, while the optimum impedances for the gain and the output power are the same in the small-signal operation, they become different at high input signals. This results in a trade-off between gain and the output power. In Fig. 5.5, transducer gain (G_t) and output power contours are given together, showing the optimum impedance for gain is (8+19i) Ω while it is (13+27i) Ω for output power at 4 dB gain compression level. This also means that the optimum matching for output power is different than the conjugate matching

for ORC (S_{22}), which causes relatively poor S_{22} values in reactively matched power amplifiers.

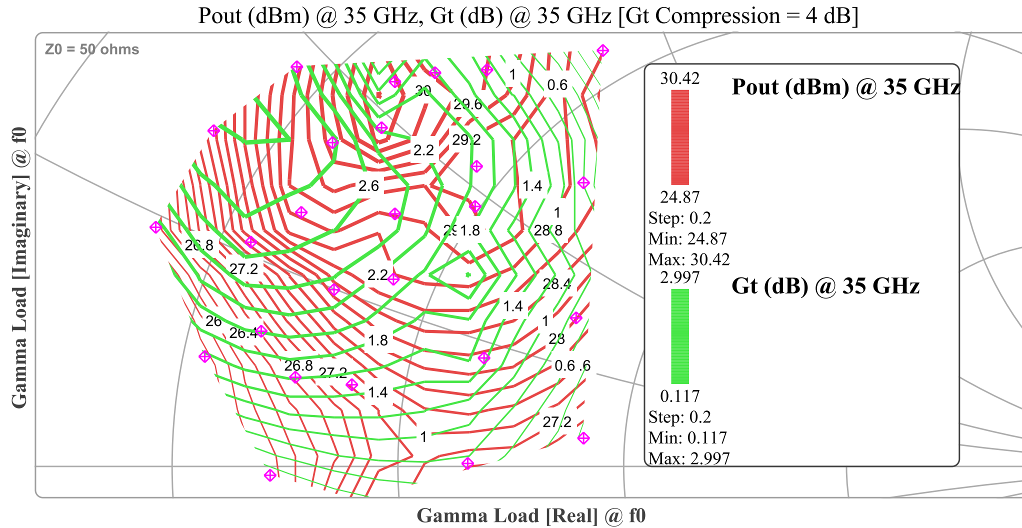


Figure 5.5: Gain (red) and output power (green) contours of the selected 4×75 µm transistor at 4 dB gain compression at 35 GHz, given together.

On the other hand, the optimum load impedance for efficiency may diverge from the optimum impedance point for output power. Fig. 5.6 shows the output power and drain efficiency contours drawn together. For the selected transistor, the impedance point for the maximum output power is inside the 56% efficiency contour, while the maximum efficiency is 58%. It shows that the optimum impedance points are not very far away in this case, meaning that it is easier to get high efficiencies with the maximum output power.

We decided to use two transistors at the output stage of the MMIC, which means the OMN would be a combiner as well as the matching circuit, i.e., cluster matching. The matching is optimized for the load impedance for the output power and drain efficiency at 35 GHz, however the impedances from 32 GHz to 37 GHz are also observed to have a proper matching for a wide frequency band. The schematic of the designed OMN is given in Fig. 5.7.

The bias line for the drain of the output transistors is also integrated into this matching. The isolation of the drain bias network is provided with 0.79 pF shunt

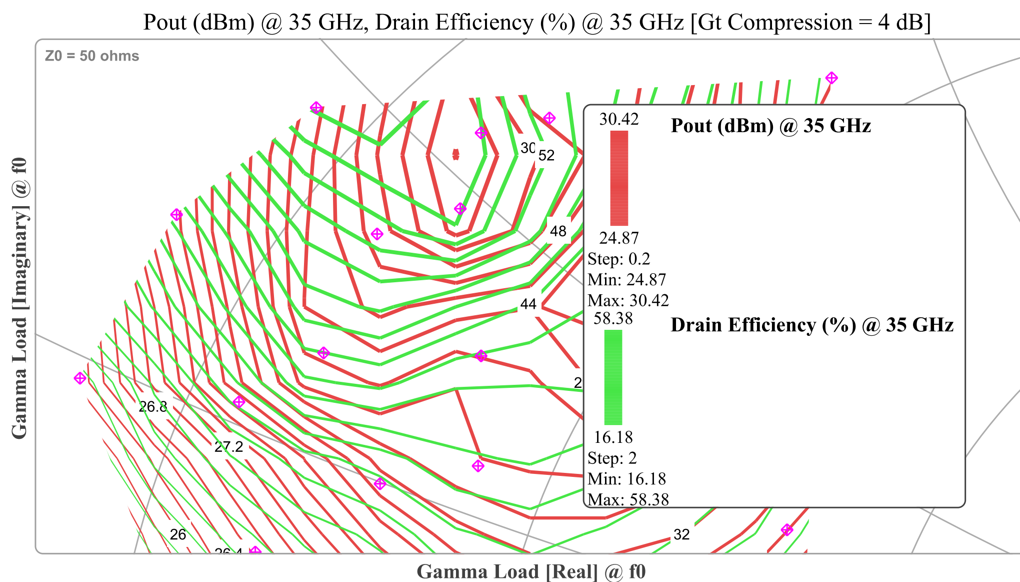


Figure 5.6: Output power and drain efficiency contours of the selected 4×75 µm transistor at 35 GHz, drawn together.

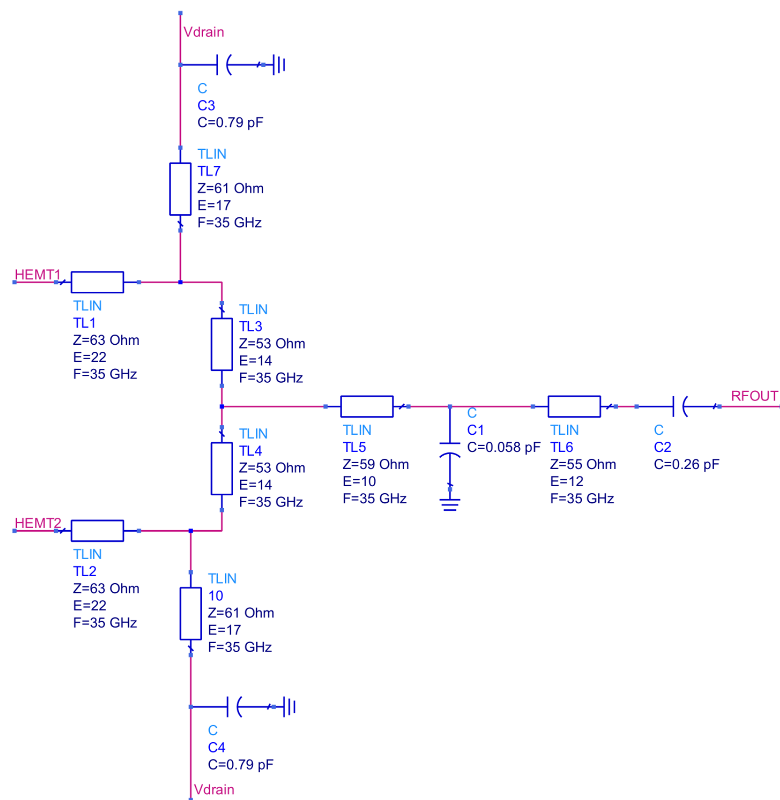
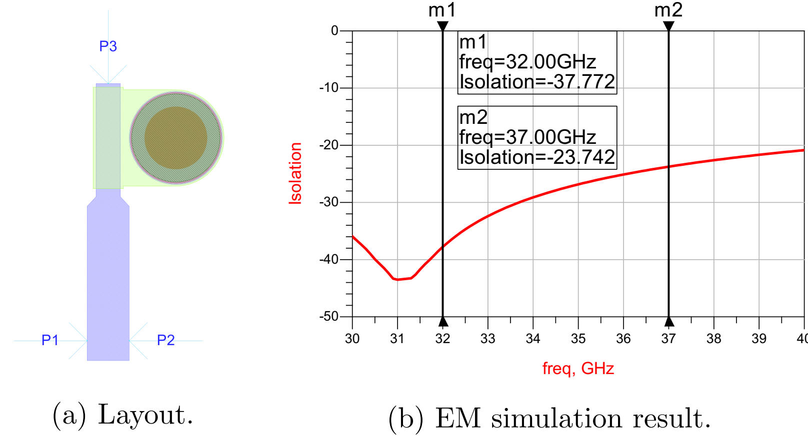


Figure 5.7: Schematic of the designed OMN.

capacitor in the line, which is checked via the EM simulation of the layout given in Fig. 5.8a. The isolation of the bias network from DC path (P3) to the RF path (P1 or P2) is below −23 dB for the frequency range of 32 GHz to 37 GHz, as shown in Fig. 5.8b. With a cluster matching, both transistors can be biased via one drain bias line. However, the bias lines are used at both sides of OMN to maintain the symmetry and to be able to give DC signal from both sides.



(a) Layout. (b) EM simulation result.

Figure 5.8: Layout and EM simulation result of drain bias network of the output stage transistors.

The load impedance that is shown to the output transistors with the designed OMN is given in Fig. 5.9, which are calculated using EM simulation results of its layout. The load impedance at 35 GHz is optimized to be (12.4+19.9i) Ω, which is between the optimum impedances for output power and drain efficiency. Also, it can be seen that the impedance range for the frequency band is very small, i.e., we have a small arc on the Smith's Chart.

As two transistors are in parallel at the output stage, the symmetry of the matching should also be considered. Two branches may have a phase difference even though the layout is symmetric, which can be observed through EM simulations by checking the impedance of each branch separately. The phase difference between the branches and the load impedances that are presented to the transistors at the upper and lower branches are shown in Fig 5.10a and Fig 5.10b, respectively. The phase difference should be as small as possible, while the presented impedances should be the same.

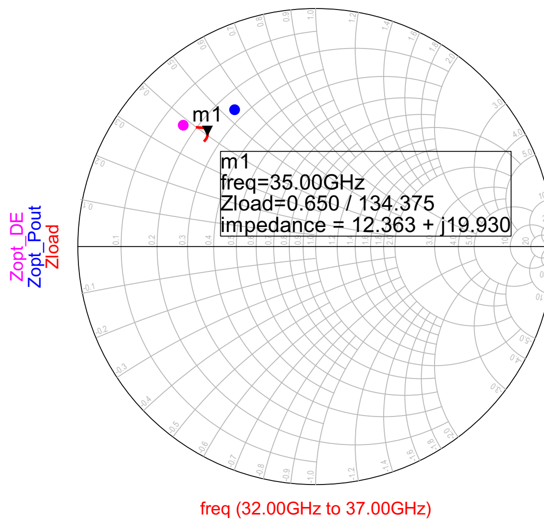
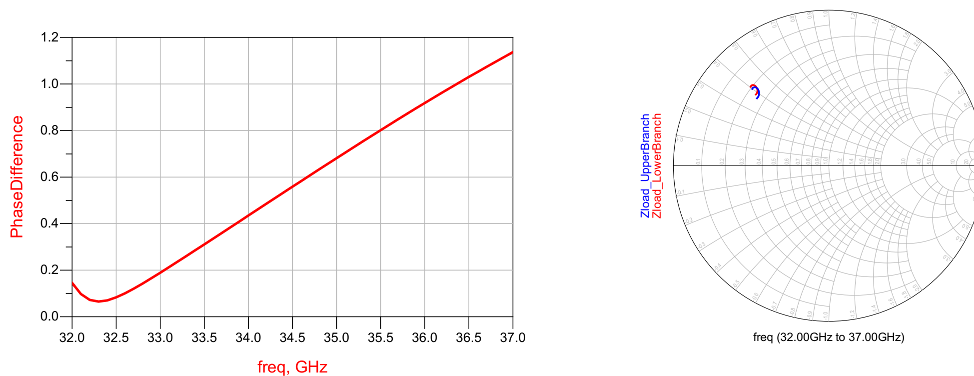


Figure 5.9: Load impedance shown to the transistors with the designed OMN from 32 GHz to 37 GHz (red), the optimum load impedance for maximum output power at 35 GHz (blue), the optimum load impedance for maximum drain efficiency at 35 GHz (magenta).



(a) Phase difference between the upper branch and the lower branch of OMN.

(b) Load impedances shown to the upper branch transistor (blue) and to the lower branch transistor (red).

Figure 5.10: Symmetry results of OMN from 32 GHz to 37 GHz.

The insertion loss of the OMN is another crucial parameter, besides the load impedance shown to the transistors. The insertion loss should be small to preserve the output power of the transistors through the matching network. This insertion loss is calculated via the MAG of the network, which gives the loss of a passive circuit by eliminating the mismatch losses. It is 0.4 dB at 35 GHz, as shown in Fig. 5.11.

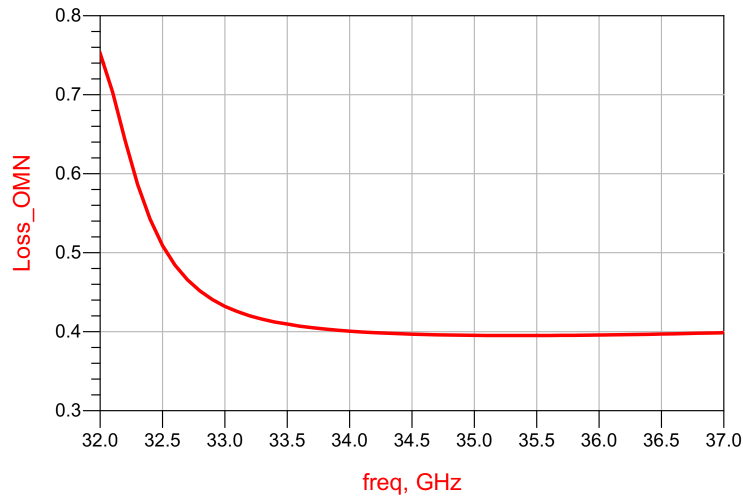


Figure 5.11: Insertion loss of the OMN from 32 GHz to 37 GHz.

The completed layout of OMN is shown in Fig. 5.12. The design is optimized as whole layout, and all of the given results are from the EM simulations of this layout.

5.4 Interstage Matching Networks

Designing a three-stage MMIC requires two interstage matching networks. While the output stage of this MMIC has two transistors, the second stage also needs to have two transistors to be able to drive the output stage sufficiently. The interstage matching network needs to present a good source impedance to the output stage transistor since this affects the gain performance of the MMIC. Besides, the load impedance shown to the second stage transistor should be considered to

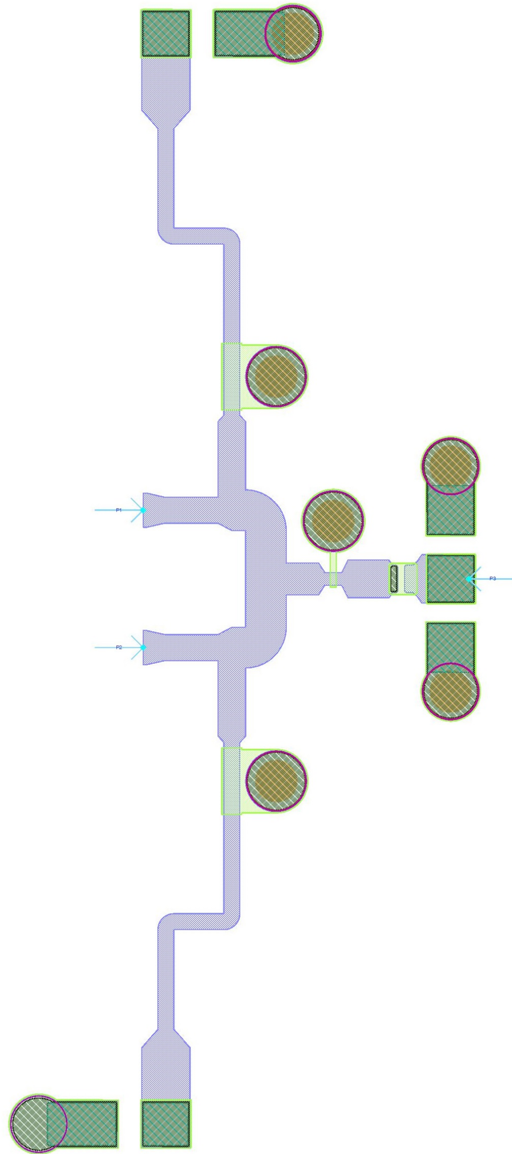


Figure 5.12: Completed layout of OMN.

get enough power to drive the output stage with the optimum gain. Therefore, this matching network is optimized considering both large-signal and small-signal operations.

The first interstage matching is from one of the second stage transistors to one of the output stage transistors. The gate bias line of the output stage and the drain bias line of the second stage are also included in the matching. The matching network is symmetrical at both branches, yet the bias lines are not connected for the parallel transistors due to its negative effect on the matching. Hence, these lines need to be biased from both sides. The schematic of the half of this interstage matching is given in Fig. 5.13.

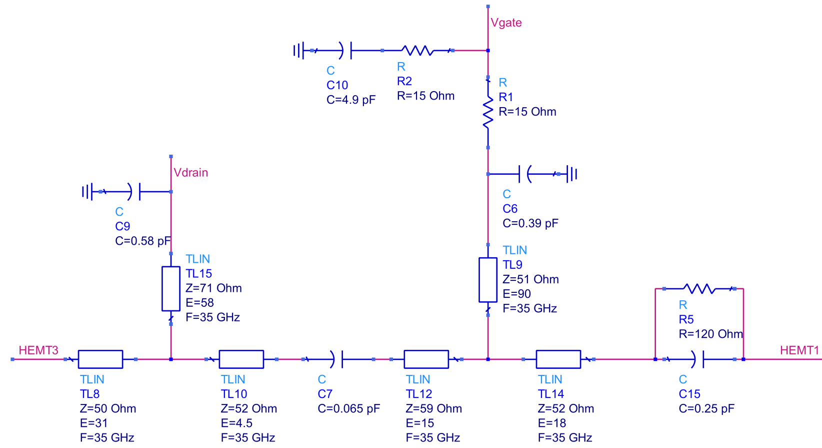


Figure 5.13: Schematic of the upper half of first interstage matching network.

The optimum source impedance for the output stage is discussed in Chapter 5.2, which is (8−17i) Ω for 4 dB gain compression point at 35 GHz, shown with source-pull contours for the optimum load impedance point in Fig. 5.14.

On the other hand, the transistors at the second stage would not saturate as far as the output stage transistors. They would work around 1 dB gain compression level, where the transistor's optimum load impedance for the output power is (15+24i) Ω at 35 GHz, while it is (13+21i) Ω for the maximum gain, shown in Fig. 5.15.

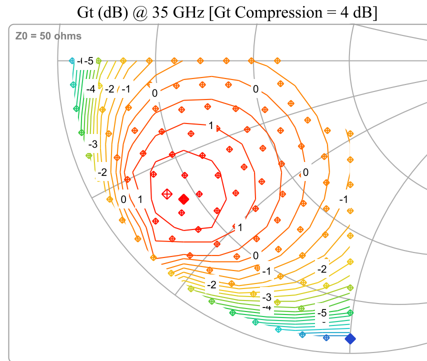
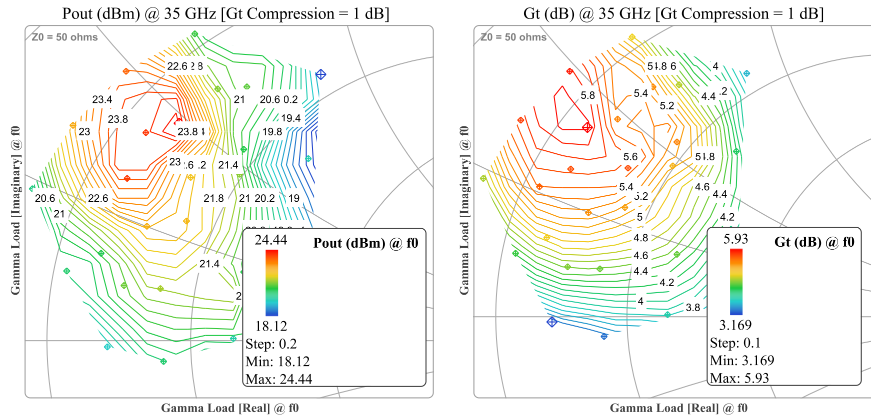


Figure 5.14: Source-pull contours of the 4×75 µm transistor at 4 dB gain compression point at 35 GHz.



(a) Output power contours. (b) Gain contours.

Figure 5.15: Output power and gain contours at 1 dB gain compression level at 35 GHz.

The matching is optimized considering the large-signal impedances at first, however it is overhauled with the second interstage matching and the input matching to achieve a better gain response for MMIC. The achieved results are given in Fig. 5.16. Considering the optimum source impedance for the output stage and the optimum load impedance for the second stage, the achieved impedances around 35 GHz are decent.

The insertion loss of the matching is also considered during the design optimization. The net insertion loss of this interstage matching network is given in Fig. 5.17.

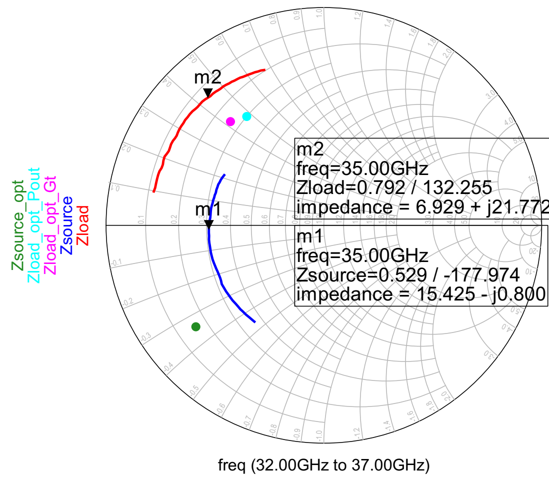


Figure 5.16: The source impedance of the output stage transistors (blue), the load impedance of the second stage transistors (red) from 32 GHz to 37 GHz, the optimum load impedance for maximum gain (magenta) and output power (cyan), and the optimum source impedance for the output stage (green) at 35 GHz.

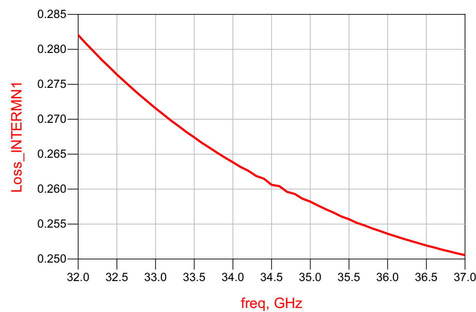


Figure 5.17: Insertion loss of the first interstage matching network from 32 GHz to 37 GHz.

The layout of this interstage matching network is shown in Fig. 5.18.

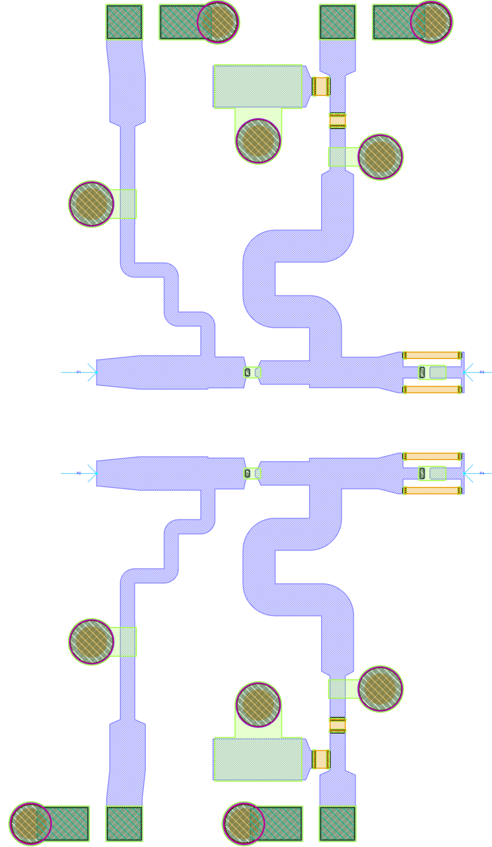
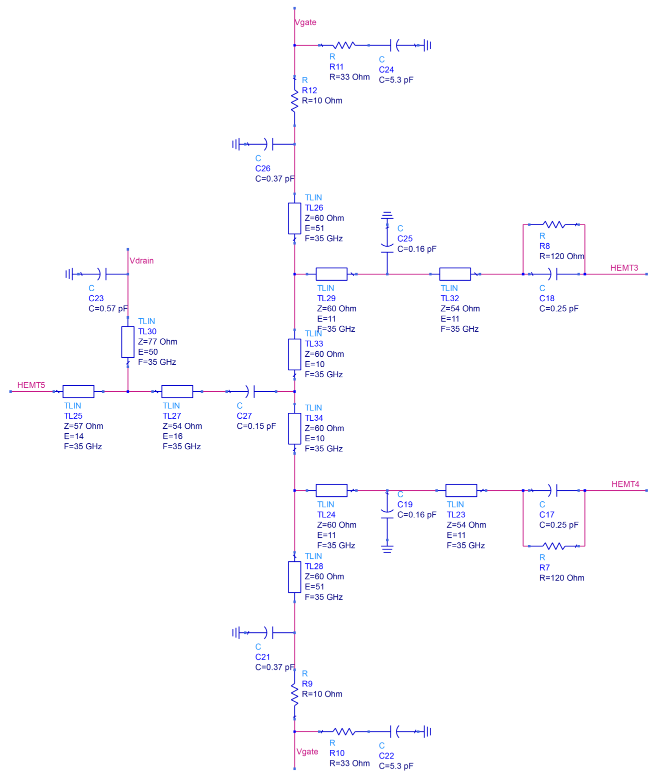


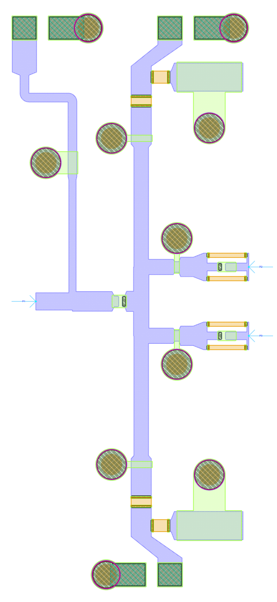
Figure 5.18: Completed layout of first interstage matching network.

The second interstage matching network is from the one first stage transistor to two of the second stage transistors. The bias networks are again integrated into the matching, while connecting the drain bias lines of the second stage transistors, which gives the flexibility of biasing from only one line. The schematic and the optimized layout of this network is given in Fig. 5.19a and Fig. 5.19b.

The aim for the second interstage matching network is boosting the overall gain of the MMIC, hence the source impedance that is shown to the second stage is more significant than the load impedance of the first stage. This source impedance is optimized to achieve the closest match to the conjugate of the transistor's input reflection coefficient to achieve the highest gain possible. Fig. 5.20 gives the results of this matching.



(a) Schematic



(b) Layout

Figure 5.19: Schematic and layout of second interstage matching network.

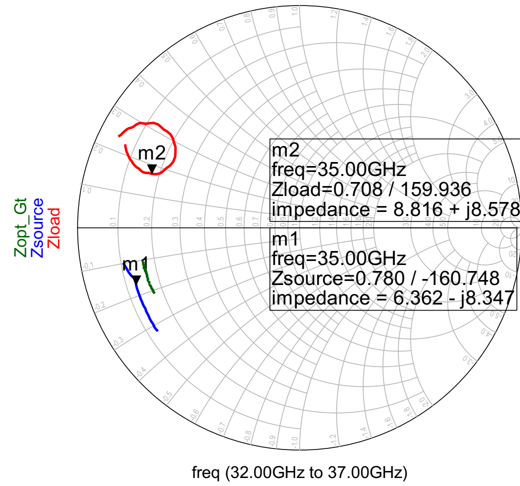


Figure 5.20: Load impedance of first stage transistor (red), the source impedance of second stage transistors (blue), and the optimum impedance for gain (green) from 32 GHz to 37 GHz.

The net insertion loss of the second interstage matching network is shown in Fig. 5.21, together with the first one. As the first interstage matching network is not a cluster, its loss is very small compared to that of the second matching which is also combining two transistors.

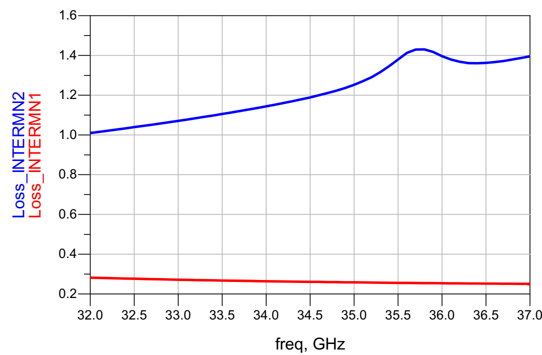
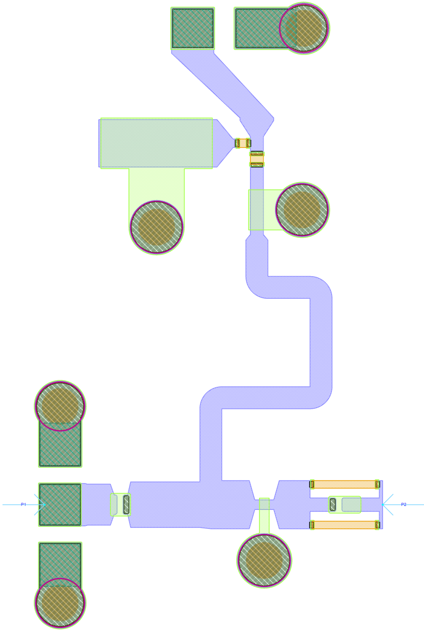


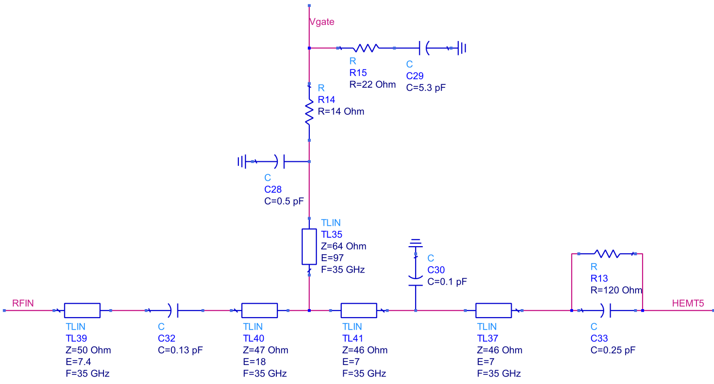
Figure 5.21: Insertion losses of the first (red) and second (blue) interstage matching networks between 32 GHz and 37 GHz.

5.5 Input Matching Network

The input matching network (IMN) of the MMIC is designed considering IRC, hence the gain, i.e., the source impedance of first stage transistor. The conjugate matching is performed to achieve good IRC. The optimized layout and the corresponding schematic of IMN is given in Fig. 5.22a and Fig. 5.22b, respectively.



(a) Layout.



(b) Schematic.

Figure 5.22: Layout and schematic of the second interstage matching network.

The EM simulation of IMN is performed with the given layout, and the source impedances of the first stage transistor from 32 GHz to 37 GHz are seen as in Fig. 5.23. The achieved impedances are very close to the optimum impedances for conjugate matching of the input reflection coefficient of the transistor, which is necessary for high gain.

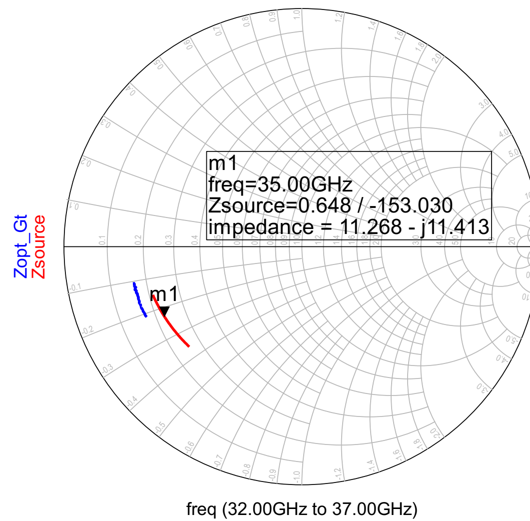


Figure 5.23: Source impedance of first stage transistors (red) and the optimum impedance for gain (blue) from 32 GHz to 37 GHz.

The insertion loss of the designed IMN is given in Fig. 5.24.

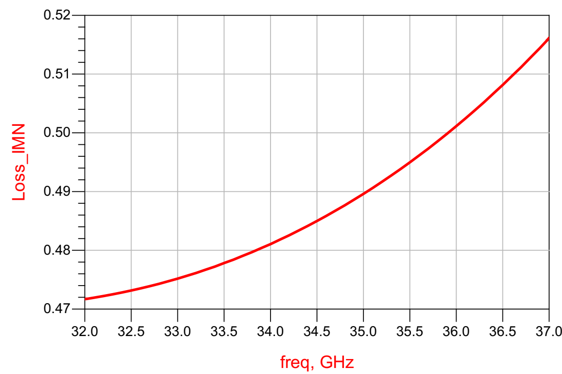


Figure 5.24: Insertion loss of IMN between 32 GHz and 37 GHz.

5.6 Stability Analysis

Stability of power amplifiers need to be ensured before completing the design, since the instability may distort the output signal by the undesired parasitic oscillations. The reason for the instability can be the positive feedback from the output of the active circuit to its input through the intrinsic device elements or the external components [25]. DC bias networks, poorly grounded components, and capacitive or inductive coupling may lead to the instability in power amplifiers [34].

For one-port or two-port networks, the oscillation may start if the magnitude of the reflected signal increases while it is reflected between the termination and the active port. Therefore, the magnitude of the reflection coefficients should not be greater than unity, which leads to the K factor equation, as mentioned in (3.2). Therefore, the even-mode stability of the designed MMIC is taken into consideration, and additional elements are introduced to the matching networks to achieve unconditional stability for the whole measurement band.

Odd-mode stability is another issue for power amplifiers due to the on-chip combining of transistors to achieve the desired power levels. The parallel combinations of transistors may lead to additional modes of oscillation, i.e., odd-mode oscillations [35]. The conditions for odd-mode stability are checked by calculating the input and output impedances and admittances for each transistor, and are provided by adding odd-mode suppression resistors between the gates and drains of the parallel transistors.

5.6.1 Even-Mode Stability

The transistor itself is unconditionally stabilized with an RC network below 1.7 GHz. For the lower frequencies, the losses introduced by the matching networks would support even-mode stability. Therefore, the even-mode stability of the MMIC is analyzed after the design of matching networks by dividing the

MMIC into three parts, as shown in Fig. 5.25.

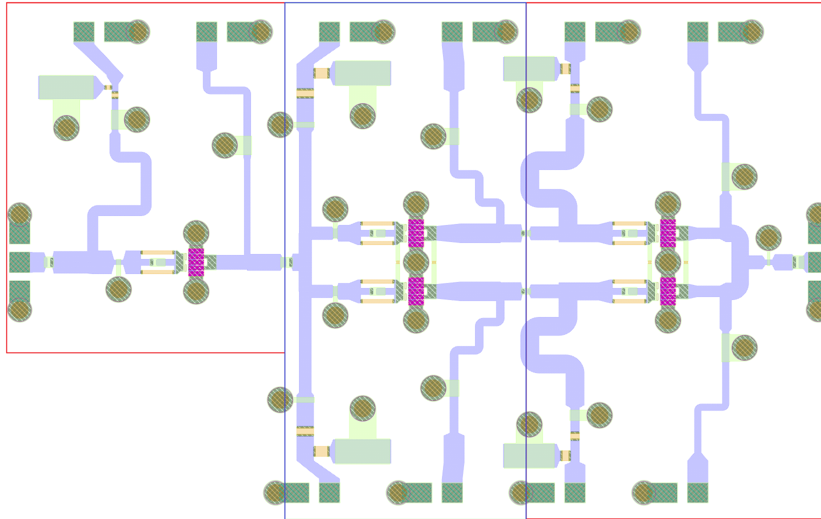


Figure 5.25: Three parts of the layout to analyze even-mode stability for each stage.

With the matching networks, μ and μ' parameters give a better idea than K factor which may give a very large value. After the design of matching networks, these parameters are checked for three parts of MMIC which are simulated separately. As shown in Fig. 5.26, the even-mode stability is not satisfied at lower frequencies for each stage, since μ and/or μ' parameters are below one at low frequencies.

This is due to the negative impedance that is presented to the transistor at low frequencies because of the bias networks' transmission lines and shunt capacitors [36]. A series resistor, as well as a shunt one, at the gate bias line would support the even-mode stability. Since the shunt resistance cannot be used alone because of the negative gate voltage of the transistors, this resistor is followed by a shunt capacitor to the ground. Therefore, series resistors and shunt RC networks are added to the gate bias lines for all three stages. After optimizing the values of these components, the even-mode stability is satisfied for the whole measurement frequencies, as shown in Fig. 5.27. The series resistors at the gate bias networks do not cause a significant voltage drop since the gate leakage current is small.

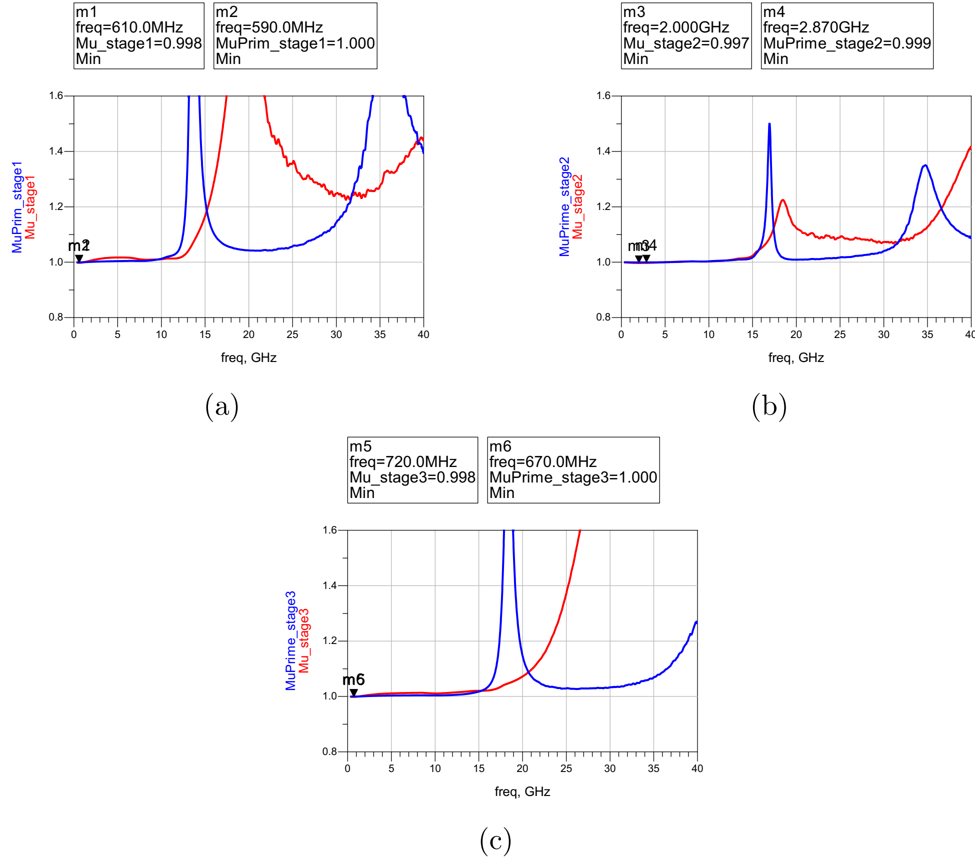


Figure 5.26: Even-mode stability results for three parts of MMIC: μ and μ' parameters for the first stage (a), second stage (b), and third stage (c).

Moreover, these elements do not affect the RF performance of the circuit, since they are positioned after RF grounding capacitors at the bias lines.

The even-mode stability is also checked using the S-probe tool of ADS to calculate inward-looking and outer-looking impedances at the gate and the drain sides of each transistor. In this method, the schematic of MMIC is used as a whole, and an S-probe tool is placed as a series element to observe the impedances. The oscillation conditions at a specific frequency can be given as [37]:

$$\mathrm{Re}(Z, f) < 0 \text{ and } \mathrm{Im}(Z, f) = 0 \tag{5.3}$$

and

$$\partial\, \mathrm{Im}(Z, f)/\partial f > 0. \tag{5.4}$$

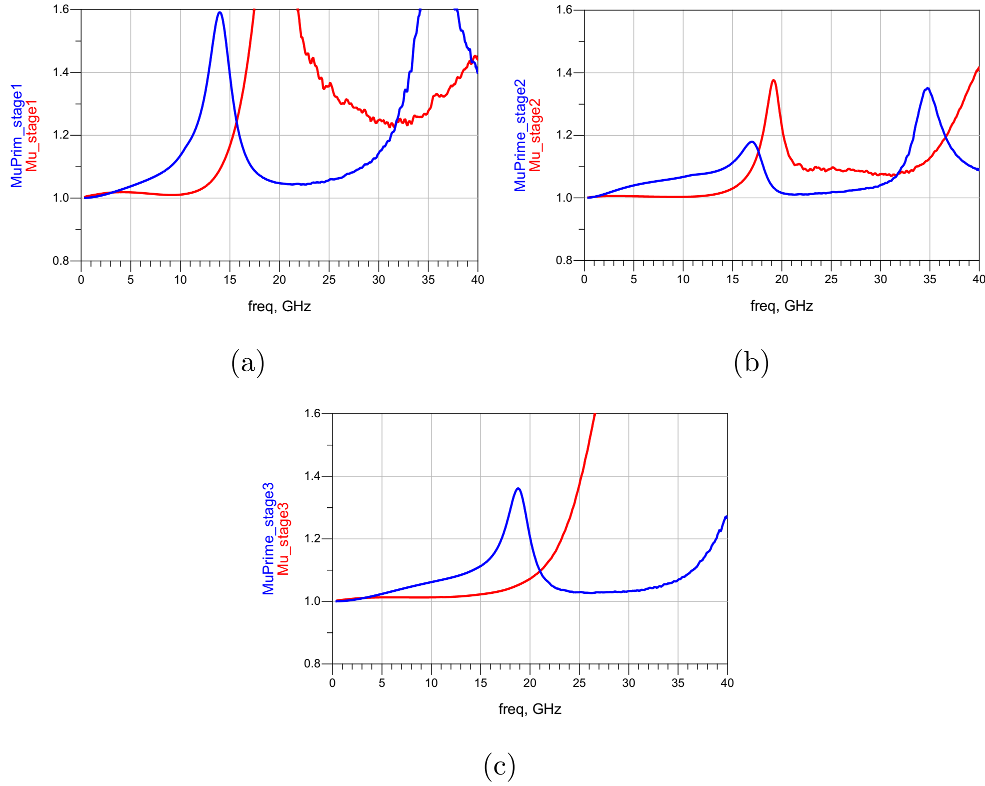


Figure 5.27: Even-mode stability results for three parts of MMIC with additional elements: μ and μ' parameters for the first stage (a), second stage (b), and third stage (c).

If these equations are satisfied for a particular frequency, it is certain to get oscillations. Therefore, the opposite of these conditions is sought for unconditional stability. The basic control method using S-probe is to calculate the real and imaginary parts of the total impedances and admittances seen at gate and drain sides of the transistors. The impedances that are calculated using S-probe at the gate of transistors are shown in Fig. 5.28. If the real part of the sum of $Z1$ and $Z2$ is higher than zero, then the imaginary part is insignificant. However, when the real part becomes negative, the imaginary part should not cross zero to avoid the first oscillation condition.

The total impedances and admittances seen at the gate and drain sides of the transistors for each stage are checked, and the results are given in Fig. 5.29, Fig. 5.30, and Fig. 5.31. The real parts of the sums of the impedances for both

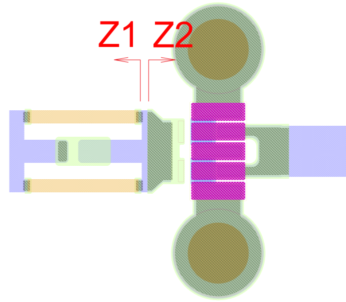


Figure 5.28: The impedances seen using S-probe component at the gate side of first stage transistor.

directions are above zero, meaning that the even-mode stability is satisfied.

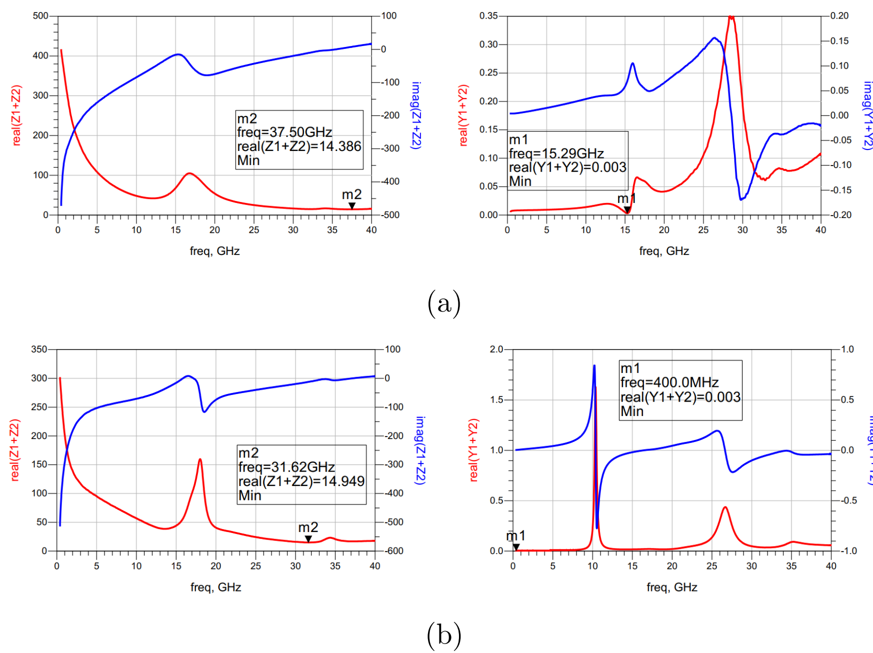


Figure 5.29: Impedance check using S-probe for even-mode stability: The sum of impedance and admittance values seen from S-probe positioned at the gate of first stage transistor (a) and at the drain of first stage transistor (b).

5.6.2 Odd-Mode Stability

Usage of parallel transistors at the output stage or driver stages is a common practice in power amplifier designs to achieve the desired output power levels. Two

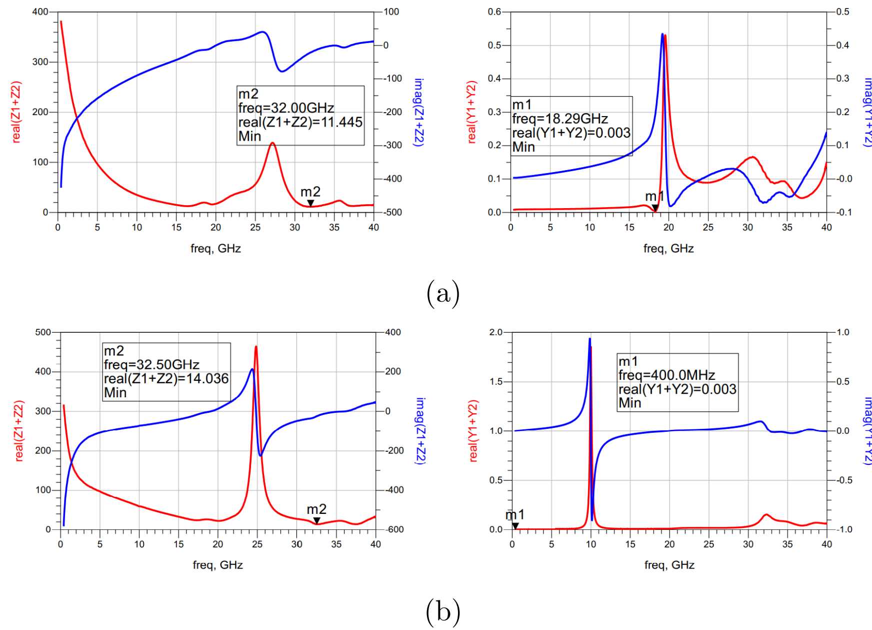


Figure 5.30: Impedance check using S-probe for even-mode stability: The sum of impedance and admittance values seen from S-probe positioned at the gate of second stage transistor (a) and at the drain of second stage transistor (b).

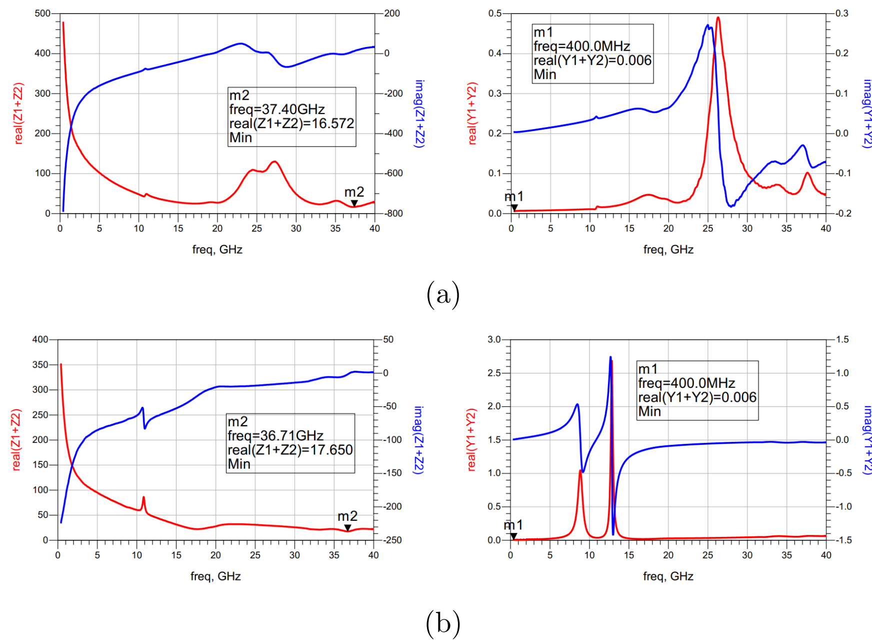


Figure 5.31: Impedance check using S-probe for even-mode stability: The sum of impedance and admittance values seen from S-probe positioned at the gate of third stage transistor (a) and at the drain of third stage transistor (b).

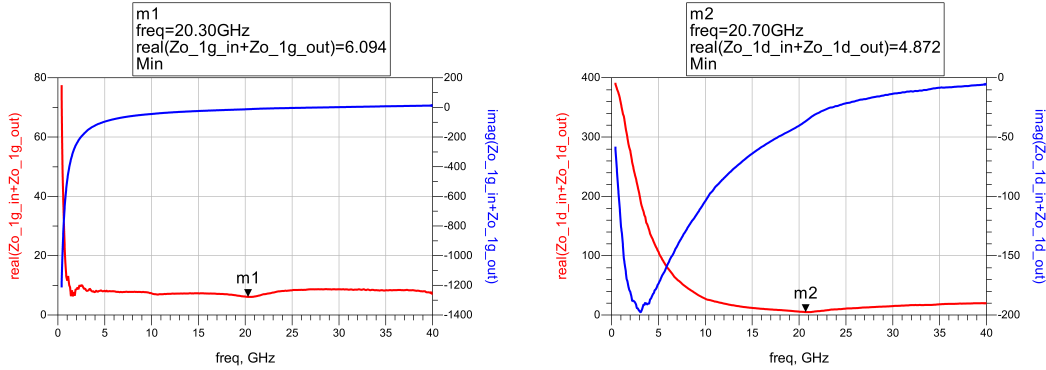
transistors are used in the second and the third stage of the designed MMIC. In the design procedure, it is assumed that these transistors work in even-mode with the same drain currents and identical RF signals in terms of phase and magnitude. However, the transistors are not identical, the matching networks are not completely symmetrical, and RF signals are not in phase. With the parallel transistors and deviating operating conditions, this multi-loop system may result in odd-mode excitations, besides the even-mode operation. The stability factor or S-probe technique cannot consider the odd-mode stability since they are performed for even-mode operation. Therefore, the odd-mode stability should be checked using the appropriate methods, such as the method proposed in [35] and explained in [38] and [33].

The oscillation conditions that are given for even-mode stability in (5.3) and (5.4) should be avoided for the odd-mode stability as well. In this case, the impedances and admittances should be calculated considering the possible odd excitation modes of the circuit. Therefore, the conditions to be avoided for the odd-mode stability, i.e., oscillation conditions, become

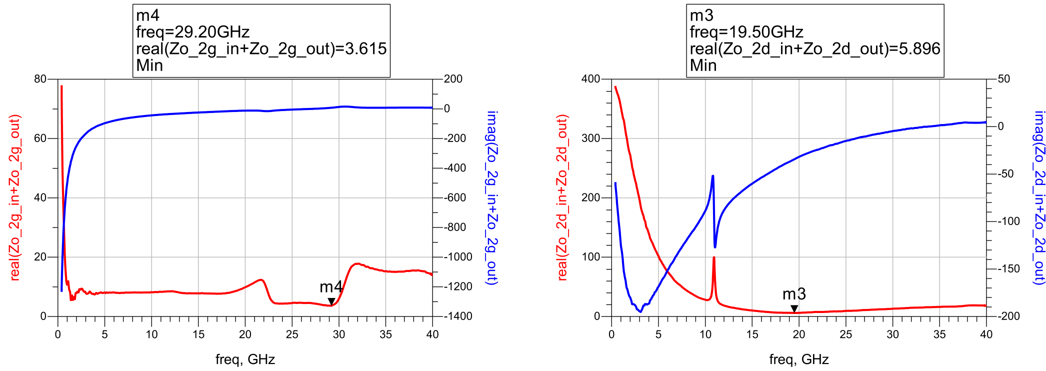
$$\begin{aligned} \mathrm{Re}(Zo,n,in + Zo,n,out) &< 0, \\ \mathrm{Im}(Zo,n,in + Zo,n,out) &= 0, \end{aligned} \tag{5.5}$$

where the input and output impedances are calculated by splitting the circuit into two from the parallel transistors' gate or drain sides (as $Z1$ and $Z2$ in Fig. 5.28).

The designed MMIC has two parallel transistors at the second and third stages, therefore the odd oscillation mode $[+,-]$ is examined for these two stages for gate and drain sides, separately. The odd-mode suppression resistors are added between the gate and drain pads of the transistors, and the values of these resistors are optimized to achieve odd-mode stability for the whole measurement band. The optimized values are $10\,\Omega$ and $5\,\Omega$ for the gate and drain sides of the second stage, respectively, and $12\,\Omega$ and $5\,\Omega$ for the gate and drain sides of the third stage. The sum of impedance values from gate and drain sides of these two stages after odd-mode stabilization are shown in Fig. 5.32, which are above zero for the entire measurement band, providing the odd-mode stability.



(a) At the gate side of the second stage. (b) At the drain side of the second stage.



(c) At the gate side of the third stage. (d) At the drain side of the third stage.

Figure 5.32: Impedance check for odd-mode stability: The sum of impedance values seen from the gate and the drain sides of the parallel second and third stage transistors in odd excitation mode.

5.7 Completed Design

The MMIC design is completed with the stability checks after designing matching circuits. Additional components are introduced to the matching networks to ensure even-mode and odd-mode stability. The EM simulation of the whole layout is performed to see the small-signal performance of the MMIC. The gain, IRC and ORC results are given in Fig. 5.33. The simulated gain is better than 13.7 dB at 35 GHz, while its highest of 15.7 dB is at 33.9 GHz. IRC and ORC of this design are better than −10.6 dB and −13 dB, respectively, at 35 GHz.

This design is optimized for 35 GHz in terms of power and efficiency, while trying the largest possible bandwidth for the small-signal operation. The overall

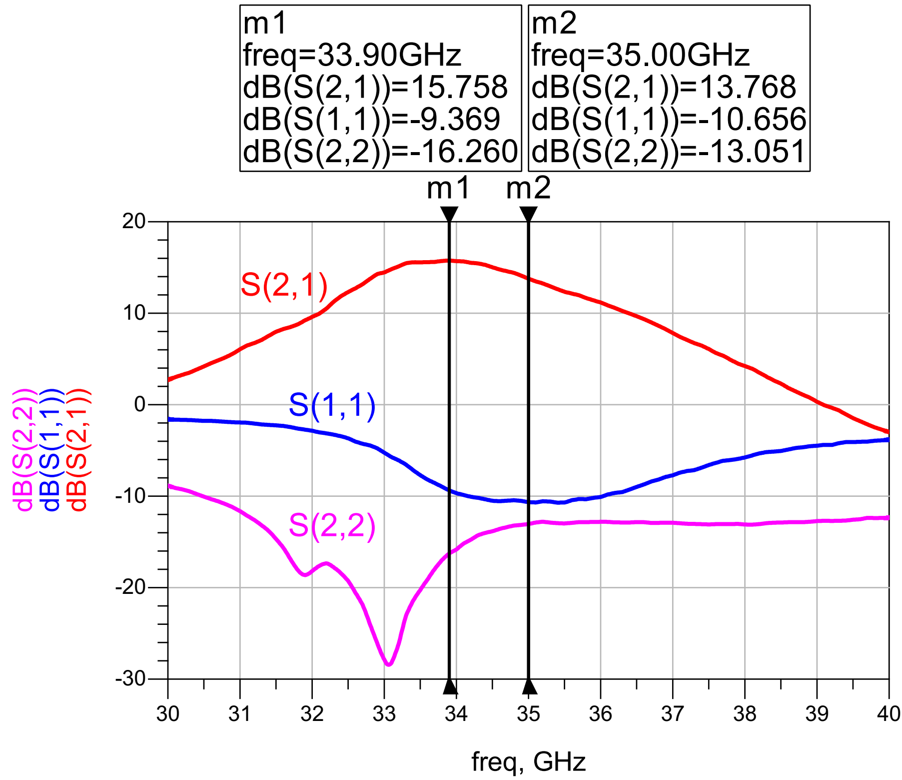


Figure 5.33: Small-signal simulation results of the final layout.

performance of MMIC is decent between 33 GHz and 37 GHz, considering the transistor performance. The impedances that are presented to transistors at 35 GHz are given in Table 5.1, which are suitable for the desired output power and efficiency performance.

Table 5.1: Load and source impedances presented to transistors at 35 GHz.

	Zsource	Zload
First Stage	(11−11i) Ω	(9+9i) Ω
Second Stage	(6−8i) Ω	(7+22i) Ω
Third Stage	(15−1i) Ω	(12+20i) Ω

The layout and the schematic of the completed MMIC are given in Fig. 5.34 and Fig. 5.35. The final size of the designed MMIC is 4 mm × 2.4 mm.

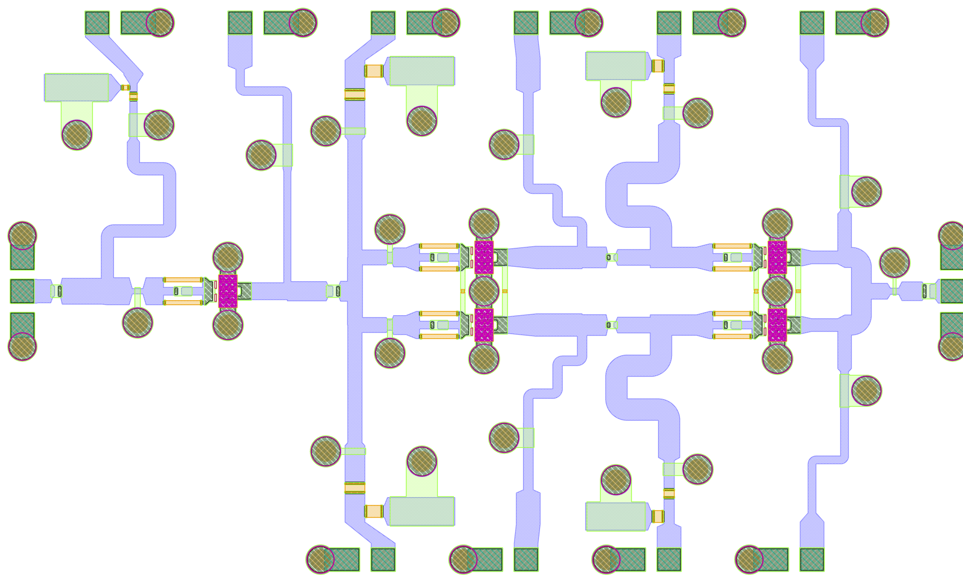


Figure 5.34: Completed layout of the three-stage MMIC, showing the transistors, the matching circuits, and the odd-mode resistors.

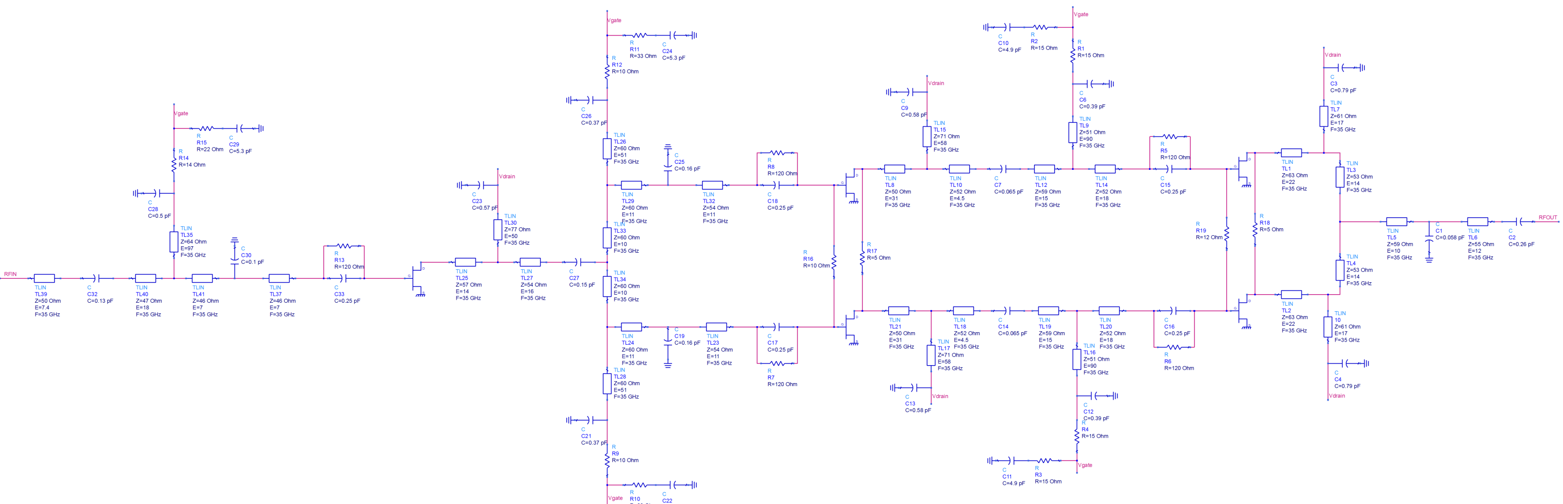


Figure 5.35: Completed schematic of the three-stage MMIC, including odd-mode resistors.

Chapter 6

MMIC Measurement Results

The designed MMIC is fabricated and characterized by performing on-wafer small-signal and large-signal measurements. The microscope image of fabricated MMIC is shown in Fig. 6.1.

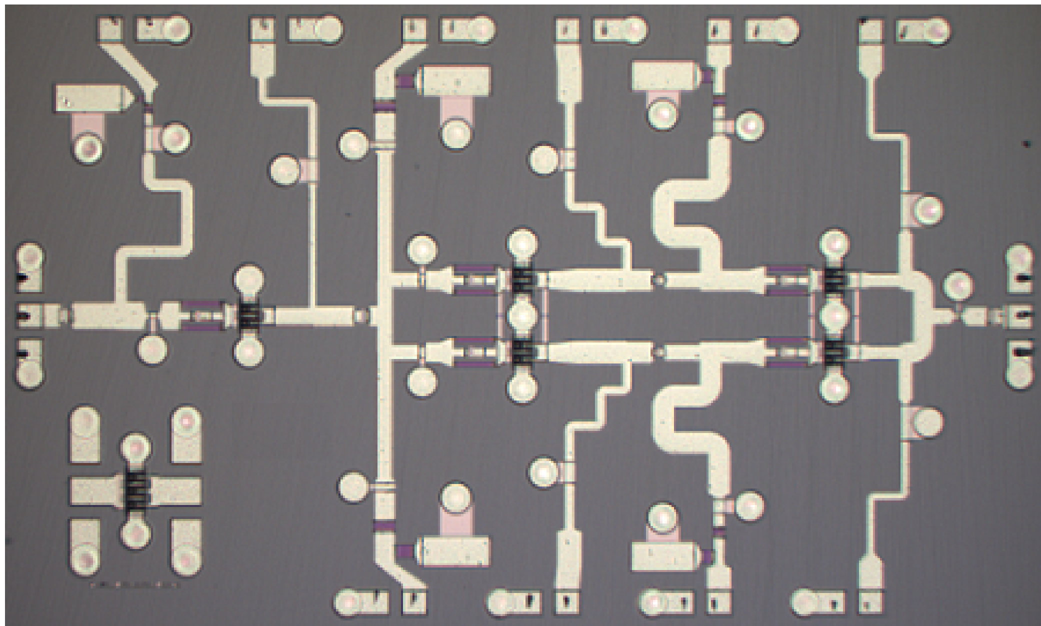


Figure 6.1: Microscope image of the fabricated MMIC.

This design fabricated with two fabrication methods in NANOTAM, first one is the regular process with T-gate. In the second one, mushroom-shaped gate

process, a T-gate structure without a dielectric under its wings, is implemented. As the design is based on the transistor data from the regular process, the measurement results of MMIC are expected to be better with the first fabrication method. The simulation of MMIC is also performed with the new transistor data from the same fabrication with MMIC to compare the simulation results and the measurements.

6.1 Small-Signal Measurements of MMIC

Small-signal measurements are performed under CW operation at room temperature, as explained in Chapter 4, using a network analyzer for the two-port characterization. Customized DC probes are used to supply gate and drain bias voltages. Two-port S-parameter results are obtained with 20 V drain voltage and 100 mA/mm drain current for each transistor.

The measurement results of 10 MMICs from the first fabrication are given in Fig. 6.2 with the simulation of MMIC using the transistor data from the same fabrication. The measurements give the highest gain of 22.3 dB around 33.5 GHz. At 35 GHz, gain performance among 10 MMICs ranges between 18.4 dB and 20.3 dB. Measured IRC and ORC are better than −8.3 dB and −17.2 dB, respectively, at 35 GHz. Measurements are in good agreement with the simulation in terms of IRL, but ORL results do not look the same, which may be because of the variations in the fabrication. Moreover, the simulated gain is lower than the measured gains for the whole frequency band, which may be a cause of sharing via holes between the parallel transistors at the second and third stages in the layout, while the transistors are characterized as separate in the simulations.

Even though the design is aimed for the fabrication with the regular gate process, the designed MMIC is also fabricated using the mushroom-shaped gate process. The measurement results of 6 MMICs from this fabrication are shown in Fig. 6.3. The simulation is also repeated using the transistor data from the same fabrication. Measured gains of MMICs from the second fabrication change

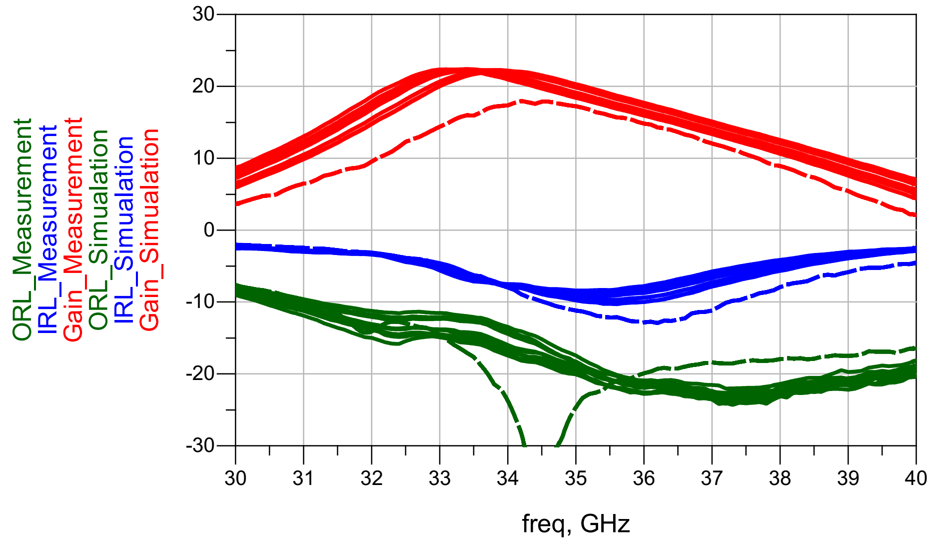


Figure 6.2: Small-signal measurement results of 10 fabricated MMICs from the first fabrication (solid lines), with the simulation results using the transistor data from the same wafer.

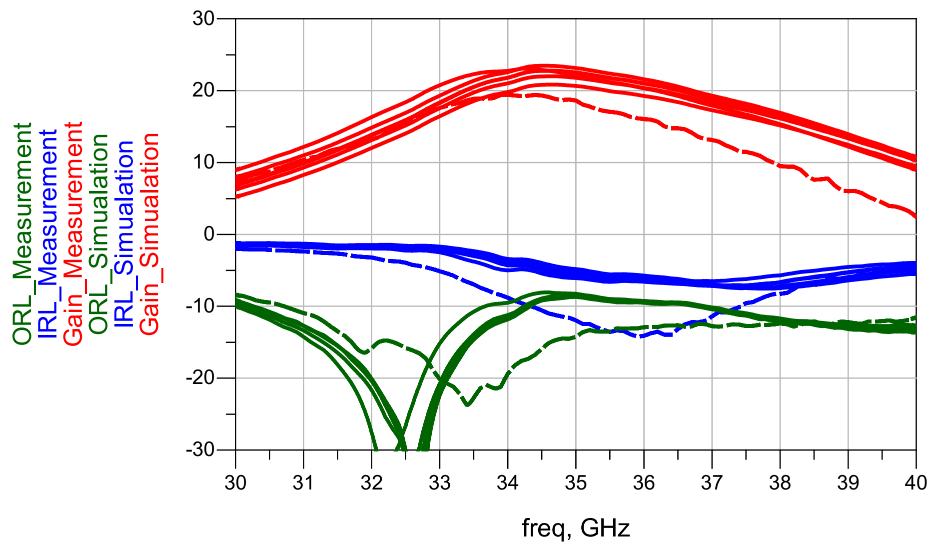


Figure 6.3: Small-signal measurement results of 6 fabricated MMICs from the second fabrication (solid lines), with the simulation results using the transistor data from the same wafer.

from 20.6 dB to 23.1 dB at 35 GHz, while the highest is 23.4 dB at 34.5 GHz. The best performing MMIC has a gain higher than 19.3 dB from 33 GHz to 36 GHz with a variation of ±2 dB. Measured IRC and ORC are better than −4.8 dB and −8.2 dB, respectively, at 35 GHz. For this fabrication, these parameters do not exactly match with the simulation. Also, the measured gain is again higher than the simulated gain, with a smaller difference this time.

6.2 Large-Signal Measurements of MMIC

Large-signal characterizations of MMICs are performed with a pulse width of 33 µs and 30% duty cycle at 35 GHz at room temperature. The vector-based load-pull measurement system, explained in Chapter 4, is used for these measurements. Since the large-signal measurements are from 50 Ω to 50 Ω for MMICs, there is no need for hybrid load-pull setup. The MMIC is fed by pulsers for both gate and drain bias voltages. Thus, the power consumption data is automatically tracked during the measurement. The available input power to MMIC is swept from small-signal region to higher values to observe the output power and efficiency performance. These power sweep measurements are obtained with 20 V drain voltage and 150 mA drain current for the whole MMIC.

The results from the first fabrication are given in Fig. 6.4. This measurement gives an output power of 23.8 dBm at 1 dB gain compression. An output power of 29.2 dBm is achieved at 5 dB compression, with 19.5% of PAE. From the graph, it can be seen that the saturation is not achieved at this compression level. These results are not as expected, since an output power of 31 dBm was expected at 5 dB gain compression. The transistors of this fabrication also show lower output power densities than expected.

The large-signal measurements of MMICs from the second fabrication are also performed, and the best result is shown in Fig. 6.5. At 5 dB compression, 31.9 dBm and 26.5% of PAE are obtained, while having a large-signal gain of 18.8 dB. Moreover, output power at 1 dB gain compression is measured as

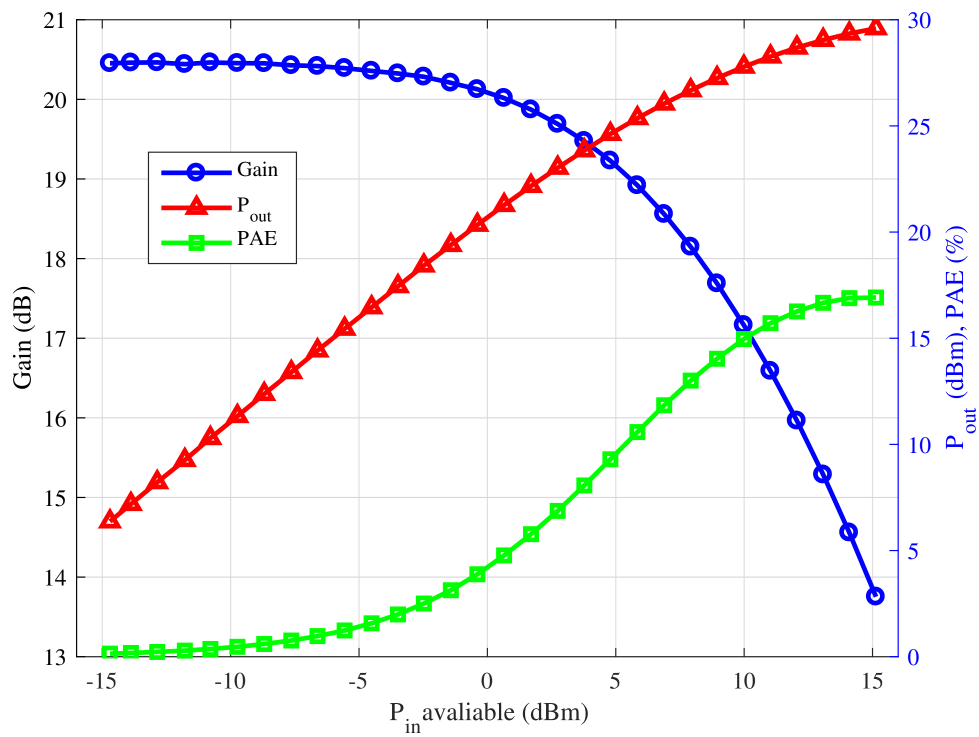


Figure 6.4: Power sweep measurement results of the fabricated MMIC from the first fabrication.

26.5 dBm. Large-signal measurement results of MMIC from the second fabrication satisfies the expectations of the design, which is 31 dBm of output power. Having an output periphery of 0.6 mm, the output power density is 2.6 W/mm for this MMIC. Moreover, achieved PAE of 26.5% is a good result, considering the duty cycle of the measurements.

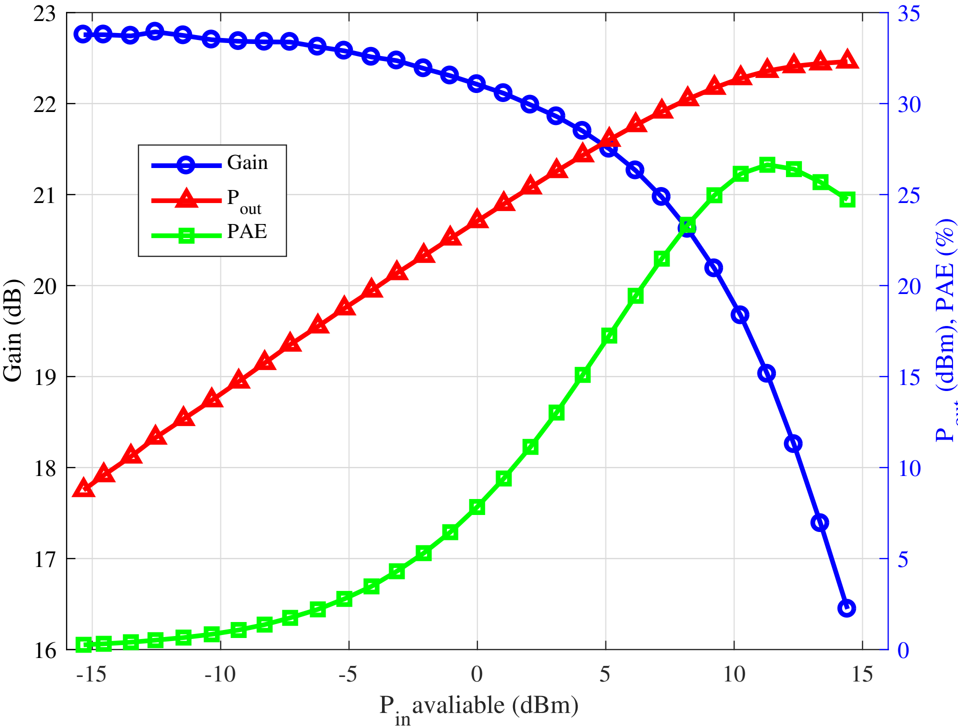


Figure 6.5: Power sweep measurement results of the fabricated MMIC from the second fabrication.

Chapter 7

Discussion and Conclusions

Amplifiers in RF chains are the most essential components to achieve high application standards, as high output power and high efficiency. MMICs are preferable in RF chains for their reliable production, lower cost, and compactness. GaN-on-SiC based HEMTs are promising candidates for high frequency and high power MMIC applications, since the structure shows high power densities and good thermal characteristics. The work on GaN HEMTs for mm-wave frequencies is consistent for the military applications, such as radars at 35 GHz, as well as the commercial usage, especially with the emerging 5G applications around 28 GHz, 37 GHz, and 39 GHz.

Aiming *Ka*-Band applications, an amplifier MMIC is designed and realized using NANOTAM's in-house AlGaN/GaN on SiC technology. This MMIC is optimized especially for 35 GHz for maximum output power and efficiency, while having a bandwidth from 33 GHz to 36 GHz in the small-signal. Three-stage MMIC has a gain higher than 19.3 dB with a variation of ± 2 dB. It exhibits 31.9 dBm output power with a PAE of 26.5% with 5 dB gain compression at 35 GHz under pulsed operation of 30% duty cycle. Having an output periphery of 0.6 mm, the output power density is 2.6 W/mm for this MMIC. Considering the output power density of the single transistor, this value is promising.

Table 7.1 shows the results of several MMICs based on AlGaN/GaN HEMTs at *Ka*-Band frequencies, including this work. The power density of each work is calculated regarding the total gate periphery of the output stages. The realized MMIC of this work exhibits high PAE value of 26.5% with a 20 V supply voltage of 30% duty cycle. This efficiency performance is promising considering the duty cycle of supply voltage, where the MMICs in [11, 12, 15] are measured with a supply voltage of 10% duty cycle and the MMIC in [17] is measured with a supply voltage of 1% duty cycle. The fabricated MMIC also shows a good power density of 2.6 W/mm, which is comparable with the mentioned works aimed for 35 GHz, even though most of these works use higher supply voltages. This work exhibits the capabilities of NANOTAM's AlGaN/GaN on SiC technology for mm-wave frequencies, with reasonable gain, high efficiency, and comparable output power.

Table 7.1: A comparison of designed MMIC with other works at *Ka*-Band.

Ref.	**Year**	**No. of Stages**	**Freq. (GHz)**	**Oper. Cond.**	**Supply Volt. (V)**	**Gain (dB)**	**Max. P_{out} (W)**	**Max. $P_{density}$ (W/mm)**	**Max. PAE (%)**
[10]	2006	2	35	CW	24	12	3.8	3.1	23
[16]	2019	3	31.5	CW	28	26	8	4.3	32
[11]	2016	3	35	10%	24	26	15	3.3	30
[12]	2014	2	30	10%	28	10	20	3.1	16
[15]	2016	2	35	10%	20	17	4.5	2.5	25
[17]	2019	3	30	1%	28	25	5.4	4.5	39.5
This Work	-	3	35	30%	20	23.1	1.5	2.6	26.5

As future works, the transistors' high frequency performance will be improved for mm-wave applications, especially for 5G technology. Though the performance of the transistors primarily depends on the epitaxial structure and the fabrication process, their layouts will also be modified. The optimum T-gate design for high frequency applications will be studied further and will be supported with the device simulations which will be carried on the Atlas module of Silvaco TCAD. The MMIC design will be improved for better matching performances, aiming higher output power and higher gain at 35 GHz.

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