ANALYTICAL MODEL AND DESIGN OF LOAD MODULATED BALANCED AMPLIFIER

A THESIS SUBMITTED TO

THE GRADUATE SCHOOL OF ENGINEERING AND SCIENCE

OF BILKENT UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR

THE DEGREE OF

MASTER OF SCIENCE

IN

ELECTRICAL AND ELECTRONICS ENGINEERING

By

Yunus Erdem Aras

February 2020

Analytical Model and Design of Load Modulated Balanced Amplifier
By Yunus Erdem Aras
February 2020

We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Abdullah Atalar(Advisor)

Ekmel Özbay

Ali Bozbey

Approved for the Graduate School of Engineering and Science:

Ezhan Karaşan
Director of the Graduate School

ABSTRACT

ANALYTICAL MODEL AND DESIGN OF LOAD MODULATED BALANCED AMPLIFIER

Yunus Erdem Aras
M.S. in Electrical and Electronics Engineering
Advisor: Abdullah Atalar
February 2020

RF power amplifiers (PA) with high efficiency and linearity are in high demand for modern communication systems. Modulated signals having a high peak-to-average power ratio (PAPR) require PA's to maintain these features in the output-back-off (OBO) region. Since higher linearity always brings the trade-off in the form of lower efficiency, a PA having both high efficiency and linearity is challenging requirement for RF designers.

Load modulation is one of the promising techniques offering good efficiency-linearity trade-off under OBO conditions for conventional PAs. This work presents an analytical model for the load modulated balanced amplifier (LMBA) using the recently introduced analytical non-linear model of a RF power transistor. We show that it is possible to predict the efficiency and nonlinearity of the LMBA reasonably well using this simple transistor model having only a small number of parameters. To test the performance of the analytical model, we designed an LMBA using three identical discrete RF transistors and 3-dB hybrid couplers. The model parameters of the 5-W GaAs PHEMT are determined from the I-V characteristics and load-pull measurements. LMBA works at 1.7 GHz with a peak output power of 37.5 dBm and with a peak efficiency of 53%. The efficiency is measured to be 47% at 6 dB output-back-off.

Keywords: Load modulation, harmonic model, balanced amplifier, high-efficient power amplifier, back-off efficiency.

ÖZET

YÜK MODÜLASYONLU DENGELİ YÜKSELTEÇLERİN ANALİTİK MODELİ VE TASARIMI

Yunus Erdem Aras
Elektrik-Elektronik Mühendisliği, Yüksek Lisans
Tez Danışmanı: Abdullah Atalar
Şubat 2020

Yüksek verimli ve doğrusallıklı RF güç yükselteçleri modern haberleşme sistemleri için önemli bir ihtiyaç haline gelmiştir. Maksimum güç - ortalama güç oranı yüksek olan modüle sinyaller güç yükselteçinin bu özelliklerini çıkış-gerisi denilen geniş bir aralıkta korumasını gerekli kılmıştır. Ancak, yüksek doğrusallığın düşüş verimlilik getirmesi, hem yüksek verimlilikli hem de yüksek doğrusalıklı güç yükselteçini RF tasarımcıları için oldukça zorlayıcı bir süreç haline getirmiştir.

Yük modülasyonu düşük güç bölgelerinde iyi verimlilik-doğrusallık ödünleşmesi sunan başarılı tekniklerden biridir. Bu çalışmada yakın bir zamanda sunulmuş RF güç transistorlerinin doğrusal-olmayan basit bir modeli kullanılarak yük modülasyonlu dengeli yükselteçler için analitik bir model sunulmuştur. Az sayıda değişkene sahip olan bu transistor modeliyle yük modülasyonlu güç yekselteçinin verimliliğini ve doğrusallığını tahmin edebileceğimizi gösterdik. Analitik modelin performansını test etmek için ayrık transistorler ve 3-dB bağlaçlar kullanarak yük modülasyonlu güç yekselteçi tasarladık. 5-W GaAs PHEMT'in model değişkenlerine I-V eğrileri ve load-pull ölçümleriyle karar verdik. 1.7 GHz bandında maksimum 37.5 dBm çıkış gücünde maksimum %53 verimliliğe sahip olan bir yük modülasyonlu güç yekselteçi elde ettik. 6 dB çıkış gücü gerisinde verimlilik %47 olarak ölçüldü.

Anahtar sözcükler: Yük modülasyonu, harmonik model, dengeli yükselteç, yüksek-verimli güç yükselteçi, düşük güç verimi.

Acknowledgement

I would like to express my sincere gratitude and deep appreciation to my thesis advisor Prof. Abdullah Atalar for his precious support and guidance throughout my M.S. study. His broad vision, deep experience, immense knowledge and endless motivation will always inspire me both in my life and studies. I feel quite fortunate to be a student of him.

I would also like to thank Prof. Ekmel Özbay and Assoc. Prof. Ali Bozbey for reviewing this thesis and being part of the thesis committee.

I would like to thank the members of Prof. Atalar's research group, Engin Estekin and Cem Bülbül, for insightful discussions in our group meetings. They are brilliant minds. It was a joy for me to work and learn together.

I am thankful to my friends/colleagues at Bilkent NANOTAM RF Group, Muhittin Taşcı, Ulaş Özipek, Batuhan Sütbaş and Büşra Çankaya, for their priceless support and help in my early months of RF Engineering.

I would like to thank my fellows at *samedu*, Mahmut Can Soydan, Ömer Arol, Abdulsamet Dağaşan, Bilal Taşdelen, Safa Öztürk, Muzaffer Özbey, Rahmetullah Çağıl and Fatih Konar for their valuable friendship and having a pleasant time together. I am thankful to my teammates from senior year project, Selahaddin Harmankaya, Numan Uyar and Furkan Alan for their continuing friendship and our accomplishments. I would also like to thank my friends at the department, Dilan Öztürk, Büşra Tegin and Ali Alper Özaslan.

I am also thankful to Yeşim Gülseren for her positive attitude and precious motivation. She is full of energy and love. I feel lucky to meet her.

Last but not least, I owe to special thanks and appreciation to my dear family. They always support, motivate and encourage me throughout my life as well as this study. Without their their teachings and efforts, I would not be able to achieve this far.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation

RF power amplifiers (PA) with high efficiency are in high demand for modern communication systems. To conserve the limited battery power, the PA on the mobile phone or the satellite has to operate as efficiently as possible. Even if the available power source is not limited on the system, the efficiency specifications still burden the designers due to the cooling issues. Conventional way to obtain an efficient PA is as simple as biasing the active device to a low quiescent current in order to reduce the conduction angle, but commonly not sufficient for the necessary efficiency enhancement in the modern wireless systems [1].

Developing the complex modulation techniques to achieve higher data rates imposes the further challenging requirements on the RF PA designers since the system efficiency has a strict trade-off between linearity and output power. The designer has to satisfy the system requirements while managing these trade-offs according to the application and the system specifications such as modulated input signal characteristics.

Efficiency-Linearity Trade-Off: In the communication link, the linearity

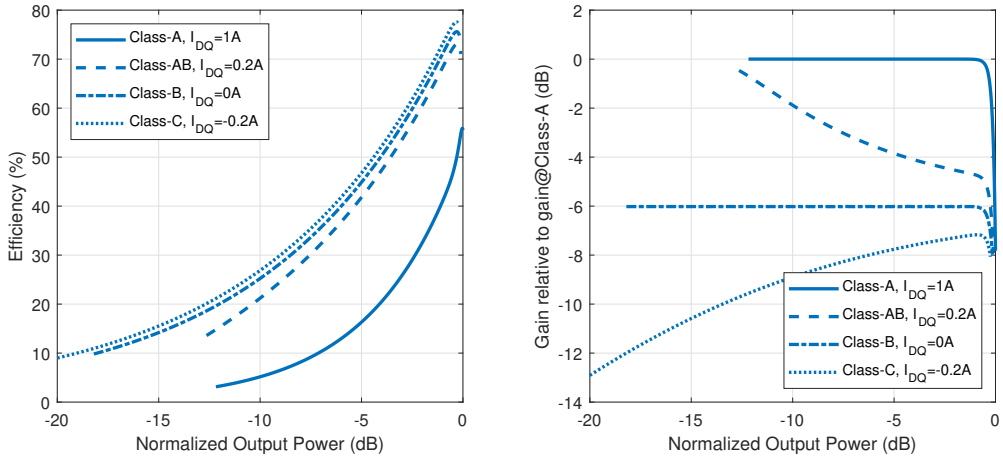


Figure 1.1: Efficiency (left) and the normalized gain (right) versus the normalized output power for the same transistor as biased in different.

of the PAs have a crucial effect to properly radiate the generated data at the transmitter and reconstruct it correctly at the receiver. Therefore, certain linearization techniques including feedforward, cross cancellation and analog/digital predistortion have been utilized for satellite and cellular base station applications [2, 3]. However these techniques mostly result in system complexity and overall efficiency degradation.

Driving the PA with a low input signal also improves the linearity, but this results in a sharp efficiency drop. Fig. 1.1 illustrates the relation between the efficiency and the normalized gain for the same active device with different bias conditions.[1] It is clear to observe the efficiency improves as the quiescent current lowers. However regardless of the bias point, as the input drive power is backed off from P_{Sat} value, the efficiency degrades significantly while the linearity of PA gets better. In order words, the PA tends to operate in high efficiency when it is pushed the saturation where the non-linearity becomes dominant.

Efficiency-Output Power Trade-Off: The conventional PAs are designed so that they achieve maximum efficiency at a single output power level mostly close to the saturation. However modern communication systems demanding high

[1]Note that results are obtained using the simple model to be described in the following chapters.

Table 1.1: Features of digital mobile communication standards.

Gen.	**Standard**	**Interface and Modulation**	**Max. Frequency (GHz)**	**Bandwidth (MHz)**	**Max. PAPR (dB)**
2G	GSM/EDGE	TDMA/FDMA, GMSK, 8PSK	1.9	0.2	3.3
3G	UMTS	W-CDMA, QPSK/64QAM	3	5	10.6
4G	LTE	OFDMA, MIMO 4x4, 64QAM	5.9	20	12
4G	LTE-Advanced	OFDMA/SC-FDMA, MIMO 8x8, CA, 64AQM	5.9	20 (100 with CA)	12
4G	WiMAX	OFDMA, MIMO 2x2, QPSK/64QAM	5.8	20	12
5G	5G	OFDMA, HetNet, massive MIMO, advanced CA, CoMP, ...	40	>100 (800-2000)	>12

data rate transmission results in the modulated signal exhibiting a very large peak-to-average power ratio (PAPR) [4]. Some features of mobile communication standards are summarized in Table 1.1 [5]. Even though certain PAPR reduction schemes including amplitude clipping and filtering, coding and partial transmit sequence have been developed in last several decades [6], a reliable solution to deal with the high PAPR lies on the PA design.

Fig. 1.2 displays the average PAPR of different modulation schemes and the efficiency of a conventional class-AB biased PA over output-back-off (OBO) region. Since the PA has to handle with the peaks of the modulated signal without clipping, the signal with high PAPR tends to stand in the high OBO region where the PA efficiency is quite low. Therefore, back-off efficiency dominates the overall system efficiency in the modern wireless systems.

In this study, we focused the design of an amplifier presenting both good linearity, reasonable high output power and enhanced OBO efficiency under the complex modulated input signals. An analytical model was developed for expressing the characteristics of a transistor and PA with complex architecture. The prototype was designed and fabricated for the verification of the proposed model.

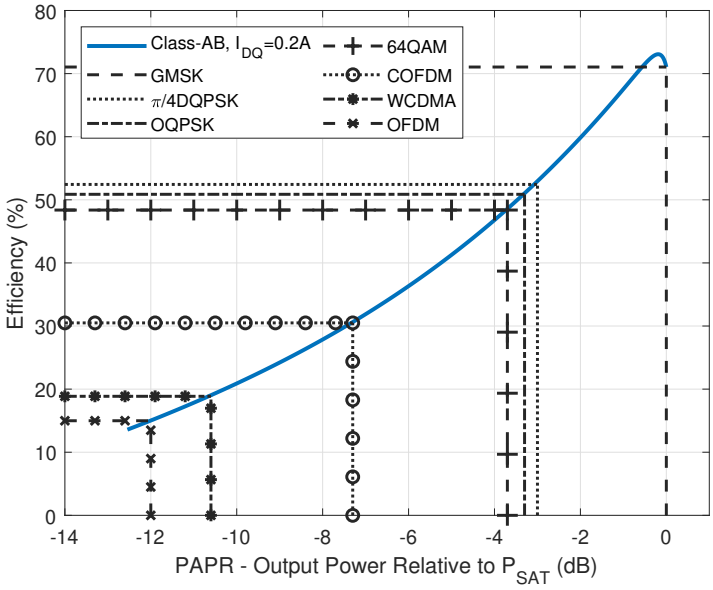


Figure 1.2: PAPR of different modulation techniques. Efficiency versus output power of the class-AB biased PA.

1.2 Efficiency Enhancement Techniques

In conventional PA modes, a high efficiency is obtained by lowering the DC bias point with a resultant sacrifice in gain. Several efficiency enhancement techniques have been studied to obtain useful RF front-ends since the early era of radio communication [1]. Overdriven PAs such as Class-F [7–9] and inverse Class-F [8, 9], switching mode amplifiers including Class-D [10] and Class-E [11] are considered as techniques with fixed supply voltage and output load, where high efficiency is achieved with a high non-linearity.

Beside those, there exist techniques with more complex topology where the load impedance or the supply voltage or both are adjusted according to input signal power, called load and supply modulation, in order to achive both linearity and OBO efficiency, as displayed in Fig. 1.3. The Envelope Elimination and Restoration (EER) [12] and the Envelope Tracking (ET) [13,14] are the techniques using supply modulation. Two classical techniques fall into the family of load modulation; the Doherty Amplifier [15–17] and the Outphasing Amplifier [18–20].

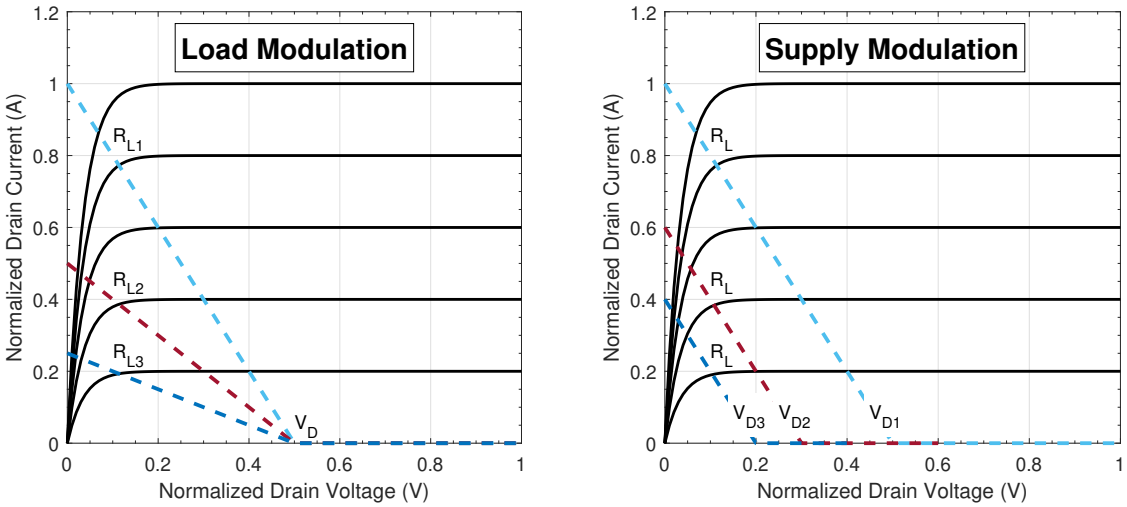


Figure 1.3: Dynamic load-lines for load and supply modulation.

A load-modulated-balanced-amplifier (LMBA) was recently introduced by Cripps as a new type of load modulation technique [21], which was also chosen as the design architecture in this thesis.

1.3 Thesis Outline

In Chapter 2, the theory of LMBA is briefly explained and the other studies done up to now are summarized. A variation of this topology is demonstrated.

Chapter 3 explains the details of the analytical model. First, a single transistor behaviour is expressed using simple polynomials by approximation of the drain current. Using linear equations of the passive components, the model is expanded to express more complex topologies like LMBA.

Chapter 4 presents the design steps of the LMBA and the measurement setups used for transistor characterization. After DC and RF characterization of a packaged transistor, each component required for LMBA is designed. The techniques used in design steps of single amplifier are given.

In Chapter 5, the fabricated components and the designed LMBA are presented. Measurements for the verification of the model simulation are demonstrated with the required measurement setups. The measured and simulated results are compared for each component and the designed LMBA.

Chapter 6 presents the conclusion of the thesis with the summary of the work done and the future directions.

Chapter 2

Load Modulated Balanced Amplifier

In this chapter, recently proposed theory of LMBA will be summarized. Load modulation mechanism and the way how LMBA improves OBO efficiency will be analytically explained. Finally, available examples in the literature will be presented.

2.1 Load Modulation

The load-modulated-balanced-amplifier (LMBA) was introduced using a classical balanced amplifier (BA) [22] with an additional control amplifier (CPA) to modulate the load impedance seen from balanced pairs as input power varies [21]. Fig. 2.1 displays the first proposed LMBA architecture.

As demonstrated in [21], the operation on the output coupler can be explained by using 4-port Z-parameters of 3 dB coupler and the port currents in each branch. As shown in Fig. 2.2, the balanced pairs are represented by the equal amplitude quadrature signals (bI_P and $-jbI_P$) while the output of the CPA can

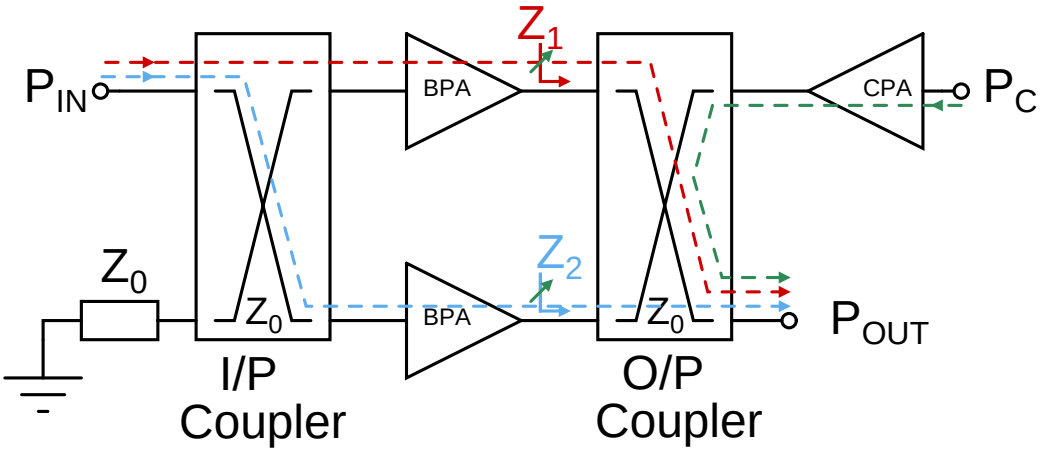


Figure 2.1: Simplified block diagram of LMBA.

be represented by cI_P where b and c are the current drive levels and I_P is the maximum drain current of balanced amplifiers. Since the fourth port is already terminated with Z_0, the output current can be written as $V_4 = -Z_0 I_4$.

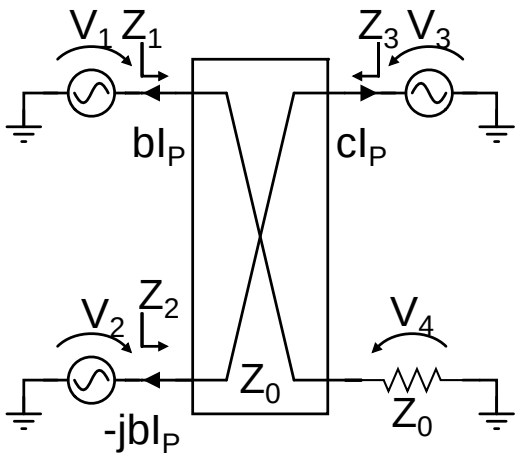


Figure 2.2: Port impedances and currents on the output coupler of the LMBA.

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = Z_0 \begin{bmatrix} 0 & j & -j\sqrt{2} & 0 \\ j & 0 & 0 & -j\sqrt{2} \\ -j\sqrt{2} & 0 & 0 & j \\ 0 & -j\sqrt{2} & j & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} \tag{2.1}$$

Using the equation (2.1) and the current relations above, the impedances seen by

balanced pairs can be found as

$$\begin{aligned} Z_1 &= Z_0\left(1+\frac{\sqrt{2}c}{b}\right) \\ Z_2 &= Z_0\left(1+\frac{\sqrt{2}c}{b}\right) \end{aligned} \tag{2.2}$$

When c is considered as complex number, Eq. 2.2 reveals important property of LMBA, which is the impedances seen by the balanced pairs are modulated by amplitude and phase of the control signal and balanced pairs are terminated at the impedance with the same amplitude and phase. As seen in Fig. 2.3, a significant portion of the Smith Chart can be obtained by this technique.

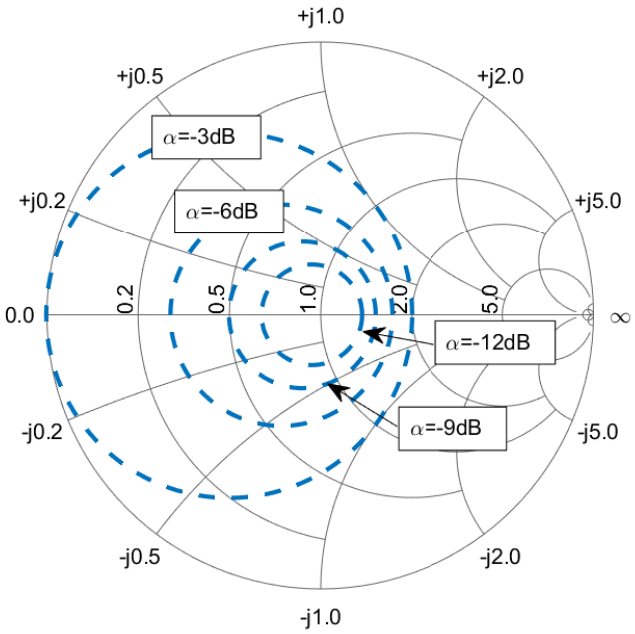


Figure 2.3: Simulation of load modulation for different ratios and phases, where α is the current ratio c/b.

When the output current I_4 is expressed in terms of I_1, I_2 and I_3, it is seen that CPA power always appears at the output. Hence, the total output power can be written as

$$\begin{aligned} P_{out} &= P_1 + P_2 + P_3 = 2P_{Bal} + P_{Cont} \\ &= \frac{1}{2} I_P^2 Z_0 \left| c + \sqrt{2} b \right|^2 \end{aligned} \tag{2.3}$$

whre Z_0 is a real number.

2.2 Back-Off Efficiency Enhancement

To achieve a high efficiency in the back-off region, the BPAs are biased in Class-B whereas the CPA starts to operate after the certain drive level, β. Thus this behaviour can be achieved by biasing it in Class-C where CPA is OFF when $0 \leq b \leq \beta$ and it is ON when $\beta \leq b \leq 1$.

It is assumed that the BPA is achieved maximum non-clipped drain voltage swing, namely maximum efficiency at $b = \beta$, $V_M = \beta Z_0 I_P$. This also results that the BPA should be terminated with $Z_0 = Z_{opt}/\beta$ where Z_{opt} is the optimal load for maximum output power of the BPA.

As the input drive keeps increasing, the drain voltage should stay constant to maintain high efficiency. The continuous drain voltage results the following identity

$$\beta Z_0 I_P = Z_0 \left(1 + \frac{\sqrt{2}c}{b}\right) b I_P = (b + \sqrt{2}c) Z_0 I_P \tag{2.4}$$

which reveals the CPA drive level condition as

$$c = \begin{cases} 0, & 0 \leq b \leq \beta \\ \frac{1}{\sqrt{2}}(\beta - b), & \beta \leq b \leq 1 \end{cases} \tag{2.5}$$

Combining Eqs. 2.3 and 2.5 results in the output power for two drive regions

$$P_{out} = \begin{cases} b^2 Z_0 I_P^2, & 0 \leq b \leq \beta \\ \frac{1}{4}(\beta + b)^2 Z_0 I_P^2, & \beta \leq b \leq 1 \end{cases} \tag{2.6}$$

When the ideal conditions in class-B biased amplifiers are considered, the total power consumption of LMBA can be written as a summation of the power

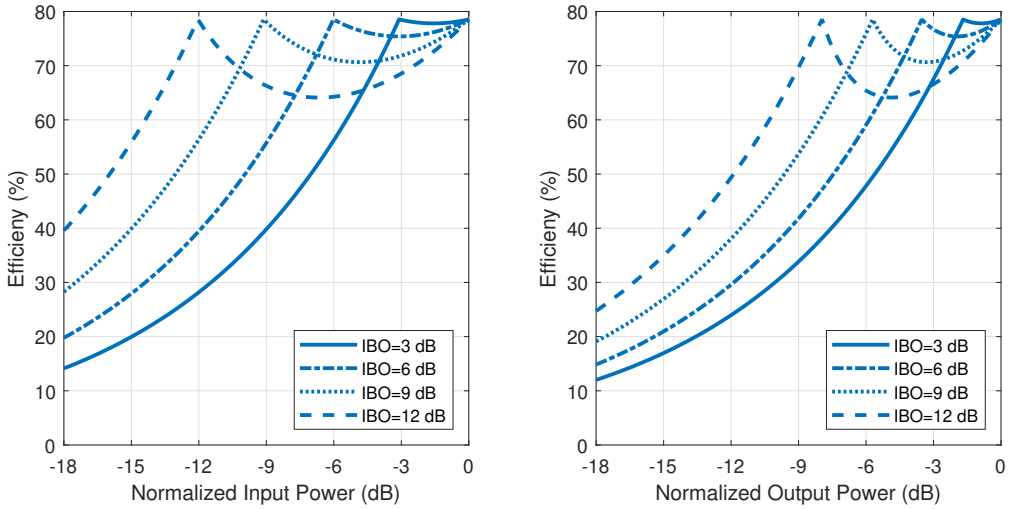


Figure 2.4: Drain efficiency versus normalized input power (left) and normalized output power (right) for different input back-off levels, β's.

consumption of each devices, $P_{DC} = 2P_{Bal_{DC}} + P_{Cont_{DC}}$,

$$P_{DC} = \begin{cases} \frac{4Z_0 I_P^2 \beta b}{\pi}, & 0 \leq b \leq \beta \\ \frac{4Z_0 I_P^2 \beta b}{\pi} + \frac{Z_0 I_P^2 |\beta - b||\beta - 1|}{\pi}, & \beta \leq b \leq 1 \end{cases} \tag{2.7}$$

Using Eqns. 2.6 and 2.7, one can calculate the drain efficiency. For different β values, the drain efficiency is plotted in Fig. 2.4 where inherent non-linearity of LMBA is observed.

2.3 Literature Review

The first LMBA was demonstrated in 2016 as a load modulation and OBO efficiency enhancement technique with a proof-of-concept prototype, which verifies the efficiency improvement by adjusting the power and the phase of the control signal [21]. Then the detailed theory of operation were demonstrated with the design steps where they achieved wide bandwidth, high OBO efficiency and linearity by a proper control signal [23, 24]. The first MMIC application was also reported as a reconfigurable high-efficiency X-band PA [25].

As a variation, a single/RF-input LMBA was proposed, where the separate supply for the control signal is eliminated [26,27]. In this architecture, modulated input signal is properly divided and delayed so that the control signal is directly synthesized from the input signal. The detailed design theory of RF-input LMBA including the transistor sizing and the control signal characteristics was explained in [28].

Finally, the architecture consisting of both supply and load modulation was demonstrated [29]. Using RF-input LMBA architecture, they achieved further OBO efficiency enhancement by properly modulating the supply voltage of the balanced pair in the LMBA, called supply- and load- modulated balanced amplifier.

Chapter 3

Analytical Model

In this section, analytical model will be developed starting from a single transistor to the complex balanced topology. Basically, the analysis depends on the simplistic approximation of drain current by means of polynomials. I-V characteristics of PA, output power and efficiency will be predicted by using this analytical model.

3.1 Stand-Alone Amplifier

Fig. 3.1 displays the schematic of the power amplifier excited with a sinusoidal voltage, where input matching is ignored. C_p and L_p represent the parasitics of the transistor and MN can be considered as an impedance transformation network where all other harmonics are shorted.

Following the method of [30], we define the knee profile with the function $k(.)$ and the baseline current waveform with the function $A(.)$. Then, the idealized drain current can be expressed as multiplication of two polynomial functions

$$i_D(\theta) = k(v_{ds})A(\theta) \tag{3.1}$$

where v_{ds} is the normalized drain-to-source voltage and since $A(.)$ represents the

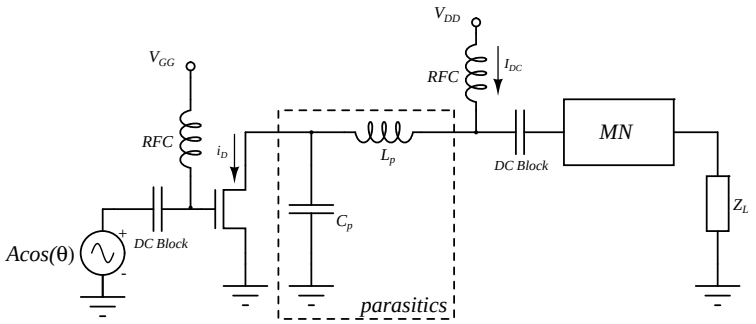


Figure 3.1: Schematic of the stand-alone amplifier showing the parasitics of the transistor.

baseline current, it is a periodic function of angle of θ as the applied input signal. Assuming all harmonics are shorted, v_{ds} can be written as

$$v_{ds} = 1 - (\overline{V}\cos(\theta + \gamma)) \tag{3.2}$$

where $\overline{V}$ is the normalized peak drain voltage given by $\overline{V} = V/V_{DD}$ and γ is the phase shift between the input and output voltages. Then, the knee profile function $k(.)$ can be expressed as,

$$\begin{aligned} k(v_{ds}) &= 1 - (1 - v_{ds})^N \\ &= 1 - (\overline{V}\cos(\theta + \gamma))^N \end{aligned} \tag{3.3}$$

where N is an even number showing the degree of the knee profile approximation. Fig. 3.2 displays the knee profile defined in Eq. 3.3 for different N values. As it is seen in the plot, while smaller values of N=4 to 8 can be considered as good approximation of a typical GaN devices, larger N values, represent GaAs devices. As N gets very large, the knee profile function approaches to that of the ideal transistor.

With a transistor bias current of I_{DQ} and a peak AC current of I_P, the baseline function, $A(\theta)$, can be written as,

$$A(\theta) = \begin{cases} I_{DQ} + I_P\cos(\theta) & \text{if } I_{DQ} > -I_P\cos(\theta) \\ 0 & \text{otherwise} \end{cases} \tag{3.4}$$

When a non-zero baseline function is applied, the intrinsic drain current can be

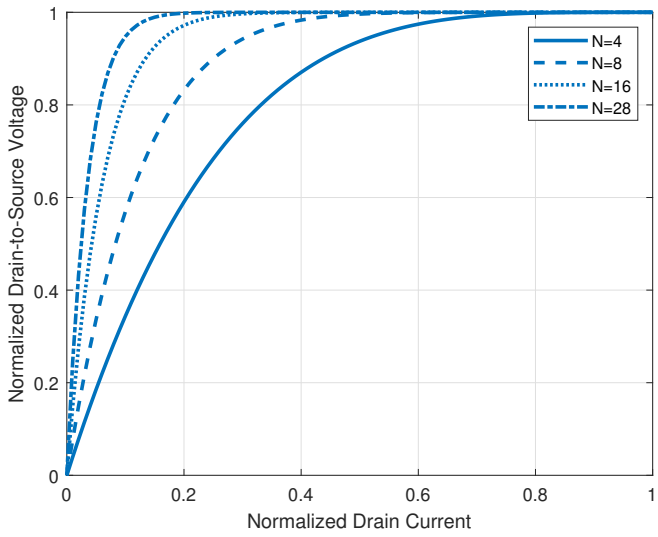


Figure 3.2: Knee profile $k(.)$ versus normalized drain-to-source voltage v_{ds} for different N values.

written as

$$\begin{aligned} i_D(\theta) &= k(v_{ds})A(\theta) \\ &= [1 - (\overline{V}\cos(\theta+\gamma))^N][I_{DQ} + I_P\cos(\theta)] \end{aligned} \tag{3.5}$$

Samples of the normalized drain current in two different cases are given in Fig. 3.3. The baseline current is chosen so that transistor is biased in class-B mode, thus $I_{DQ} = 0$.

Both periodic functions given in Eqns. 3.3 and 3.4 can be expanded as series,

$$\begin{aligned} k(v_{ds}) &= k_0 + \sum_{n=1}^{N/2}[k_{2n,R}\cos(2n\theta) + k_{2n,Q}\cos(2n\theta)] \\ A(\theta) &= A_0 + \sum_{n=1}^{\infty} A_n\cos(n\theta) \end{aligned} \tag{3.6}$$

Multiplying the two series with each other to find the DC and the fundamental components, DC current I_{DC} and the phasor at the fundamental frequency, $\boldsymbol{I}$, of drain current i_D can be obtained. The exact expressions of k_j's, A_j's and $\boldsymbol{I}$ are given in Appendix A. Thus both I_{DC} and $\boldsymbol{I}$ can be written as nonlinear functions of four variables as

$$I_{DC} = f_1(I_{DQ}, \boldsymbol{I_P}, N, \overline{\boldsymbol{V}}) \tag{3.7}$$

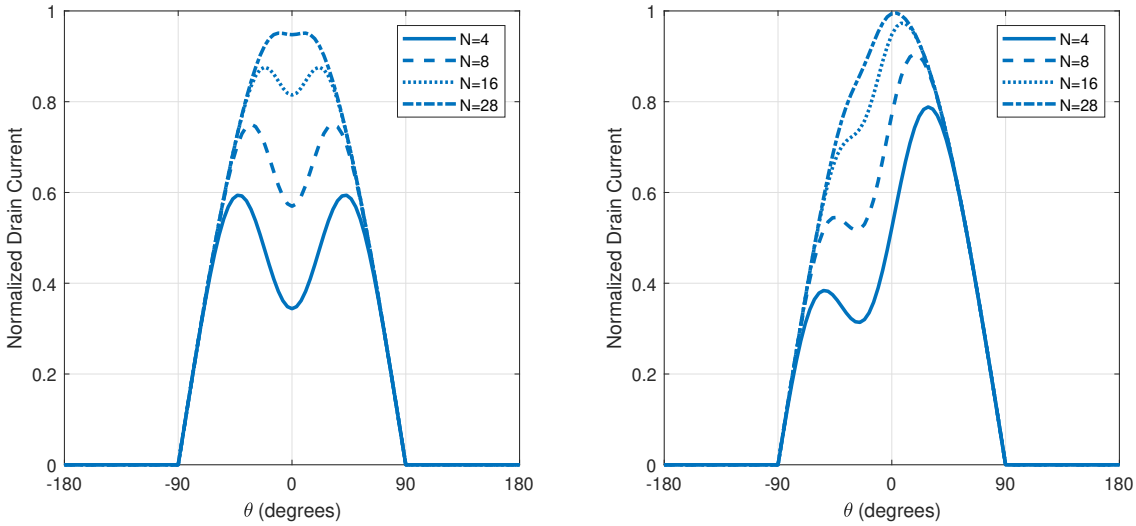


Figure 3.3: Normalized drain current for different N values. Transistor is biased in class-B, $I_P = 1$ and $I_{DQ} = 0$. $\overline{V} = 0.9$ and $\gamma = 0$ (left), $\gamma = \pi/8$ (right).

$$\boldsymbol{I} = f_2(I_{DQ}, \boldsymbol{I_P}, N, \overline{\boldsymbol{V}}) \tag{3.8}$$

where $\overline{\boldsymbol{V}}$ is the normalized voltage phasor. If the load impedance at the fundamental frequency is Z_L, we also have

$$\overline{\boldsymbol{V}} = -\frac{Z_L \boldsymbol{I}}{V_{DD}} = -\frac{Z_L f_2(I_{DQ}, \boldsymbol{I_P}, N, \overline{\boldsymbol{V}})}{V_{DD}} \tag{3.9}$$

With the given I_{DQ}, $\boldsymbol{I_P}$ and N, one can solve the nonlinear equation for $\overline{\boldsymbol{V}}$ numerically. Once $\overline{\boldsymbol{V}}$ is found, the output power and the efficiency can be easily found as

$$\begin{aligned} P_{out} &= -\frac{V_{DD}}{2} \mathcal{R}e\{\overline{\boldsymbol{V}} \boldsymbol{I}^*\} \\ \eta &= \frac{P_{out}}{V_{DD} I_{DC}} \end{aligned} \tag{3.10}$$

As Z_L is swept on the Smith chart, the output power and efficiency can be found for each Z_L value to obtain load-pull contours. Varying $\boldsymbol{I_P}$ for a fixed Z_L, the gain compression, linearity and back-off efficiency can be determined. Different bias conditions can be also analyzed by changing I_{DQ}.

The main algorithm of the program developed in MATLAB is given in Appendix B. As an example, load-pull contours and the saturation characteristics of

a transistor biased in class-B are shown in Fig. 3.4. First, the efficiency and the output power are recorded for varying the load impedance Z_L. Using MATLAB's *contour* command, the efficiency and the output power contours are obtained for corresponding load impedance and plotted. The maximum output power and maximum efficiency are achieved at different load values. Then, the load impedance is set the value first at maximum efficiency and then the maximum power, $Z_L = 31.4\ \Omega$ and $Z_L = 18.6\ \Omega$, respectively. The efficiency, the output power and the gain compression are recorded for varying the input drive level, I_P. Since low N value is chosen in model, early-slow compression behaviour is observed as it is the case with GaN devices.

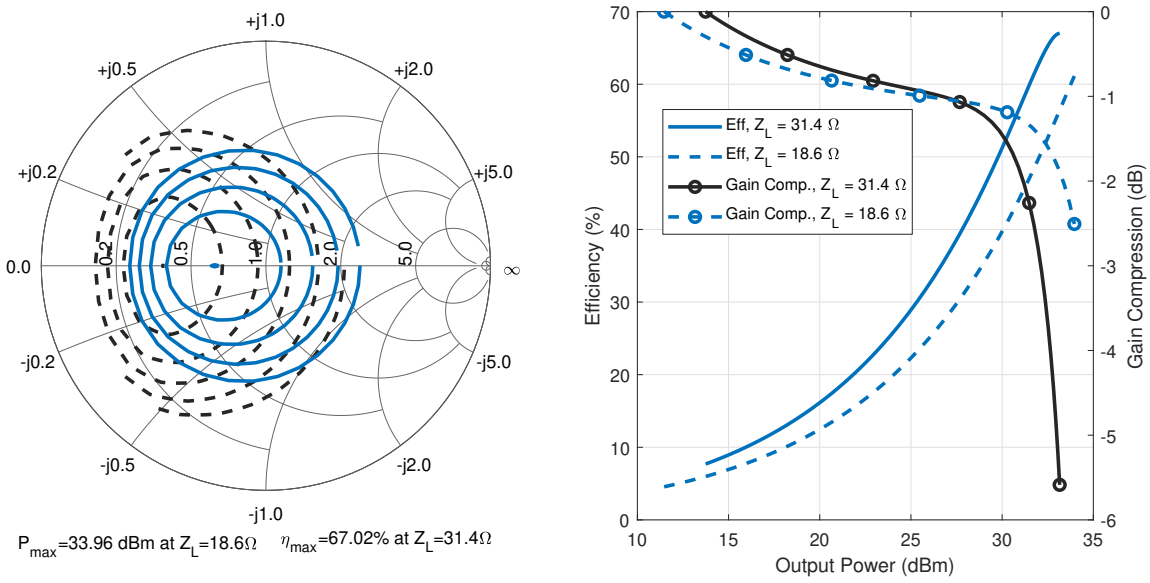


Figure 3.4: Single transistor behaviour with model parameters $N = 6$, $V_{DD} = 12$ and $I_{DQ} = 0$. Load-pull contours when $I_P = 1.2$ and varying Z_L (left), Efficiency and gain compression versus output power when $Z_L = 31.4\ \Omega$ and $Z_L = 18.6\ \Omega$ for sweeping I_P from 1.2 to -25 dB back-off (right).

The transistor parasitics affects only the impedance seen from intrinsic drain node of the transistor. Therefore, they are easily considered by rotating the contours on the Smith chart by taking the normalized impedance or admittance of L_p and C_p.

3.2 Load Modulated Balanced Amplifier

Fig. 3.5 depicts the block-diagram of LMBA [28] consisting of a balanced amplifier and a control amplifier in single *RF-input* configuration. The balanced amplifier is built using two identical amplifiers and two hybrid couplers. An unequal Wilkinson power divider provides part of the input signal to the control amplifier whose output feeds the normally terminated port of the output hybrid divider. The output load impedance of Class-AB balanced pairs are chosen to operate efficiently at a back-off level, while the output matching of Class-C control amplifier is designed to achieve a good efficiency at the saturation level.

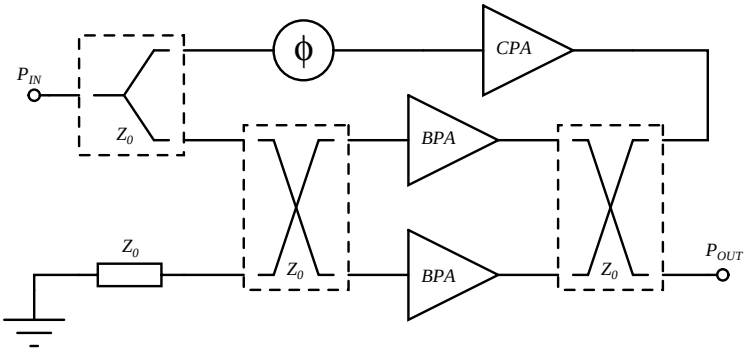


Figure 3.5: Block diagram of single RF-input LMBA.

The parasitic capacitance and inductance, C_p, L_p, of the RF transistors become a part of the π-type output matching network, when combined with external inductance and capacitance, L_m and C_m.

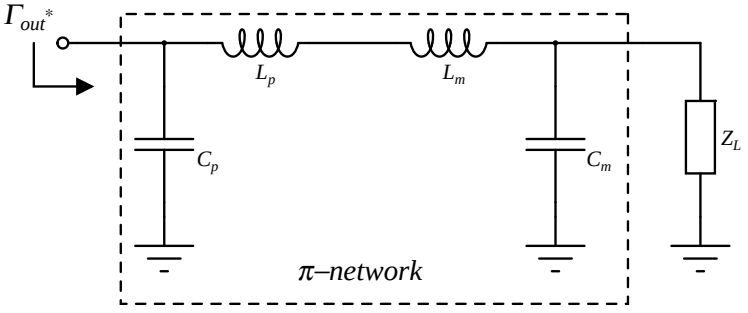


Figure 3.6: π-type matching network between the intrinsic drain of the transistor and the load.

Y-parameters of overall π-type output matching networks of balanced amplifiers and control amplifier are written as

$$Y_{bpa} = \begin{bmatrix} j(\frac{-1}{X_{m_{bpa}}+X_p} + B_p) & j\frac{1}{X_{m_{bpa}}+X_p} \\ j\frac{1}{X_{m_{bpa}}+X_p} & j(\frac{-1}{X_{m_{bpa}}+X_p} + B_{m_{bpa}}) \end{bmatrix} \frac{1}{Z_0}$$
$$Y_{cpa} = \begin{bmatrix} j(\frac{-1}{X_{m_{cpa}}+X_p} + B_p) & j\frac{1}{X_{m_{cpa}}+X_p} \\ j\frac{1}{X_{m_{cpa}}+X_p} & j(\frac{-1}{X_{m_{cpa}}+X_p} + B_{m_{cpa}}) \end{bmatrix} \frac{1}{Z_0} \quad (3.11)$$

where X_p, $X_{m_{bpa}}$ and $X_{m_{cpa}}$ are the normalized impedance of series inductors, $\frac{\omega L}{Z_0}$ and B_p, $B_{m_{bpa}}$ and $B_{m_{cpa}}$ are the normalized admittance of shunt capacitors, $\omega C Z_0$. As displayed in Fig. 3.7, the linear part of the circuit consisting of hybrid-coupler terminated with three matching networks at three ports can be modeled as a 4-port network with a 4×4 $[Y_{n_{ij}}]$ matrix.

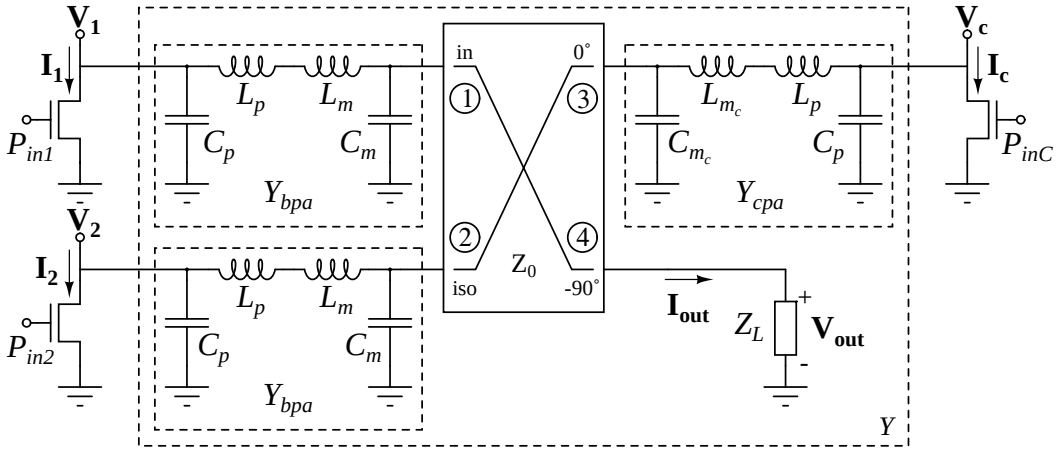


Figure 3.7: The model of output side of LMBA at fundamental frequency.

When its fourth port is terminated with load impedance Z_L, the linear circuit can be expressed as a new 3-port network with a 3×3 $[Y_{ij}]$.

$$Y = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \quad (3.12)$$

where $Y_{i,j} = Y_{n_{i,j}} - \frac{Y_{n_{i,4}} Y_{n_{4,j}} Z_L}{1+Y_{n_{4,4}} Z_L}$.

We assume that the balanced amplifiers have equal bias currents of I_{DQ} and are excited with equal amplitude quadrature signals ($\boldsymbol{I_P}$ and $-j\boldsymbol{I_P}$). CPA has a bias current of I_{DQc} (a negative value for a Class-C amplifier) and excited with $\alpha \boldsymbol{I_P} e^{-j\phi}$, where α is a multiplier factor and ϕ is the phase of control path. The DC currents of balanced amplifiers, I_{DC1} and I_{DC2}, and CPA (I_{DCc}) can be expressed as nonlinear functions:

$$\begin{aligned} I_{DC1} &= f_1(I_{DQ}, \boldsymbol{I_P}, N, \overline{\boldsymbol{V_1}}) \\ I_{DC2} &= f_1(I_{DQ}, -j\boldsymbol{I_P}, N, \overline{\boldsymbol{V_2}}) \\ I_{DCc} &= f_1(I_{DQc}, \alpha e^{-j\phi}\boldsymbol{I_P}, N, \overline{\boldsymbol{V_c}}) \end{aligned} \tag{3.13}$$

Note that with a Z_L different than the nominal impedance of the hybrid-coupler, the balance of the balanced pair is destroyed resulting in unequal DC currents.

In a similar manner, we can write the current phasors of the fundamental components as

$$\begin{aligned} \boldsymbol{I_1} &= f_2(I_{DQ}, \boldsymbol{I_P}, N, \overline{\boldsymbol{V}}_{\boldsymbol{1}}) \\ \boldsymbol{I_2} &= f_2(I_{DQ}, -j\boldsymbol{I_P}, N, \overline{\boldsymbol{V}}_{\boldsymbol{2}}) \\ \boldsymbol{I_c} &= f_2(I_{DQc}, \alpha e^{-j\phi}\boldsymbol{I_P}, N, \overline{\boldsymbol{V}}_{\boldsymbol{c}}) \end{aligned} \tag{3.14}$$

where $\overline{\boldsymbol{V}}_{\boldsymbol{1}}$, $\overline{\boldsymbol{V}}_{\boldsymbol{2}}$ and $\overline{\boldsymbol{V}}_{\boldsymbol{c}}$, are normalized drain voltage phasors of balanced pair and CPA, respectively.

From the linear part of the circuit, the drain current phasors can be written in terms of voltage phasors as

$$\begin{bmatrix} \boldsymbol{I_1} \\ \boldsymbol{I_2} \\ \boldsymbol{I_c} \end{bmatrix} = - \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \begin{bmatrix} \overline{\boldsymbol{V}}_{\boldsymbol{1}} \\ \overline{\boldsymbol{V}}_{\boldsymbol{2}} \\ \overline{\boldsymbol{V}}_{\boldsymbol{c}} \end{bmatrix} \tag{3.15}$$

With the given parameters, Eqns. 3.14 and 3.15 can be solved simultaneously[1] to find the drain voltage phasors, $\overline{\boldsymbol{V}}_{\boldsymbol{1}}$, $\overline{\boldsymbol{V}}_{\boldsymbol{2}}$ and $\overline{\boldsymbol{V}}_{\boldsymbol{c}}$. Once the drain voltages are found, the load current phasor, $\boldsymbol{I_{out}}$, and normalized load voltage phasor, $\overline{\boldsymbol{V}}_{\boldsymbol{out}}$, can be found in a straightforward manner using the linear part of the circuit.

[1] We use *fsolve* function of MATLAB for simultaneous solution of three nonlinear equations.

$$\begin{aligned} \boldsymbol{I_{out}} &= \frac{\overline{\boldsymbol{V}}_{\boldsymbol{1}} Y n_{4,1} + \overline{\boldsymbol{V}}_{\boldsymbol{2}} Y n_{4,2} + \overline{\boldsymbol{V}}_{\boldsymbol{3}} Y n_{4,3}}{1 + Y n_{4,4} Z_L} \\ \overline{\boldsymbol{V}}_{\boldsymbol{out}} &= -\frac{\boldsymbol{I_{out}}}{Z_L} \end{aligned} \tag{3.16}$$

Finally, the total output power, P_{out}, and the overall efficiency, η, can be expressed as

$$\begin{aligned} P_{out} &= \frac{V_{DD}}{2} \mathcal{R}e\{\overline{\boldsymbol{V}}_{\boldsymbol{out}} (\boldsymbol{I_{out}}^*)\} \\ \eta &= \frac{P_{out}}{V_{DD}(I_{DC1} + I_{DC2} + I_{DCc})} \end{aligned} \tag{3.17}$$

Chapter 4

Design of LMBA

A prototype LMBA is designed and manufactured based on 5-W GaAs PHEMT packaged transistor, MRFG35005, and off-the-shelf couplers [1] targeting 1.7 GHz center frequency and 6 dB OBO efficiency to verify the model.

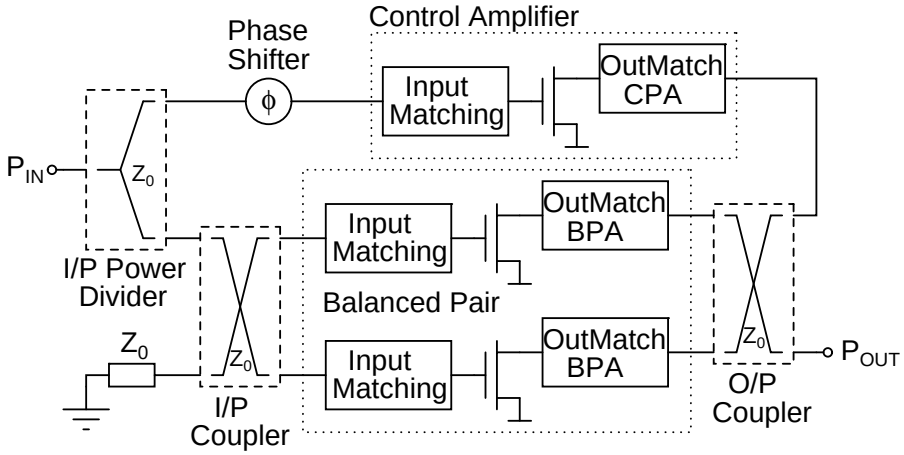


Figure 4.1: Basic block diagram of LMBA.

Fig. 4.1 depicts the required components for the design of LMBA. In this section, the measurement setups to characterize the transistor will be explained. The prototype design with the balanced pair, control amplifier and the voltage-controlled phase shifter will be discussed in detail.

[1] AV03L from Sirenza Microdevices

4.1 Transistor Characterization

As an initial phase of the design, 5-W GaAs PHEMT packaged transistor, MRFG35005, is characterized by several measurements to obtain the model and the design parameters.

4.1.1 DC Pulsed I-V Measurements

Fig. 4.2 depicts the DC pulsed I-V measurement setup to obtain the knee profile of the transistor by varying the drain-to-source voltage while observing the drain current. This can be applied for different gate-to-source voltages to acquire I-V curves in different levels. The device under test (DUT) is adjusted so that a controlled gate pulsed signal is applied while the drain current is observed through reference resistor, R_{ref}.

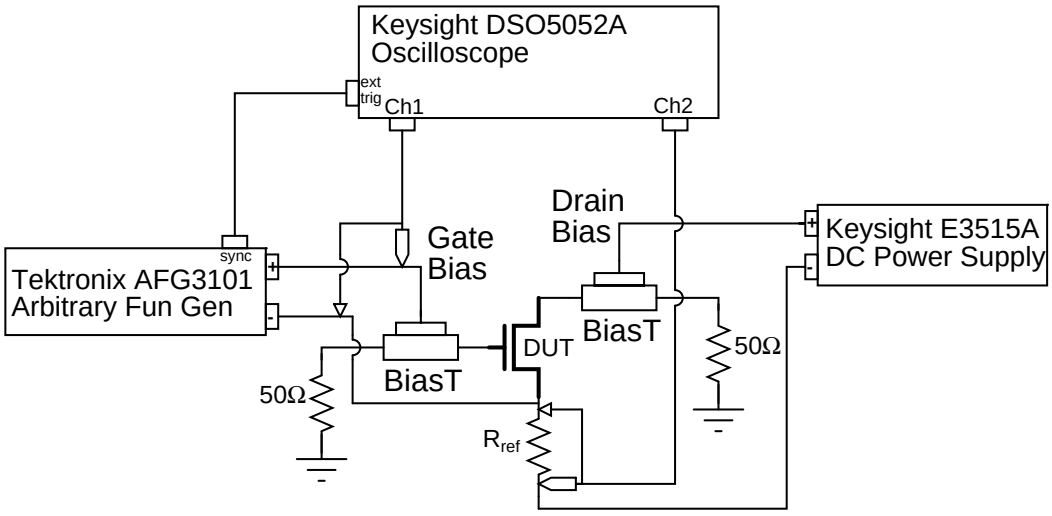


Figure 4.2: DC Pulsed I-V Measurement Setup.

We applied the gate pulse with 1% duty cycle with varying peak voltages from -1.2V to 0V and 0.1V step size where the gate threshold voltage, $V_{th} = -1.2$V. A low duty-cycle is preferred to avoid an excessive temperature increase on the transistor. The measurement is repeated for different V_{DS} voltages from 0V to 15V. Fig. 4.3 depicts the I-V curves measured and generated in the model.

$N = 28$ is well-matched with the measurements to express the knee profile of the GaAs PHEMT.

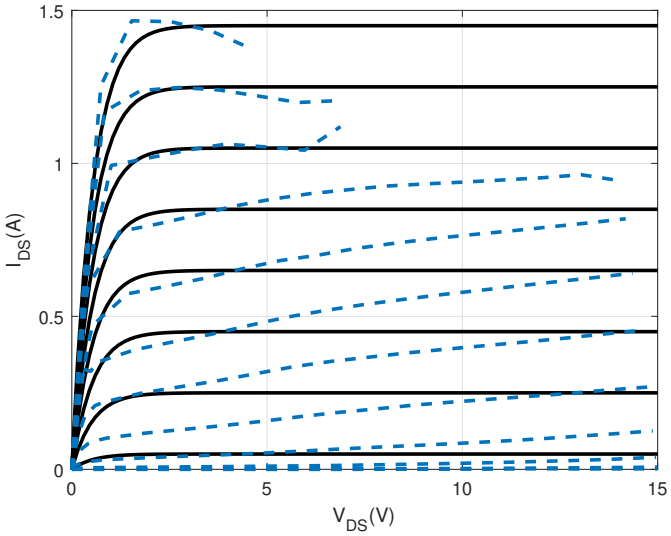


Figure 4.3: Pulsed I-V measurements of GaAs PHEMT MRFG35005(blue-dashed), I-V curves in model when $N = 28$(black-line).

4.1.2 Load-Pull Measurements

Load-pull measurement is quite crucial for PA design to analyze the device behaviour with a varying load impedance. The main purpose of the load-pull setup is to record the output power and the dissipated DC power on the transistor for different load impedances to obtain the output power and the efficiency contours. Fig. 4.4 depicts the setup consisting of a network analyzer (NA), an oscilloscope, two manual tuners [2] and a current probe to acquire load-pull contours.

First, tuner positions are calibrated before the measurements so that tuner position of each impedance on Smith chart is determined. Then, the input tuner is fixed so that the maximum power is delivered to DUT, assuming that the input impedance is nearly independent of the load impedance. For each predetermined output tuner position, the input RF power is swept in the targeted design frequency while the output power and the drain current are recorded. When the

[2]MST982BN from Maury Microwave.

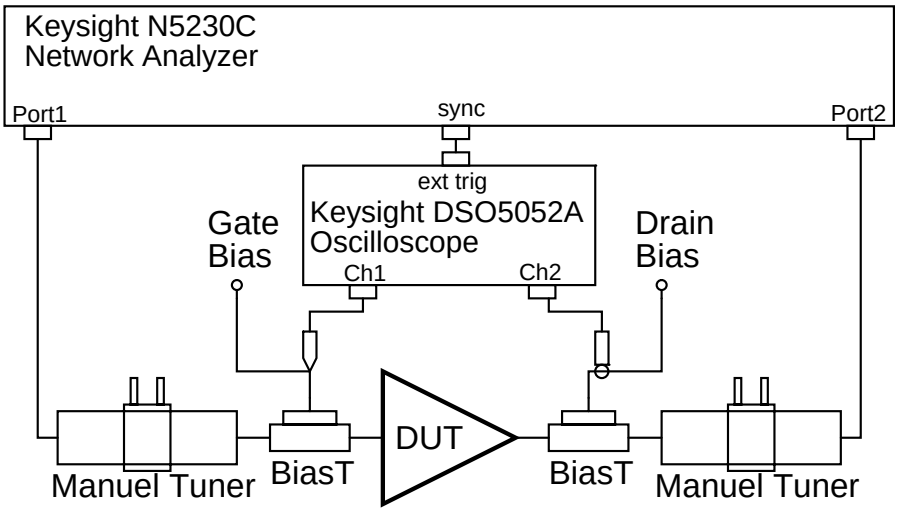


Figure 4.4: Manual Load-Pull Measurement Setup.

whole scan is finished, the recorded data is post-processed in MATLAB to obtain the output power and the efficiency curves.

The output loads are chosen so that the balanced pairs achieve the maximum efficiency at the output power of almost 30 dBm whereas the peak efficiency is obtained at approximately 36 dBm output power for the control amplifier.

Using those measurements, the parasitics, L_p and C_p in the model are found by using an optimization tool. The optimum load at maximum output power and the optimum load for maximum efficiency at approximately 6 dB OBO as well as load-pull contours obtained from the model are shown in Fig. 4.5. We note that the solution of simultaneous nonlinear equations becomes difficult for large N and large I_P values.

4.1.3 Harmonic Load-Pull Measurements

Harmonic load-pull setup is similar to the conventional load-pull setup instead it has additional harmonic tuner, triple stub tuner [3]. The main purpose is to acquire the phase of the 2^{nd} and 3^{rd} harmonic load for fixed fundamental impedance

[3] S3-05N from Microlab.

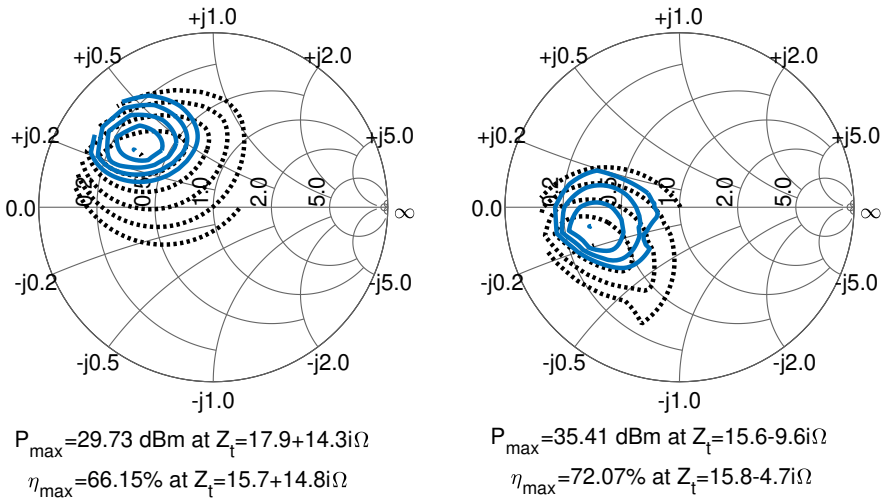


Figure 4.5: Simulated power (black-dotted) and efficiency (blue-line) contours on Smith chart for $V_{DD} = 12$ V, $I_{DQ} = 80$ mA, $N = 28$ at different input drive levels, at back-off (left) and at saturation (right). Z_t is the impedance seen by the transistor with parasitics, $L_p = 1.40$ nH and $C_p = 2.43$ pF.

to enhance the efficiency by harmonic wave engineering. Fig. 4.6 depicts the harmonic load-pull setup having an additional stub tuner.

After the fundamental impedance is determined by the load-pull measurements, the stub tuner and the output manual tuner are calibrated together so that the tuner positions are mapped for the fixed fundamental impedance at different phases of the 3^{rd} harmonic load at $\Gamma = 1$ circle. When the middle stub of the harmonic tuner is fixed so that the 3^{rd} harmonic load seen from the drain is shorted, the left stub is used to adjust the phase of the 3^{rd} harmonic load without distorting the impedance seen at the fundamental frequency adjusted by the output manual tuner. Note that the right stub is not used and only the 3^{rd} harmonic load is considered.

Fig. 4.7 displays the results of the harmonic load-pull measurements. From 45° to $-145°$ can be considered as the forbidden phase region for 3^{rd} harmonic load. Approximately an 8% enhancement is observed by 3^{rd} harmonic tuning. Note that zero-phase is right-hand-side of Smith chart and counter-clockwise rotation

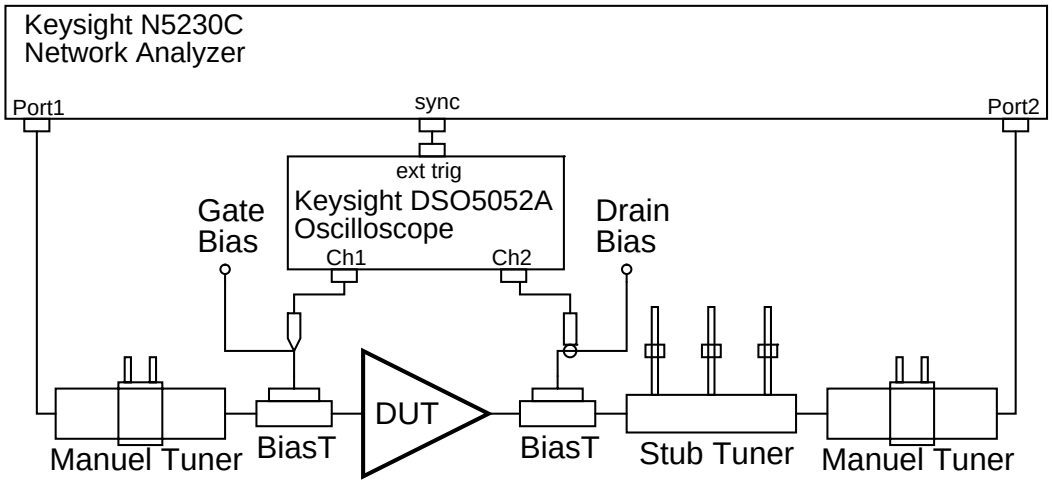


Figure 4.6: Harmonic Load-Pull Measurement Setup with Stub Tuner.

is positive direction.

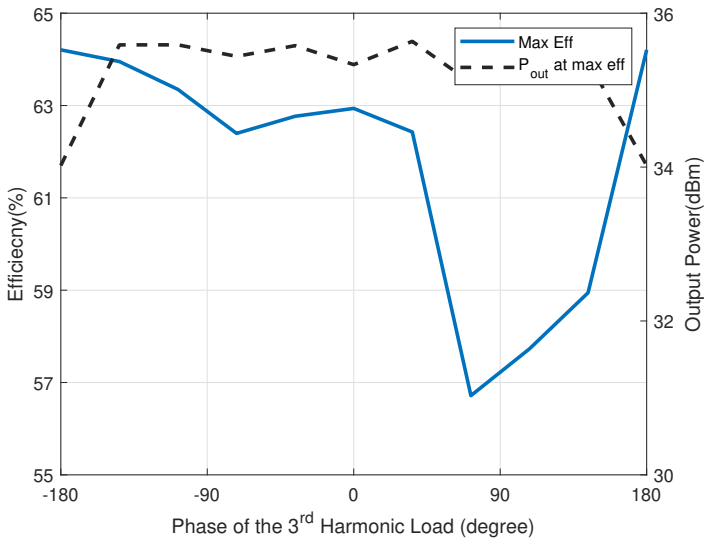


Figure 4.7: Efficiency and output power versus the phase of the 3^{rd} harmonic load for fixed fundamental impedance, Z_{fund} for $V_{DD} = 12$ V, $I_{DQ} = 80$ mA.

4.2 Active Devices

While the same supply voltage, $V_{DD} = 12$ V, is applied for all three amplifiers, the balanced pair is biased as Class-AB ($I_{DQ} = 80$ mA), and CPA is biased as

Class-C ($I_{DQc} = -450$ mA).

4.2.1 Input Matching Network

The input matching network, identical for all three devices is shown in Fig. 4.8. It is designed to ensure maximum power transfer to the active device. A parallel RC circuit is connected in series with the transistor gate to assure unconditionally stability. A 50 Ω transmission line is placed between the input and the RC circuit. A shunt capacitor is utilized to match input impedance at the targeted frequency by changing the position of the capacitor on the transmission line. The gate bias voltage is supplied through a resistor and an RFC to improve the transistor stability.

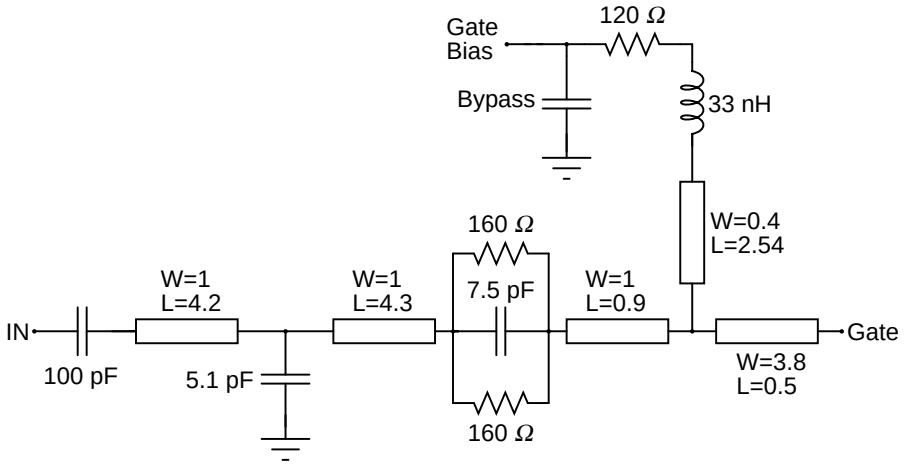


Figure 4.8: Schematic of the input matching network including bias and stabilization, length and width in mm.

4.2.2 Output Matching Networks

4.2.2.1 Balanced Pair

Fig. 4.9 depicts the basic block diagram of the balanced pair. The load impedance, Z_{BPA} is chosen so that the balanced pair achieves the maximum efficiency at 6 dB

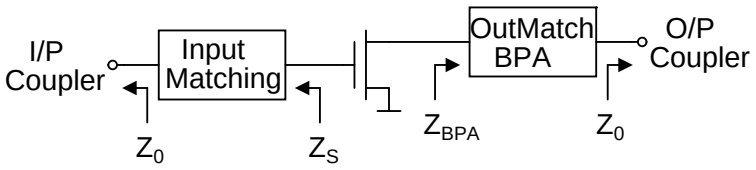


Figure 4.9: Basic scheme of the balanced pair and impedance transformation.

OBO, approximately 30 dBm. Tt is designed to transform the coupler impedance $Z_0 = 50\ \Omega$ to the optimum load impedance at 6dB-back-off, $Z_{BPA} = 9.8 + j9.3\ \Omega$. Fig. 4.10 shows the output matching network and the simulated impedance at the fundamental and the harmonic frequencies. The output-network is designed using transmission lines and the open stubs to ease post-fabrication tuning. Following the technique in [31], TL1 and TL2 are arranged so that third harmonic load is in the region where the phase variation is less sensitive. TL4 and TL5 are the same open-stubs, divided equally, to enhance the stub-matching performance with TL3 for fundamental impedance at targeted frequency.

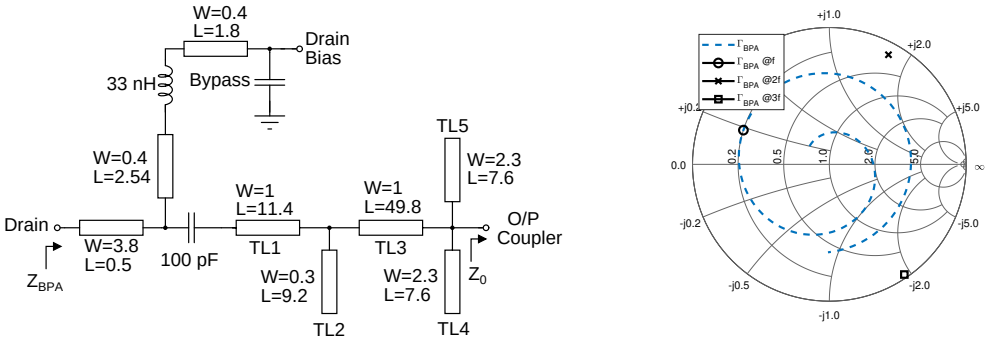


Figure 4.10: (a) Schematic of the BPA output matching network, length and width in mm (b) simulated impedance seen at the drain of BPA for the fundamental, 2^{nd} and 3^{rd} harmonic frequencies.

Layout of the balanced pair is completed in ADS according to the input and output matching networks as displayed in Fig. 4.14.

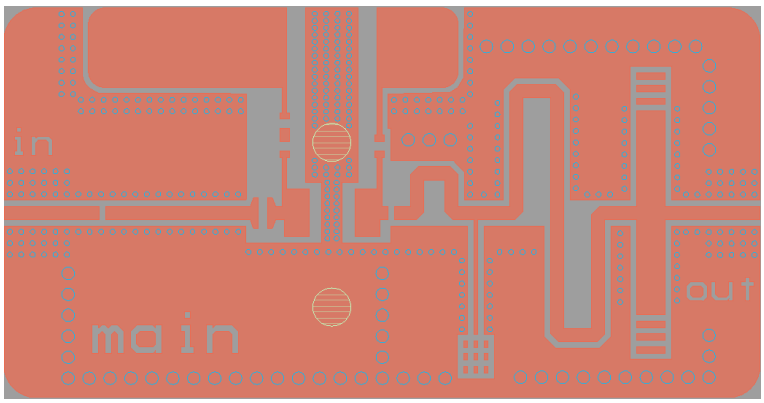


Figure 4.11: Layout of the balanced pair generated in ADS.

4.2.2.2 Control Amplifier

Fig. 4.12 depicts the basic block diagram of the control amplifier. The load impedance, Z_{CPA} is chosen so that the control amplifier achieves the maximum efficiency at saturation, at approximately 36 dBm.

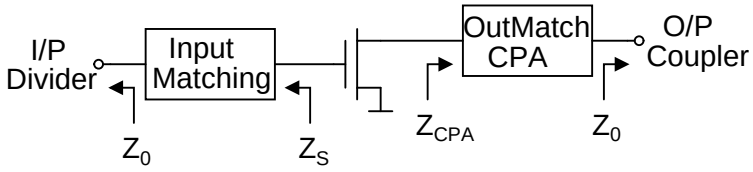


Figure 4.12: Basic scheme of the control amplifier and impedance transformation.

It is designed to transform the coupler impedance $Z_0 = 50\ \Omega$ to the optimum load impedance at saturation, $Z_{CPA} = 15.5 - j3.2\ \Omega$. Figs. 4.13a and 4.13b show the output matching network and the simulated impedance at the fundamental and the harmonic frequencies. Similar to the output network of BPA, the transmission lines and the open stubs are used for the network design of CPA. By adjusting length of TL4 and TL5, the fundamental impedance seen at external drain of CPA is arranged accordingly. Third harmonic load is again terminated so that it is away from the forbidden region according to harmonic load-pull measurements.

Overall layout design of the control amplifier is completed in ADS according to the input and output matching networks as displayed in Fig. 4.14.

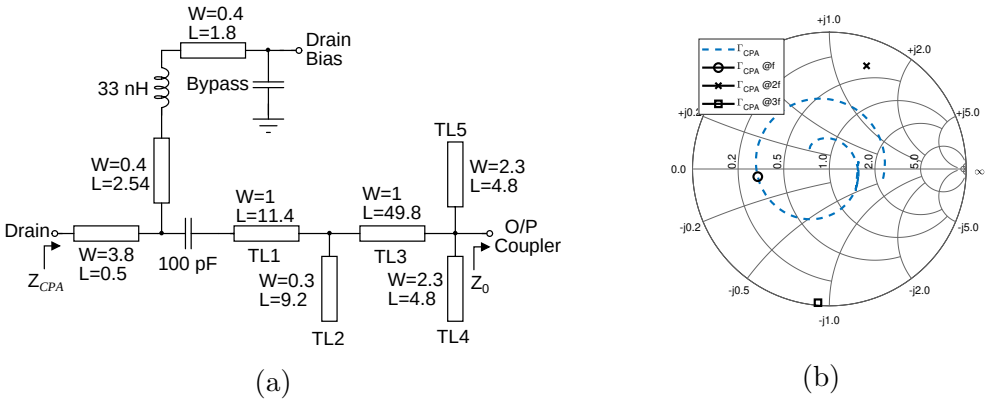


Figure 4.13: (a) Schematic of the CPA output matching network, length and width in mm (b) simulated impedance seen at the drain of CPA for the fundamental, 2^{nd} and 3^{rd} harmonic frequencies.

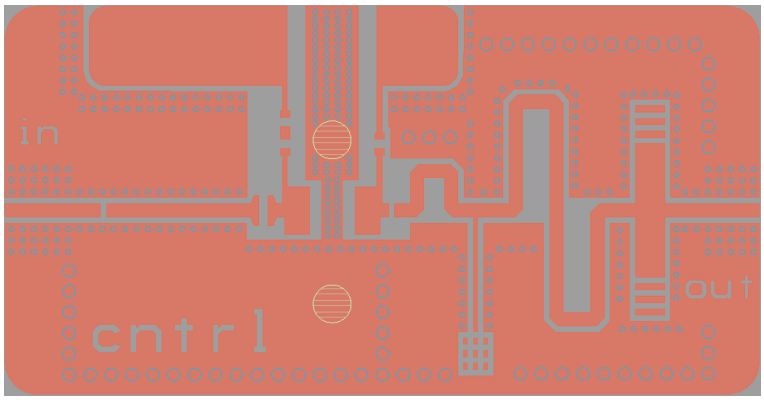


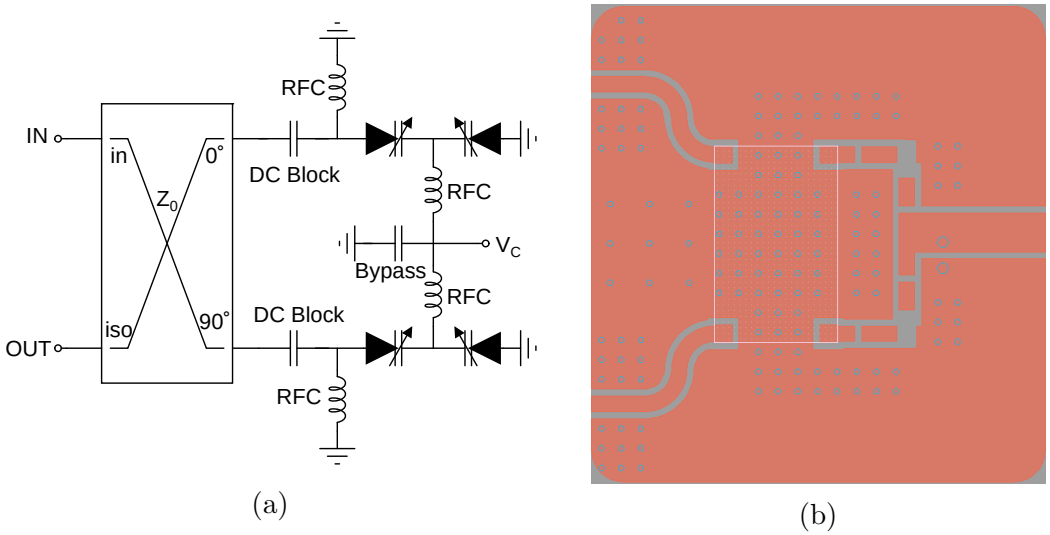
Figure 4.14: Layout of the control amplifier generated in ADS.

4.3 Phase-Shifter

To tune the phase of the control path, a voltage controlled phase shifter is designed using an off-the-shelf coupler [4] and the varactors [5]. Fig. 4.15a depicts the schematic of the phase shifter. Since 3^{rd} and 4^{th} port of the coupler are terminated with a capacitive reactance, the signal at input port is exposed to phase shift at the output while the amplitude stays constant. By changing the capacitance values, the phase can be adjusted as well. The common cathode varactors are used to minimize the effect of the sudden DC voltage change. Fig. 4.15b

[4] AV03L from Sirenza Microdevices
[5] SMV2022 from Skyworks

shows the phase shifter layout generated in ADS.



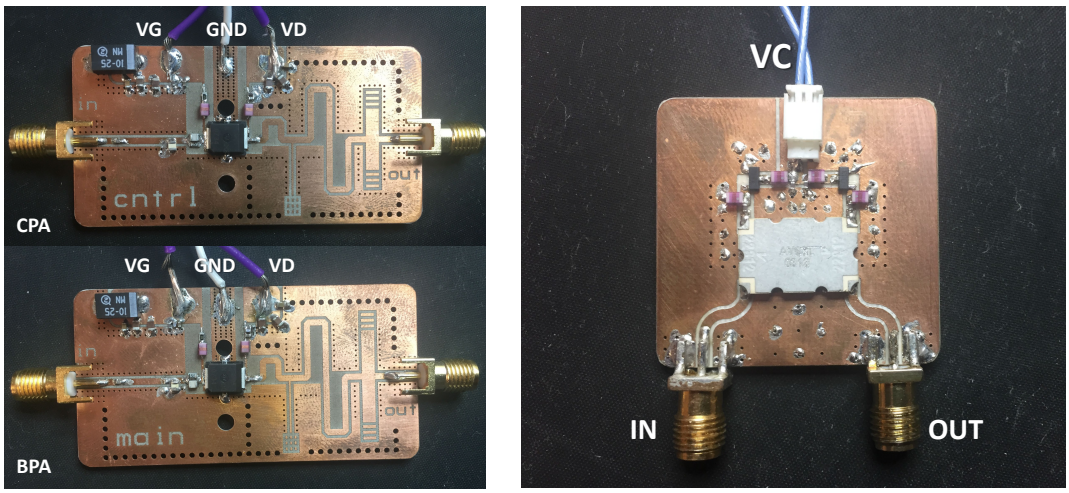
(a) (b)

Figure 4.15: (a) Basic schematic and (b) Layout designed in ADS of the voltage controlled phase shifter.

Chapter 5

Simulation and Measurement Results

Each PA and the phase shifter are fabricated on 20 mil Rogers RO4350B substrate. Fig. 5.1 depicts the fabricated PCBs of the power amplifiers and the phase shifter.



(a) (b)

Figure 5.1: (a) Fabricated control amplifier (top) and one of the balanced pair (bottom), (b) Fabricated voltage controlled phase shifter.

The Wilkinson power divider is used as the input power splitter, so the input power is supplied equally for both the balanced and the control amplifier. Fig. 5.2 depicts LMBA generated by combining the amplifiers, the phase shifter, the divider and the couplers.

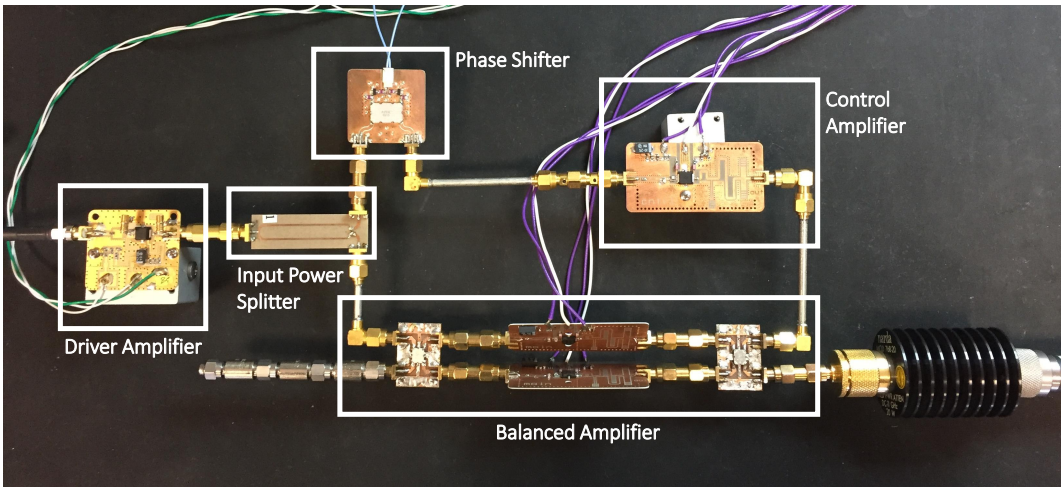


Figure 5.2: Photograph of the LMBA prototype.

Fig. 5.3 shows some model parameters in the basic block diagram of LMBA. α corresponds to input power split ratio. Since the Wilkinson power divider is used, it is 0.5. ϕ represents the phase delay in the control path, required for proper load modulation. Since the DC current on the drain is directly adjusted by the gate voltages, V_G's represent I_{DQ}'s in the model.

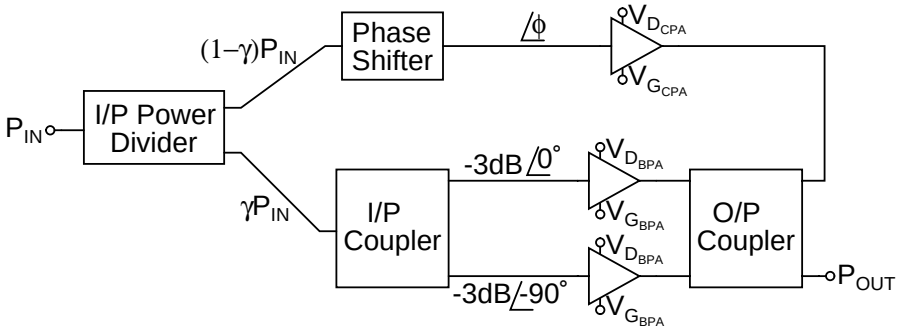


Figure 5.3: Basic block diagran of LMBA in model.

The parameters used in simulation are given in Table 5.1.

Table 5.1: Model Parameters in Simulation.

Model Symbol	$V_{D_{BPA}}$	$I_{DQ_{BPA}}$	$V_{D_{CPA}}$	$I_{DQ_{CPA}}$	N	γ	ϕ
Value	12	0.08	12	-0.45	28	0.5	-100

5.1 Scattering Measurements

As an initial assessment, scattering measurements of the fabricated devices is carried out. Fig. 5.4 shows the system used for the S-parameter measurements of active devices, where we use Keysight N5230C Network Analyzer (NA). Both BPA and CPA are biased at 12 V and 80 mA for test purposes.

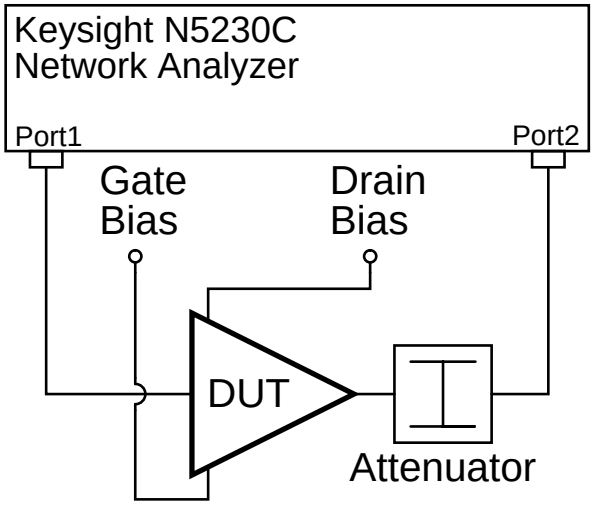


Figure 5.4: Small Signal Measurement Setup.

Scattering measurements are performed in frequency range of $1.5 - 2$ GHz. Fig. 5.5 depicts the simulated and the measured input reflection and transmission of one of the balanced pair and CPA. Note that simulations are done in ADS at schematic level. Approximately 10 dB input return loss with 15 dB small-signal gain achieved both PAs after fabrication. The measurement results are in good agreement with the simulations in both PAs.

Measured S-parameters and phase of S21 at 1.7 GHz are given in Fig. 5.6. The phase of the signal can be adjusted from $-70°$ to $80°$ by tuning the control voltage as the signal has almost no loss in forward direction. Since the varactors

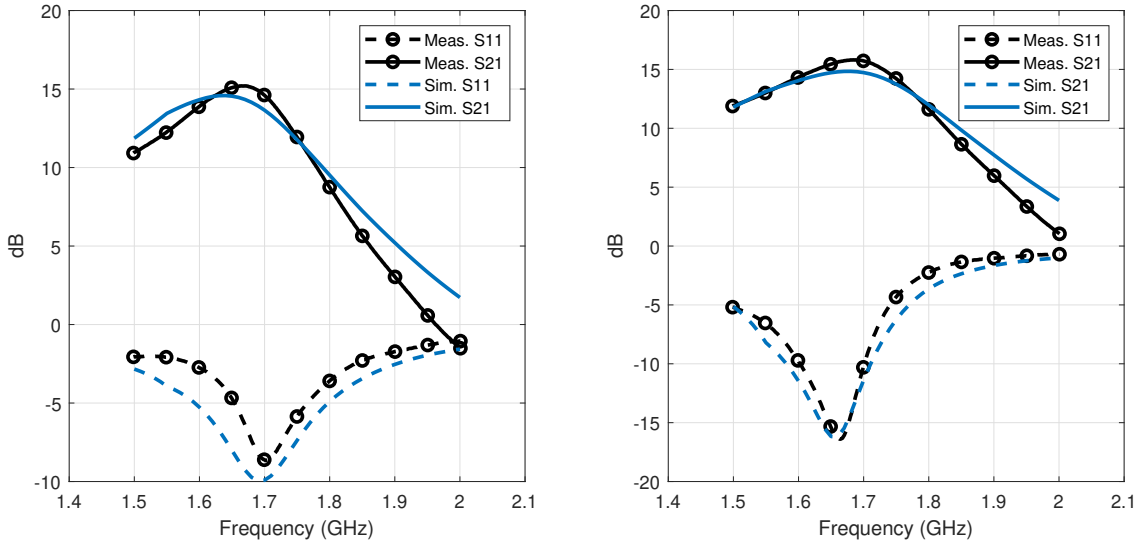


Figure 5.5: Measured and simulated scattering parameters: the balanced pair (left) and CPA (right).

is non-ideal, there is approximately 2 dB loss at low V_C values.

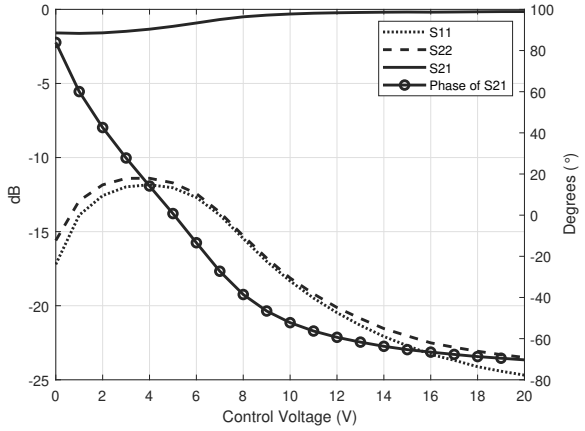


Figure 5.6: Measured characteristics of the fabricated phase shifter for varying control voltage V_C.

5.2 CW Measurements

In measurements, we utilized the network analyzer and the oscilloscope with current probe as CW measurement setup. As seen in Fig. 5.7, NA and the oscilloscope are synchronized with external trigger of NA. A linear driver amplifier is used to amplify input signal power to proper level. A high power attenuator is used to protect NA from excessive power level. While the input power is varying, the drain current is recorded by current probe. Then, one can obtain for dissipated power on the drain for the corresponding input power.

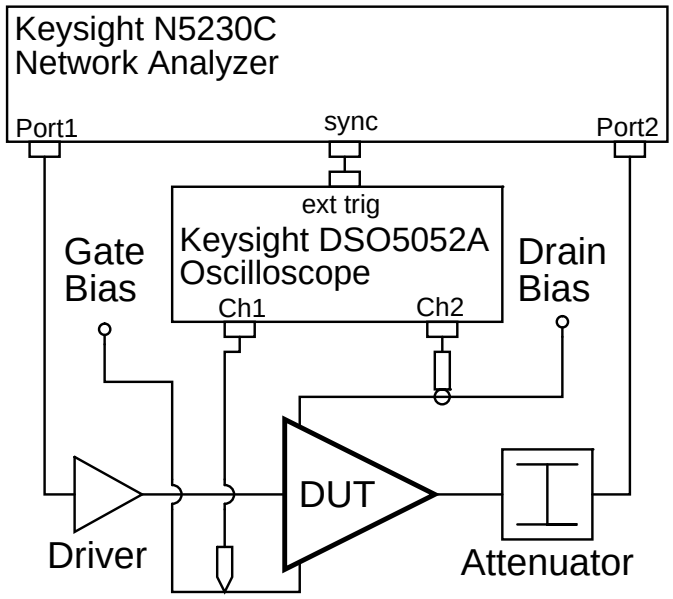
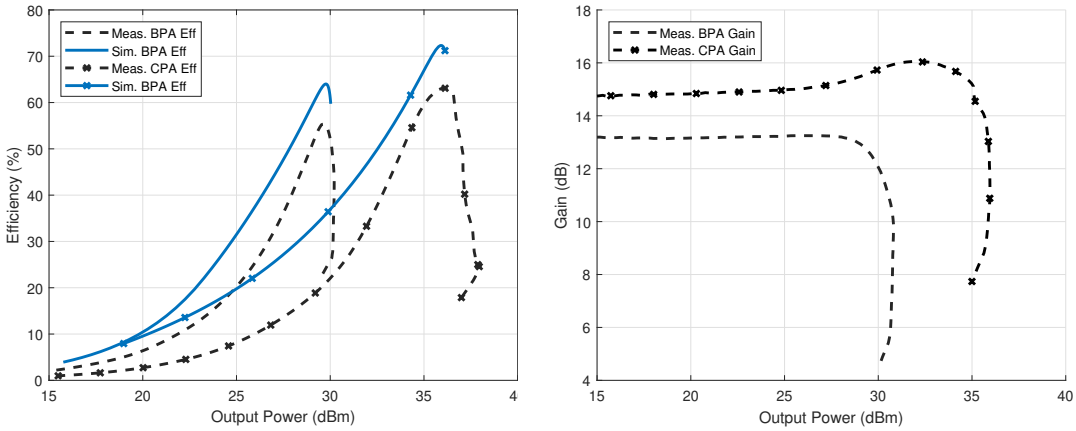


Figure 5.7: CW Large Signal Measurement Setup.

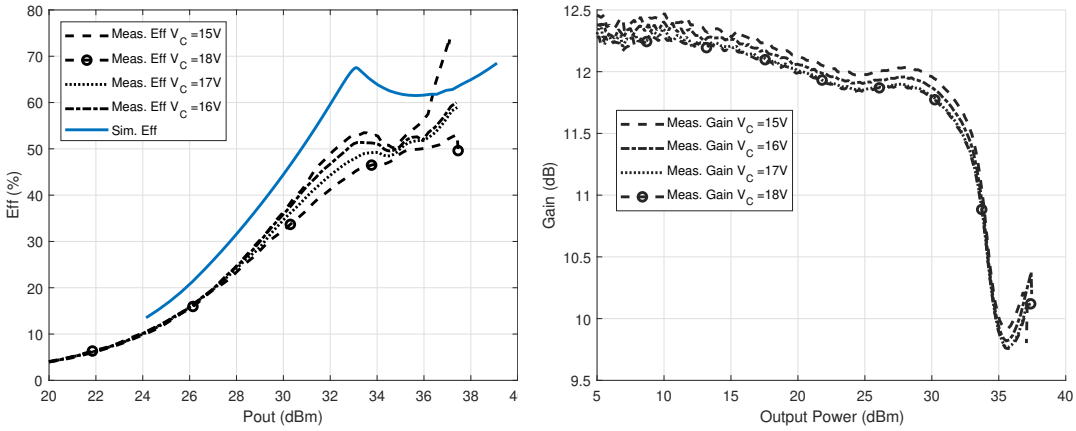
CW measurements are done at 1.7 GHz. Fig. 5.8 depicts the simulated and measurement results of both BPA and CPA individually when they are biased at 12 V and 80 mA. Approximately, 10% difference between the measured and the simulated results is clearly seen in Fig. 5.8. The loss on PCB and discrete components on the RF path can result some difference between measured and simulated results. Overall, both BPAs and CPA operate at targeted efficiency and output power region. For balanced pairs, the drain efficiency is achieved above 50% at peak power of approximately 30 dBm. CPA operates at saturation so that it achieves peak output power of 35.7 dBm with 62% drain efficiency.



(a) (b)

Figure 5.8: (a) Simulated and measured drain efficiency and (b) measured gain versus output power for balanced pairs and control amplifier with $V_{DD} = 12$ V, $I_{DQ} = 80$ mA, $N = 28$ and $Z_L = 50\ \Omega$ obtained by varying the input drive level, I_P.

By adjusting the gate bias level of CPA and the phase of the phase shifter, LMBA is tuned experimentally. Our analytical model indicates that the optimum is reached when $\phi = -100°$. This value is in agreement with the theoretical prediction of $\phi = -90°$ given in [28]. Balanced PAs operates conventionally till the output power reaches the peak power of combined pairs, 33 dBm. For the higher input power levels, CPA starts to operate in such a way to modulate the output impedance of balanced pairs towards the optimum load at saturation. Fig. 5.9 depicts the simulated and the measured results of LMBA. As it is seen in plot, the efficiency characteristic is quite similar in both simulation and measurement. In the simulation, the efficiency stays above 60% throughout 6 dB output-back-off region. The measured efficiency is 53%, 50% and 47% at peak power of 37.5 dBm, 3 dB and 6 dB output-back-off, respectively.



(a) (b)

Figure 5.9: (a) Measured and simulated efficiency versus output power for LMBA at 1.7 GHz with model parameters: $V_{DD} = 12$ V, $I_{DQ} = I_{DQ} = 80$ mA, $I_{DQc} = -0.45$ A, $N = 28$, $\alpha = \sqrt{2}$ and $\phi = -100°$. (b) Measured gain versus output power for LMBA at 1.7 GHz.

5.3 Modulated Signal Measurements

The linearity of LMBA is evaluated by OFDM signal with 10 MHz channel bandwidth and 12 dB PAPR, centered at 1.705 GHz. The I-Q components of the signal are obtained in MATLAB using LTE toolbox. Then, the modulated signal is generated using IQ modulation utility of Keysight MXG N5182B generator. The input power of DUT is adjusted while the average output power is observed by Keysight N9913A Spectrum Analyzer. The measurement setup is given in Fig. 5.10.

Fig. 5.11 depicts the measured output spectrum of LMBA with no digital predistortion. A respectable adjacent channel leakage ratio (ACLR) of -33 dBc is measured with an average output power of 29 dBm and a drain efficiency of 41%.

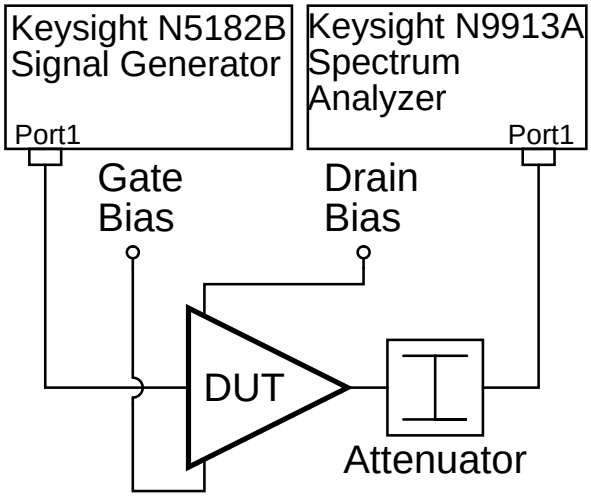


Figure 5.10: Modulated Signal Measurement Setup.

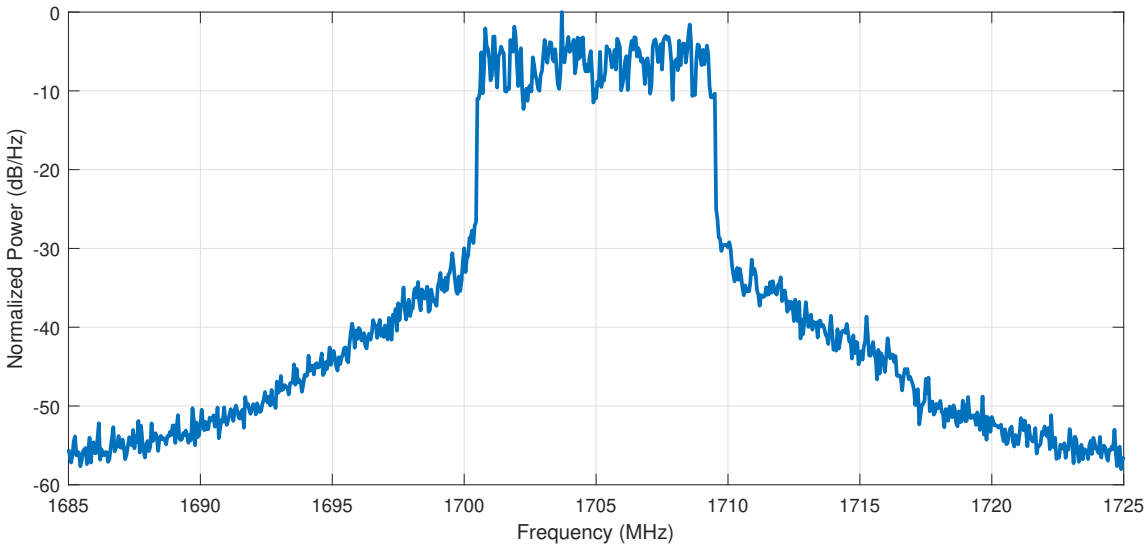


Figure 5.11: Measured output power spectrum of LMBA. LTE signal with 10 MHz channel bandwidth and 12 dB PAPR obtained from Keysight N5182B signal generator is used as the modulated input signal.

Chapter 6

Conclusion

As the thesis subject, a recently proposed load modulation topology, load modulated balanced amplifier, is chosen to achieve high output back-off efficiency and linearity. The operation theory of LMBA is briefly reviewed and a new analytical model of LMBA using simple RF transistor model is presented. Although the match between measurements and model predictions is not perfect, the model is able to predict the high efficiency and good linearity behavior of LMBA under OBO conditions.

The design steps of LMBA are explained and an LMBA is designed operating at 1.7 GHz to verify the analytical results. Three single-ended power amplifiers are designed, two of which are identical balanced pair achieving maximum efficiency at 6 dB output back-off in class-AB configuration, the other is the class-C biased control amplifier designed to reach maximum efficiency at saturation. Additionally, the voltage controlled phase shifter is designed to adjust the phase of the control signal for proper load modulation. LMBA is built after each component is fabricated and individually tested.

An efficiency of more than 47% is achieved within the 6 dB OBO region with the peak output power of 37.5 dBm. Using an LTE input signal with 12 dB PAPR, an average 29 dBm output power (approximately 9 dB OBO) is demonstrated

with a 41% drain efficiency and -33 dBc ACLR.

As a future work, the integrated version of LMBA can be built. There is only one example of X-band MMIC application of the presented topology. With the recent advances in 5G technology, the realization of LMBA in higher frequencies as MMIC design may play important role for achieving highly efficient RF front-ends. Also, behaviour of LMBA under the varying load should be investigated, which is crucial for the transmitter applications where the output of LMBA is connected to an antenna.

Bibliography

[1] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*. Norwood, MA: Artech House, 2nd ed., 2006.

[2] A. Grebennikov, "Linearity improvement techniques for wireless transmitters: Part 1," *High Frequency Electronics*, pp. 16–26, May. 2009.

[3] A. Grebennikov, "Linearity improvement techniques for wireless transmitters: Part 2," *High Frequency Electronics*, pp. 44–53, May. 2009.

[4] H. Rohling, ed., *OFDM: Concepts for Future Communication Systems*. Verlag Berlin Heidelberg: Springer, 2011.

[5] C. Ramella, A. Piacibello, R. Quaglia, V. Camarchia, and M. Pirola, "High efficiency power amplifiers for modern mobile communications: The load-modulation approach," *Electronics*, vol. 96, Nov. 2017.

[6] J. L. S.H. Han, "An overview of peak-to-average power ratio reduction techniques for multicarrier transmission," *IEEE Wireless Communications*, pp. 56–65, Apr. 2005.

[7] S. Gao, "High efficiency class F RF/Microwave power amplifiers," *IEEE Microwave Magazine*, pp. 40–48, Feb. 2006.

[8] Y. Y. Woo, Y. Yang, and B. Kim, "Analysis and experiments for high-efficiency class-F and inverse class-F power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, pp. 1969–1974, May. 2006.

[9] E. Cipriani, P. Colantonio, F. Giannini, and R. Giofre, "Theoretical and experimental comparison of class F vs. class-F^{-1} PAs," *European Microwave Integrated Circuits Conference*, pp. 428–431, 2010.

[10] S. El-Hamamsy, "Design of high-efficiency RF class-D power amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 9, pp. 297–308, May. 1994.

[11] A. Mediano, P. Molina-Gaudo, and C. Bernal, "Design of class E amplifier with nonlinear and linear shunt capacitances for any duty cycle," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, pp. 484–492, Mar. 2007.

[12] D. Wang, D. F. Kimball, J. D. Popp, A. H. Yang, D. Y. Lie, P. M. Asbeck, and L. E. Larson, "An improved power-added efficiency 19-dbm hybrid envelope elimination and restoration power amplifier for 802.11g WLAN applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, pp. 4086–4099, Dec. 2006.

[13] D. Kim, D. Kang, J. Choi, J. Kim, Y. Cho, and K. Kim, "Optimization for envelope shaped operation of envelope tracking power amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, pp. 1787–1795, Jul. 2011.

[14] F. Yang, A. Ojo, D. Kimball, P. Asbeck, and L. Larson, "Envelope tracking power amplifier with pre-distortion linearization for WLAN 802.11g," *IEEE MTT-S*, pp. 1543–1546, 2004.

[15] W. H. Doherty, "A new high efficiency power for modulated waves," *Proceedings of the Institute of Radio Engineers*, vol. 24, pp. 1163–1182, Sep. 1936.

[16] B. Kim, J. Kim, I. Kim, and J. Cha, "The Doherty power amplifier," *IEE Microwave Magazine*, pp. 42–50, Oct. 2006.

[17] N. Srirattana, A. Raghavan, D. Heo, P. E. Allen, and J. Laskar, "Analysis and design of a high-efficiency multistage Doherty power amplifier for

wireless communications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, pp. 852–860, Mar. 2005.

[18] H. Chirex, "High power outphasing modulation," *Proceedings of the Institute of Radio Engineers*, vol. 23, pp. 1370–1392, Nov. 1935.

[19] A. Birafane and A. B. Kouki, "On the linearity and efficiency of outphasing microwave amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, pp. 1702–1708, Jul. 2004.

[20] Z. Zhang, L. E. Larson, and P. M. Asbeck, *Design of Linear RF Outphasing Power Amplifiers*. Norwood, MA: Artech House, 1st ed., 2003.

[21] D. J. Shepphard, J. R. Powell, and S. C. Cripps, "An efficient broadband reconfigurable power amplifier using active load modulation," *IEEE Microwave and wireless components letters*, vol. 26, pp. 443–445, June 2016.

[22] K. B. Niclas, W. T. Wilser, R. B. Gold, and W. R. Hitchens, "Amplification of the two-way balanced amplifier concept to wide-band power amplification using GaAs MESFET's," *IEEE Transactions on Microwave Theory and Techniques*, vol. 28, pp. 172–179, Mar. 1980.

[23] R. Quaglia and S. C. Cripps, "A load modulated balanced amplifier for telecom applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, pp. 1328–1338, Mar. 2018.

[24] D. J. Sheppard, J. Powell, and S. C. Cripps, "A broadband reconfigurable load modulated balanced amplifier (LMBA)," *IEEE MTT-S International Microwave Symposium*, pp. 947–949, 2017.

[25] J. R. Powell, D. J. Shepphard, R. Quaglia, and S. C. Cripps, "A power reconfigurable high-efficiency X-band power amplifier MMIC using the load modulated balanced amplifier technique," *IEEE Microwave and wireless components letters*, vol. 28, pp. 527–529, June 2018.

[26] P. H. Pednekar and T. W. Barton, "RF-input load modulated balanced amplifier," *IEEE MTT-S International Microwave Symposium*, pp. 1730–1733, 2017.

[27] P. H. Pednekar, E. Berry, and T. W. Barton, "RF-Input load modulated balanced amplifier with octave bandwidth," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, pp. 5181–5191, Dec. 2017.

[28] P. H. Pednekar, W. Hallberg, C. Fager, and T. W. Barton, "Analysis and design of Doherty-Like RF-Input load modulated balanced amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, pp. 5322–5335, Dec. 2018.

[29] T. Cappello, P. Pednekar, C. Florian, S. Cripps, Z. Popovic, and T. W. Barton, "Supply- and load-modulated balanced amplifier for efficient broadband 5G base stations," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, pp. 3122–3133, Jul. 2019.

[30] R. Quaglia, D. J. Shepphard, and S. C. Cripps, "A reappraisal of optimum output matching conditions in microwave power transistors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, pp. 838–845, Mar. 2017.

[31] A. Grebennikov, "Load network design technique for class F and inverse class F power amplifiers," *High Frequency Electronics.*, vol. 10, pp. 58–76, May. 2011.

Appendix A

Series Expansion

The knee profile function given in 3.3 can be expanded as,

$$k(v_{ds}) = k_0 + \sum_{n=1}^{N/2} [k_{2n,R}\cos(2n\theta) + k_{2n,Q}\cos(2n\theta)] \tag{A.1}$$

The components k_j's can be found as,

$$\begin{aligned} k_0 &= 1 - \binom{V}{2}^N \binom{N}{N/2} \\ k_{2n,R} &= -2\binom{V}{2}^N \binom{N}{N/2-n}\cos(2n\gamma) \\ k_{2n,Q} &= 2\binom{V}{2}^N \binom{N}{N/2-n}\sin(2n\gamma) \end{aligned} \tag{A.2}$$

where V and γ are the magnitude and negative of the phase of the normalized drain voltage, respectively.

The DC and the fundamental components of the drain current can be written

in terms of k_j's and A_j's,

$$\begin{aligned} I_0 &= A_0 I_0 + \frac{1}{2}\sum_{n=1}^{N/2} A_{2n} k_{2n,R} \\ I_{1R} &= A_1 I_0 + \frac{1}{2}\sum_{n=1}^{N/2} (A_{2n-1} + A_{2n+1}) k_{2n,R} \\ I_{1Q} &= \frac{1}{2}\sum_{n=1}^{N/2} (A_{2n-1} - A_{2n+1}) k_{2n,Q} \end{aligned} \tag{A.3}$$

Then the drain current in the phasor at the fundamental can be written as,

$$I = I_{1R} + jI_{1Q} \tag{A.4}$$

Appendix B

Algorithm for Single-Ended Amplifier (Load Impedance Sweep)

1. **input** N, IDQ, IP, VDD and $Z0$
2. **input** number of phase steps of load Γ, np, number of amplitude steps of load Γ, ng and maximum Γ amplitude, gm
3. **initialize** matrices to reserve space, $POUT$, EFF, VDS, IDS, $I0$ and ZL
4. **define** a function $I0 = f1(N, IDQ, IP, VDS)$
5. **define** a function $IDS = f2(N, IDQ, IP, VDS)$
6. **define** the solver
7. **for** phi from $2\pi/np$ to 2π with step size $2\pi/np$ **do**
8. **for** g from 0 to gm with step size $gm/(np-1)$ **do**
   (a) **find** corresponding normalized load impedance, ZL/VDD
   (b) **solve** the non-linear function system for VDS, $IDS = f2(N, IDQ, IP, VDS)$ and $VDS = ZL \times IDS$

(c) **find** $I0$ using function $f1$

(d) **find** $IDS = VDS/ZL$

(e) **find** $POUT = real(VDS \times conj(IDS))VDD/2$

(f) **find** $EFF = POUT/I0$

(g) **save** $POUT$, EFF, VDS, IDS, $I0$ and ZL

9. **end**