Normally-off p-GaN gate InAlN/GaN HEMTs grown on silicon substrates

Melisa Ekin Gulseren[1,2], Berkay Bozok[1,2], Gokhan Kurt[2], Omer Ahmet Kayal[2], Mustafa Ozturk[2], Sertac Ural[2], Bayram Butun[2], Ekmel Ozbay[1,2,3,4]

[1] Department of Electrical and Electronics Engineering, Bilkent University, 06800 Ankara, Turkey
[2] Nanotechnology Research Center, Bilkent University, 06800 Ankara, Turkey
[3] UNAM-Institute of Materials Science and Nanotechnology, Bilkent University, 06800 Ankara, Turkey
[4] Department of Physics, Bilkent University, 06800 Ankara, Turkey

ABSTRACT

A normally-off InAlN/GaN high electron mobility transistor (HEMT) on Si substrate with a p-GaN gate is reported. Devices are fabricated on two different epitaxial structures, one containing a high resistive GaN buffer layer and one containing an AlGaN back-barrier, and the threshold voltage, drain current density, and buffer leakage current are compared. With the epitaxial structure containing a high resistive GaN layer, normally-off operation with a threshold voltage of +0.5 V is achieved. The threshold voltage is further increased to +2 V with the AlGaN back-barrier, and the buffer leakage current was improved by over an order of magnitude.

Keywords: back-barrier, buffer leakage, GaN, high-electron-mobility transistors (HEMTs), InAlN, normally-off, p-GaN gate

1. INTRODUCTION

GaN-based high electron mobility transistors (HEMTs) are widely popular for high-power and high-frequency devices in many defense and commercial applications owing to their wide bandgap, high electron saturation velocity, high breakdown field, large polarization, and high two-dimensional electron gas (2DEG) density[1-3]. Lattice matched InAlN/GaN heterostructures have the advantages of higher 2DEG density due to higher spontaneous polarization fields, less strain and less crystal defects compared to the AlGaN/GaN counterpart and are thus promising candidates for power and RF device applications[4-8]. GaN-based HEMTs are inherently normally-on devices; in many power electronics applications, such as in switching applications, normally-off operation is preferred for security, reliability, and compatibility reasons. Various different approaches, such as a gate recess, fluorine treatment, p-type gate, and thin AlGaN barrier have been demonstrated to obtain normally-off HEMTs for AlGaN/GaN based devices[9-13]. Similarly, using fluorine treatment, gate recess, and ultrathin (e.g. 2 nm) InAlN barrier layers InAlN/GaN enhancement mode HEMTs have been realized[14-16].

In the p-type gate approach, a p-(Al)GaN layer acts to lift up the conduction band above the Fermi level, resulting in the depletion of the 2DEG channel by the p-n junction even in the absence of an external applied bias. This method is utilized in commercially available normally-off GaN HEMT devices. The p-type gate method has the advantage of controllability of the threshold voltage, also, it is a reliable method. The disadvantages are that the obtainable threshold voltages are relatively low and the gate leakage is larger. An AlGaN back-barrier can further improve these characteristics through increasing the threshold voltage by acting as a virtual p-type doping and mitigating the buffer leakage current by providing effective confinement of the electrons in the 2DEG region[17].

This study aims to achieve normally-off operation in InAlN/GaN HEMTs by utilizing a p-GaN gate. The effects of an AlGaN back-barrier on these normally-off devices are investigated. Devices are fabricated on two different epitaxial structures, one containing a high resistive GaN layer and one containing an AlGaN back-barrier. The AlGaN back-barrier serves to further increase the threshold voltage by acting as virtual p-type doping, and to mitigate the buffer leakage current. A threshold voltage of +0.5 V is achieved from the epitaxial structure with the high resistive GaN layer.

Gallium Nitride Materials and Devices XIV, edited by Hiroshi Fujioka, Hadis Morkoç,
Ulrich T. Schwarz, Proc. of SPIE Vol. 10918, 109181A · © 2019 SPIE
CCC code: 0277-786X/19/$18 · doi: 10.1117/12.2507398

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This threshold voltage increases to +2 V with the addition of the AlGaN back-barrier. The AlGaN back-barrier supresses the buffer leakage current by five orders of magnitude.

2. DESIGN OF DEVICE AND EPITAXY

Using a 2D self-consistent Poisson-Schrödinger solver (Silvaco Atlas)[18], the energy band diagrams were simulated in order to gain insight into the achievable threshold voltages and understand the physical mechanism of the AlGaN back-barrier. A simplified structure consisting of a 20 nm p-GaN layer, $In_{0.17}Al_{0.83}N$ barrier layer, GaN channel layer and an AlGaN back-barrier was used in the simulations. A 2DEG sheet carrier density of 2×10^{13} cm^{-2} was assumed according to typical values in the literature. Uniform doping with a density of 3.0×10^{17} cm^{-3} was assumed for the p-GaN layer. Various barrier layer thicknesses and AlGaN back-barrier Al-concentrations were tested. The obtained band diagrams are shown in Fig. 1 and Fig. 2. The conduction band diagrams for the p-GaN/InAlN/GaN structure in the gate region with and without the AlGaN back-barrier are given in Fig. 1(a) for three different InAlN barrier thicknesses (6 nm, 8 nm, 10 nm) and in Fig. 1(b) for three different $Al_xGa_{1-x}N$ back-barrier concentrations (x = 0.05, 0.10, 0.15) for a barrier thickness of 8 nm. Fermi carrier statistics, concentration dependent recombination models, direct transition of three carriers, and separate low field mobility models for electron and holes were used. The use of a p-GaN gate causes the depletion of the channel under the gate region in the absence of a gate bias through raising the conduction band and enables normally-off operation. According to the simulation results, a threshold voltage in the range of 0.5-2 V is expected for the varying barrier thicknesses for the p-GaN/InAlN/GaN structure. For the p-GaN/InAlN/GaN/AlGaN structure a threshold voltage in the range of 1-2.3 V is expected for the varying Al content of the AlGaN back-barrier.

The AlGaN back-barrier acts in a similar manner and in the enhancement of the p-GaN gate, further lifting the conduction band above the Fermi level to deplete the 2DEG. Due to the conduction band notch at the interface with the GaN channel, electrons are better confined in the 2DEG region, thereby leading to the suppression of the buffer current. However, the steep slope of the conduction band caused by Al-content in the buffer leads to decreased electron population in the channel.

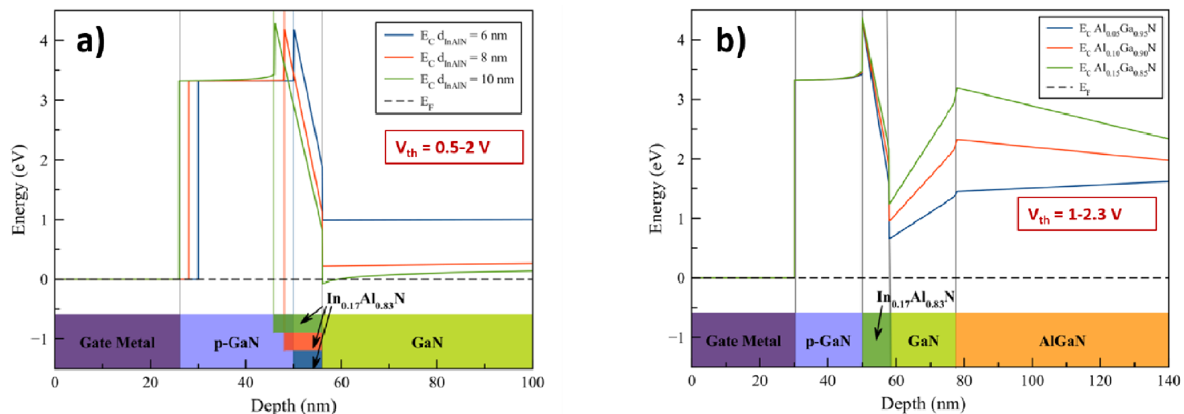

Figure 1. Simulated energy band structure for the structure a) without and b) with AlGaN back-barrier in the gate region.

The simulated band diagrams of the p-GaN/InAlN/GaN structures without and with the AlGaN back-barrier in the gate region under applied gate voltage are shown in Figure 2. Due to the p-GaN layer, the 2DEG is depleted under equilibrium conditions and begins to form when a gate bias is applied. The 2DEG begins to form at higher gate biases compared to the standard structure for the structure with the AlGaN back-barrier, thus a higher threshold voltage is achievable.

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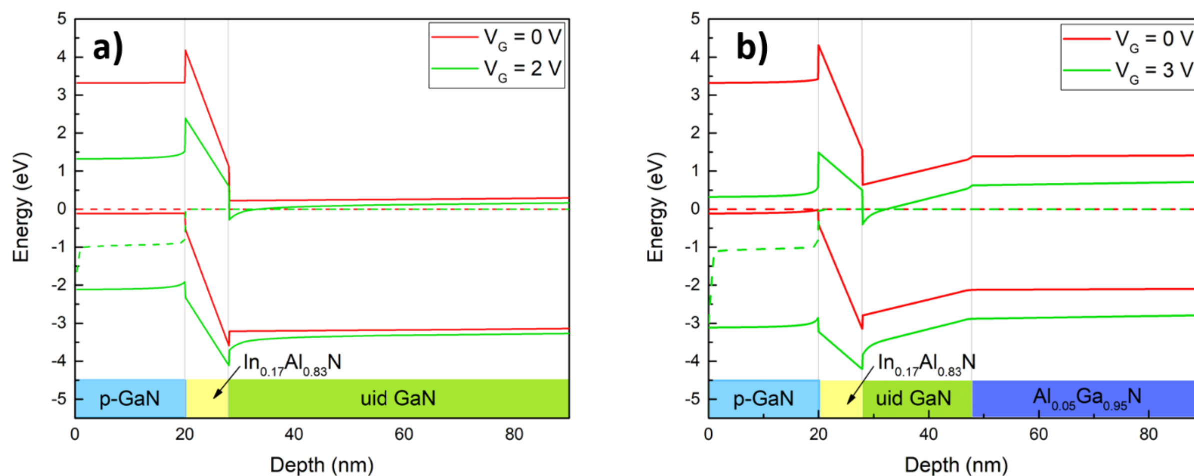

Figure 2. Simulated band structure in the gate region under equilibrium (red) and gate bias (green) conditions for the structure a) without and b) with AlGaN back-barrier.

3. DEVICE STRUCTURE AND FABRICATION

The epitaxial structures used in the fabrication of the devices are shown in Figure 3. Two E-mode epitaxial HEMT structures (Figure 3) were grown on 100 mm (111) silicon wafer with resistivity higher than 10 kΩ·cm. The HEMT structures begin with a 300 nm AlN nucleation layer, followed by AlGaN strain managing layer stack, 1100 nm high resistive GaN buffer, and a 130 nm high mobility channel GaN grown at 350 mbar. The first epitaxial structure contains a high resistive GaN layer before the GaN channel, which is replaced with a 1200 nm low Al content $Al_{0.06}Ga_{0.94}N$ back-barrier in the second structure. A 1-2 nm AlN spacer was grown prior to the 8 nm InAlN barrier and epitaxial growth was completed with 20 nm Mg-doped GaN capping layer with the hole concentration of approximately 3.0×10^{17} cm^{-3}. Using XRD fitting, the indium content of the InAlN layer extracted from was found to be 0.17. Finally, for the activation of the Mg acceptors, the wafers were annealed in an N_2+Air mixture at 830°C for 15 minutes.

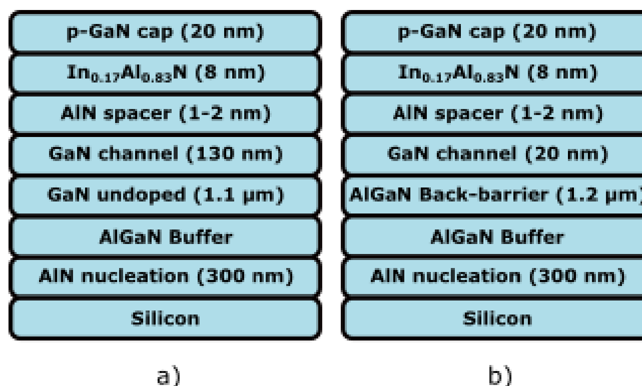

Figure 3. a) p-GaN/InAlN/GaN and b) p-GaN/InAlN/GaN/AlGaN epitaxial structures studied.

Figure 4 shows a cross section view, micrograph and SEM image of the fabricated devices. The first step of the device fabrication was to pattern and dry etch the p-GaN layer in the drain and source regions with inductively-coupled plasma reactive ion etching (ICP-RIE). Ohmic contact was metallization was done using Ti/Al/Ni/Au. Annealling was done for 30 s at 875°C under N_2 ambient. Mesa isolation was performed using BCl_3/Cl_2 gas mixture in an ICP-RIE system. Ni/Au gate electrodes and subsequently Ti/Au contact pads were deposited with e-beam evaporation. The p-GaN layer in the

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access regions was then etched away using ICP-RIE in 5-nm increments. Selective etch of p-GaN over InAlN, with a selectivity between 6 and 13.5, was achieved using BCl_3 gas at an ICP power of 100 W and RF power 30 W. Device fabrication was completed with the deposition of 200 nm SiN using plasma enhanced chemical vapor deposition (PECVD) for surface passivation. The gate length, L_G, is 1.5 µm, and the gate width, W_G, is 100 µm. The source-to-gate, L_{SG}, and the gate-to-drain, L_{DG}, spacings are 1.75 µm.

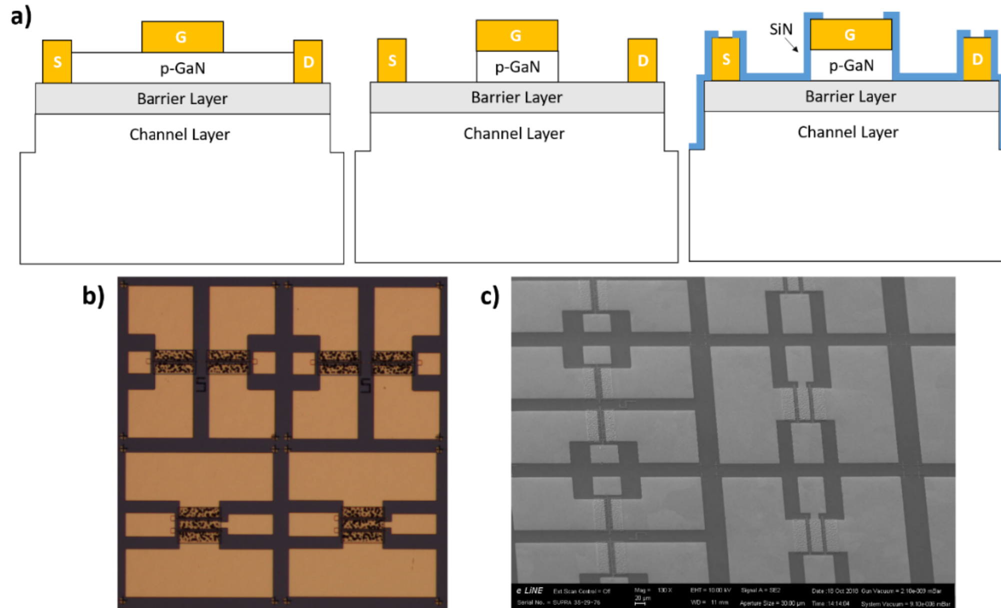

Figure 4. a) Cross sectional representation of the measured devices, b) optical micrograph and c) SEM image of the fabricated devices.

4. RESULTS AND DISCUSSION

4.1 Electrical Characterization

DC characterization was carried out using a Keysight B1500A Semiconductor Device Parameter Analyzer. Figure 5 shows the transfer characteristics as a function of gate bias at a drain bias of V_d = 10 V for the devices without and with an AlGaN back-barrier layer. Measurements were taken before the p-GaN layer in the access regions was etched, after the p-GaN was etched, and after SiN deposition. In Fig. 5(a), it can be seen that a significant amount of leakage current is present for negative gate biases. This current decreases after the p-GaN in the access region is etched and after SiN passivation. This leakage current is attributed to buffer leakage, surface defects, and conduction from the p-GaN surface in the case before the access region p-GaN is etched. With the etching of the p-GaN in the access regions, leakage from the conduction at the surface is suppressed; with the SiN passivation, the leakage from the surface defects is suppressed and only the buffer leakage remains. This remaining leakage current is suppressed by the AlGaN back-barrier, as shown in Fig. 5(b). With the p-GaN etch and SiN passivation, the transconductance of the devices also increases. The threshold voltages for the devices with and without an AlGaN back-barrier after SiN passivation are obtained as 0.5 V and 2 V, respectively, using the extrapolation of the current at the maximum linear slope. In the case of Fig. 5(a), where large leakage current is present for negative gate biases, in the bias range where the transistor is accepted to be "off", V_{th} is located at the intersection of the extrapolated leakage current and the linear extrapolation of the I_d-V_g curve.

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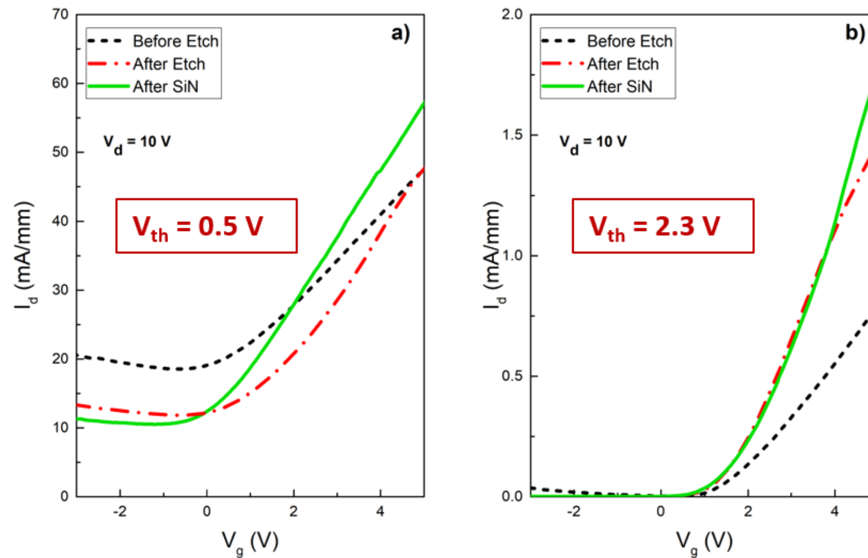

Figure 5. Measured transfer characteristics of the p-GaN/InAlN/GaN HEMT a) without and b) with an AlGaN back-barrier.

The output characteristics of the fabricated devices on the two heterostructures are shown in Fig. 6. Similarly to the transfer characteristic measurements, the devices were measured before the p-GaN etch, after the p-GaN etch, and after SiN passivation. An increase in the drain current was observed at each step. A drain current of 30 mA/mm is obtained at V_g = 5 V for the SiN passivated device without the back-barrier. For the SiN passivated device with the AlGaN back-barrier, a drain current of 2.2 mA/mm at V_g = 5 V was obtained, corresponding to an order of magnitude decrease from the standard device. The AlGaN back-barrier leads to a lower sheet carrier density and therefore higher threshold voltage and lower drain current density. The decreased current in the device with the back-barrier is a result of the higher threshold voltage and mainly the lower sheet charge density. In the standard device, Fig. 6(a), the output characteristics show signs of buffer leakage. The upward slope in the drain current seen in Figure 6(a) and the suppression of this slope in Fig. 6(b) demonstrates that the AlGaN back-barrier is effective in mitigating the buffer leakage current.

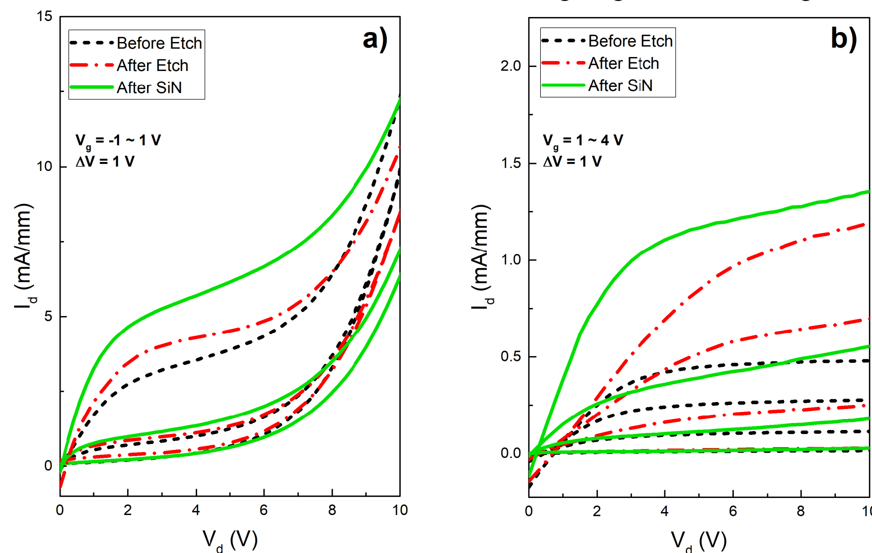

Figure 6. Measured output characteristics of the p-GaN/InAlN/GaN HEMT a) without and b) with an AlGaN back-barrier.

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The presented HEMTs in their current state show poor performance in terms of driving current and off-state leakage performance. This may evoke a false notion that p-GaN concept is inappropriate for InAlN/GaN-based devices, however, the reason for the poor performance is unoptimized epitaxy and processing. The obtained drain current density is lower than what can be achieved with the InAlN/GaN[19-21], owing to the trade-off in the annealing temperature for Ti/Al/Ni/Au Ohmic contacts between achieving low contact resistance and the degradation of the channels sheet resistance[22]. For Ti/Al/Ni/Au Ohmic contact metallization, the Ohmic contact resistance has been shown to decrease while carrier mobility has been shown to be stable up to annealing temperatures of 850°C, after which a significant degradation of the mobility accompanied by a decrease in sheet carrier density begins to occur[22]. The off-state leakage is due to poor buffer design in the epitaxy.

4.2 Leakage Characterization

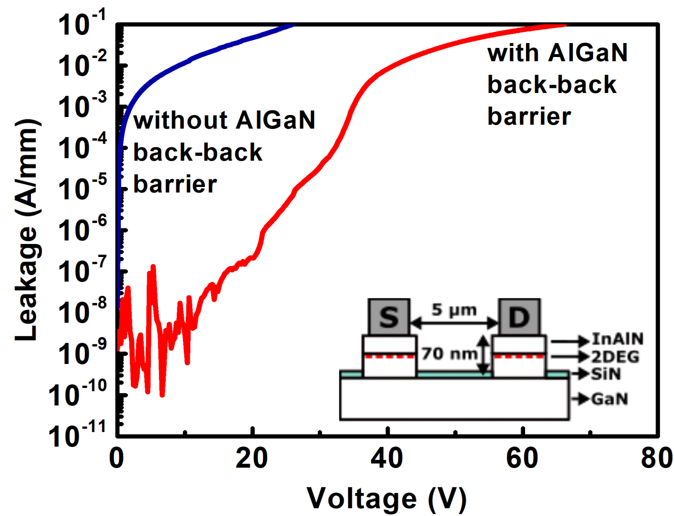

Figure 7. Leakage test structure (inset) and leakage plot.

The leakages of the SiN passivated devices were characterized using leakage test structures (Fig. 7 inset). The test structures consist of source-drain metallization separated by 5 µm with the channel removed in the mesa isolation step. The structure without an AlGaN back-barrier demonstrates leakage starting from the order of mA/mm for the measured voltage range, whereas the structure with an AlGaN back-barrier demonstrates leakage on the order of uA/mm up to 15 V and less than 1 mA/mm up to 35 V. For typical operation voltages of a transistor, an improvement of 5 to 6 orders magnitude in leakage is observed for structures utilizing an AlGaN back-barrier over devices without a back-barrier.

5. CONCLUSION

In summary, we have demonstrated normally-off p-GaN gate HEMTs based on the InAlN/GaN heterostructure and studied the effect of AlGaN back-barriers on the DC characteristics of the said device. A positive threshold voltage of +0.5 V is achieved with the p-GaN/InAlN/GaN structure which further increases to +2 V with the use of an AlGaN back-barrier. In addition, AlGaN back-barrier devices show improved buffer leakage currents by five orders of magnitude. The reduction in drain current observed for structures with AlGaN back-barrier can be compensated by means of introducing an AlN spacer layer between the barrier layer and GaN channel or increasing the Al content of the barrier layer.

ACKNOWLEDGEMENTS

This work is supported by the TUBITAK under Project No. 116F041. One of the authors (E.O.) also acknowledges partial support from the Turkish Academy of Sciences.

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