Introduction to the Special Section on Advances in Physical Design Automation

Physical design automation has been a key enabler for high-quality and cost-effective integrated circuit design. However, several recent developments in integrated circuit design have brought many new challenges to this area. Advances in integrated circuit manufacturing processes have introduced new and complicated design constraints and objectives. Also, applications in diverse design domains have brought several different new issues that were not considered by the existing tools. Moreover, continued increase in the scale of integration has made the physical design process computationally more and more intensive. All these new challenges call for advances in methodologies and algorithms in physical design automation.

This special section focuses on recent advances in physical design automation. Although the top papers published in the 2017 ACM International Symposium on Physical Design (ISPD) were especially encouraged to submit, this special section was open to the whole community. All the submissions have been reviewed rigorously following the guidelines of *the ACM Transactions on Design Automation of Electronic Systems (TODAES)*. The reviewers are experts in their fields who provided high-quality reviews for multiple revisions of the submitted papers. Through a rigorous review process, the guest editors have selected nine papers on a diverse set of topics in the field. The following is a brief introduction.

The first article is on the FPGA placement problem. Li et al. present "UTPlaceF 2.0: A High-Performance Clock-Aware FPGA Placement Engine." which won the first place in the ISPD 2017 clock-aware FPGA placement contest organized by Xilinx. To produce clock-legal yet high-quality placement solutions, they propose an iterative minimum-cost-flow–based cell assignment algorithm as well as clock-aware packing.

In the article titled "Eh?Legalizer: A High-Performance Standard-Cell Legalizer Observing Technology Constraints," Darav et al. propose to preserve the quality of the global placement in terms of routability, wire length, and timing during legalization by imposing maximum and average cell movement constraints. They accomplish this through a novel network flow-based legalization approach.

The next article investigates the layout issues of the carbon-nanotube field effect transistor (CNFET) technology. CNFET is a promising alternative to the conventional silicon-based CMOS devices for sub-10nm regime. In "Variation-Aware Global Placement for Improving Timing-Yield of Carbon-Nanotube Field Effect Transistor Circuit," Wang et al. propose novel global placement algorithms to reduce the timing yield loss caused by CNT density variation.

In "A Maze Routing-Based Methodology with Bounded Exploration and Path-Assessed Retracing for Constrained Multi-Layer Obstacle-Avoiding Rectilinear Steiner Tree Construction," Lin et al. present a rectilinear Steiner tree construction algorithm, which can efficiently handle multi-layer obstacles.

In another routing related article, "Ordered Escape Routing with Consideration of Differential Pair and Blockage," Jiao and Dong propose a min-cost multi-commodity flow (MMCF) algorithm to solve the ordered escape routing problem for PCBs. Their methodology achieves good routability, wire length, and runtime.

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The next article tackles analog design automation, which has always been considered an important but very difficult problem. In the article titled "Routable and Matched Layout-styles for Analog Module Generation," Liu et al. present two novel automatic generation methods for analog layout that are shown to be effective in terms of routability, matching property, and layout area.

As designs continue to grow in size and complexity, timing analysis has shifted from flat to hierarchical. Lee and Jiang have developed a timing macro model for hierarchical timing analysis, which has high model accuracy and small model size. Their work is presented in "iTimerM: A Compact and Accurate Timing Macro Model for Efficient Hierarchical Timing Analysis."

For the purpose of enhancing the efficiency of the overall power delivery system, the approach of connecting multiple on-chip voltage regulators to the same power grid has recently attracted significant attention. In the article titled "Optimal Allocation of LDOs and Decoupling Capacitors within a Distributed On-Chip Power Grid," Sadat et al. propose a mixed integer nonlinear programming formulation to optimize the number, size, and location of parallel low-dropout (LDO) regulators and intentional decoupling capacitors.

The final article is about hardware security. In the article titled "Reverse Engineering Digital ICs through Geometric Embedding of Circuit Graphs," Cakir and Malik present an automated approach to reverse-engineer manufactured netlists to help identify malicious insertions.

This special section covers many important directions in physical design research. However, new challenges will keep emerging as long as the manufacturing technologies, design requirements, and applications evolve. We hope that this special section will inspire more research in the field of physical design automation.

We would like to thank all the authors who submitted papers to this special section. We are also grateful to the reviewers for their comprehensive and rigorous reviews and the valuable feedback they provided. Finally, we would like to thank all the staff members of *IEEE TODAES,* including the editors-in-chief, administrative, and editorial staff members for helping us develop this special section.

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