IMPROVED WILKINSON POWER DIVIDER STRUCTURES FOR MILLIMETER-WAVE APPLICATIONS

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By

Batuhan Sütbaş

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We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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M.S. in Electrical and Electronics Engineering
Advisor: Abdullah Atalar
January 2019

Communication systems, radars, electronic warfare and space applications desire integrated circuits with higher operating frequencies. Working at the millimeter-wave region increases data rates, provides a more efficient use of the spectrum and enables smaller products. Power dividers are used as building blocks for such applications to split and combine RF signals. Wilkinson power divider is one of the most commonly used topology, providing high return loss and isolation with low insertion loss. However, it occupies valuable chip area, has a limited bandwidth, requires accurate modeling and precise fabrication. In addition, the layout becomes complicated for three or more outputs and cannot be realized on a planar circuit. This work presents three techniques to address the drawbacks of the original Wilkinson divider. The first structure achieves a compact size without bandwidth degradation and provides additional physical isolation at the output. The second divider improves the bandwidth of operation and increases tolerance to sheet resistance variance, enabling robustness and higher yields. The third technique simplifies the layout of three-way dividers and allows a planar fabrication technology. The proposed structures are analyzed using even-odd mode analysis and design equations are derived. Three high performance dividers with 30 GHz center frequency are designed employing the developed methods. The circuits are realized using GaN based coplanar waveguide and microstrip monolithic microwave integrated circuit technology. Experimental results demonstrate good agreement with theory and simulations, proving that the presented improvements could be useful in future millimeter-wave RF applications.

Keywords: Wilkinson power divider, coplanar waveguide, microstrip, millimeter-wave, *Ka*-band, integrated circuit, compact, wide band, process independent, sheet resistance, tolerance, planar, three-way.

ÖZET

MİLİMETRE-DALGA UYGULAMALARI İÇİN GELİŞTİRİLMİŞ WİLKİNSON GÜÇ BÖLÜCÜ YAPILARI

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İletişim sistemleri, radarlar, elektronik harp ve uzay uygulamaları, daha yüksek frekanslarda çalışan entegre devreler istemektedir. Milimetre dalga bandında çalışmak, veri hızını artırmakta, spektrumu daha verimli kullanmayı sağlamakta ve daha küçük ürünler ortaya çıkarmaktadır. Güç bölücüler bu tür uygulamalarda RF sinyalleri bölmek ve birleştirmek için kullanılan yapı taşlarındandır. Wilkinson güç bölücü düşük kayıpla yüksek yansıma kaybı ve izolasyon sağladığı için en yaygın olarak kullanılan topolojilerden biridir; ama çok yer tutar, sınırlı bir bantta çalışır, isabetli bir model ve kusursuz üretim gerektirir. Ayrıca, üç ya da daha çok çıkış için serim karmaşıklaşır ve düzlemsel bir devre üzerinde gerçeklenemez. Bu çalışma, Wilkinson bölücüsünün sorunlarını çözmeye yönelik olarak üç teknik sunmaktadır. Birinci yapı, bandı daraltmadan devre alanını küçültmekte ve çıkıştaki fiziksel izolasyonu artırmaktadır. İkinci bölücü, çalışma bandını genişletmekte ve tabaka direncindeki değişimlere toleransı artırarak dayanıklılığı ve çalışma oranını iyileştirmektedir. Üçüncü teknik, üç kollu bölücülerin serimini sadeleştirmekte ve düzlemsel üretim yöntemleri ile üretilebilmelerini sağlamaktadır. Yapılar, eşzıt mod analiziyle çözülmüş ve tasarım denklemleri çıkarılmıştır. Geliştirilen yöntemler kullanılarak 30 GHz merkez frekanslı ve yüksek performanslı üç bölücü tasarlanmıştır. Tasarlanan devreler GaN tabanlı eşdüzlemli dalga kılavuzu ve mikroşerit temelli MMIC teknolojisi kullanılarak üretilmiştir. Deneysel sonuçlar, teori ve benzetimler ile uyuşmakta ve sunulan yöntemlerin gelecek milimetre dalga RF uygulamalarında yararlı olabileceğini göstermektedir.

Anahtar sözcükler: Wilkinson güç bölücü, eşdüzlemli dalga kılavuzu, mikroşerit, milimetre-dalga, *Ka*-bant, entegre devre, yoğun, geniş bantlı, üretimden bağımsız, tabaka direnci, tolerans, düzlemsel, üç yönlü.

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Chapter 1

Introduction

Power dividers are typically three-port devices widely used in power amplifiers, mixers and phased arrays to split and combine RF signals. Ideally, a power divider divides the input signal into two output signals with equal amplitude and equal phase without additional insertion loss. All three ports are matched to the reference impedance.

However, basic network theory shows that a three-port device composed of only isotropic materials cannot be passive, perfectly matched at all ports and lossless simultaneously [1]. In order to prove this statement, assume that the opposite of it is true, and a three-port power divider with a scattering matrix $[S]$ achieves the three properties at the same time.

$$[S] = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \tag{1.1}$$

Since the device is passive and does not contain anisotropic materials, it is a reciprocal network, and the S-matrix must be symmetric with $S_{12} = S_{21}$, $S_{13} = S_{31}$ and $S_{23} = S_{32}$.

All diagonal entries of the S-matrix must be 0, because all three ports are matched to the corresponding port impedances, then $S_{11} = S_{22} = S_{33} = 0$.

If the network is lossless, it implies that the S-matrix is unitary with $SS^* = I$, where I is the identity matrix. Combining this with the previous results, the following conditions are satisfied.

$$|S_{12}|^2 + |S_{13}|^2 = 1 \tag{1.2}$$

$$|S_{12}|^2 + |S_{23}|^2 = 1 \tag{1.3}$$

$$|S_{13}|^2 + |S_{23}|^2 = 1 \tag{1.4}$$

$$S_{12}^* S_{13} = 0 \tag{1.5}$$

$$S_{12} S_{23}^* = 0 \tag{1.6}$$

$$S_{13}^* S_{23} = 0 \tag{1.7}$$

At least two of the entries (S_{12}, S_{13}, S_{23}) must be zero for (1.5)–(1.7) to hold. However, in that case, at least one of (1.2)–(1.4) fails to be true. This contradiction establishes the fact that it is impossible to build a three-port passive, matched and lossless device using only isotropic materials.

In 1960, Ernest Wilkinson invented the famous Wilkinson power divider [2] which achieves perfect input and output port matching and complete isolates the output signals at the center frequency. The Wilkinson power divider uses two quarter-wave length transmission lines with characteristic impedances of $\sqrt{2}$

times the reference impedance (Z_0) between the input port and the two output ports in order to achieve port matching. The device obtains port isolation using a resistor which bridges the output ports with a resistance of $2Z_0$. When an RF signal enters the input port, two RF signals with equal phase and equal amplitude appear at the output ports. Thanks to the bilateral symmetry of the Wilkinson power divider, there is no current flow through the resistor, because the output signals at the each end of it are identical, and the device works without any additional loss. However, when any of the two output ports is excited, half of the total power reaches the input port, while the other half is dissipated in the isolation resistor. The device avoids the impossibility of being a passive, matched and lossless three-port network by having a 3 dB loss when it is excited in the opposite direction. Nevertheless, when the two output ports are excited simultaneously with two identical signals, the network acts as a combiner and the total power is delivered to the input port without loss.

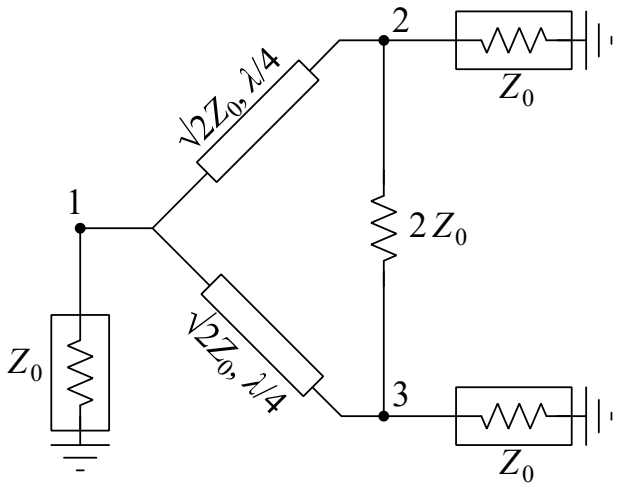


Figure 1.1: Schematic of the original two-way Wilkinson power divider structure.

Although the Wilkinson power divider has been desirable as a part of microwave circuits and systems for many years since its invention, it has the following drawbacks.

- The circuit occupies valuable chip area due to its quarter-wave length arms.
- It is difficult to avoid coupling between the transmission line arms since they need to be separated by a single resistor at their output terminals.

- The separation that a single resistor provides is not enough to maintain physical spacing and isolation between the output ports.
- Quarter-wave length arms of the divider limit the operational bandwidth.
- Circuit performance degrades quickly with variations in the value of the isolation resistor.
- Three-way version of the power divider requires a complicated layout because the three isolation resistors cannot be realized on a planar circuit.
- It is difficult to construct a layout for the three-way version of the power divider with sufficient spacing between the transmission line arms since the lines are required to come close for bridging resistors.

This work presents improved structures for the Wilkinson power divider to overcome the aforementioned problems. The modified topologies are analyzed using S-parameter relations and even-odd mode analysis technique. The proposed methods are employed to design three high performance dividers at Ka-band. The designs are implemented using gallium nitride (GaN) based coplanar waveguide (CPW) and microstrip (MS) monolithic microwave integrated circuit (MMIC) technology. All of the fabricated devices are measured and comparison with the simulation results are presented at the end of each chapter. The experimental results prove that the proposed methods are applicable at mm-wave frequencies.

Chapter 2 explores the trade-off between the size and the bandwidth of the Wilkinson power divider. A power divider structure with compact size and wide bandwidth is introduced. Size of this structure can be arbitrarily miniaturized by loading the transmission line arms capacitively while the associated bandwidth degradation is compensated with additional circuit in the isolation network.

In Chapter 3, sheet resistance dependence of the Wilkinson power divider performance is investigated. Improved isolation network of the proposed power divider structure achieves wide bandwidth and process independence at the same time. This increases the robustness of the design and allows the devices to be

placed outside the normally unusable edge exclusion zone on the photomask where sheet resistance variance can be very high.

Chapter 4 analyzes a planar three-way power divider structure which uses only two isolation resistors. Planar devices are easier to model and fabricate making them more reliable. Layout of the three-way Wilkinson power divider is simplified as the power division is obtained by line coupling. Also, since the topology inherently needs the transmission line arms close to each other, the spacing between them is not an issue anymore.

Chapter 2

A Compact Size Power Divider Structure with Wide Bandwidth

Ideally, the Wilkinson power divider provides perfect port matching and output isolation at the design center frequency. However, it occupies valuable chip area in MMICs due to its quarter-wave length arms. Studies have shown that the circuit size can be reduced by capacitive [3, 4] and inductive [5] line loading or by replacing the transmission lines with their lumped element equivalents [6]. More compact design topologies reduce the 36% fractional bandwidth for 20 dB return loss and isolation levels of the original divider. On the other hand, researchers obtained improved bandwidth capability by increasing the number of sections in the Wilkinson power divider [7] or by modifying the isolation network [8]. However, divider topologies for wide band applications with higher fractional bandwidth consume more chip area. Design of a small size and wide band power divider is difficult due to the trade-off between the size and the bandwidth of power dividers.

The proposed two-way power divider structure not only reduces the circuit size, but also compensates for the related bandwidth degradation. The improvement in the compact size and wide bandwidth trade-off is obtained by capacitive line loading and a series symmetrical RLC resonant circuit at the isolation network.

2.1 Analysis and Design Equations

Proposed network for the modified Wilkinson power divider and its even-odd mode equivalents [9] are shown in Fig. 2.1 and Figs. 2.2–2.3. Shunt capacitors are added at the input and output ports to decrease the length of the transmission line arms. A series RLC resonant circuit is used as the isolation network. The inductor and capacitor values in the isolation network, L_{iso} and C_{iso}, are optimized to improve the overall bandwidth performance. The series RLC circuit is kept symmetrical to preserve the bilateral symmetry of the overall structure. Component values for perfect port matching and isolation at the design center frequency are found using even-odd mode analysis.

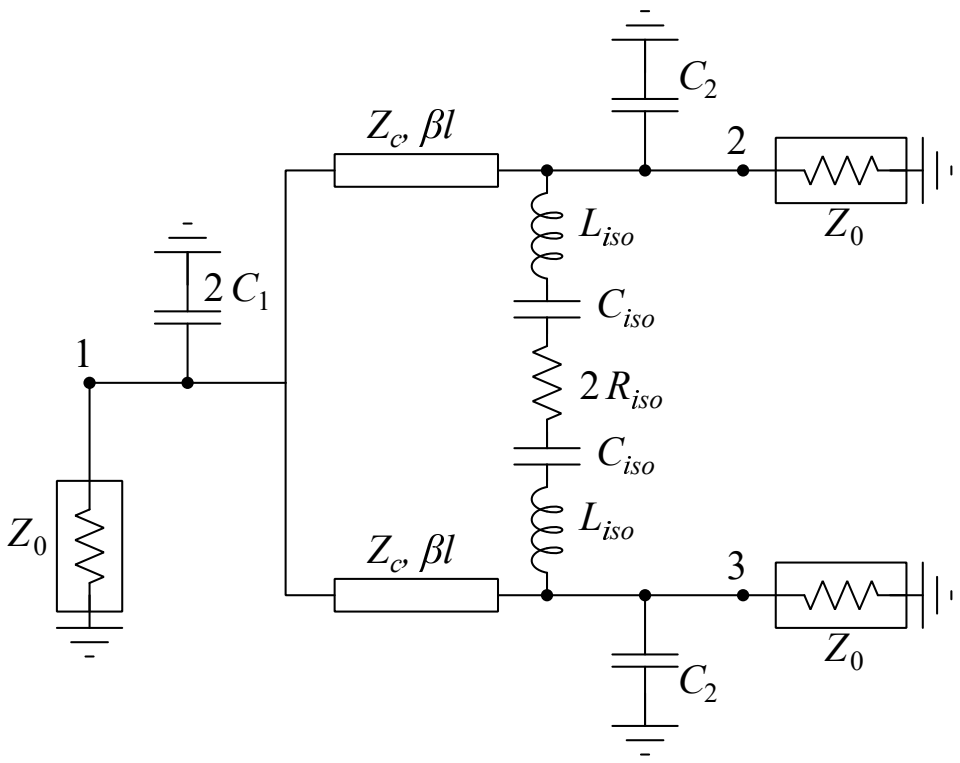


Figure 2.1: Schematic of the proposed compact Wilkinson power divider structure with the electrical design parameters.

In [10], it is shown that, in order to obtain input/output reflection coefficients and isolation better than a desired level of δ, it is sufficient to design for even-mode (Γ_e) and odd-mode (Γ_o) reflection coefficients better than δ. Therefore, the even-mode reflection coefficient of the circuit given in Fig. 2.2 should satisfy

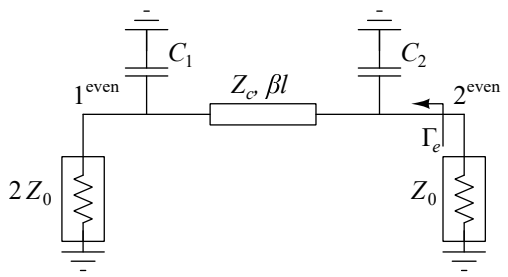


Figure 2.2: Even-mode analysis for the proposed compact divider.

$$|\Gamma_e| = \left|\frac{Z_e - Z_0}{Z_e + Z_0}\right| < \delta \tag{2.1}$$

$$Z_e = Z_c \frac{(2Z_0 /\!/ Z_{C_1}) + jZ_c \tan(\beta l \hat{f})}{Z_c + j(2Z_0 /\!/ Z_{C_1}) \tan(\beta l \hat{f})} /\!/ Z_{C_2} \tag{2.2}$$

at the bandwidth of interest. Similarly, the odd-mode reflection coefficient of the circuit shown in Fig. 2.3 should satisfy

$$|\Gamma_o| = \left|\frac{Z_o - Z_0}{Z_o + Z_0}\right| < \delta \tag{2.3}$$

$$Z_o = jZ_c \tan(\beta l \hat{f}) /\!/ Z_{C_2} /\!/ \frac{2\pi \hat{f} f_0 R_{iso} C_{iso} + j(4\pi^2 \hat{f}^2 f_0^2 L_{iso} C_{iso} - 1)}{2\pi \hat{f} f_0 C_{iso}} \tag{2.4}$$

Here, Z_{C_1} and Z_{C_2} are the complex impedances of the capacitors C_1 and C_2. Z_c is the characteristic impedance and βl is the electrical length of the divider arm at the design center frequency, f_0. Also, $\hat{f}$ is the normalized frequency f/f_0 and Z_0 is the characteristic impedance of the system.

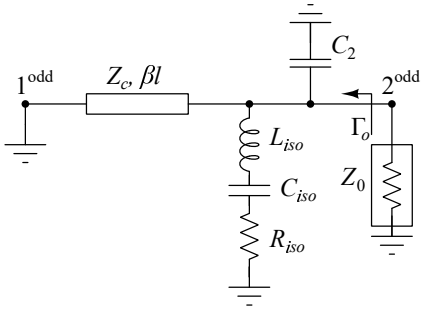


Figure 2.3: Odd-mode analysis for the proposed compact divider.

The required component values can be found analytically for zero even and odd mode reflection coefficients at f_0. Admittance parameters are used to simplify the derivation for design variables. For perfect port matching in the odd-mode equivalent circuit

$$\frac{1}{Z_0} = Y_0 = j2\pi f_0 C_2 + \frac{1}{R_{iso}} - j\frac{1}{Z_c \tan \beta l} \tag{2.5}$$

and equating the real and imaginary parts separately, value of the isolation resistor, R_{iso} and a relation between Z_c and C_2 are found.

$$R_{iso} = Z_0 \tag{2.6}$$

$$C_2 = \frac{1}{2\pi f_0 Z_c \tan \beta l} \tag{2.7}$$

Similarly, for perfect port matching in the even-mode equivalent circuit

$$\frac{1}{Z_0} = Y_0 = jC_2 2\pi f_0 + Y_{in} \tag{2.8}$$

$$Y_{in} = Y_c \frac{Y_0 + j4\pi f_0 C_1 + j2Y_c \tan \beta l}{2Y_c - 4\pi f_0 C_1 \tan \beta l + jY_0 \tan \beta l} \tag{2.9}$$

and solving the admittance equation, another relation between $Z_c = 1/Y_c$ and the capacitor values, C_1 and C_2 is found. Separating the equation into real and imaginary parts, two new equations are obtained

$$\mathrm{Re}(Y_{in}) = Y_c \frac{2Y_0 Y_c + 2Y_0 Y_c \tan^2 \beta l}{4(Y_c - 2\pi f_0 C_1 \tan \beta l)^2 + {Y_0}^2 \tan^2 \beta l} = Y_0 \tag{2.10}$$

$$\mathrm{Im}(Y_{in}) = Y_c \frac{({Y_0}^2 + 2\pi {f_0}^2 C_1^2 - 4{Y_c}^2)\tan\beta l - 8\pi f_0 C_1 Y_c(1-\tan^2\beta l)}{4(Y_c - 2\pi f_0 C_1 \tan\beta l)^2 + {Y_0}^2\tan^2\beta l} = 2\pi f_0 C_2 \tag{2.11}$$

and solving them together, a single analytical result is calculated. The capacitor values and the line impedance in terms of βl are found as

$$Z_c = \frac{\sqrt{2}Z_0}{\sin\beta l} \tag{2.12}$$

$$C_1 = C_2 = \frac{\sqrt{2}\cos\beta l}{2\pi f_0 Z_0} \tag{2.13}$$

Also, the resonance frequency of L_{iso} and C_{iso} at the isolation network is f_0 and

$$L_{iso}C_{iso} = \frac{1}{4\pi^2 f_0^2} \tag{2.14}$$

2.2 Circuit Design

The component values derived in the previous section can be optimized to achieve S-parameter levels better than δ in a bandwidth of BW, as perfect port matching at the center frequency is unnecessary. Fig. 2.4 compares the obtainable fractional bandwidth ($FBW = BW/f_0$) using capacitive loading with and without a series RLC compensation network. Points on the $\beta l = 90$ degrees line with only capacitive loading indicate the original Wilkinson power divider performance, the 20 dB return loss and isolation bandwidth is 36%. The line length can be arbitrarily shortened using capacitive line loading, but the bandwidth becomes limited. The additional circuitry in the isolation network boosts the divider bandwidth and the drawback of building a small circuit is avoided. For good performance balanced amplifiers, one needs dividers with δ values of 0.1 or even smaller [11]. Therefore,

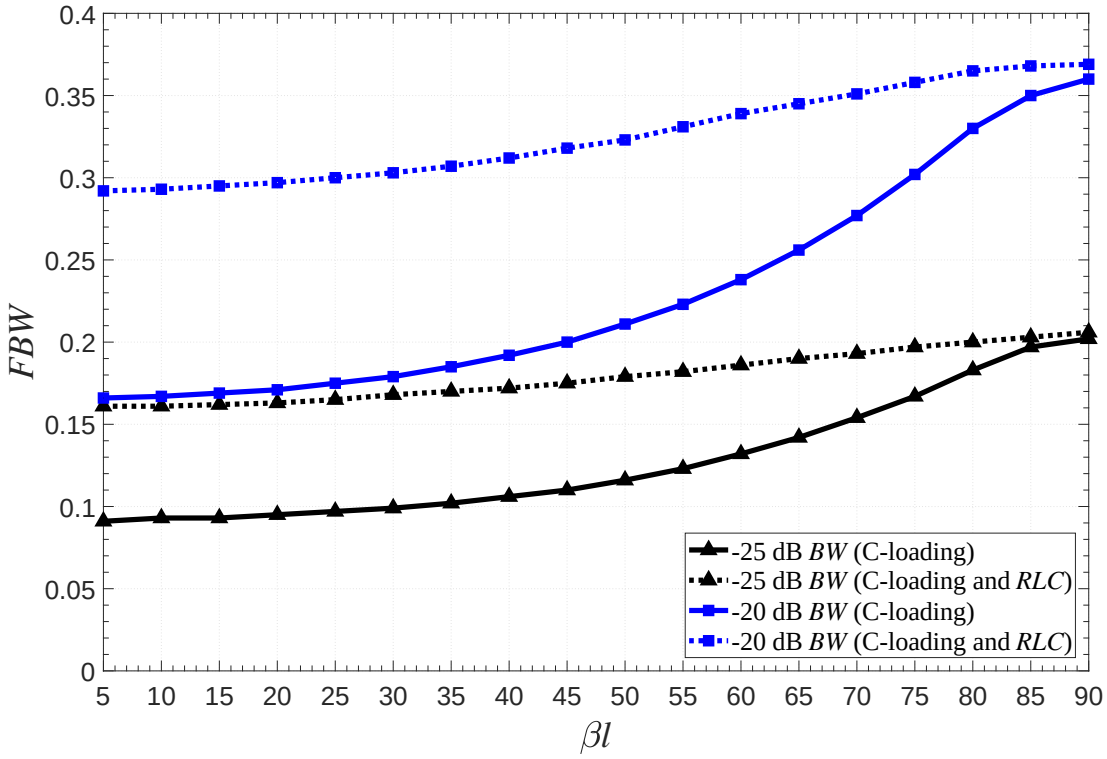


Figure 2.4: Fractional bandwidth capability of the Wilkinson power divider as a function of the electrical length of the capacitively loaded transmission line arm with and without series RLC compensation circuit for 20 dB ($\delta = 0.1$) and 25 dB ($\delta = 0.056$) return loss and isolation levels.

the goal of the miniaturized prototype divider is to achieve 20 dB return loss and isolation at the operational bandwidth.

A power divider at Ka-band with 30 GHz center frequency is designed to demonstrate the presented technique. The electrical length of the transmission line arm is reduced to $\lambda/9$ (40 degrees) which corresponds to a length reduction of 55% with a characteristic impedance of $Z_c = 90\,\Omega$ after optimization for bandwidth. Fig. 2.4 shows that for the chosen size reduction ratio, using the two techniques together instead of using line loading only increases the 20 dB return loss and isolation bandwidth from 17% to 32% which is a key improvement for small size and wide band power dividers. (2.12) shows that if a higher reduction ratio is desired, higher and infeasible Z_c values are necessary. However, additional structures can be used to artificially increase the line impedance for ultra compact dividers.

The original Wilkinson power divider requires the transmission line arms to come closer at their output ends as they need to be connected to the isolation resistor. This becomes an issue because physical isolation between output ports cannot be maintained and line coupling is problematic especially at high frequency designs. It is possible to add extra transmission line segments with phase θ_{ext} between the output ports and the isolation resistor to overcome this problem. However, this limits the bandwidth unless the transmission line arms are also extended by the same length, θ_{ext} which increases the total circuit area [12]. Another approach is to place the isolation network closer to the input port so that the output ports can have additional physical isolation [13]. However, in that case, divider bandwidth and return losses degrade significantly. The proposed structure avoids the complications related to output port isolation as the additional LC resonant circuit in the isolation network provides the necessary spacing. Thus, the undesired and unpredictable coupling effect between the quarter-wave length arms which becomes more unforgiving at higher frequencies is mitigated without increasing the circuit area.

The CPW transmission line arms of the divider design are 13 µm wide with 52 µm gap to the ground plane. A metal-insulator-metal (MIM) capacitor is used to realize the shunt capacitor C_1 at the input port, whereas the shunt capacitors C_2 at the output ports are obtained by parasitic capacitances of the tee junctions. Distance between the capacitive load C_1 and the node of the tee junction is 84 µm ($\lambda/52$) and directly affected by the ground spacing of the CPW line. At higher operating frequencies, electrical length of this distance becomes significant. In that case, it might be better to use a cross junction instead, and place C_1 as close as possible to the loaded line. Air-bridges are concentrated at tee junctions to prevent undesired fringing effects. Inductive effect in the isolation network is achieved by using transmission lines in order to provide additional physical distance between the output ports. This becomes especially useful in balanced amplifiers when power is split to two transistors, because the transistors need to be reasonably separated, longer than a single 100 Ω resistor allows. The overall circuit size is less than 0.54 mm × 0.88 mm including the measurement pads. Layout design of the divider is shown in Fig. 2.5.

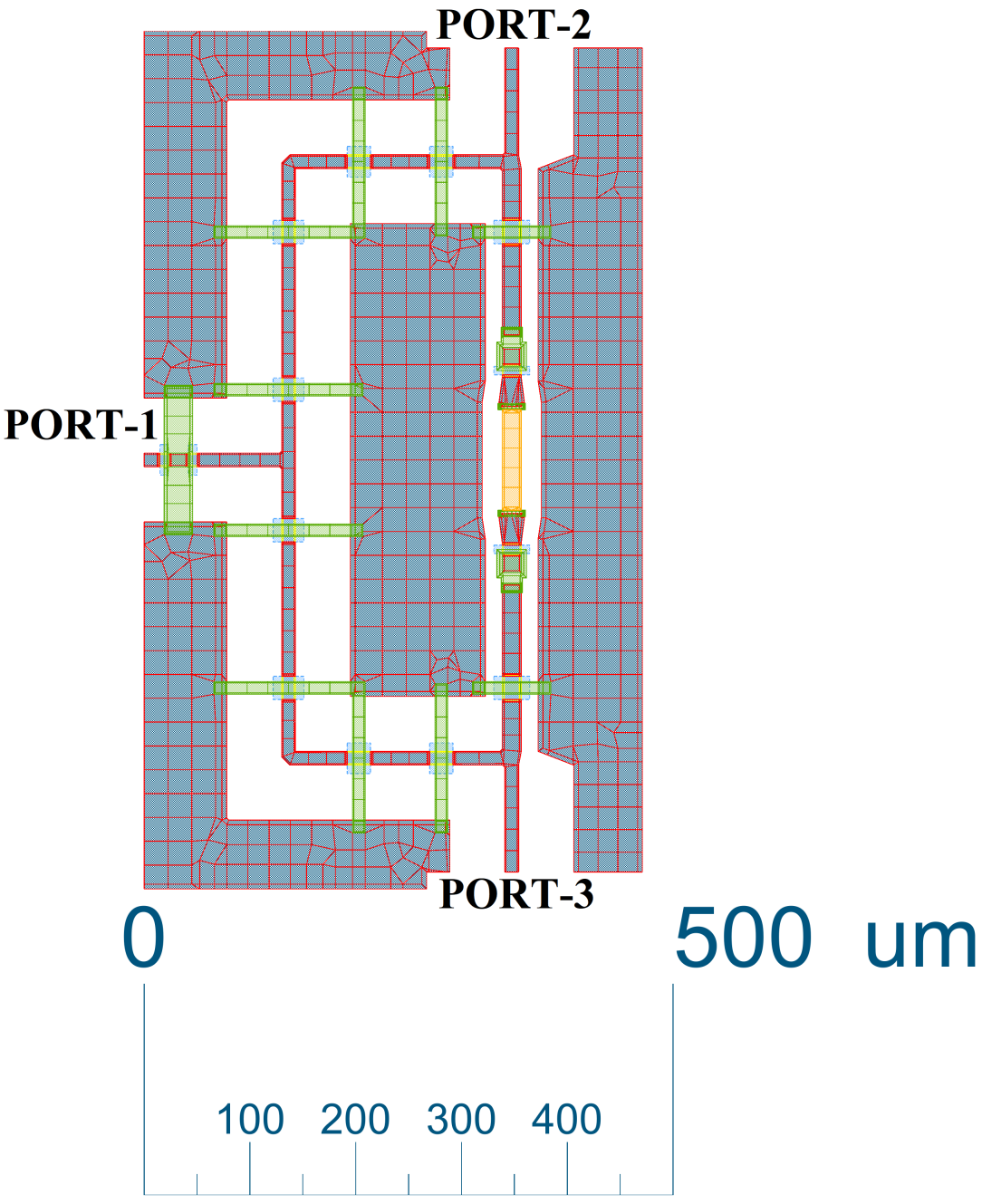


Figure 2.5: Layout of the compact two-way divider meshed for EM simulation.

2.3 Fabrication and Measurement Results

The modified compact and wide band Wilkinson power divider design at Ka-band is fabricated using a coplanar waveguide MMIC process with two metal layers. SiC substrate thickness is 300 µm and the dielectric constant (ϵ_r) is 9.66. Thin film resistors are formed using Ni–Cr with a sheet resistance of 15 Ω/□. MIM capacitors use Si_xN_y as an insulator with a dielectric constant of 7.35. Fig. 2.6 shows the microscope image of the fabricated divider.

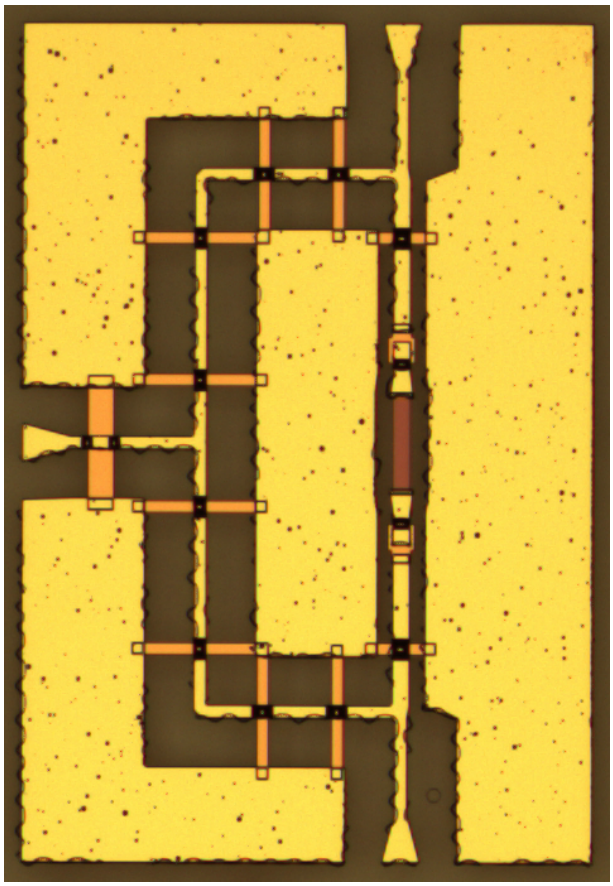


Figure 2.6: Microscope photograph of the compact two-way divider.

SEM image of the air-bridges across the divider arm is shown in Fig. 2.7. The air-bridge height is approximately 4 µm with 12 µm length and 5 µm open-end gap width at either side. Another image of the isolation network in Fig. 2.8 shows the resistor dimensions and the additional air-bridges used at the series capacitors to provide a smooth metal path preventing possible cracks and increasing yield.

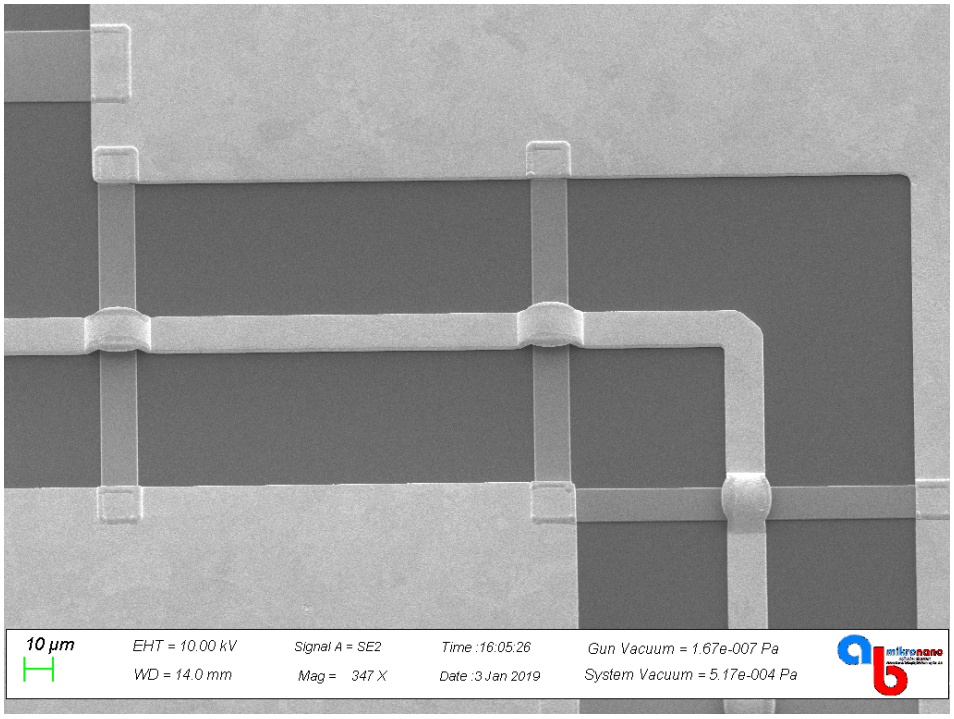


Figure 2.7: A scanning electron microscope image of the air-bridges.

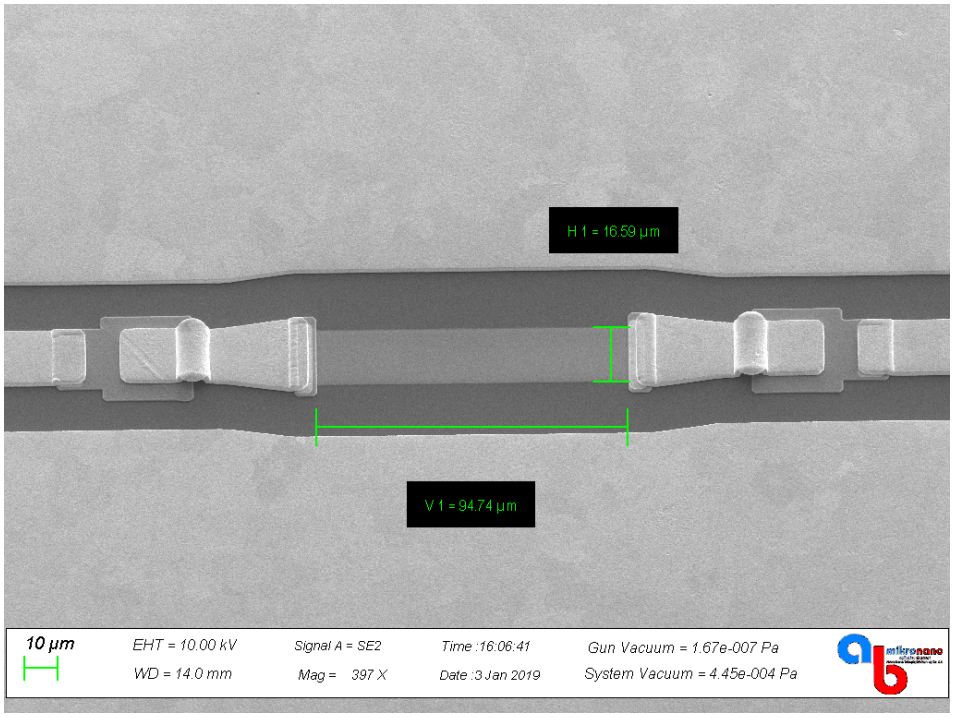


Figure 2.8: A scanning electron microscope image of the isolation network.

3-port on-wafer calibration and measurements are performed using Cascade[1] RF wafer probe station, GGB[2] GSG150 picoprobes and R&S[3] ZVA40 vector network analyzer. The simulated[4] and measured S-parameter values of the power divider are shown in Figs. 2.9–2.12, demonstrating the good agreement between them. The divider achieves 26 dB input and output port matching and 24 dB isolation with 0.2 dB extra insertion loss at the design center frequency of 30 GHz. The measured input and output return losses are better than 20 dB from 25.7 GHz to 33.9 GHz. The measured isolation between output ports is at least 20 dB and the measured extra insertion loss is less than 0.3 dB from 27.2 GHz to 35.5 GHz. The amplitude imbalance and the phase imbalance at the output ports across the operational bandwidth are less than 0.1 dB and 1.3°, respectively. The overall 20 dB performance is achieved from 27.2 GHz to 33.9 GHz and the operational fractional bandwidth is 22%. A comparison of this work with recent studies at high frequencies is tabulated in Table 2.1.

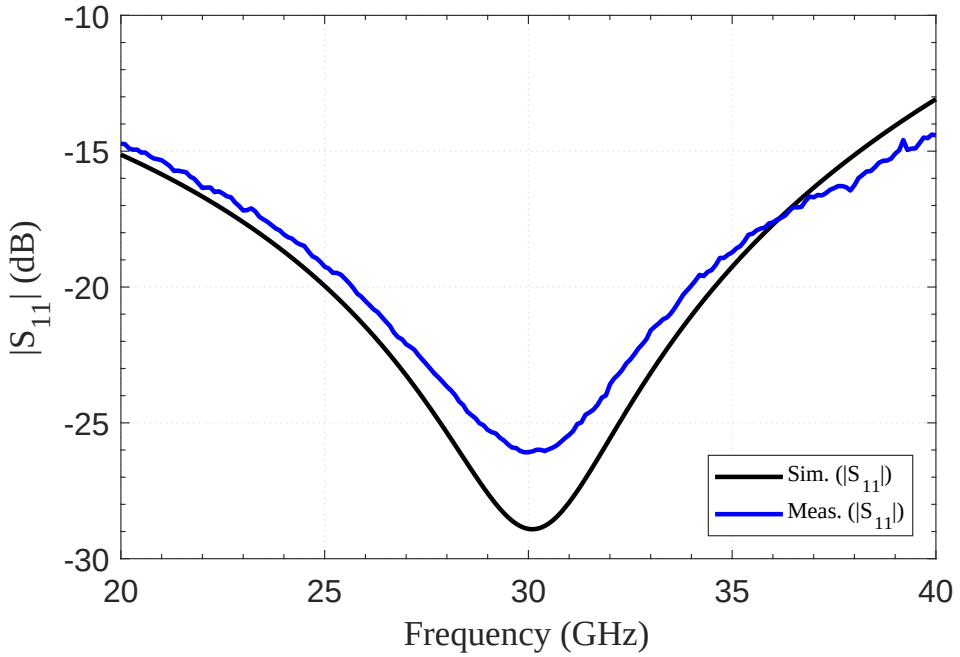


Figure 2.9: Simulated and measured parameters associated to input reflection coefficient of the compact divider as a function of frequency.

[1]Cascade Microtech, Inc., Beaverton, OR 97008, USA
[2]GGB Industries, Inc., Naples, FL 34104, USA
[3]Rohde & Schwarz GmbH & Co. KG, Munich, Germany
[4]ADS 2016.01, Keysight Technologies, Inc., Santa Rosa, CA 95403, USA

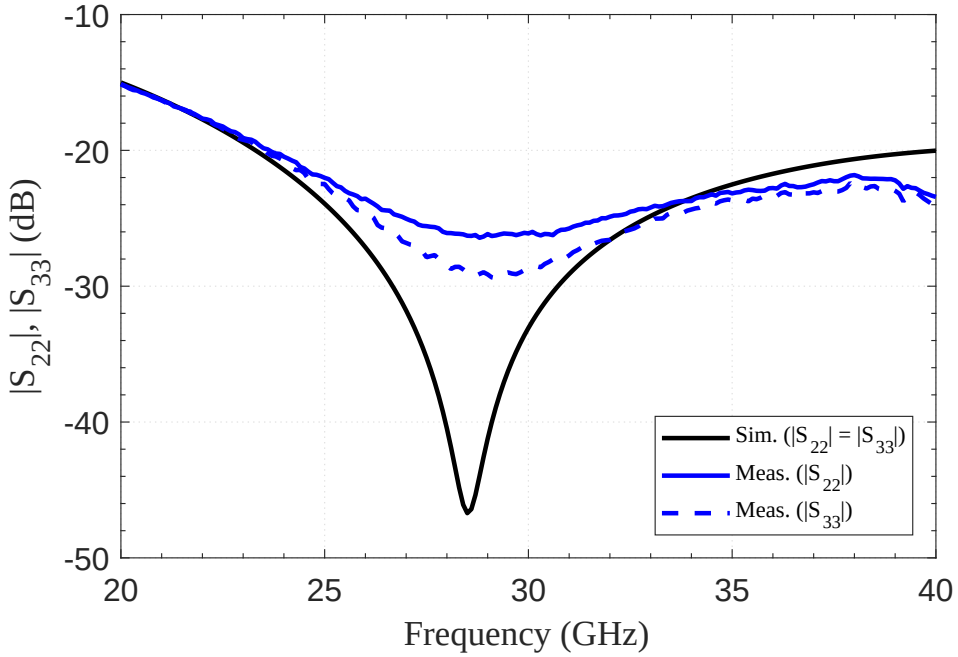


Figure 2.10: Simulated and measured parameters associated to output reflection coefficients of the compact divider as a function of frequency.

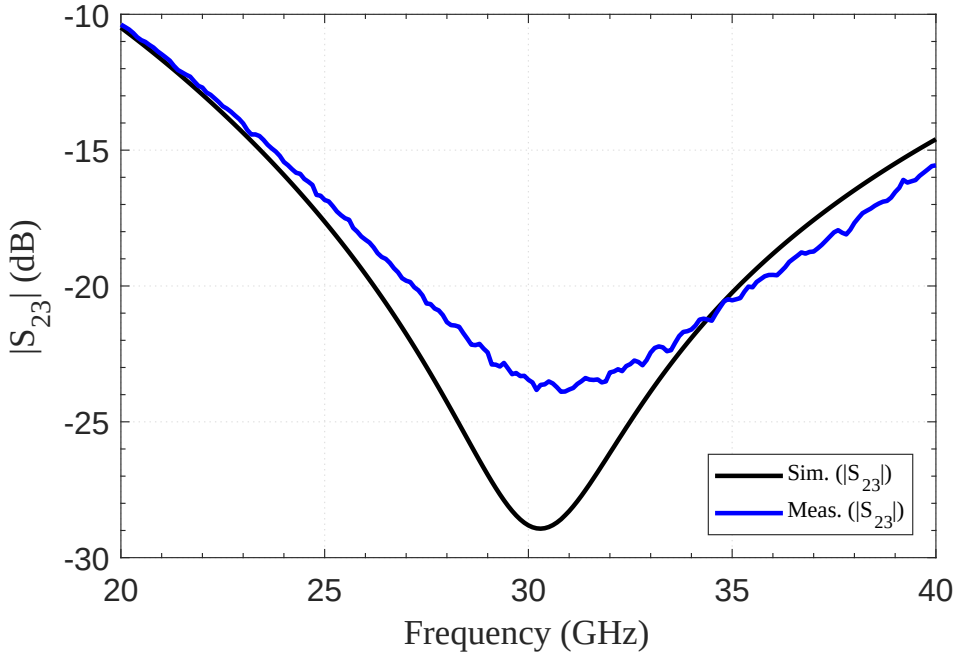


Figure 2.11: Simulated and measured parameters associated to isolation of the compact divider as a function of frequency.

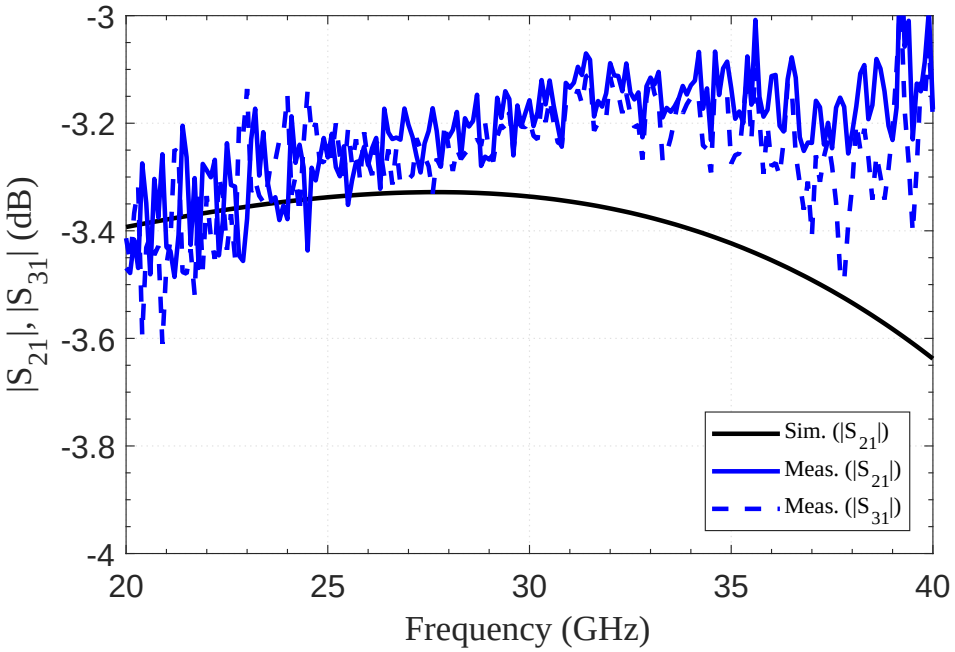


Figure 2.12: Simulated and measured parameters associated to insertion losses of the compact divider as a function of frequency.

Table 2.1: Size and bandwidth comparison of two-way power dividers

Reference	**Technology**	**Topology**	**Length**	**Loss**[a] **(decibel)**	$\boldsymbol{f_0}$ **(GHz)**	$\boldsymbol{\delta}^b$ **(decibel)**	$\boldsymbol{FBW}^c$ **(%)**
[3]	CPW HRS[d]	Capacitive loading	$\lambda/6$	0.5	10	-15	22
[4]	CPW MMIC	Capacitive loading	$\lambda/8$	0.4	10	-14	18
[8]	MS PCB	RLC isolation	$\lambda/4$	0.6	4	-18	36
[13]	MS MMIC	Modified isolation	$\lambda/4$	0.5	30	-18	21
[12]	MS MMIC	Modified isolation	$\lambda/3$	0.3	60	-11	11
This work	CPW MMIC	Capacitive loading and RLC isolation	$\lambda/9$	0.2	30.5	-20	32

[a]Extra insertion loss
[b]Measured return loss and isolation levels in the FBW of this work (22%)
[c]Theoretical fractional bandwidth (FBW) for -20 dB return loss and isolation levels
[d]High resistivity silicon

Chapter 3

A Power Divider Structure Tolerant to Resistance Variance

The Wilkinson power divider ideally provides matched conditions at all ports and high isolation between the output ports with low insertion loss. The Gysel power divider [14] is another popular divider structure with the same attractive properties and has an additional high output power handling capability at the cost of increased circuit area. Recent works show that combining the Wilkinson power divider and the Gysel power divider isolation networks increases the operational bandwidth [15]. However, for all divider structures, the high performance and bandwidth is dependent on the accuracy of the resistors. Researchers aim to minimize the sheet resistance variance to obtain high performance dividers in integrated circuits by optimizing the fabrication processes [16, 17]. Although many other structures in the integrated circuits also benefit from a more stable fabrication process, it is a highly expensive and time-consuming solution without tackling the core issue of the structures. The more general solution is to make the design structures tunable after fabrication and measurements or to have an inherent process independence. The former is difficult in the case of integrated circuits, whereas the latter can be achieved utilizing the local uniformity of sheet resistance in fabricated wafers.

In this chapter, a power divider structure is introduced to achieve a wide band divider with tolerance to high sheet resistance variances. The presented method not only adds robustness to the divider, but also the normally unusable edge exclusion zone becomes available for devices, this wasted area can be as high as 8% of the useful area for a 3-inch wafer with a typical 3 mm edge exclusion.

3.1 Analysis and Design Equations

Proposed network for the sheet resistance tolerant power divider is shown in Fig. 3.1. The isolation network resembles a combination of the Wilkinson and Gysel divider isolation networks. The divider requires one bridging resistor R_1 and two shunt resistors with resistance values of R_2. The structure uses six quarter-wave length transmission lines, $\theta_1 = \theta_2 = \theta_3 = \pi/4$ at the center frequency with characteristic impedances of Z_1, Z_2 and Z_3. The network is analyzed using the even-mode equivalent circuit in Fig. 3.2 and the odd-mode equivalent circuit in Fig. 3.3. Similar to the analysis in Chapter 2, even-mode (Γ_e) and odd-mode (Γ_o) reflection coefficients better than δ is aimed to obtain input/output reflection coefficients and isolation better than a desired level of δ.

Resistor values in discrete circuits are independent. Therefore, it is difficult to design a circuit which is tolerant to deviations from nominal resistances. However, resistor values in an integrated circuit are related through sheet resistance of the resistive material. Although the sheet resistance varies between subsequent fabrications, the variation in a reticle in a single wafer is negligible. In the circuit analysis, a sheet resistance factor of ρ is added to the design equations to represent the deviation in resistor values and it is assumed that all of the resistors on the device change with the same factor. In the ideal case, the resistor values would not change with $\rho = 1$.

Even-mode impedance of the original Wilkinson power divider is independent of the sheet resistance factor ρ, since the isolation resistor is open circuited. At the design center frequency, the even-mode network of the proposed structure is

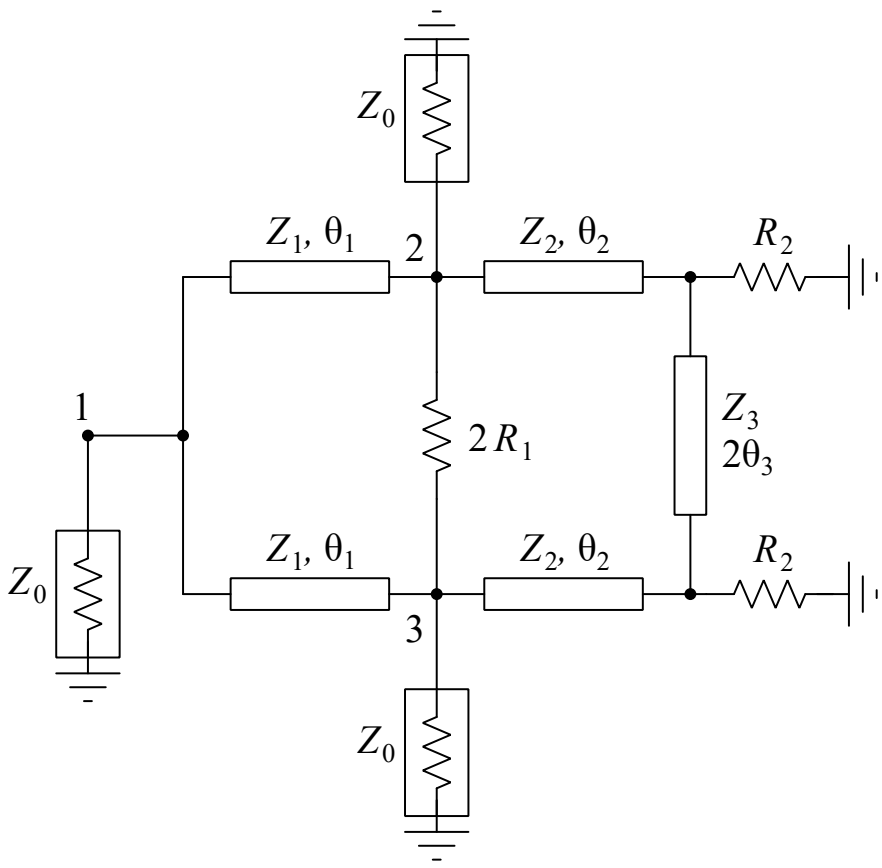


Figure 3.1: Schematic of the proposed sheet resistance tolerant power divider.

equivalent to that of the original Wilkinson power divider. At lower and higher frequencies, the transmission line arms and the additional shunt resistor R_2 provide better port matching, which results in a wider band compared to the original network. Although the additional circuitry in the even-mode adds a sheet resistance dependence, the effect is very minimal and can be ignored. This is clearly demonstrated with the simulation results in Fig. 3.7, and measurement results in Fig. 3.13. For even-mode reflection coefficient better than δ with the presented structure, one needs

$$|\Gamma_e| = \left|\frac{Z_e - Z_0}{Z_e + Z_0}\right| < \delta \tag{3.1}$$

$$Z_e = Z_1 \frac{2Z_0 + jZ_1T}{Z_1 + j2Z_0T} /\!/ Z_2 \frac{\rho Z_3R_2 - \rho Z_2R_2T^2 + jZ_2Z_3T}{Z_2Z_3 + j\rho Z_2R_2T + j\rho Z_3R_2T} \tag{3.2}$$

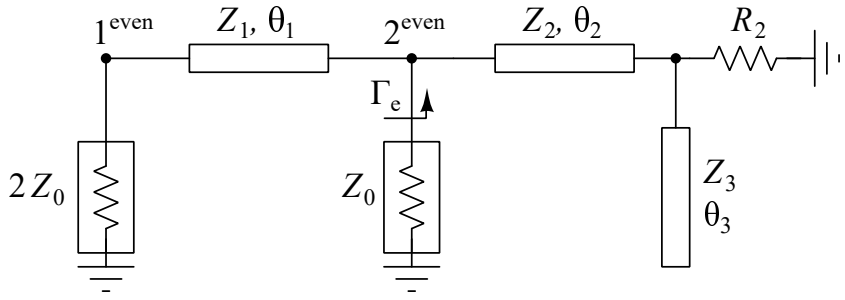


Figure 3.2: Even-mode equivalent schematic of the proposed sheet resistance tolerant power divider.

with $T = \tan(\pi\hat{f}/2)$ where $\hat{f}$ is the normalized frequency f/f_0. At the center frequency f_0, the even-mode impedance can be simplified and line impedance Z_1 can be found for perfect matching.

$$Z_e = \frac{Z_1^2}{2Z_0} = Z_0 \tag{3.3}$$

$$Z_1 = \sqrt{2}Z_0 \tag{3.4}$$

Similarly, for odd-mode reflection coefficient better than δ with the presented structure, one needs

$$|\Gamma_o| = \left|\frac{Z_o - Z_0}{Z_o + Z_0}\right| < \delta \tag{3.5}$$

$$Z_o = Z_2\frac{Z_2Z_3T^2 - j\rho Z_2R_2T - j\rho Z_3R_2T}{\rho Z_2R_2 - \rho Z_3R_2T + jZ_2Z_3T} /\!\!/ \rho R_1 /\!\!/ jZ_1T \tag{3.6}$$

in the bandwidth of interest. Odd-mode impedance of the original Wilkinson power divider is $Z_o^W = \rho Z_0$ at the center frequency. In this case, the odd-mode reflection coefficient Γ_o^W of the original Wilkinson power divider is

$$\left|\Gamma_o^W\right| = \left|\frac{\rho - 1}{\rho + 1}\right| \tag{3.7}$$

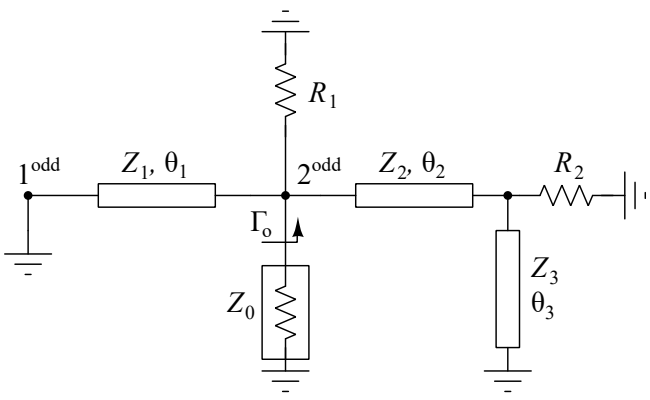


Figure 3.3: Odd-mode equivalent schematic of the proposed sheet resistance tolerant power divider.

and dependent on sheet resistance variance. The presented structure aims to cancel these dependencies at the odd-mode, improving the output return loss and isolation tolerances.

In the odd mode equivalent circuit of the proposed structure, the resistors R_1 and R_2 are connected in parallel after a quarter-wave transformation. For $\rho > 1$, both of the resistor values increase, however, the increase in R_2 is translated as a decrease after quarter-wave transformation. Due to the cancellation in the parallel sum, the overall impedance stays nearly unchanged. Similarly, when the sheet resistance is lower than its nominal value with $\rho < 1$, impedance at the output node preserves the same cancellation effect with little change. For perfect matching at the center frequency, $R_1 = R_2 = Z_2 = 2Z_0$ is one of the possible solutions and it is used for the rest of the analysis. The bridging arm impedance Z_3 is not critical and can be optimized for best tolerance response in the band. The odd-mode impedance of the proposed structure at the center frequency is

$$Z_o = \frac{2\rho Z_0}{2+\rho^2} \tag{3.8}$$

In this case, the odd-mode reflection coefficient becomes

$$|\Gamma_o| = \frac{(\rho-1)^2}{(\rho+1)^2} = \left|\Gamma_o^W\right|^2 \tag{3.9}$$

which shows that at odd multiples of the center frequency, the proposed divider achieves twice the odd-mode reflection coefficient that the original divider achieves in dB-scale. Fig. 3.4 shows the odd-mode reflection coefficient improvement in $[0.5f_0, 1.5f_0]$ for $0.7 \leq \rho \leq 1.3$ based on (3.6) with $R_1 = R_2 = Z_2 = 2Z_0$ and $Z_3 = Z_1 = \sqrt{2}Z_0$. Odd-mode reflection coefficient of the original Wilkinson power divider is below 20 dB for more than 18% deviation in ρ, while the proposed divider still achieves 40 dB return loss at that point. The proposed structure allows a 48% change in ρ before the 20 dB crossing. In a practical design, component values can be optimized for the desired sheet resistance tolerance, matching level and bandwidth to obtain further improvement.

Although the proposed divider introduces additional transmission lines to the original design, line impedance is a more forgiving design parameter in the sense that it changes slowly with respect to deviations in the physical parameters. For instance, an unlikely ±20% perturbation in substrate height results only in a ±5% change in line impedance. Moreover, line width, substrate height and substrate permittivity are more robust to process variations compared to sheet resistance.

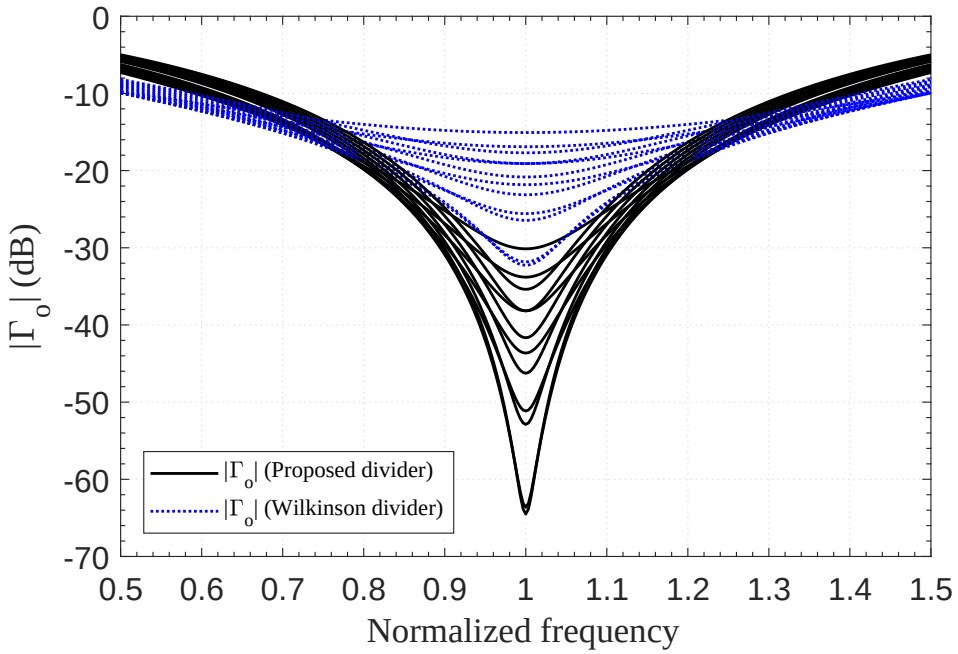


Figure 3.4: Odd-mode reflection coefficient of the proposed power divider versus the original Wilkinson divider for ±30% deviation in sheet resistance.

3.2 Circuit Design

Component values of the proposed structure are optimized for tolerance and bandwidth, starting from an initial point based on the analysis in the previous section. A comparison of the ideal fractional bandwidth performance of the optimized divider, Wilkinson divider and Gysel divider is shown in Fig. 3.5. The proposed structure nearly doubles the operational bandwidth for 20 dB return loss and isolation levels. Moreover, change in sheet resistance affects the performance and decreases the overall bandwidth for both Wilkinson and Gysel dividers. Gysel divider does not work anymore after 30% reduction in the resistor values, whereas bandwidth of the Wilkinson divider is halved. At the same conditions, the proposed divider preserves its original bandwidth.

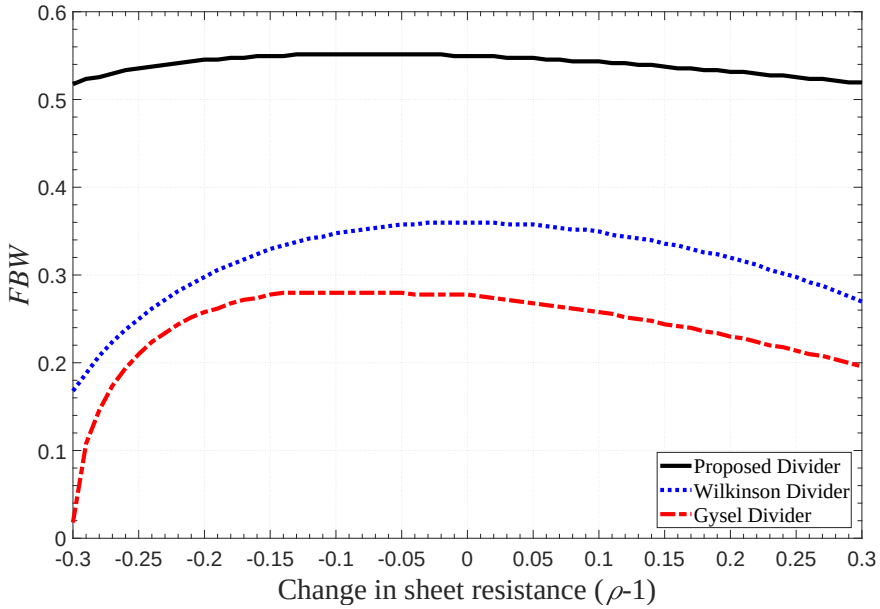


Figure 3.5: Fractional bandwidth capability of the proposed power divider versus the original Wilkinson and Gysel power dividers as a function of the deviation in sheet resistance for 20 dB ($\delta = 0.1$) return loss and isolation levels.

A wide band and sheet resistance tolerant modified Wilkinson power divider is designed at *Ka*-band with 30 GHz center frequency. Top view of the layout of the divider is shown in Fig. 3.6. For the simulations[1], a three-dimensional electromagnetic model is used to account for line coupling and via electric fields, since

[1]HFSS 12, ANSYS, Inc., Canonsburg, PA 15317, USA

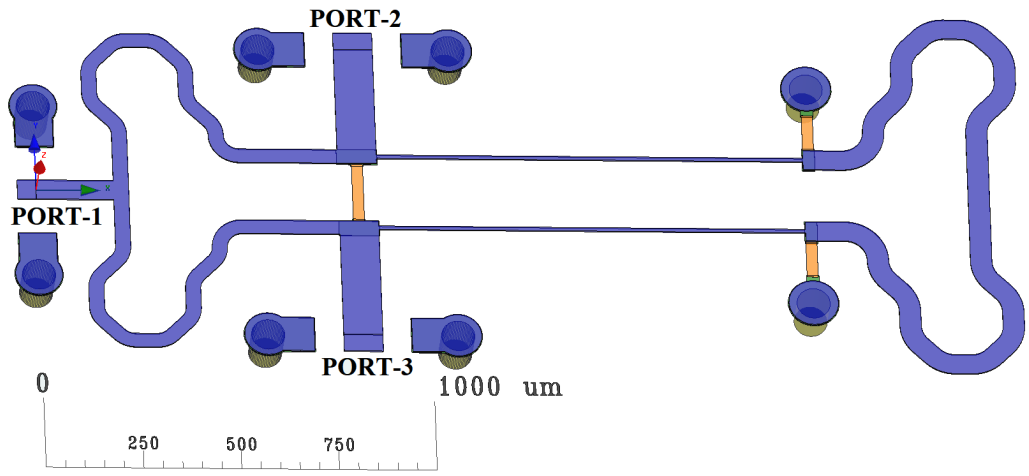


Figure 3.6: Three-dimensional layout of the sheet resistance tolerant divider for FEM simulation.

they are next to the transmission lines. The quarter-wave length line impedances, Z_1, Z_2 and Z_3 are 71 Ω, 102 Ω and 63 Ω, respectively. The bridging resistor R_1 is 160 Ω and the shunt resistors R_2 are 96 Ω. The transmission lines are meandered for a compact design. The total circuit size is 2.58 mm × 1.02 mm including all measurement pads.

The designed layout is simulated with different sheet resistance values ranging from 21 Ω/□ to 39 Ω/□ (using 0.3 Ω/□ steps) with ±30% change around the nominal sheet resistance of 30 Ω/□. The simulation results are presented in Figs. 3.7–3.10. According to the simulation results, the divider is capable of at least 20 dB port matching and isolation from 22.1 GHz to 38.0 GHz with 53% fractional bandwidth when the sheet resistance is not altered by the fabrication process. The bandwidth decreases slightly even if there is a ±30% change in sheet resistance. The 20 dB return loss and isolation bandwidth in that case is from 23.9 GHz to 37.2 GHz with 44% fractional bandwidth. The extra insertion loss is less than 0.45 dB at the center frequency for all of the swept simulations. Simulation results show that the worst case scenario happens when the sheet resistance deviation is the highest. Hence, it is efficient to design the divider by only checking the performance at the sheet resistance corners with $\pm|1-\rho|$ variations.

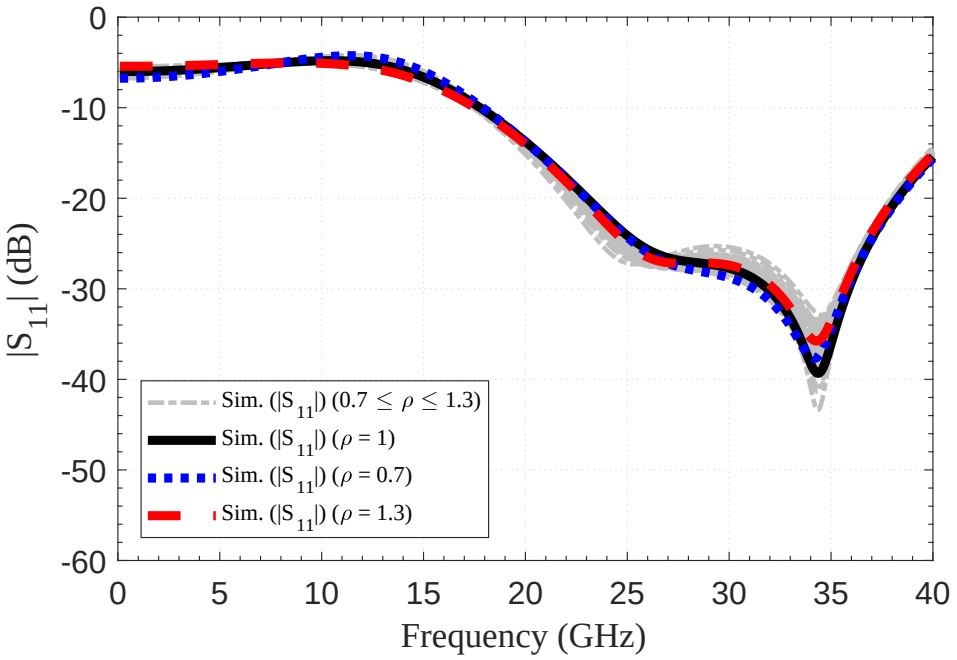


Figure 3.7: Simulated parameters associated to input reflection coefficient of the divider tolerant to ±30% change in sheet resistance as a function of frequency.

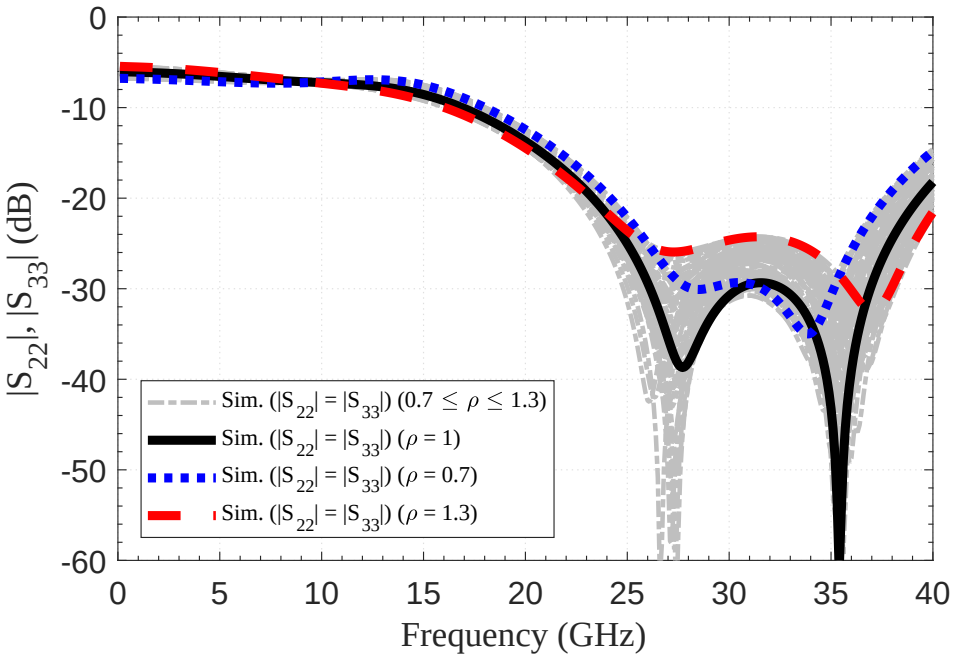


Figure 3.8: Simulated parameters associated to output reflection coefficients of the divider tolerant to ±30% change in sheet resistance as a function of frequency.

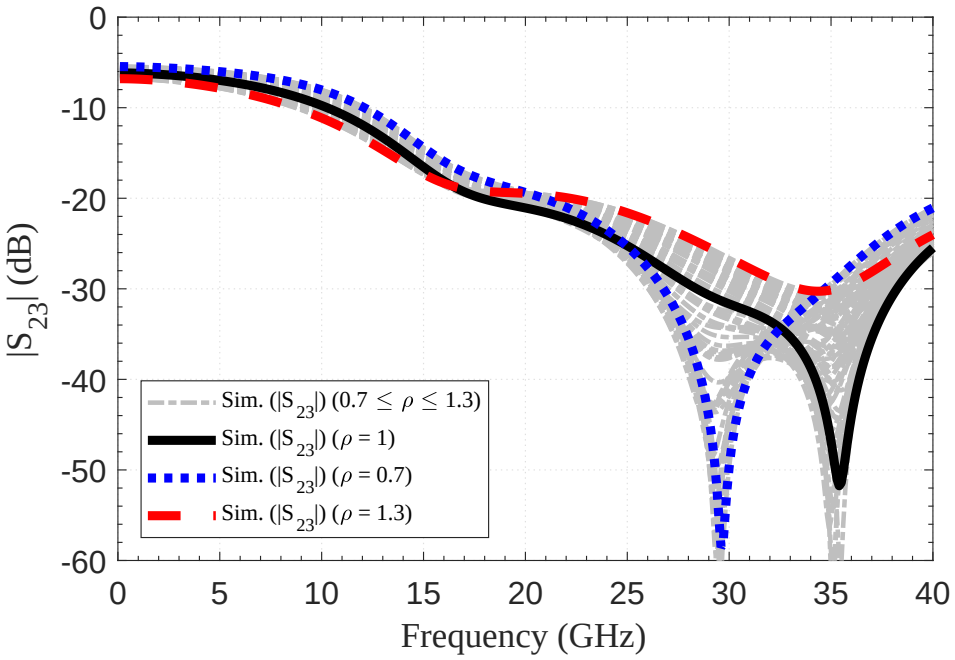


Figure 3.9: Simulated parameters associated to isolation of the divider tolerant to ±30% change in sheet resistance as a function of frequency.

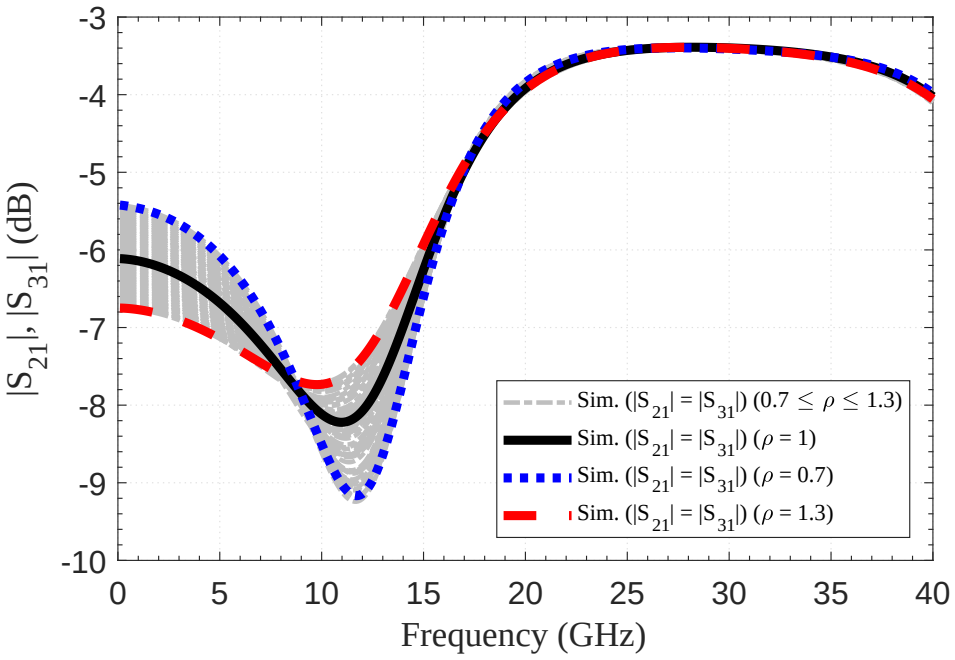
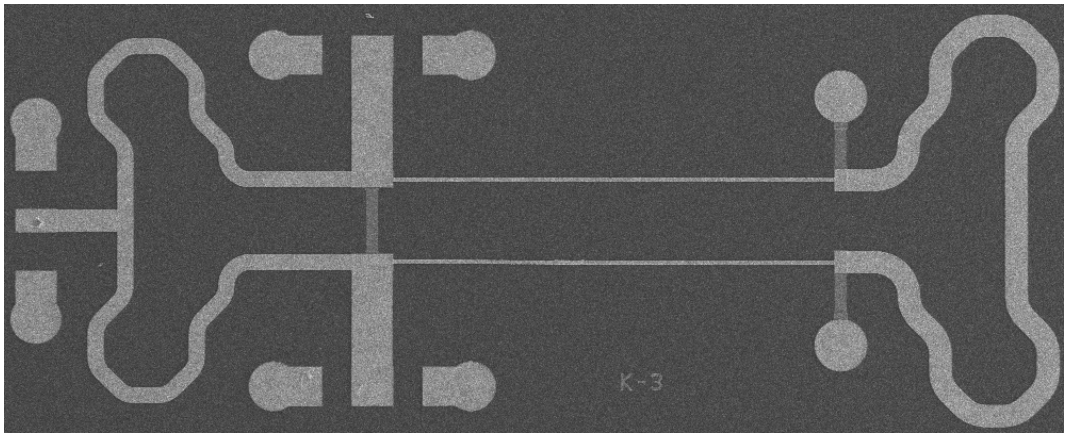


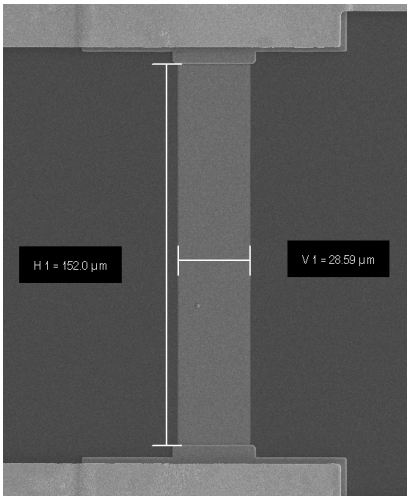
Figure 3.10: Simulated parameters associated to insertion losses of the divider tolerant to ±30% change in sheet resistance as a function of frequency.

3.3 Fabrication and Measurement Results

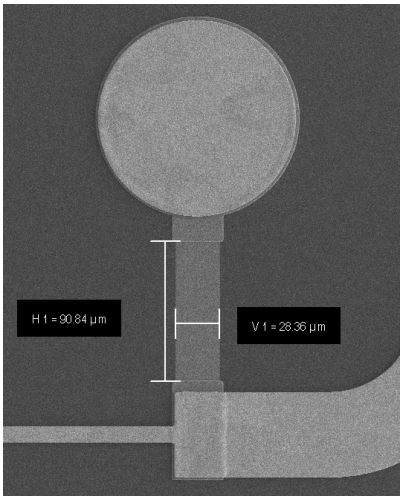
Width of the resistors in the divider design are intentionally altered to artificially decrease and increase all resistor values by 30%. The designed power divider and the altered dividers are fabricated using a microstrip MMIC process with two metal layers. SiC substrate is 100 µm thick with a dielectric constant (ϵ_r) of 9.66. Thin film resistors are formed by TaN sputtering with a nominal sheet resistance of 30 Ω/□. Fig. 3.11 shows the SEM image of the fabricated nominal power divider along with close-up SEM photos of the resistors R_1 and R_2.



(a)



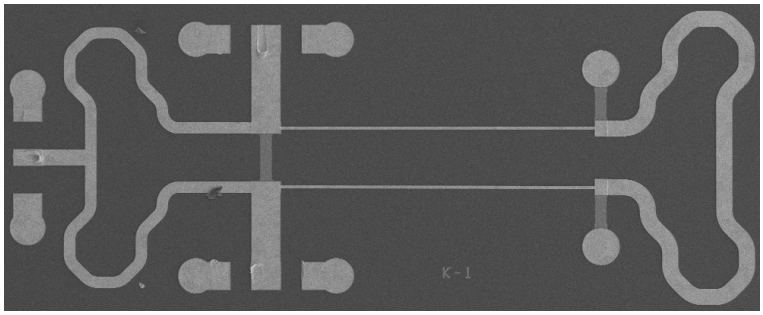
(b)



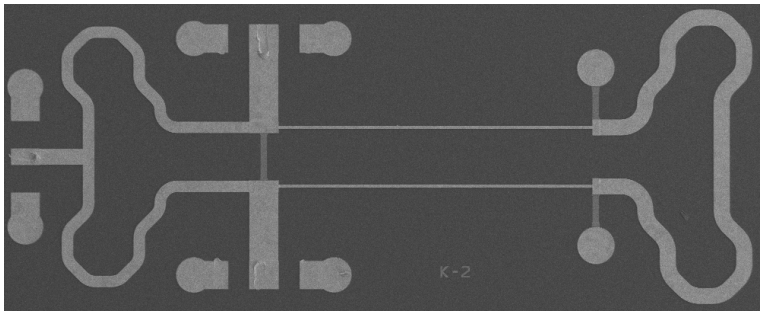
(c)

Figure 3.11: Scanning electron microscope photograph of: (a) the nominal sheet resistance tolerant divider; (b) R_1 of the divider; (c) R_2 of the divider.

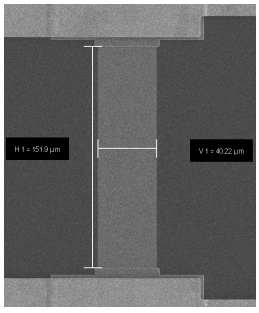
SEM photographs of the fabricated dividers with intentionally modified resistors to have 30% lower and 30% higher resistance than the intended values are shown in Fig. 3.12 with associated dimensions displayed on the resistor close-ups.



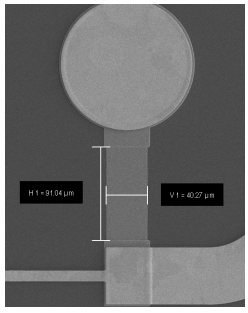
(a)



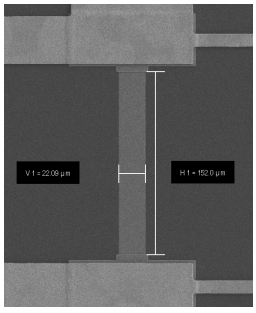
(b)



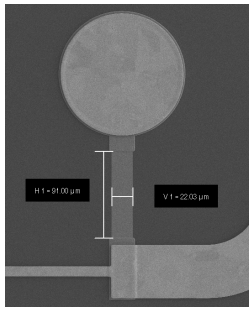
(c)



(d)



(e)



(f)

Figure 3.12: Scanning electron microscope photograph of: (a) the sheet resistance tolerant divider with smaller resistances; (b) the sheet resistance tolerant divider with larger resistances; (c) R_1 of the divider with smaller resistances; (d) R_2 of the divider with smaller resistances; (e) R_1 of the divider with larger resistances; (f) R_2 of the divider with larger resistances.

3-port on-wafer calibration and measurements are performed using Cascade RF wafer probe station, GGB GSG150 picoprobes and R&S ZVA40 vector network analyzer. The measured S-parameter values of the sheet resistance tolerant power divider are shown in Figs. 3.13–3.16, proving tolerance of the divider to resistance variations. In the graphs below, the three separate curves represent the measurement results for the nominal design, the design with resistor values intentionally decreased by 30% and the design with resistor values intentionally increased by 30%. The measured center frequency is 27.3 GHz and shifted approximately 9% to lower frequencies. However, the bandwidth and performance of the divider is parallel to design expectations. The divider has at least 20 dB input/output return losses and isolation from 21.9 GHz to 32.7 GHz with 40% fractional bandwidth even if its resistor values are increased or decreased by 30%. The nominal design achieves a 50% fractional bandwidth with an extra insertion loss less than 0.45 dB. The sheet resistance measured from process control monitor test structures around the fabricated wafer is about 28.5 $\Omega/\square$ which is 5% less than the simulated parameter. Therefore, the bandwidth degradation when the resistor values are decreased is slightly worse than the simulation expectations of 44% fractional bandwidth as shown in Fig. 3.15.

The nominal design achieves an input return loss better than 20 dB from 17.6 GHz to 33.1 GHz with a fractional bandwidth of 61%. Output return loss of the divider is at least 20 dB from 18.5 GHz to 32.7 GHz with a fractional bandwidth of 55%. When the ±30% change in sheet resistance is imposed, the fractional bandwidths for 20 dB input and output return losses decrease to 56% (18.6 GHz to 33.1 GHz) and 49% (19.8 GHz to 32.7 GHz), respectively.

The nominal design provides isolation better than 20 dB from 19.7 GHz to more than 40 GHz. The isolation is at least 20 dB from 21.9 GHz to more than 40 GHz even if the sheet resistance deviates up to 30% from its nominal value. The additional insertion loss is less than 0.25 dB at the center frequency and less than 0.5 dB from 19.4 GHz to 34.0 GHz despite a ±30% change in sheet resistance.

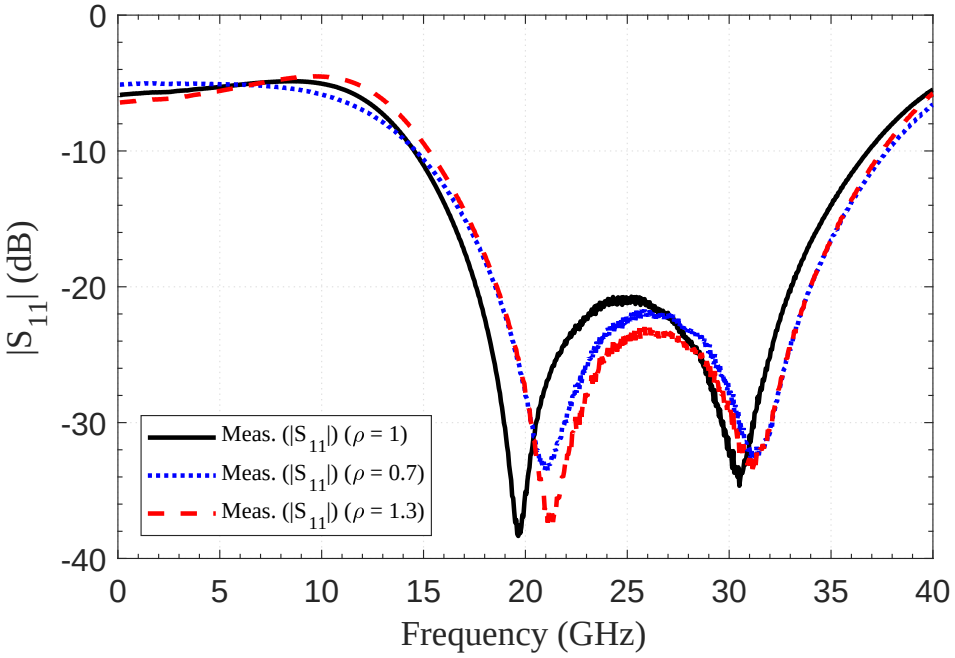


Figure 3.13: Measured parameters associated to input reflection coefficients of the divider tolerant to ±30% change in sheet resistance as a function of frequency.

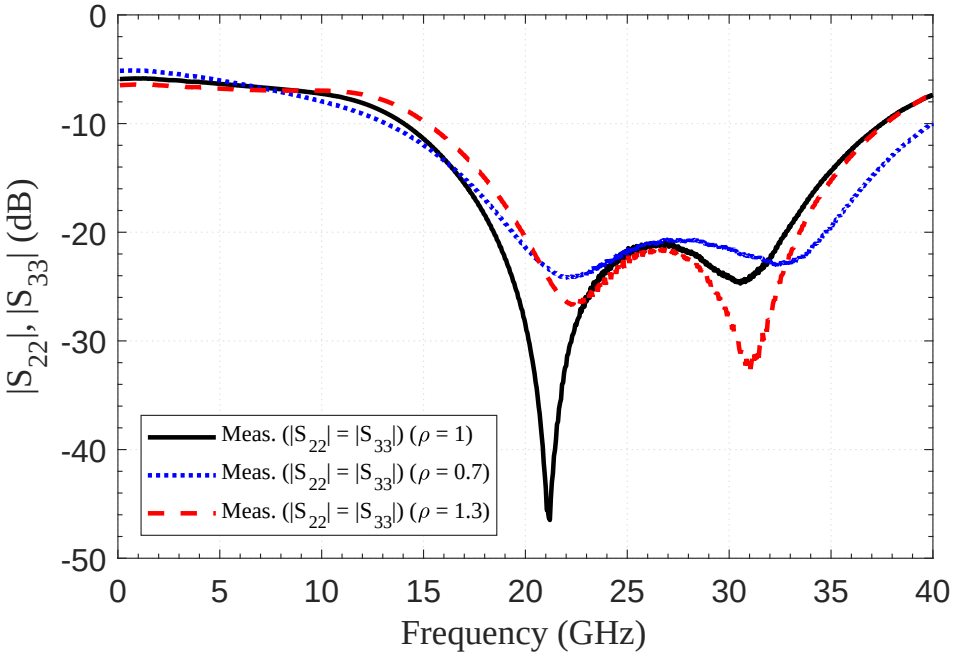


Figure 3.14: Measured parameters associated to output reflection coefficients of the divider tolerant to ±30% change in sheet resistance as a function of frequency.

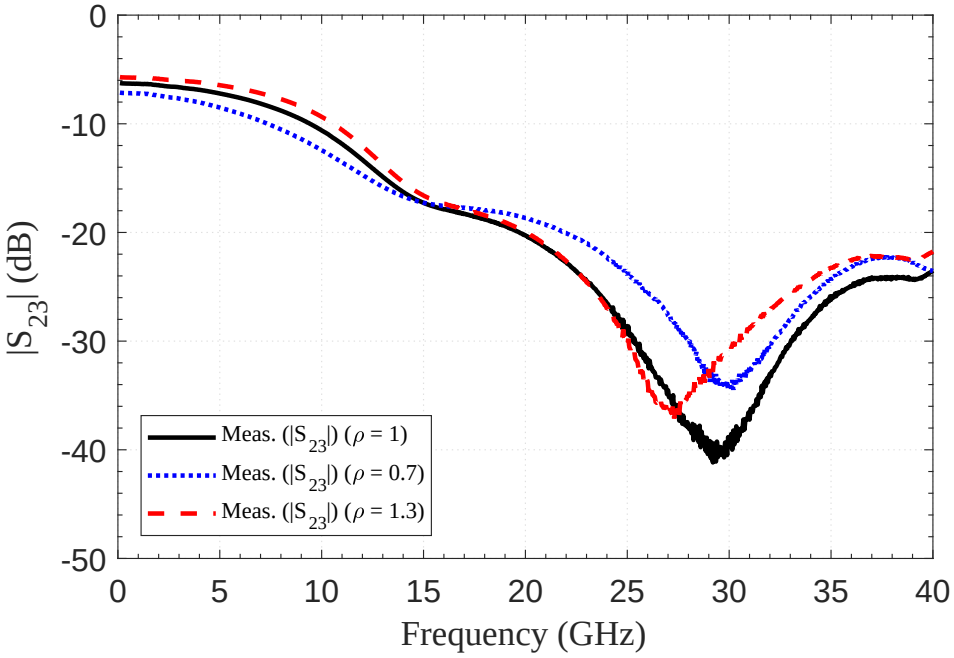


Figure 3.15: Measured parameters associated to isolation of the divider tolerant to ±30% change in sheet resistance as a function of frequency.

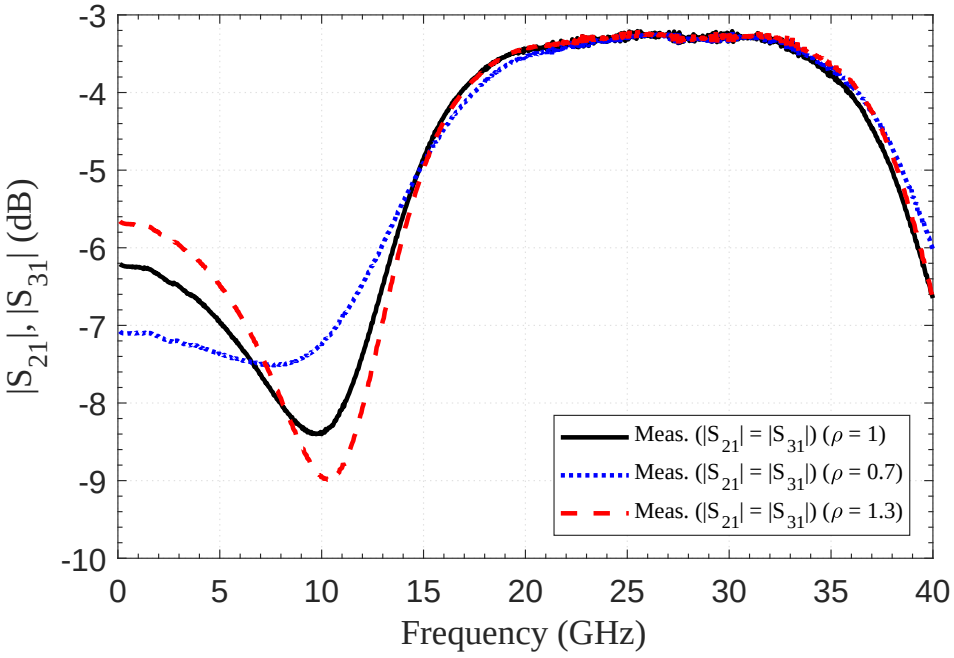


Figure 3.16: Measured parameters associated to insertion losses of the divider tolerant to ±30% change in sheet resistance as a function of frequency.

Chapter 4

A Planar Power Divider Structure with Three Output Ports

Two-way power dividers are usually preferred over three-way power dividers since high power MMICs typically have 2^N active devices at the output stage, where N is a positive integer. Moreover, three-way power divider layouts require isolation resistors between each output port or the isolation resistors need to be connected in a common floating node which result in a non-planar divider structure [18, 19]. Also, the standard three-way divider topologies cannot easily accommodate the necessary spacing for the three transmission line arms without cross-coupling. On the one hand, the divider requires three-dimensional process and complicates the fabrication technology. On the other hand, as the design complexity increases, a predictable model becomes more difficult. However, three-way power dividers might still be suitable for mm-wave MMICs with 3 or 6 output transistors depending on the output power and efficiency requirements.

Researchers have used coupled line structures to make use of the inevitable coupling between divider arms [20, 21] and studies have revealed that the third isolation resistor can be omitted in such a structure to have planarity, sacrificing

high return loss and isolation performance in return [22, 23]. The proposed three-way planar power divider structure in this chapter can operate at mm-wave frequencies with its high-frequency components. The structure utilizes a five-line coupling network to achieve power split, therefore it also offers DC block capability at all RF ports. The sacrificed return loss performance is recovered by additional reactive matching at the output ports without increasing the circuit size.

4.1 Analysis and Design Equations

Proposed network for the modified planar three-way Wilkinson power divider is shown in Fig. 4.1. Input signal with power P is split into two equal amplitude signals with power $P/2$ and fed into a symmetrical five-line coupling structure. Electrical length of the coupling network is $\lambda/4$ (90 degrees). The coupled lines are designed in such a way that two-thirds of the incoming power of $P/2$ is coupled to the outer lines, and the remaining one-third is coupled to the middle line. Since power is coupled to the middle line from both sides of the structure, all output ports receive one-third of the input power, $P/3$. In order to achieve the desired coupling ratios, the line width parameters W_1, W_2, W_3 and the line to line spacing parameters S_1, S_2 are adjusted. Two inter-connecting resistors provide the necessary isolation between the output ports. Moreover, symmetrical shunt capacitors are connected at the output ports for improved port matching.

Once the coupled lines are designed for power split, the resistor and capacitor values can be found based on the complex impedances seen looking into the 5-line coupling structure: Z_1, Z_2 and Z_3. Several design iterations may be necessary, because Z_1 is also dependent on the lumped element values. The reflection coefficient at the input port is simply

$$|\Gamma_1| = \left| \frac{Z_1 - 2Z_0}{Z_1 + 2Z_0} \right| \tag{4.1}$$

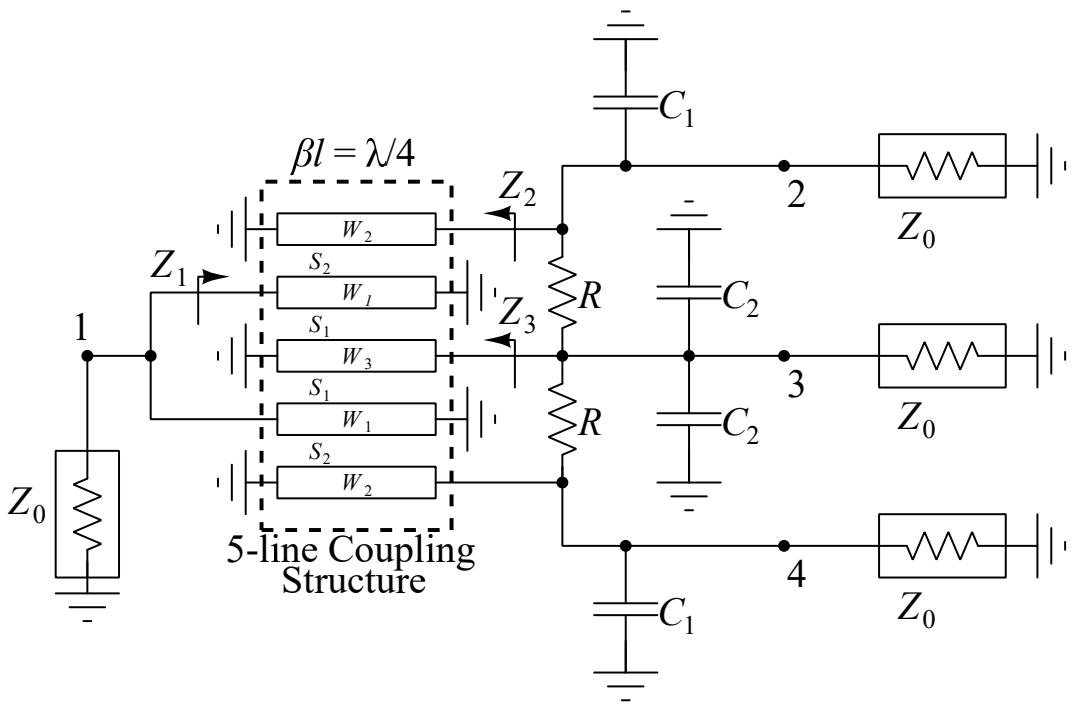


Figure 4.1: Schematic of the modified planar three-way Wilkinson power divider structure with the electrical and corresponding physical design parameters.

The reflection coefficients at the symmetrical output ports become

$$|\Gamma_2| = |\Gamma_4| = \left| \frac{Z_{C_1} /\!\!/ Z_2 /\!\!/ (R + Z_x) - Z_0}{Z_{C_1} /\!\!/ Z_2 /\!\!/ (R + Z_x) + Z_0} \right| \tag{4.2}$$

$$Z_x = Z_3 /\!\!/ (R + Z_2 /\!\!/ Z_{C_1} /\!\!/ Z_0) /\!\!/ (Z_{C_2}/2) /\!\!/ Z_0 \tag{4.3}$$

Here, Z_{C_1} and Z_{C_2} are the complex impedances of the capacitors C_1 and C_2, R is the isolation resistance, and Z_0 is the characteristic impedance of the system. The reflection coefficient at the asymmetrical output port is

$$|\Gamma_3| = \left| \frac{2Z_3 /\!\!/ Z_x /\!\!/ Z_{C_2} - 2Z_0}{2Z_3 /\!\!/ Z_x /\!\!/ Z_{C_2} + 2Z_0} \right| \tag{4.4}$$

4.2 Circuit Design

Layout design of the proposed divider operating at Ka-band is shown in Fig. 4.2. Bilateral symmetry is preserved for predictable operation. Width of the coupled lines, W_1, W_2, and W_3 are 11 µm, 28 µm, and 25 µm, respectively. Spacing between the outer lines S_2 is 8 µm, considerably smaller than the spacing between the middle lines S_1, which is 27 µm, for higher power coupling ratio as described. Resistance of the isolation resistors are 77 Ω. Shunt capacitors with small capacitances at the output ports are realized by high-frequency radial stubs. A butterfly stub is used at the third port to maintain bilateral symmetry. An additional butterfly stub for improved matching can be utilized at the input as well. However, in this case, the input return loss is at an acceptable level without it, and stubs are only connected at the output ports. The RF measurement pads are placed in the north-south and west-east directions for measurement convenience. The overall circuit size is 1.66 mm × 1.08 mm.

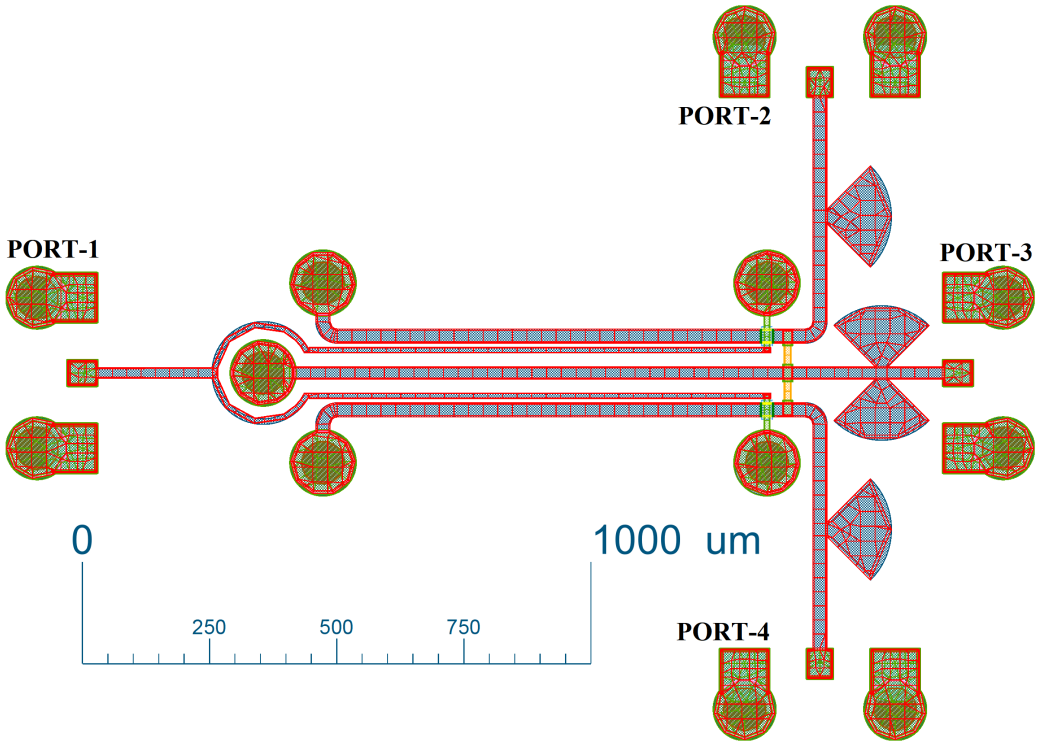


Figure 4.2: Layout of the proposed three-way divider meshed for EM simulation.

4.3 Fabrication and Measurement Results

The modified planar three-way Wilkinson power divider design at *Ka*-band is fabricated using a microstrip MMIC process with two metal layers. SiC substrate is thinned to 100 µm and the dielectric constant (ϵ_r) is 9.66. Thin film resistors are formed by TaN sputtering with a sheet resistance of 30 Ω/□. The back-via diameter is 85 µm. Fig. 4.3 shows the microscope image of the fabricated divider (multiple images are stitched).

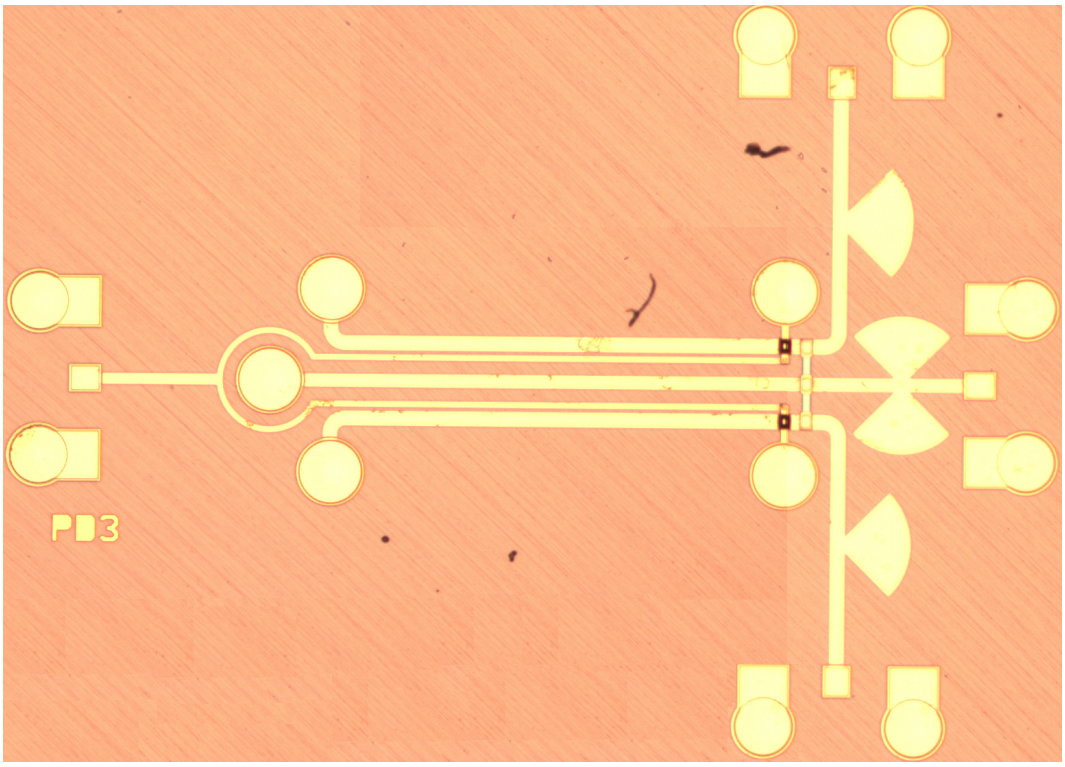


Figure 4.3: Microscope photograph of the fabricated three-way divider.

SEM image of the 5-line coupling structure in the three-way power divider is shown in Fig. 4.4 and Fig. 4.5 with line width and spacing parameters indicated separately. The measured dimensions are similar to the designed values.

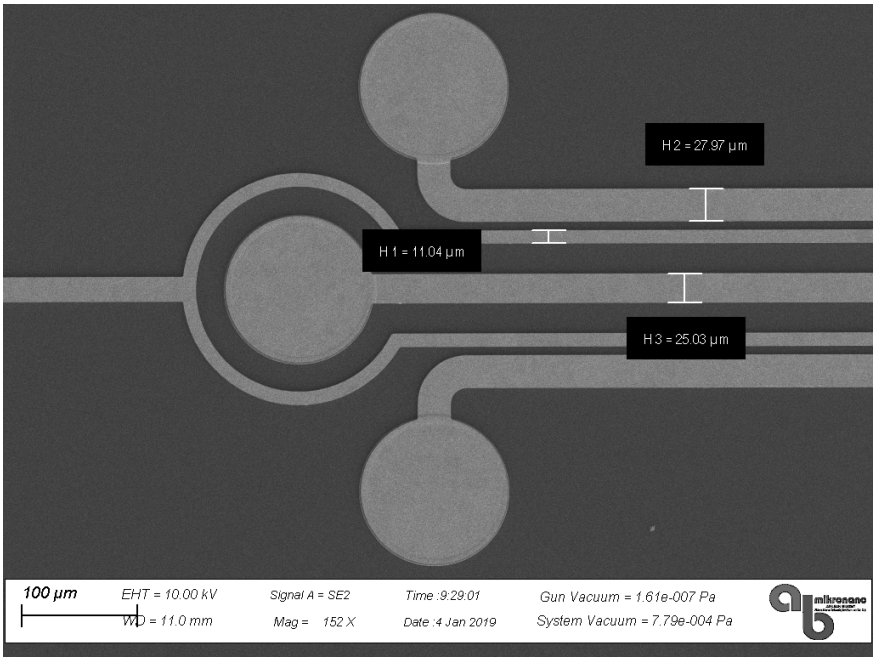


Figure 4.4: Scanning electron microscope image of the three-way power divider that shows the width of the coupled line structure.

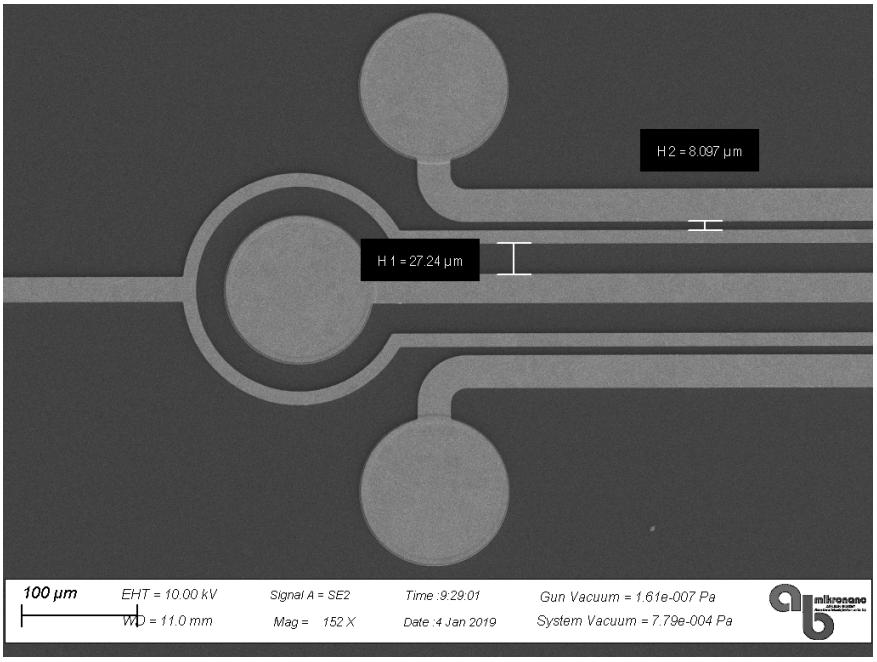


Figure 4.5: Scanning electron microscope image of the three-way power divider that shows the spacing of the coupled line structure.

4-port on-wafer calibration and measurements are performed using Cascade RF wafer probe station, GGB GSG150 picoprobes and R&S ZVA40 vector network analyzer. The simulated[1] and measured S-parameter values of the three-way power divider are shown in Figs. 4.6–4.9, there is a good agreement between them. The measured input return loss is better than 20 dB from 27.9 GHz to 30.8 GHz and the measured output return losses are better than 20 dB from 26 GHz to 33 GHz. The measured isolation levels between all output ports are at least 15 dB from 27.6 GHz to 36.0 GHz. The measured extra insertion loss is less than 0.75 dB and the amplitude imbalance between the asymmetrical ports is less than 0.2 dB from 25.0 GHz to 34.3 GHz. It is almost impossible to obtain such a level of balance at a wide bandwidth using traditional couplers. The overall 15 dB operational fractional bandwidth is 19%. This divider is compared to similar studies in Table 4.1. Results obtained at relatively low frequencies from devices fabricated on PCB are also included in the table since research is very limited at *Ka*-band and higher frequencies or the reported divider bandwidths for 15 dB return loss and isolation are slim.

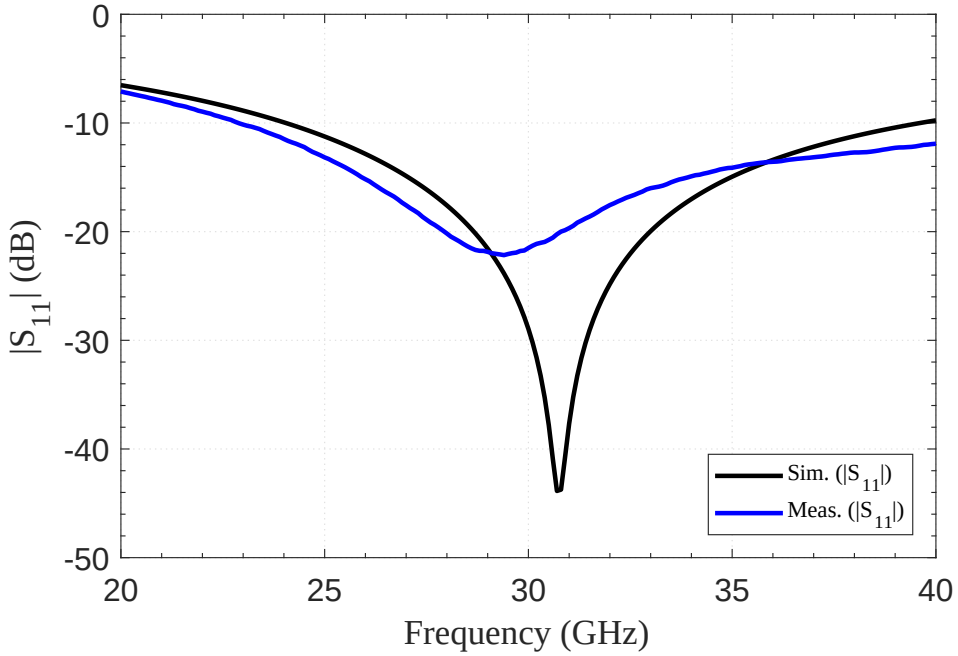


Figure 4.6: Simulated and measured parameters associated to input reflection coefficient of the three-way divider as a function of frequency.

[1]ADS 2017.01, Keysight Technologies, Inc., Santa Rosa, CA 95403, USA

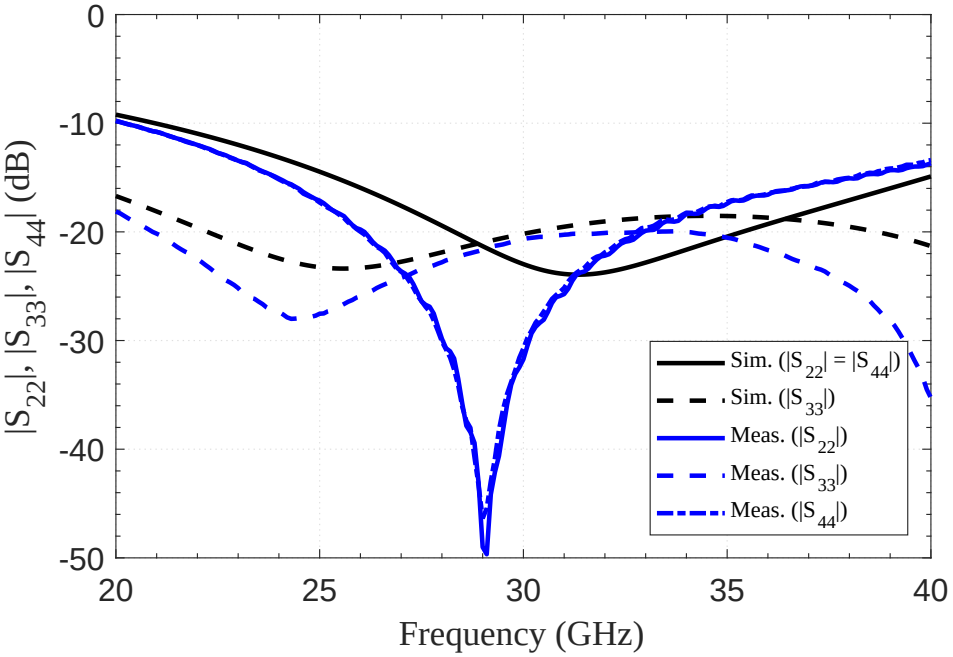


Figure 4.7: Simulated and measured parameters associated to output reflection coefficients of the three-way divider as a function of frequency.

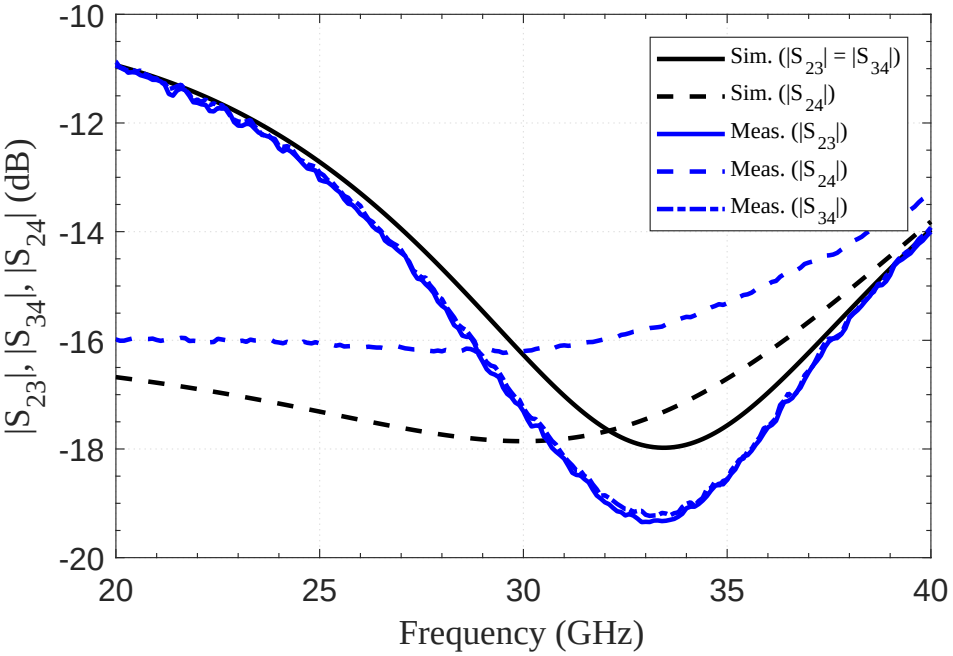


Figure 4.8: Simulated and measured parameters associated to isolation levels of the three-way divider as a function of frequency.

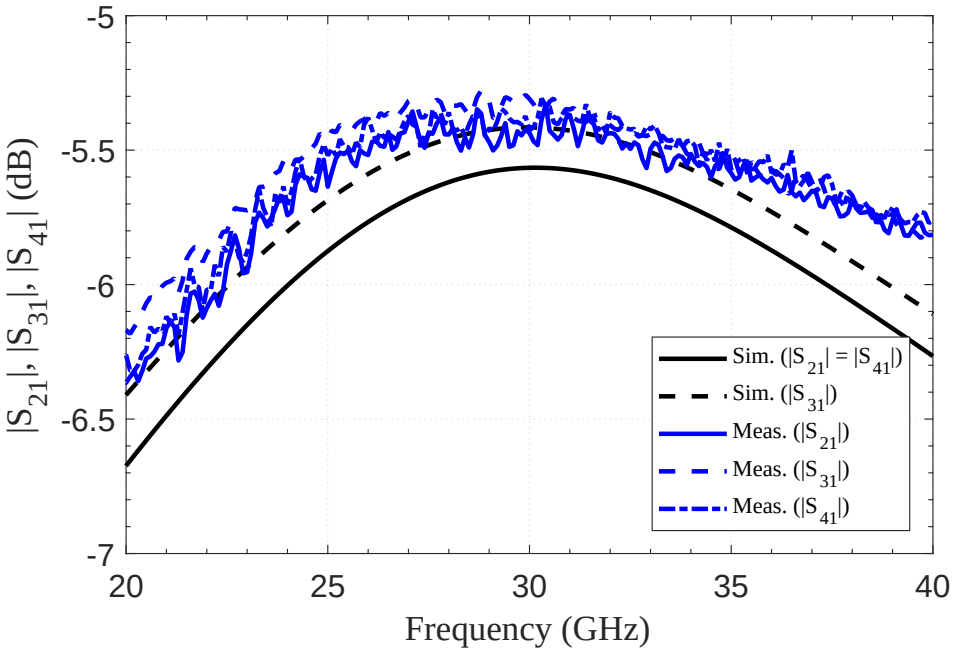


Figure 4.9: Simulated and measured parameters associated to insertion losses of the three-way divider as a function of frequency.

Table 4.1: Size and bandwidth comparison of three-way power dividers

Reference	**Technology**	**Topology**	**Planar**[a]	**Length**	**15 dB Operational *FBW***
[18]	DSPSL[b] PCB	DSPSL	No	$\lambda/2$	1.7 GHz – 2.3 GHz (30%)
[19]	RT6010 PCB	Modified isolation	No	$\lambda/4$	1.7 GHz – 2.1 GHz (21%)
[20]	FR4 PCB	Coupled lines	No	$\lambda/4$	1.7 GHz – 2.4 GHz (34%)
[21]	RO4003C PCB	Coupled lines	No	$\lambda/4$	3.8 GHz – 4.5 GHz (17%)
[22]	FR4 PCB	Coupled lines	Yes	$\lambda/4$	2.0 GHz – 3.0 GHz (40%)
[23]	GaAs MMIC	Coupled lines	Yes	$\lambda/4$	28.5 GHz – 33.5 GHz (16%)
This work	GaN MMIC	Coupled lines and reactive matching	Yes	$\lambda/4$	27.6 GHz – 33.4 GHz (19%)

[a]The design structure can be fabricated in a two-dimensional configuration
[b]Double-sided parallel-strip line

Chapter 5

Conclusion

Three power divider structures are presented to solve several issues with the original Wilkinson power divider and improve its overall performance. The first divider miniaturizes the quarter-wave length arms of the Wilkinson divider while compensating for the bandwidth degradation. The proposed layout provides additional physical isolation at the output ports and prevents coupling between the divider arms. The second divider achieves a wide bandwidth by combining Wilkinson and Gysel isolation networks. The divider demonstrates high tolerance to variances in the sheet resistance of integrated circuit fabrication. The third divider is a three-way variant of the Wilkinson power divider using a coupled line structure for power split to avoid the negative effects of unintentional coupling between the three transmission line arms in the original divider. The presented structure uses only two isolation resistors and can be manufactured with a planar technology. Design equations for the proposed dividers are derived based on S-parameter relations and even-odd mode analysis. The analytical expressions relate component values with divider return loss and isolation levels, bandwidth, circuit size and tolerance to material parameters. Dividers are designed with 30 GHz center frequency at *Ka*-band and realized using in-house coplanar waveguide and microstrip GaN based MMIC technology. The experimental results confirm that the methods introduced in this thesis are applicable at mm-wave frequencies.

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