MULTIPHYSICS MODELING OF $Ge_2Sb_2Te_5$ BASED SYNAPTIC DEVICES FOR BRAIN INSPIRED COMPUTING

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By

Yiğit Demirağ

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Multiphysics Modeling of $Ge_2Sb_2Te_5$ Based Synaptic Devices for Brain Inspired Computing
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We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

MULTIPHYSICS MODELING OF $Ge_2Sb_2Te_5$ BASED SYNAPTIC DEVICES FOR BRAIN INSPIRED COMPUTING

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Modeling nanoscale devices that emulate the functionality of synapses of the biological brain is a fundamental operation for developing brain-inspired computational systems. Phase-change material based synaptic devices offer promising performance in speed, spatial and power efficiency metrics, up to human brain level, when connected in a massively parallel crossbar array architecture. In this work, we modeled electrothermal characteristics of a single synaptic device consisting of phase-change material based memory and its selector. First, we proposed a finite element method based simulation framework for modeling electrical, thermal and probabilistic crystallization dynamics of the memory unit. Gradual phase transitions that form device memory between amorphous and crystalline states are studied under nanosecond voltage pulses. Second, we implemented time and temperature dependent resistance drift saturation model for phase-change material based selector device. Our model is in close agreement with the ultrafast saturation phenomena which is observed for the first time in fabricated devices with 8 nm node technology.

Keywords: Phase change memory, device modeling, synaptic device, neuromorphic computing, GST, multiphysics.

ÖZET

BEYİNDEN ESİNLENEN HESAPLAMALAR İÇİN $Ge_2Sb_2Te_5$ TABANLI SİNAPTİK CİHAZLARIN MULTİFİZİK MODELLENMESİ

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Beynin yapısındaki sinapsları taklit etmek için üretilen nano boyutlardaki cihazların modellenmesi, insan beyninden ilham alan hesaplama sistemlerinin geliştirilmesinde temel bir rol oynamaktadır. Faz-değişim malzemesi kullanan bu sinaptik aygıtlar, krosbar mimarisi ile paralel olarak bağlandığında, insan beyni ile hız, enerji ve kapladığı hacim bakımından kıyaslanabilir bir performans göstermektedir. Bu çalışmada ise faz-değişim malzemesi kullanılarak üretilen seri bağlanmış hafıza ve seçiciden oluşan tek bir sinaptik aygıtın, elektrotermal özellikleri modellenmiştir. Çalışmanın ilk kısmında, sonlu element yöntemi tabanlı bir simülasyon yapısı sunulmuş, sinaptik cihazın hafıza kısmının elektriksel, ısıl ve olasılıksal faz-değişim dinamikleri modellenmiştir. Ek olarak, hafıza kodlanmasını sağlayan amorf ve kristal hallerinin arasındaki kademeli geçişin nano saniye uzunluğundaki voltaj vuruşlarıyla yapılabildiği gösterilmiştir. İkinci kısımda, sinaptik cihazın seçici kısmının zamanla elektriksel iletkenliğinin değişimi ve doyumu, sıcaklık ve zamana bağlı olarak modellenmiştir. Geliştirdiğimiz model, 8 nm teknolojisi ile üretilmiş cihazlarda ilk defa gözlemlenen, çok hızlı oluşan elektriksel iletkenlik değişiminin doyumu ile yakın uyum göstermiştir.

Anahtar sözcükler: Faz-değişim hafızası, aygıt modellemesi, sinaptik aygıt, nöromorfik hesaplama, GST, multifizik.

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Chapter 1

Introduction

The computational ability of biological brain is outstanding. A human brain is a 1.5-kilogram mass that can learn, reason and conceive the universe and abstract ideas. Much progress towards building a similar information processor has been made using brain-inspired artificial neural networks (ANNs) [1]. These ANNs have nearly reached or surpassed human-level performance in various domains e.g. image recognition [2,3], speech recognition [4,5], natural language understanding [6] and even domains requiring the challenging competition such as game of Go [7,8] and classical Atari 2600 games [9].

Evidence shows that increasing the number of parameters in ANNs (analogous to increasing the number of synapses) leads to predictively better performances in a wide range of tasks [10]. To cope with larger neural network models, more computation power is needed. The trend shows that the amount of computation used in ANN training has been increasing exponentially as shown in Fig. 1.1. Despite the exponential trend, the amount of parameters (synapses) in the human brain is $\sim 10^{15}$, which is 7 order of magnitude higher than the number of parameters in currently the largest neural network [11]. If the aim is to achieve a similar model capacity of the human brain, we require at least 4–5 orders of magnitude improvement in computational power.

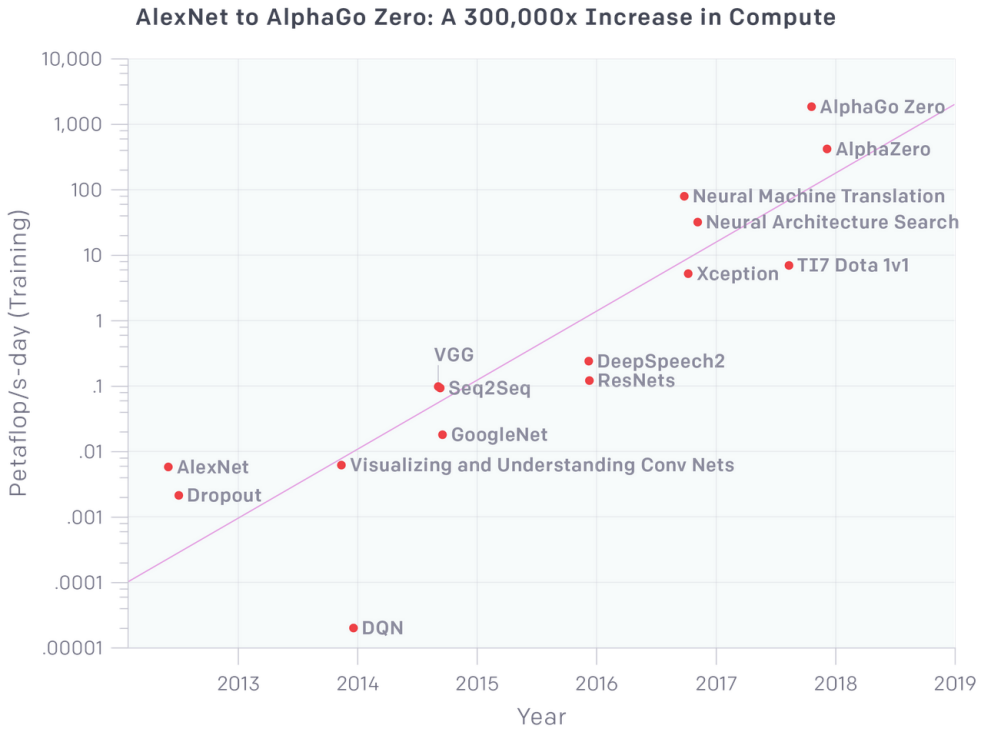

Figure 1.1: The required amount of computation to train some well known neural network models [12].

The conventional computing is based on von Neumann architecture [13], and radically different than architecture and working principles of a biological brain. The biological brain combines information processing and storage in a massively parallel, three-dimensionally organized, fault and variation tolerant architecture. On the other hand, von Neumann architecture separates processing and storage and is optimized for well-defined, logic-based information processing. Any problem can be represented via different layers of abstraction build upon logic gates, but this reduces the efficiency through each layer of computation. Hence scaling hardware architecture which is fundamentally misaligned with the type of computation that artificial neural networks require, is an insufficient solution.

Recently, companies such as Google, IBM and NVIDIA put serious research effort to optimize their hardware running neural networks, by designing specific TPUs [14] , ASICs [15], FPGAs [16] or GPUs [17] that rely on conventional CMOS-technology. Beside this efforts, the field of neuromorphic computing has

been actively searching the most optimized hardware candidates inspired directly by the operation principles, algorithms, and architectures of the biological brain. In this thesis, the focus is the modeling of a hardware representation of the most abundant computational element of the biological brain, a synapse.

1.1 Computational Memory

Synapses are < 50 nm structures that permit a neuron to pass an electrical or chemical signal to another neuron. Being at the intersection of neurons, synapses can change the strength of connection depending on the timing of pre/post spikes and neuro-modulators, which is known as synaptic plasticity [18]. This mechanism is believed to underlie learning and memory of biological brain [19].

Nanoscale synaptic devices can store information on the history of electrical current passed through them in their resistance states [20, 21]. The opportunity to be able to tune their conductance with short pulses makes them analogous to synapses in the biological brain.

To connect synaptic devices in a massively parallel way, crossbar array architecture, which is similar to grid-like connectivity of brain fibers is generally used [22]. Fig. 1.2 is an illustration of a crossbar architecture and Fig. 1.3 demonstrates SEM image of a fabricated crossbar array which contains one memory and one selector device at junctions, fabricated with 90 nm CMOS technology [23].

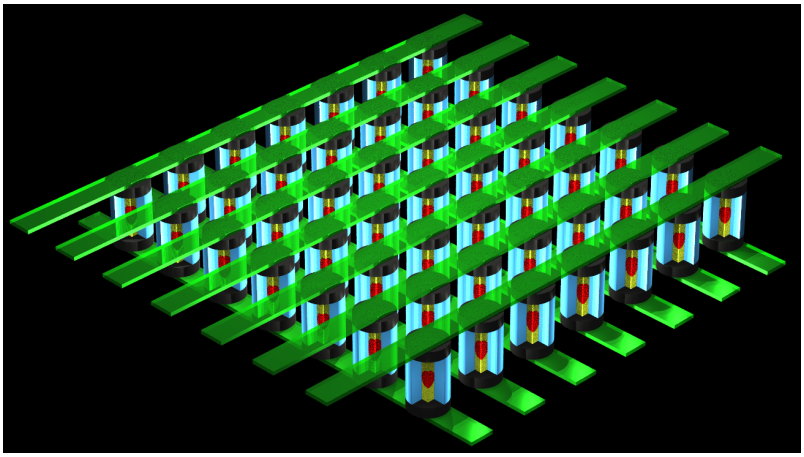

Figure 1.2: An illustration of crossbar array architecture containing synaptic memory cells at the junctions.

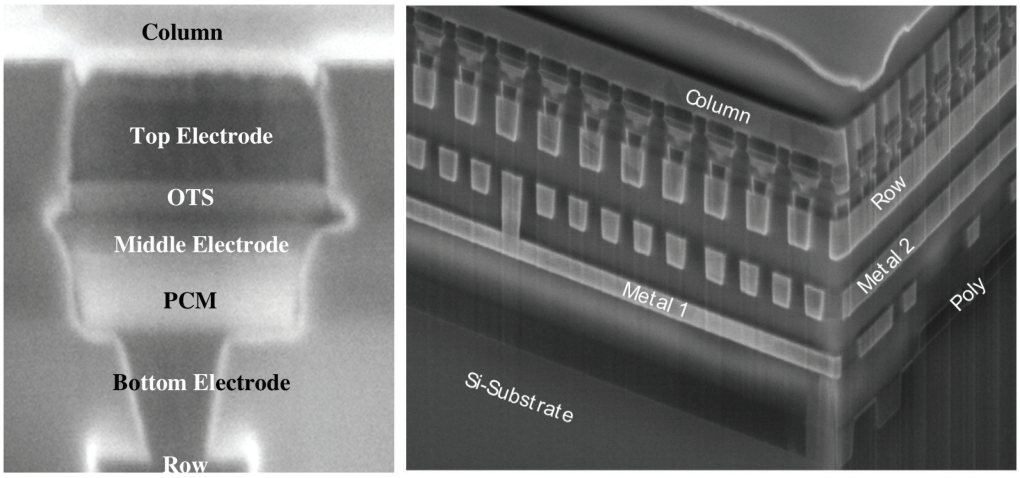

Figure 1.3: SEM cross section of combination of Ovonic Memory Switching (OMS) and Ovonic Threshold Switching (OTS) device and one floor crossbar array fully integrated with CMOS technology. Taken from [23].

Crossbar array technology with synaptic devices unveils a unique opportunity for ANN hardware to scale massively. It is previously reported that 4 bit per synapse is achievable [24, 25] and high synaptic density, 10^{10} synapse/cm^2, is possible to obtain by 100 nm pitch size, which is readily achievable by current lithographic techniques [26]. Owing to massively parallel crossbar array architecture and ultrafast READ/WRITE operations of synaptic devices, acceleration factors ranging from 20 – 2000 compared to conventional CPU/GPU based approaches are reported in neural network training [27–30]. Recently, Gokmen et al.

Table 1.1: Desirable performance metrics for synaptic devices [37].

Performance Metrics	**Targets**
Device dimensions	<20 nm×20 nm
Energy consumption	<10 fJ
Operating speed/Programming time	<1 ms
Multi-level states	20–100
Dynamic range	>4
Retention	∼10 years

achieved 30000 times acceleration and 84000 GigaOps/s/W power efficiency for training a larger ANN model which have 1 billion weights, using crossbar array of synaptic devices [31].

To achieve much further computational performance up to human brain scale parallelism, speed and power efficiency, Kuzum et al., proposed a set of desirable metrics for an ideal synaptic device to meet, which are shown at Table 1.1. Performance metrics listed in Table 1.1 has become achievable by exploiting different physical mechanisms leading to memory formation in nanoscale devices. Among these:

- Phase change devices [32]
- Resistive memory [33]
- Conductive bridge devices [34]
- Ferroelectric based devices [35, 36]

have been selected as good synaptic device candidates that offer promising features [37]. In this thesis, phase change material based synaptic devices are studied due to their outstanding performances in reliability, dynamic range, programming speed and multi-level programmable states [37].

1.2 Phase-Change Memory Technology

1.2.1 Concept

Phase-Change Memory (PCM) is a non-volatile memory (NVM) technology, exploiting the unique properties of chalcogenide materials [38]. The reports for special switching and information storage behavior of PCM date back to 1970s [39, 40]. The field matured with the discovery of novel chalcogenide alloys like $Ge_2Sb_2Te_5$ (GST) which offers several advantages such as reliability, endurance, speed and multiple programming resistance levels.

1.2.2 Basic characteristics of PCM

PCM technology is based on a PCM material (usually $Ge_2Sb_2Te_5$) sandwiched between two electrodes to form a typical memory unit, called mushroom cell (see Fig. 1.4). PCM utilizes large resistivity contrast between high resistive amorphous and low resistive crystalline phases. The ratio between fully amorphous and full crystalline states can be as large as three orders of magnitude, and gradual conductance transition between these states are experimentally demonstrated [25, 32, 37].

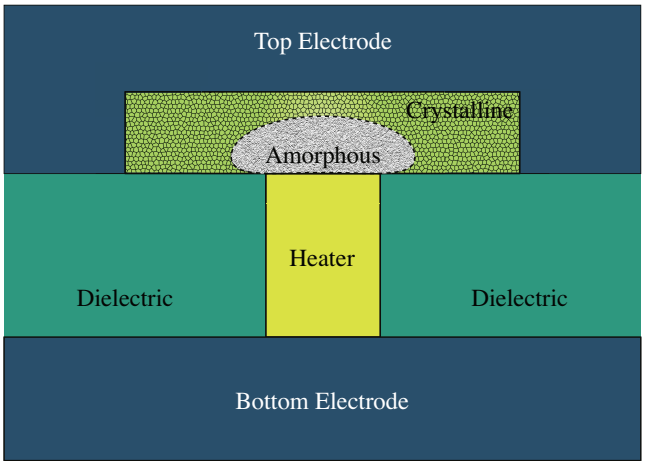

Figure 1.4: A typical mushroom cell synaptic device consists of GST sandwiched between two electrode layers.

The operating principle of PCM based synaptic device is simple. Short electrical pulses that are applied to the top electrode draw large current through the heater and increases the local temperature inside GST, via Joule heating. By controlling electrical pulse amplitude and duration, the temperature can be precisely adjusted; hence crystalline/amorphous volume ratio of GST can be programmed.

1.2.3 READ and WRITE Operations

The programming electrical conductivity of memory cell is performed through controlling temperature distribution of PCM. Fig. 1.5 demonstrates two different temperature regions which are targeted by applied short electrical pulses to tune crystalline and amorphous ratio of the device gradually.

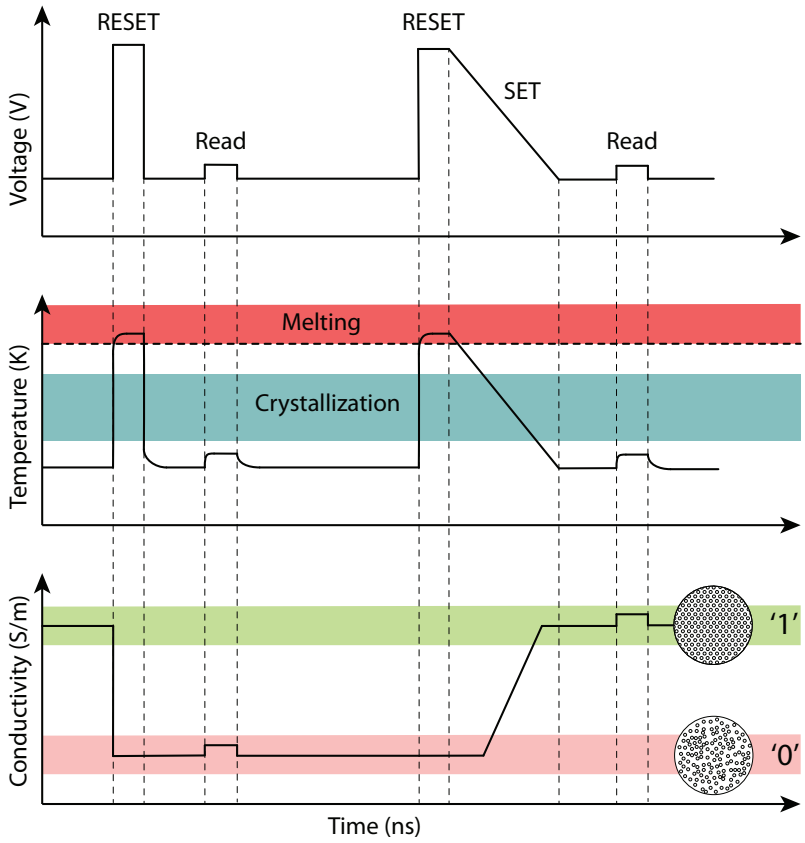

Figure 1.5: The working principle of PCM based synaptic device, with applied nanosecond voltage pulses.

The WRITE and READ operations can be summarized as follows:

1. **RESET Operation:**

   To RESET PCM into high resistive amorphous phase, a large voltage pulse (3–4 V) is applied for a short duration (∼50–100 ns). This operation increases the temperature of a specific region in PCM volume above the melting point. When the melted region is exposed to rapid cooling process, atomic structure freezes in high resistive amorphous phase. By increasing RESET voltage value, its duration, or applying consequent RESET pulse trains, the volume of melted PCM region can be gradually tuned.

2. **SET Operation:** To SET PCM into a low resistive crystalline state, the temperature level of PCM should be kept in crystallization region for some

period long enough to proceed crystallization process. This can be achieved either by applying medium amplitude voltage for a long period or by first RESET the cell then slowly decrease the temperature.

3. **READ Operation:** To READ electrical resistivity level of PCM, a small voltage pulse (~ 0.2 V) is applied such that phase stability of the device is not disturbed.

1.3 Thesis Goal

The goal of this thesis is to model temperature dependent electrical characteristics of a single synaptic device, which consists of a mushroom type memory cell and a selector device located at each junction of crossbar array.

1. Comprehensive thermoelectric model with crystallization dynamics: The memory function of the synaptic cell is based on phase state of PCM, which is controlled by heat generation induced by applied short electrical pulses. We propose a complete FEM-based simulation framework, build upon recently developed thermoelectrical characteristics and phase change dynamics of nanoscale PCM devices.

The integrity of the simulation framework and proposed thermoelectrical and phase change models will be validated on experimental results published in the literature. Therefore one goal of the thesis is to develop a proof-of-concept simulation framework in which thermal, electrical and phase change dynamics interact to represent nanoscale device characteristics accurately. The simulation method and selected physical models combined provides numerous insights into the operation of the PCM based synaptic device in nanoscale time and space resolution.

2. Simulating resistivity drift with the saturation of selector device: To realize large-scale, densely connected crossbar arrays of non-volatile memory, a selector element is required to be serially connected with a memory cell. One of the promising selector candidates is Ovonic Threshold Switch (OTS). The problem with OTS is that its resistivity, therefore threshold voltage changes with time. We propose an extension for previously introduced time and temperature dependent resistance drift model for PCM, such that saturation time of drift phenomena can be predicted for OTS selector.

The proposed drift saturation model will be validated with OTS selectors fabricated with 8 nm technology node. Therefore, the second goal of the thesis is to design a novel drift saturation model which can accurately predict the drift saturation time of fabricated selectors. Investigated OTS selector devices will be integrated into next-generation PCM crossbar technology.

Chapter 2

Thermoelectrical Simulation of PCM Based Synaptic Device

2.1 Device Modeling Techniques

Semiconductor-based devices form building blocks of today's electronics market. With the ever-increasing demand for smaller, faster and lower power requiring devices, the constant search for better semiconductor-based devices became an industry norm. Due to necessary rapid research and development iteration, researchers have shown significant interest in device modeling in the past decades. In the optimization process of design parameters such as material properties, device geometry and aging of such intricate semiconductor-based devices, device modeling and simulations play an essential role.

Device modeling is, in essence, representing the equations governing fundamental physical rules of operating device, in a closed form expression. The solution of formulated equations, if there exist, gives grounded insights on not always measurable device states (electric field distribution, temperature distribution, stress, etc.). On the other hand, the complexity of finding solutions increases with the modeling detail and intrinsic non-linear nature of the device.

2.1.1 Numerical Techniques

To solve set of equations governing physical properties of a system, the general approach is to employ numerical techniques. Solutions obtained with numerical techniques may deviate from analytical calculations. However, they are favorable when the error of approximation is small and computation time is shorter, which are usually the case in device modeling.

In semiconductor device modeling, physical equations mostly are in the form of partial differential equations with well-defined boundary conditions. The most common numerical technique to solve these equations is discretizing the equation and representing it in a finite-dimensional subspace using approaches such as finite difference method and finite element method. The numerical accuracy of these methods depends on the nature of the problem, discretization scheme employed and the numerical algorithm used.

2.1.2 Finite-Difference Method

Finite-difference method (FDM) replaces the partial continues derivatives by approximations obtained by local Taylor expansions near the point of interests. The point of interests are the nodes of a finite discrete space-time grid. Each node can be described as an approximation or an initial conditions, and edges correspond to boundary conditions. By representing a discrete finite-difference model of the problem, FDM provides a large set of algebraic equations that can be easier to solve using computational power.

2.1.3 Finite Element Method

Finite element method (FEM) is a similar method to finite-difference method except it is more powerful at studying complex device geometries. Instead of using a regular space-time grid, FEM divides the device geometry into non-overlapping

substructures called finite-elements or domains. The topology of each finite-element is defined by meshes such as linear-triangular, quadratic, triangular, linear tetrahedral. Neighbor finite elements connect each other with several nodes. Each dependent variable (temperature, voltage, etc.) is present in all nodes. With this spatial discretization step, it is assumed that each element has simpler analytical forms of continues PDEs which can be solved with numerical methods. The solutions to these equations are an approximation of the real solution of PDEs.

The solution time and memory requirement of FEM simulations scale with the multiplication of number of nodes and number of dependent variables, which is called degrees of freedom (DOF). DOF can be very large (on the order of $10^7 - 10^8$) if a semiconductor device geometry is modeled with sufficient mesh size in 3D. Therefore it is a simulation engineer's aim to optimize the number of dependent variables, mesh size/type and device dimensions to obtain the most physically accurate results using minimum DOF.

In this thesis, COMSOL Multiphysics® FEM solver software is used to model the physical properties of the device and to solve physics-based partial differential equations by finite element method. Owing to multiphysics simulation feature of COMSOL, separately declared electrical and thermal device properties, interact under Joule heating, as explained in COMSOL Implementation.

2.2 Thermoelectrical Modeling with Structural Dynamics

To gain a clear understanding of any emerging exotic technology, it is necessary to obtain a grounded representation of physical dynamics governing the device operations. In a PCM based synaptic device, prominent physical dynamics are electrical, thermal and molecular structure dynamics that are intricately interacting with each other during device operation. Thus, developing a complete

simulation infrastructure for PCM based synaptic devices provides an opportunity to observe complex physical interactions on nanoscale time/space, which are not always easy to foresee or to be measured.

As PCM based synaptic device dimensions shrink to meet higher density requirements of crossbar arrays, the fabricated synapse dimensions dropped to below 100 nm in recent years [41, 42]. Given this aggressive scaling trend and complex thermoelectrical and molecular structure dependent device state; achieving promised device characteristics via optimizing the process flow becomes another significant challenge. Detailed modeling of a synaptic device, can save tremendous amount of money and time by reducing the number of fabrication iterations required to understand working principles of such devices. Additionally, device modeling offers profound insight to nanoscale device properties (electric field and temperature distribution, crystallization probabilities, etc.) which are impossible to be measured.

Based upon motivations listed above, several phase change material based synaptic device simulations have been recently proposed in the literature. The first type simulations have considered SPICE modeling to obtain IV curves of PCM based synaptic devices. Some researchers developed SPICE models consisting of temperature sensing and storage sub-circuits to change device resistivity between two discrete SET and RESET levels, using a calculation of device temperature based on input current [43, 44]. A more advanced model is proposed by Li et al., which provides continues resistivity transition between SET and RESET states using temperature dependent electrical conductivity of a constant size amorphous volume [45].

While SPICE models provide faster simulation time and more advanced circuit simulation interface compared to FEM, by operating at too high abstraction level, they lack sufficiently detailed information of the device. If the aim of simulation is to understand the complex interaction between electrical transportation, thermal behavior, structural dynamics and device geometry; SPICE simulations are not practical due to following reasons:

1. Any spatially dependent material property is overly simplified. For example, SPICE models calculate a homogenous temperature distribution for a PCM based synaptic device. However, the temperature difference of two points inside PCM can be as high as 700 K.

2. SPICE models hyper-parameters should be tuned whenever device geometry (hotspot radius, bottom electrode thickness, etc.) changes.

First FEM simulations of PCM based synaptic devices solely focused on temperature distributions caused by Joule heating inside mushroom-type device geometry. Yin et al. demonstrated that decreasing electrical conductivity of crystal region due to nitrogen doping, increases I_{RESET}, however, assumes no electrical or thermal material property dependence of temperature and simulated only fully crystal configuration [46]. Kuzum et al. reported tunability of the amorphous region and temperature distribution of initially fully SET device after applying different RESET voltage pulses [32]. More improved thermoelectrical simulation is proposed by Le Gallo et al., utilizing an electrical transportation model following Poole-Frenkel effect, thermoelectrical Seebeck and Peltier effects and thermal boundary resistances [47]. They successfully proposed thermally activated threshold switching mechanism; nevertheless, proposed simulation is designed only for simulating RESET operations.

SET operation of the synaptic device, unlike RESET operation, is a stochastic process [48, 49]. Hence supporting SET operation in FEM/FDM simulation requires implementation of probability assignment of nucleation and following crystal growth mechanisms. Kim et al. and Cinar et al. implemented Classical Nucleation Theory based SET model into FDM simulation to study temporal and spatial characteristics of switching operations and phase transitions [50]. However, this simulation ignored field dependence of electrical conductivity of amorphous PCM, which has been reported as primary electrical transportation below switching region due to prominent Poole-Frenkel effect [39, 47, 51, 52]. Besides, thermal boundary resistances (TBR) and temperature dependent thermal conductivity of materials that have significant effects on thermal device property

was not included in the report [53]. Reifenberg et al. proposed a similar simulation model with TBR support however ignored any field-temperature dependent material property and violated non-dimensionalization of transient heat transfer requirement of FEM by simulating a material with high thermal conductivity using too coarse mesh size with too small time steps [54]. Recently, Cinar et al. reported programmable intermediate resistance levels on a PCM based synaptic device on FEM simulation, but employed temperature and field independent material properties and neglected TBR effects [55].

In this thesis, a comprehensive thermoelectrical finite element model simulation is proposed. Unlike previous work, our simulation infrastructure supports both gradual RESET and SET operations, includes field and temperature dependent material properties and thermal boundary resistances to capture internal dynamics of a PCM based synaptic device closely.

2.2.1 Multiphysics Models of Phase Change Materials

In this section, we provide a detailed list of electrical, thermal and phase change properties of PCM. These material properties have been accepted to capture physical dynamics of PCM and implemented in our simulation framework.

2.2.1.1 Electrical Model

The programming (SET and RESET) and reading (READ) operations of the synaptic device are initiated with applied nanosecond wide voltage pulses to top electrode of the device. The current passes through device mostly dependent on the electrical conductivity of phase change material and electrodes. Electrodes practically have constant electrical conductivities, on the other hand, the electrical conductivity of phase change material is highly dependent on temperature and electric field.

Amorphous materials follow exponential current-voltage dependent ($\sigma \propto \exp(\alpha V^{1/2})$) Poole-Frenkel conductivity model [56]. The Poole-Frenkel effect suggests that thermal excitation and strong electric field release trapped carriers from ionizable defect centers which are believed to create Coulomb potential well in highly disordered amorphous materials [56, 57]. Amorphous conductivity dominated RESET state of phase change materials is also shown to be following this conduction mechanism in subthreshold region [39, 51]. Recently, Le Gallo et al. proposed an extended version of Poole-Frenkel effect based subthreshold conduction mechanism for chalcogenide materials and validated it against a wide range of ambient temperatures and applied potentials [52]. The proposed conduction mechanism is given below:

The Poole-Frenkel effect suggests that the ionization energy barrier is lowered between ionizable defect centers by a factor of $\beta F^{1/2}$. β is Poole-Frenkel constant and defined as:

$$\beta = \frac{e^2}{\sqrt{e\pi\epsilon_r\epsilon_0}}, \tag{2.1}$$

where e is electric charge, ϵ_0 is vacuum dielectric constant and ϵ_r is relative permittivity of material. The potential profile between two Coulombic wells is considered as:

$$V(r, \theta, F) = -eFr\cos(\theta) - \frac{\beta^2}{4e}(\frac{1}{r} + \frac{1}{s-r}) + \frac{\beta^2}{es}, \tag{2.2}$$

where F is applied electric field, $r = 0$ and $r = s$ are trap locations with s defining inter-trap distance. θ is the angle between electric field and direction of the escape, which allows modeling of all possible escape scenarios for trapped charge carrier. The potential profiles calculated with Eq. 2.2 between two Coulombic traps are shown in Figure 2.1 for two different escape routes $\theta = \pi$ and $\theta = 0$. The Poole-Frenkel effect reduces to potential barrier of escape significantly when electric field and emission are in the same direction ($\theta = 0$).

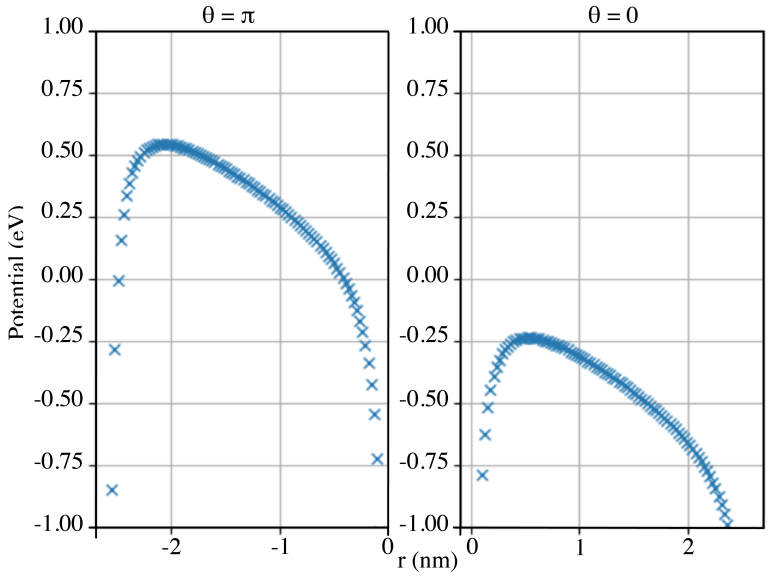

Figure 2.1: The amount of energy barrier may increase or decrease significantly due to the direction of strong electric field (3×10^8 V m^{-1}).

The amount of barrier lowering due to Poole-Frenkel effect can be calculated as:

$$E_{PF}(F, \theta) = -\max_{r} V(r, \theta, F), \tag{2.3}$$

which is approximately 0.25 eV in Fig. 2.1. We observed that for low E-fields, this model estimates the amount of barrier lowering very similar to model proposed by Ielmini et. al ($\Delta\theta = q\sqrt{qV/\pi\epsilon_r u_a}$). On the other hand, in high E-fields ($F_T > (\beta/e\Delta z)^2$), this model attains two order of magnitude stronger barrier lowering [51].

For electrons, in order to calculate the density of free carrier under applied electric field F, Boltzmann statistics is assumed rather than Fermi-Dirac statistics. To calculate density of free charge carrier emission to complete sphere the following formula is used:

$$n(F,T) = \frac{K}{4\pi}\int_0^{\pi} \exp\left(-\frac{E_a - E_{\mathrm{PF}}(F,\theta)}{k_{\mathrm{B}}T}\right) 2\pi\sin(\theta)d\theta. \tag{2.4}$$

In Eq. 2.4, θ is defined as the angle between the applied electric field and the direction of emission of a trapped electron, K is a free parameter, E_a is the activation energy and E_{PF} is calculated barrier lowering due to Poole-Frenkel effect. 3D spherical emission of trapped charge carriers is important to capture experimentally observed Ohmic behavior of the material in the low fields [52, 58]. The activation energy used in Equation 2.4 is assumed to be changed with temperature following Varshni Equation ($E_a = E_{a0} - \xi T^2$) since temperature dependence of optical bandgap is observed in the literature [59].

Once free carrier density is calculated, field and temperature dependent electrical conductivity of amorphous region of synaptic device is obtained by $\sigma(F,T) = e \cdot \mu \cdot n(F,T)$.

2.2.1.2 Thermal Model

For any applied power, temperature distribution changes according to thermal, electrical and structural state of the synaptic device. Even though electrical input and outputs are the observables, temperature distribution is the most critical factor that determines the resistivity state of the device by controlling crystallization and amorphization processes. In a mushroom shape device topology, the region where temperature distribution is localized is called the hotspot. The dashed line in Figure 2.2 shows the approximate hotspot region where the temperature reaches its peak value.

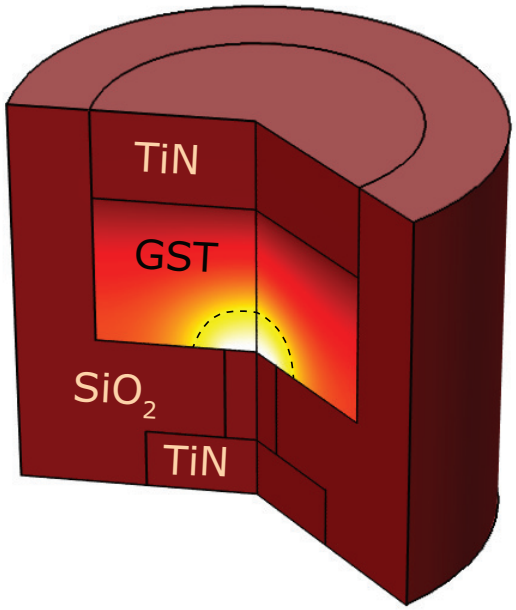

Figure 2.2: Thermal distribution of synaptic device is shown. Temperature is localized above the heater, which is called hotspot point.

Wiedemann-Franz Law suggests that in metals, charge carriers dominates the thermal transport, hence thermal conductivity and electrical conductivity showing a first order relationship [60]. Recently, Risk et al., experimentally (see Figure 2.3) demonstrated with 3ω method that thermal conductivity of both GST and N-doped GST follow Wiedemann-Franz law [61]. Hence, we assumed both amorphous and crystalline phases of GST to follow Wiedemann-Franz law, whereas electrodes and dielectric material assumed to have constant thermal conductivities.

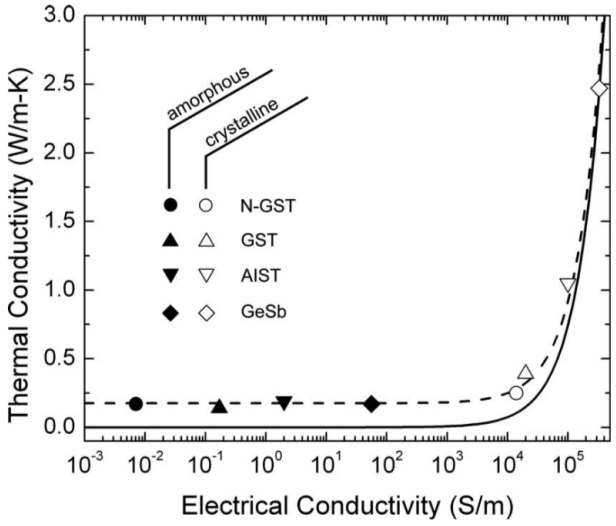

Figure 2.3: Thermal conductivity of various chalcogenide materials [62].

Wiedemann-Franz law is given as follows:

$$\frac{\kappa}{\sigma} = LT, \tag{2.5}$$

where κ is thermal conductivity, σ is electrical conductivity, L is the Lorentz number, and T is the temperature in Kelvin.

2.2.1.3 Crystallization Model

A particularly significant property of phase change materials is crystallization process that occurs in nanoscale time and volume [63]. Unlike amorphization of molten phase, crystallization is a complicated process including stochastic nucleation and growth of independent crystalline clusters. The existing theories of nucleation dynamics are mainly based on JMAK Theory and Classical Nucleation Theory (CNT) [48, 64]. However, for PCM based synaptic devices, JMAK theory is shown to be inapplicable due to following drawbacks listed by Senkader et al. [65].

1. JMAK theory requires uniform and random nucleation process inside GST. However, it is experimentally shown that nucleation starts at GST interfaces. Ohshima and Kashchiev et al. throughly studied the influence of interface crystallization [66, 67].

2. Contrary to JMAK theory, nucleation rate in PCM has been proved to be a time-dependent process [68]. The required time period for nucleation to occur is called incubation time.

One CNT based nucleation and growth mechanism of PCM is proposed by Senkander et al. [65]. This extended version of CNT, explains the nucleation and growth mechanism of PCM:

The amount of free energy, ΔG, required by a formation of a cluster is given by:

$$\Delta G = 4\pi r^2 \sigma - n\Delta g, \tag{2.6}$$

where σ is the interfacial energy density between amorphous and crystalline phases and r is the radius of the cluster if clusters are assumed to have spherical shapes. Therefore, number of GST molecules in one cluster can be calculated with

$$n = \frac{4}{3}\pi\frac{r^3}{v_m}, \tag{2.7}$$

where v_m is the volume of GST molecule. The approximation of Δg in Eq 2.6, is calculated by Singh et al. for phase change material as:

$$\Delta g = \Delta H_f \frac{T_m - T}{T_m}\left(\frac{7T}{T_m + 6T}\right)v_m, \tag{2.8}$$

where T_m is melting temperature and ΔH_f is the enthalpy of fusion at the

melting point which can be estimated via differential scanning calorimetry experiments [69]. The free energy calculated by Eq 2.6 increases with the number of molecules in the cluster up to a certain critical n_c given by:

$$n_c = \frac{32\pi}{3}\frac{v_m^2\sigma^3}{\Delta g^3}. \tag{2.9}$$

Therefore the critical value of ΔG can quantify energy barrier for nucleation, which is:

$$\Delta G_c = \frac{16\pi}{3}\frac{v_m^2\sigma^3}{\Delta g^2}. \tag{2.10}$$

From here, steady-state nucleation rate per unit volume of GST can be approximated by:

$$I_{ss} = \frac{4k_BT}{3\pi\lambda^3\eta}n_c^{2/3}\sqrt{\frac{\Delta g}{6\pi n_c k_B T}}\exp\frac{-\Delta G_c}{k_B T}, \tag{2.11}$$

where η is temperature dependent viscosity of GST, calculated by $1.94 \times 10^{-14}\exp(\frac{2\pm0.1}{k_BT})$ $\mathrm{kg\,m^{-1}\,s^{-1}}$ [65]. Figure 2.6 shows the time dependence of nucleation, where nucleation starts between 400-600 K, with a peak around 500 K.

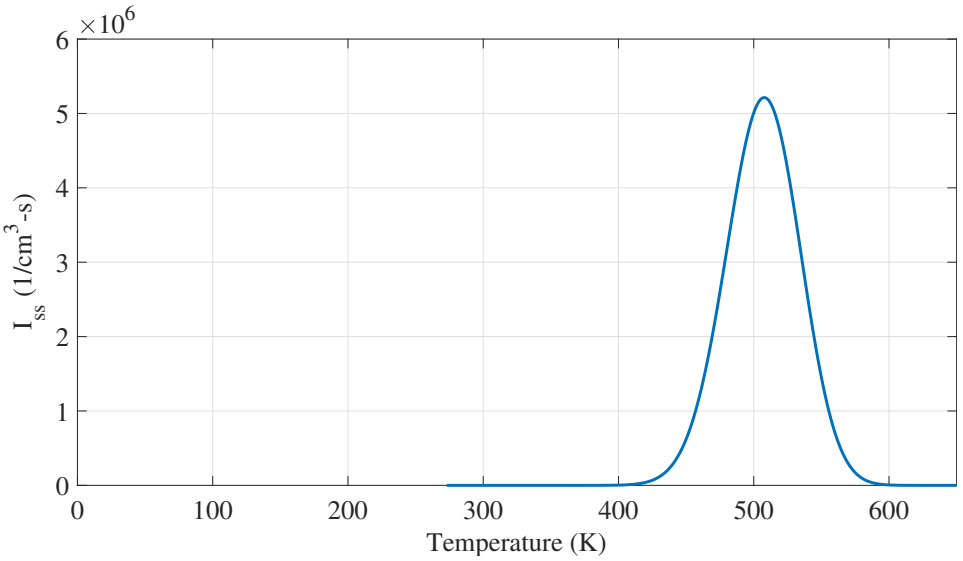

Figure 2.4: Steady state homogeneous nucleation rate.

Homogeneous nucleation is not the only nucleation process that effects GST. Heterogeneous nucleation which takes place in the material contacts with other molecular species is much more dominant for GST, as it is more frequently observed in the nature [67]. This is because contacts with different materials cause surface impurities and lattice defects which usually lower surface energy, hence reduces the required free energy barrier for the nucleation. The heterogeneous nucleation rate of interface molecules is calculated by:

$$\frac{I_{ss,het}}{I_{ss,hom}} = \epsilon \exp(\frac{\Delta G_c}{k_B T}[1 - f(\theta)]), \tag{2.12}$$

where ϵ is adjustable factor, $f(\theta) = ((2 + \cos(\theta))(1 - cos(\theta))^2)/4$ and θ is the wetting angle, which is experimentally demonstrated as under 20 degrees. It is clear in Eq. 2.12 that heterogeneous nucleation is exponentially more probable than homogenous nucleation.

As previously shown by Kashchiev, both homogeneous and heterogeneous nucleations are time-dependent processes and require an incubation time to reach its steady state value represented by Eq. 2.11 [67]. The transient effect of nucleation can be calculated by:

$$I_{trans} = I_{ss}\sqrt{\frac{4\pi\tau_s}{t}}\exp(\frac{-\pi^2\tau_s}{t}), \tag{2.13}$$

where τ_s is incubation time constant which defined as:

$$\tau_s = \frac{1}{\pi^3 n_c^{2/3}\gamma\frac{\Delta g}{6\pi n_c k_B T}}. \tag{2.14}$$

.

Figure 2.5 shows an important incubation property of nucleation that even in the ideal nucleation temperature, the required time for nucleation to start is on the order of 0.1 milliseconds.

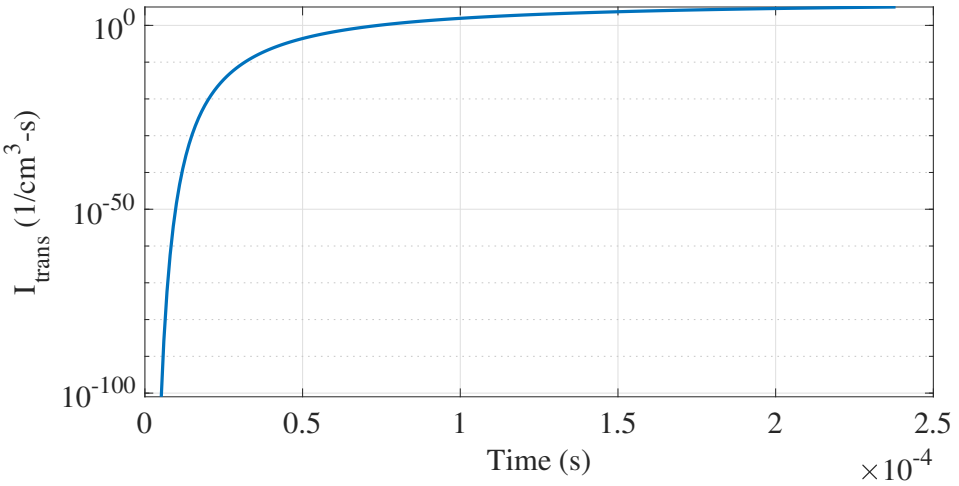

Figure 2.5: Transient nucleation rate, I_{trans} converges to I_{ss} during incubation time.

Crystal Growth Model:

Once nucleation occurs with stochastic nature, crystallized nuclei clusters may grow by attachment of GST molecules. Crystal growth is a nucleation mediated event, and like the nucleation, it is both time and temperature dependent. The rate of growth is well studied by *ab-initio* molecular dynamics simulations; however, transfer of obtained knowledge to FEM or FDM simulations are limited given the observation from *ab-initio* simulations can capture only picosecond time

events [63]. According to a widely accepted model of crystal growth developed by Kelton and Geer, temperature dependent growth rate can be calculated by:

$$\frac{dr}{dt} = \frac{16k_BT}{3\pi^3\lambda\eta}\left(\frac{3v_m}{4\pi}\right)^{1/3}\sinh\left(\frac{1}{2k_BT}\left(\Delta g - \frac{2\sigma}{r}v_m\right)\right), \tag{2.15}$$

where Δg is calculated with Eq. 2.6 [70]. This growth model assumes that nuclei clusters have spherical shape and attachment of GST molecules increases the radius of the cluster. Due to the increase of cluster radius with growth, the curvature of cluster interface become more flattened. Therefore the rate of attachments of new GST molecules accumulates. The growth rate dependence of cluster radius and temperature is given in Fig. 2.6.

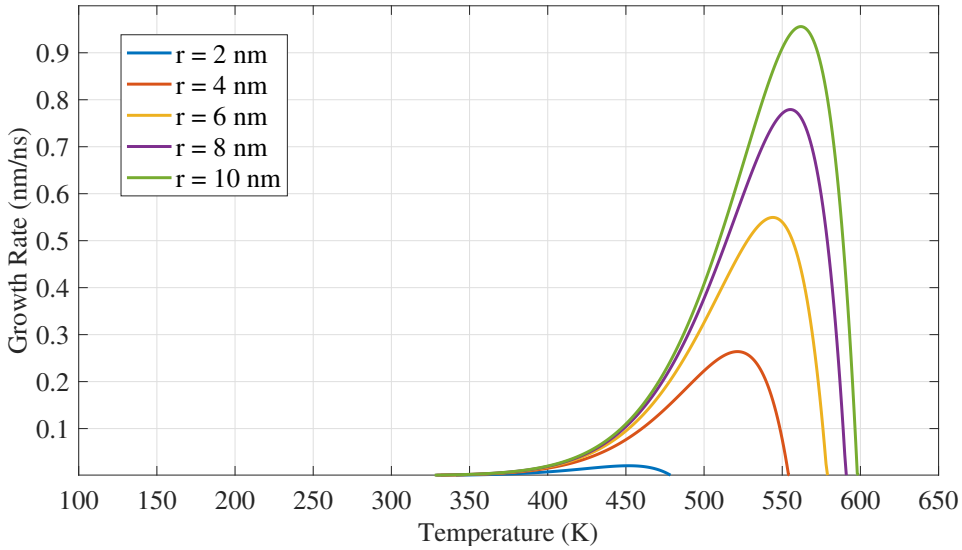

Figure 2.6: Growth rate dependence on temperature and cluster size.

2.2.1.4 Amorphization Model

In the presence of a large current input (300-500 µA) temperature around hotspot increases to a point, T_m, where chalcogenide material melts and changes to the liquid phase. If the current pulse is to end with a very short trailing edge, hotspot temperature drops rapidly, and the bonds cannot be rearranged due to the short

span of time. The phase change material is therefore left in high-resistivity amorphous state [71]. In the majority of PCM simulations, momentarily existed liquid phase is not included to simplify phase transition model [32, 47, 53, 55]. Crystal to amorphous phase change is assumed to occur instantly when the temperature exceeds melting temperature of phase change material.

In summary, there are three principal thermally operational regions in GST based synaptic device: nucleation region, growth region, and amorphization region. As Fig 2.7 shows, heterogeneous nucleation favors 600-750 K and crystal growth is confined approximately between 500-600 K, while any region inside GST with higher than melting temperature, melts and become amorphous.

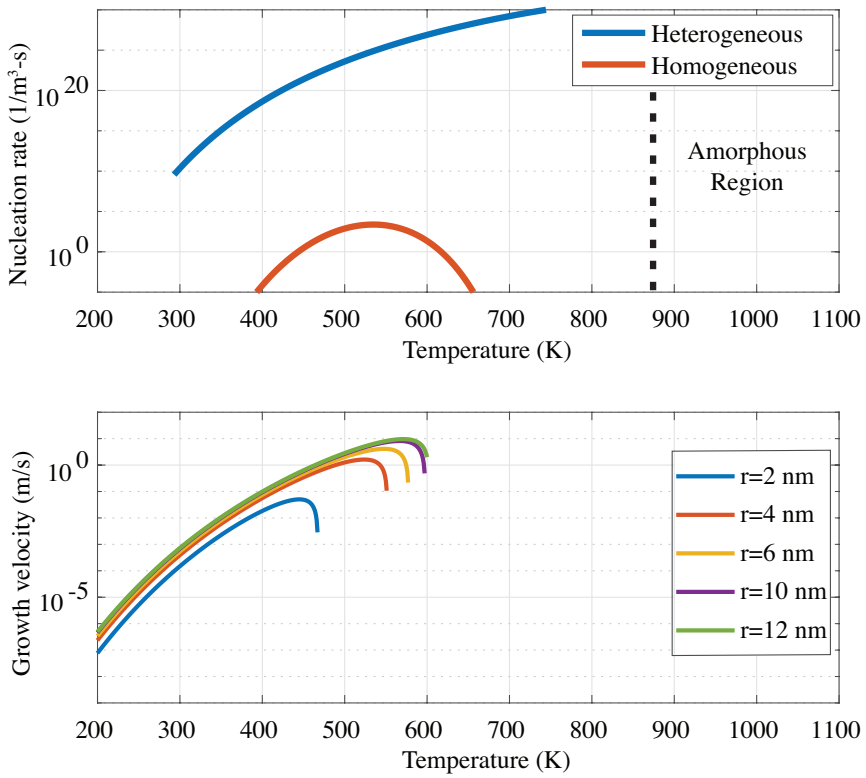

Figure 2.7: A PCM based synaptic device has three main regions, where device conductivity can be tuned with adjusting temperature for nucleation, growth or amorphization.

2.2.2 Simulation Approach

In this section, we provide a detailed description of our simulation framework which employs thermal, electrical and phase change models previously explained in Multiphysics Models of Phase Change Materials. FEM simulation settings, nucleation calculation details and coupling between COMSOL Multiphysics and MATLAB are explained.

2.2.2.1 Device Geometry

In simulations, a fixed geometry mushroom type synaptic device consisting of GST based active region sandwiched between two Titanium Nitride (TiN) electrode is used. The bottom electrode is connected to GST by a heater with 40 nm diameter. The device is electrically isolated with Silicon Oxide (SiO_2). Device geometry is chosen to be comparable in size with previously reported devices in the literature to make a fair comparison of experimental and simulated results.

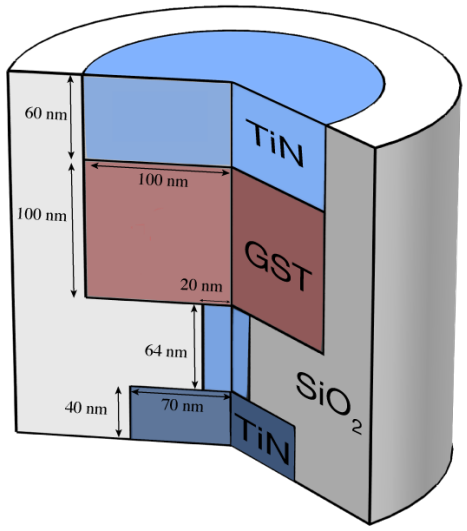

Figure 2.8: A mushroom type synaptic device with GST sandwiched between top and bottom electrodes.

2.2.2.2 COMSOL Implementation

Electrical Module: Electrical characteristics of the synaptic device is implemented using *Electric currents (ec)* module at COMSOL. *Electric currents* module calculates current density, electric field and voltage distribution inside the device. Using the applied voltage to device, Eq. 2.16 is solved at each simulation time step to obtain electric field distribution inside the device. Then Eq. 2.17 is computed to obtain current density using conservation of current:

$$E = -\nabla V \tag{2.16}$$

$$\nabla \cdot \vec{J} = \nabla \cdot \left(\sigma \vec{E} + \vec{J}_e \right) = 0, \tag{2.17}$$

where σ is temperature and field dependent electrical conductivity of conductive materials.

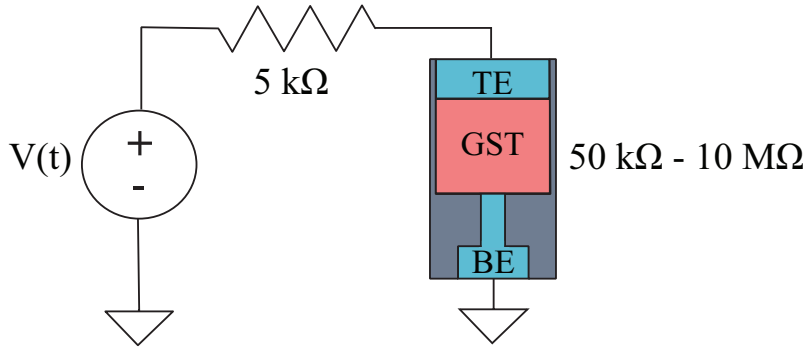

Figure 2.9: Electrical circuit that is used to apply potential to synaptic device.

The demonstrated electrical circuit in Fig. 2.9 is implemented by *Electrical circuit (cir)* module at COMSOL to simplify crossbar array cross section, where the voltage pulse is applied to the top electrode, and the bottom electrode is grounded. A 5 kΩ resistance is used to coarsely model the impact of load resistivity, which is employed in some of the experimental devices [47].

Concerning boundary conditions, GST-TiN interface is modeled to have a contact resistance of 2.6×10^{-11} $\Omega\,\mathrm{m}$ [47]. The outside of surrounding SiO_2 region is modeled as electrical isolation, $(\vec{n} \cdot \vec{J} = 0)$.

Thermal Module:

Thermal characteristics of the synaptic device is implemented using *Heat transfer (ht)* module at COMSOL. *Heat transfer* module calculates the temperature distribution within the synaptic device by solving heat diffusion equation (Eq. 2.18):

$$\rho C_p \frac{\partial T}{\partial t} + \rho C_\rho \mathbf{u} \cdot \nabla T = \nabla \cdot (\kappa \nabla T) + Q_{ext}. \tag{2.18}$$

The heat flow formulation describes the relationship between material density, ρ, heat capacitance, C_p, thermal conductivity, κ and additional heat source, Q_{ext}, which is due to applied voltage pulses (Joule heating) and calculated with $Q_{ext} = J^2/\sigma$, where J is current density by Eq. 2.17.

Table 2.1: Thermal boundary resistivity values that are used at GST boundaries.

	Thermal Resistivity ($\mathrm{m^2\,K\,GW^{-1}}$)
GST-TiN	26
GST-SiO_2	70

Thermal boundary resistance (TBR) exists between two different heat conductive materials due to energy carrier mismatch (mostly phonons in heat conduction) during transversing at the interface. The thermal boundary resistance values used between GST-TiN [72] and GST-SiO_2 [73] in the simulation are given at Table 2.1.

Considering thermal boundary conditions, the parts of top and bottom electrodes that are in contact with air is assumed to be constant at room temperature. The distance between neighbor synaptic devices is assumed to sufficiently large, therefore SiO_2 is modeled to allow convective heat flux as each synaptic device is confined by large SiO_2 isolation. To approximate heat flux from device boundary, thermal heat transfer coefficient, h, is matched with actual thermal environment as proposed by Le Gallo et al [47]:

$$
\begin{aligned}
q &= h\Delta T = hqAR_{th} \\
R_{th} &= \int_{r_s}^{\infty} \frac{1}{\kappa_{th}} \frac{\partial r}{\partial 4\pi r_s^2} \\
&= \frac{1}{4\pi r_s \kappa_{th}} \\
\therefore \quad h &= \frac{\kappa_{th}}{r_s},
\end{aligned}
\tag{2.19}
$$

where h is heat transfer coefficient, q is heat flux, R_{th} is the thermal resistance silicon dioxide, κ_{th} is the effective thermal conductivity of silicon dioxide, and r_s is the radius of the synaptic device.

2.2.2.3 MATLAB Implementation

MATLAB takes temperature and field distribution as inputs from COMSOL, in each simulation time step and determines amorphous and crystalline regions with their corresponding electrical and thermal conductivities using previously explained models. For each sufficiently small simulation time step (Δt = 0.1 ns), transient nucleation rate in Eq. 2.13 is calculated via MATLAB. However, Eq. 2.13 requires constant temperature during millisecond long incubation time. Therefore, special care is taken to discretize Eq. 2.13 for each time step by:

$$
I^*_{trans}(T_n) = I^*_{trans}(T_{n-1}) + [I_{ss}(T_n)\sqrt{\frac{4\pi\tau(T_n)}{t}} - I^*_{trans}(T_{n-1})] \exp{(-\frac{\tau(T_n)}{t})},
\tag{2.20}
$$

where $I^*_{trans}(T_n)$ is the nucleation rate in the n^{th} time step, and $I^*_{trans}(T_{n-1})$ is the transient nucleation rate calculated at the end of $(n-1)^{\text{th}}$ time step. I^*_{trans} corresponds to nuclei formation in unit time and volume, therefore it can be interpreted as constant rate for a Poisson distribution. The probability of forming m nuclei in a unit time interval is

$$P_m = \frac{N^m}{m!} \exp(-N), \tag{2.21}$$

where N is average number of nuclei that form in the interval. Therefore the probability $P^*(t_j, V, I^*_{trans})$ that at least 1 nucleus has formed in time interval t_j and in volume V, given transient nucleation rate is:

$$P^*(V, t_j, I^*_{trans}) = 1 - \exp(-V t_j I^*_{trans}). \tag{2.22}$$

Once homogenous and heterogeneous nucleation probabilities per unit volume and time step are calculated with Eq. 2.22, newly created nuclei positions inside GST can be determined. Each calculated mesh probability is compared with a random number sampled from a uniform distribution between 0 and 1, inclusive. If calculated probability is higher than the generated floating random number, the mesh state is declared as nucleated.

2.2.2.4 Infrastructure for FEM Modeling of PCRAM Device

To implement probabilistic homogenous and heterogeneous nucleation, COMSOL is required to be coupled with an external computing software since calculating nucleation probability and sampling from the distribution in Eq. 2.22 was not supported by COMSOL. Hence, we utilized COMSOL Multiphysics® via LiveLink™ for MATLAB® which allows exporting temperature and electric field distributions calculated at COMSOL, into MATLAB to determine the material properties and return to COMSOL for the subsequent time step.

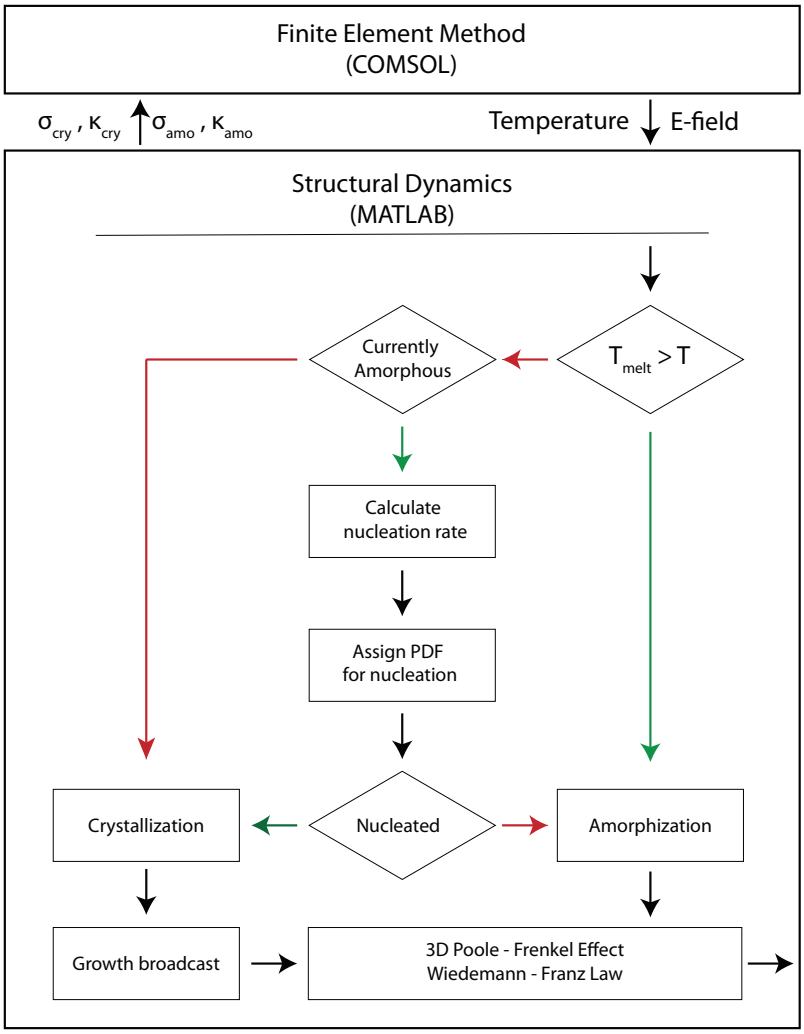

Figure 2.10: A diagram showing the coupling between COMSOL and MATLAB in each simulation time step.

In a nutshell, COMSOL-MATLAB coupling works as follows (see Fig. 2.10):

1. Starting with initial crystalline / amorphous volume ratio, based upon applied voltage pulse, COMSOL calculates transient potential and thermal distributions inside GST for 0.1 ns.

2. MATLAB takes temperature and field distribution, interpolates the data into its own 2 nm $\times$ 2 nm meshes, which is the minimum size for a crystalline nuclei can exist.

3. First, MATLAB checks whether each mesh is melted by comparing simulation temperature to melting temperature (T_{melt} = 877 K).

4. If a mesh is not melted in this time step, but already amorphous, transient homogenous and heterogeneous nucleation probabilities ($P^*(V, t_j, I^*_{trans})$) are calculated, and nucleation decision is made afterward.

5. The growth rate ($\partial r/\partial t$) is calculated and for each nuclei clusters, as a function of local temperature and cluster radius. If conditions fit, clusters grow.

6. Once determining amorphous and crystalline regions inside GST, using Poole-Frenkel and Wiedemann-Franz Law, space-dependent electrical and thermal conductivity of GST is returned to COMSOL for the next 0.1 ns simulation.

7. Special care is taken to initiate next COMSOL simulation run with previously found solution vector (U) and solution vector gradient ($\dot{U}$).

2.3 Validation of Thermoelectric Model with Structural Dynamics

To validate complex interaction of selected electrical, thermal and structural models of the synaptic device under proposed simulation framework, several tests are conducted. These tests are selected according to their similarity to previously reported experiments.

2.3.1 Electrical Model Tests

The first electrical test to validate electrical characteristics of proposed models is to investigate electrical conductivity of different device states. In this test, the synaptic device is generated with different amorphous dome volumes, and

electrical conductivity of the device is tested with conventional 0.2 V READ voltages as in the literature [44, 74–76]. The low voltage READ operation is necessary as thermally activated Poole-Frenkel electrical transportation otherwise increases the observed conductivity level or disturbs the device state. The unchanged temperature distribution of the device during READ can be seen at RESET-and-READ simulation, shown in Figure 2.16.

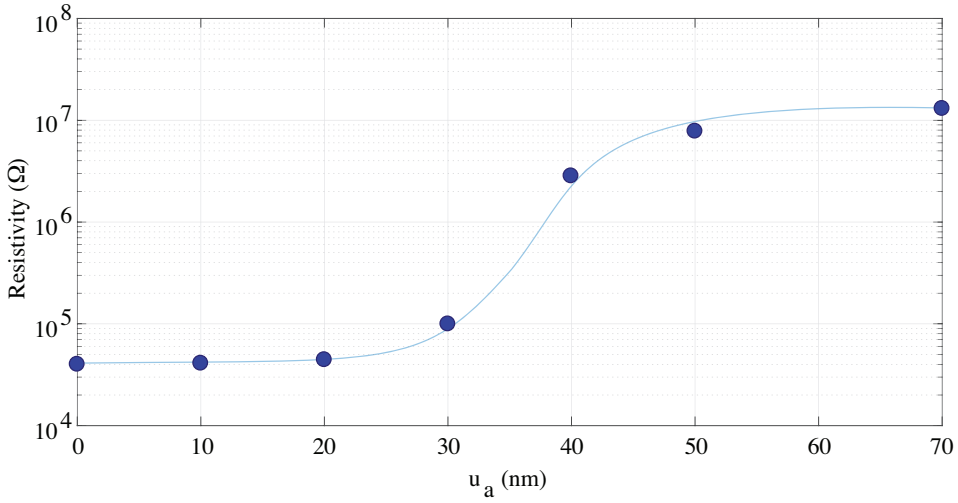

Figure 2.11: Electrical characteristics are tested for different sizes of amorphous regions by 0.2 V READ voltages to avoid thermal activation of Poole-Frenkel effect.

Figure 2.11 demonstrates that as amorphous dome radius increases, the resistivity of the synaptic cell increases. The sigmoid-like trend is closely matched with experimentally demonstrated results and satisfies large resistivity window (on/off ratio) between fully SET and fully RESET states [74, 77, 78].

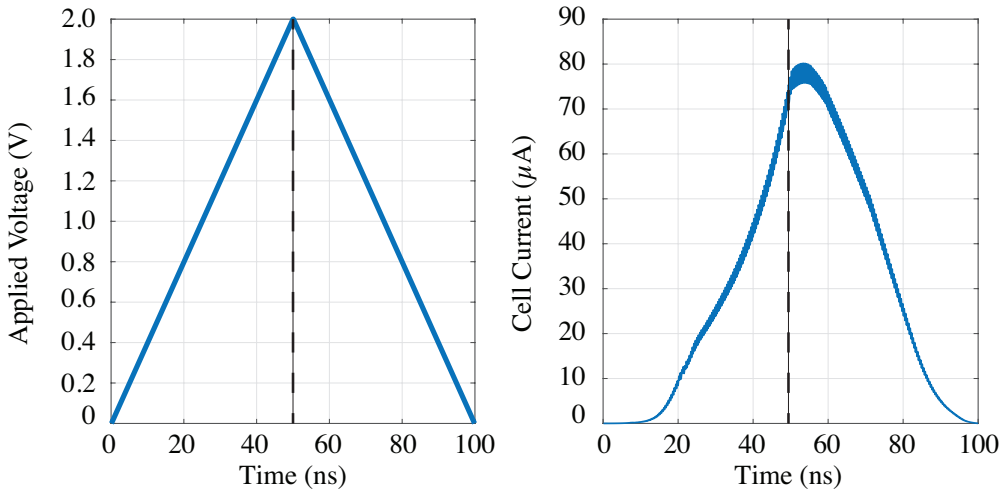

Figure 2.12: Applied ramped voltage showing the effect of asymmetric cell current due to temperature dependent Poole-Frenkel electrical transportation model.

The second electrical conductivity test is conducted to demonstrate the effect of thermally activated three-dimensional Poole-Frenkel effect. A ramped voltage pulse is applied to the device to observe the effect of different temperature profiles. During the first 50 ns, device temperature rises and cell current starts to break linearity due to Poole-Frenkel effect (see Fig. 2.12). As voltage starts to decrease, the current passing through the cell decreases but due to the high-temperature profile, conductivity shows an asymmetric tail characteristic.

2.3.2 Thermal Model Tests

To validate the thermal model, two different tests are conducted. First, the temperature distribution in the synaptic cell is analyzed after applying a typical RESET pulse level. Second, the thermal time constant of the device is calculated to prove that thermal dynamics are as fast as reported in the literature.

In Fig. 2.13, temperature profile of simulated mushroom shape device reaches up to maximum 1600 K locally, while overall hotspot temperature is around 1400 K just after applying a RESET pulse with amplitude of 2.5 V with (2.5 ns/20 ns/2.5 ns) rise/width/fall time. The maximum hotspot temperature is a good agreement with reported temperature values of 1400–1800 K, obtained after RESET pulses [79].

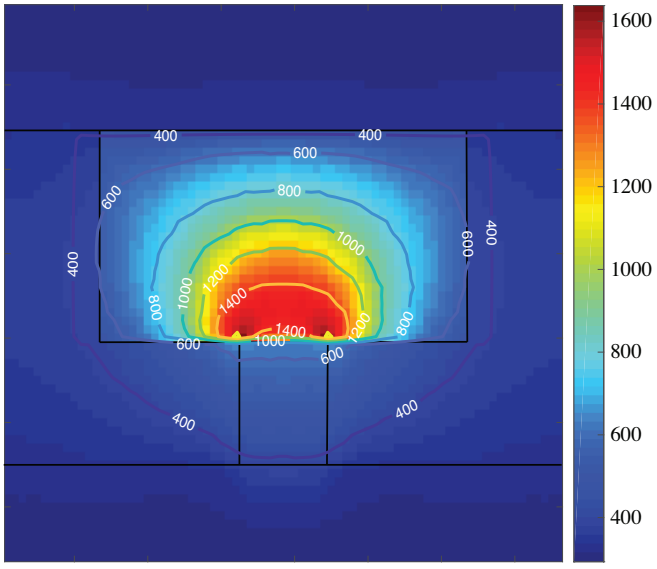

Figure 2.13: Temperature profile of synaptic device after applying 20 ns, 3.5 V RESET pulse.

Thermal time constant of synaptic device is also calculated with the method proposed by Reifenberg et. al,: $\tau_{th} = \Delta T_m / RC_{th}$, where RC_{th} is approximately 2.9×10^{11} K s^{-1} and ΔT_m is the temperature change required to melting, yielding τ_{th} to be $2-3$ ns. This value is in the range of what is expected in experimentally observed very fast thermal dynamics of PCM based nanoscale devices [47, 72].

2.3.3 RESET Programming Tests

RESET tests are conducted to check the agreement of simulated device and experimentally reported device states after RESET operation. Before starting RESET tests, the device is manually programmed into the fully SET state. In the literature, RESET pulses are usually constant-current pulses. However, in our simulation which couples COMSOL and MATLAB, we observed that applying a current pulse breaks the temperature stability of simulation and leads to unrealistic temperature and electric field calculations. Hence alternatively, we applied large voltage pulses (between 3–4 V) with (2.5 ns/20 ns/2.5 ns) rise/width/fall times and made sure that temperature and current is stable inside the synaptic device during the RESET operation. The stabilized current level through the device is assumed to be I_{RESET}. After applying RESET pulses, the device cooled down for 15 ns then 0.2 V READ pulse is applied to measure the final programmed conductivity of the synaptic device.

Fig. 2.14, shows applied RESET currents vs. final resistivity state of the synaptic device. RESET pulses with less than 100 µA did not increase device temperature enough to melt, hence fall short for initiating RESET operation. The gradual RESET is observed around 275–400 µA and successful fully RESET state is achieved with 450 µA RESET pulses.

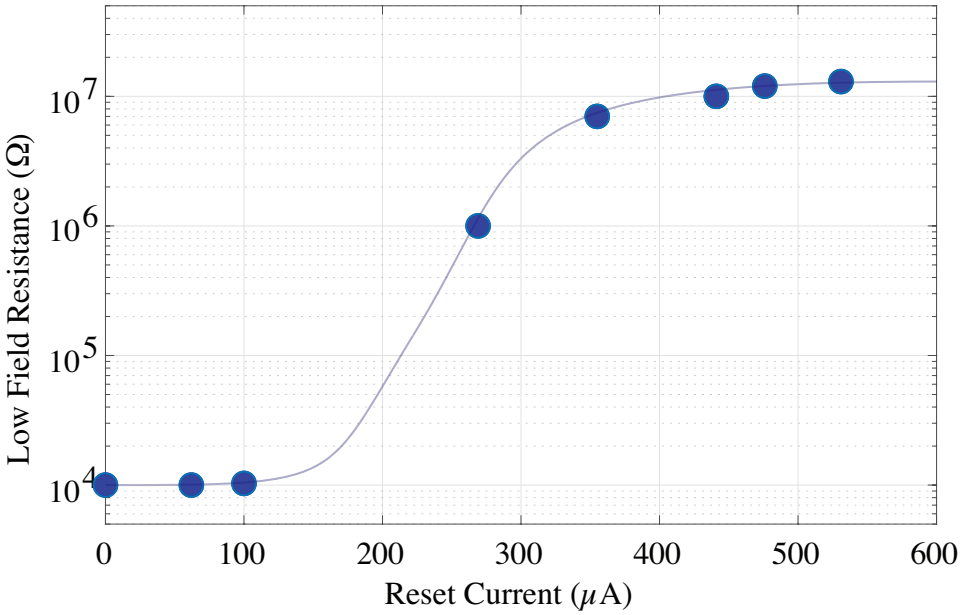

Figure 2.14: Electrical characteristics of synaptic device after RESET pulses with different current levels.

The scaling charts presented in Fig. 2.15 represents required reset currents reported in the literature to achieve a fully RESET state as a function of heater contact size. With 450 µA RESET current and, 40 nm heater radius, our RESET simulation results are shown to be in a good agreement with previously reported similar devices found in the literature.

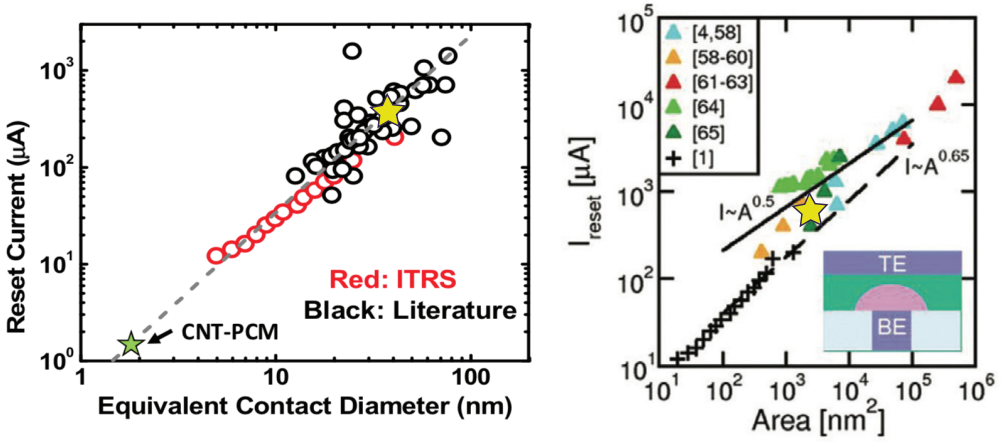

Figure 2.15: On the left, scaling trend of RESET current vs. heater contact diameter of PCM based switching devices are shown [41] . On the right, experimental RESET current vs. heater area from several sources is given [80]. Yellow stars on both charts represent our simulation results.

Top plot of Fig. 2.16 shows one RESET and READ pulse sequence applied to the device. Although we report quasi-stable RESET current levels, our applied voltage levels are close to values reported in the literature. In the bottom plot, each line represents the temperature of only one mesh inside GST during RESET and READ operations. A snapshot of cell temperature profile at the end of this RESET pulse (at 22.5^{th} ns) is given in Fig. 2.13. Fig. 2.16 also demonstrates that owing to very fast thermal dynamics of the device, READ operation can be started as close as 15 ns after cutting RESET pulse.

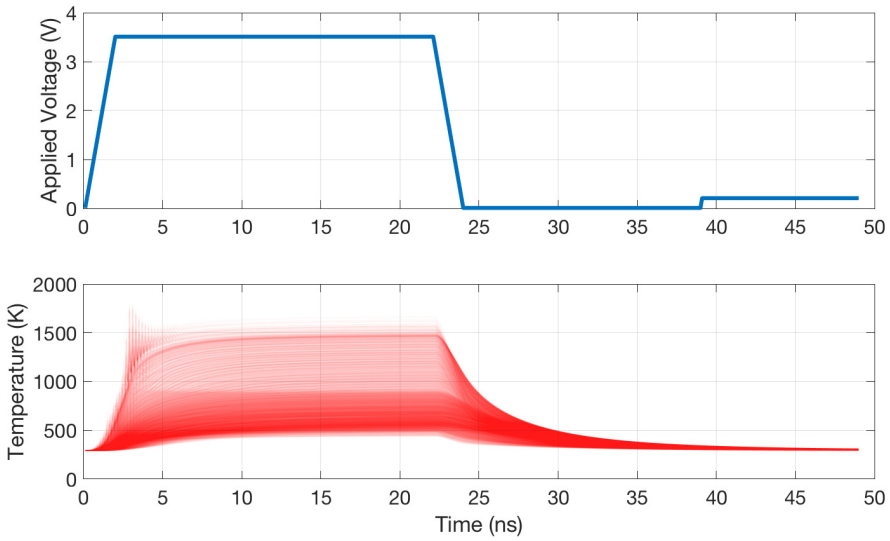

Figure 2.16: Temperature histogram of synaptic device during RESET and consecutive READ pulses.

Fig. 2.17 shows the temperature and electric field distribution inside GST after application 2.5 V, 3 V and 3.7 V RESET pulses. Both the temperature and electric field concentrated on the corners of the heater. Elevated temperature and electric field levels causes higher electrical conductivity due to Poole-Frenkel effect, which leads to larger melted volume in GST.

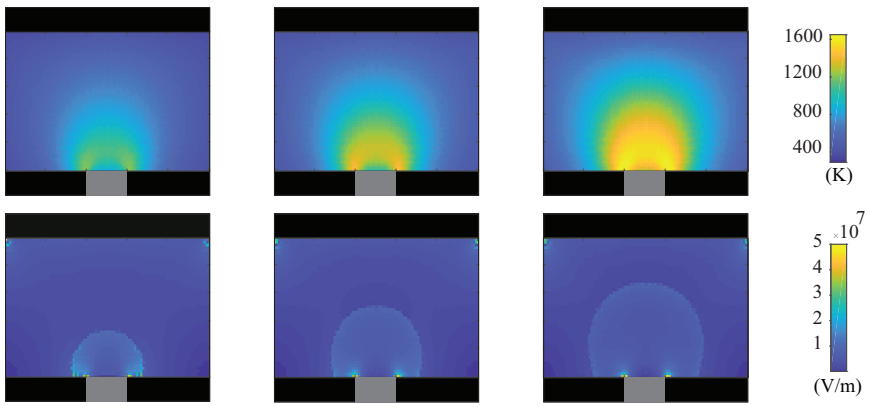

Figure 2.17: Temperature and electric field distribution inside GST after different applied RESET pulses.

2.3.4 SET Programming Tests

SET tests are conducted to check the agreement of simulated device and experimentally reported crystallization growth during SET operation. The initial device state is manually programmed into RESET state to observe a complete phase transition. SET operation controls nucleation and crystal growth inside GST; hence initial crystal cluster positions and sizes before SET, are essential and should be defined.

The initial distribution of nuclei cluster sizes is assumed to follow an exponential distribution as previously stated in the literature [65]. Fig. 2.18 demonstrates a scaled version of randomly positioned, initial crystalline nuclei cluster distribution of GST. Calculated GST positions and nuclei size distributions show a good agreement with TEM image of the crystalline phase of GST. To avoid random effects due to sampling, the simulation uses the same crystal cluster settings for all SET tests.

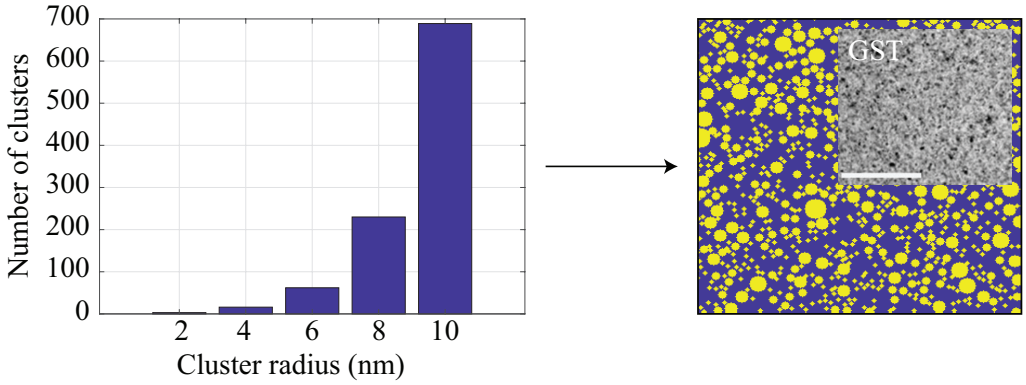

Figure 2.18: Initial distribution of crystal cluster sizes is given. Clusters are randomly positioned without an overlap. Intake figure on the right shows a similar TEM image of cluster distribution, taken from [81].

SET test pulses are 3V RESET pulses finished with long tails. As Sebastian et al. reported [79], applying a 100 ns SET pulse following a RESET provides enough time and temperature requirement for crystallization. To investigate time-dependent crystallization growth, we applied $t_{SET} = 50, 100, 150$ ns SET pulses. Figure 2.19 demonstrates applied SET pulses to the synaptic device and

crystallization/amorphous volume distributions before and after different SET pulses. Yellow region represents the amorphous part, whereas blue region is crystal nuclei clusters on crystal background represented with the navy color.

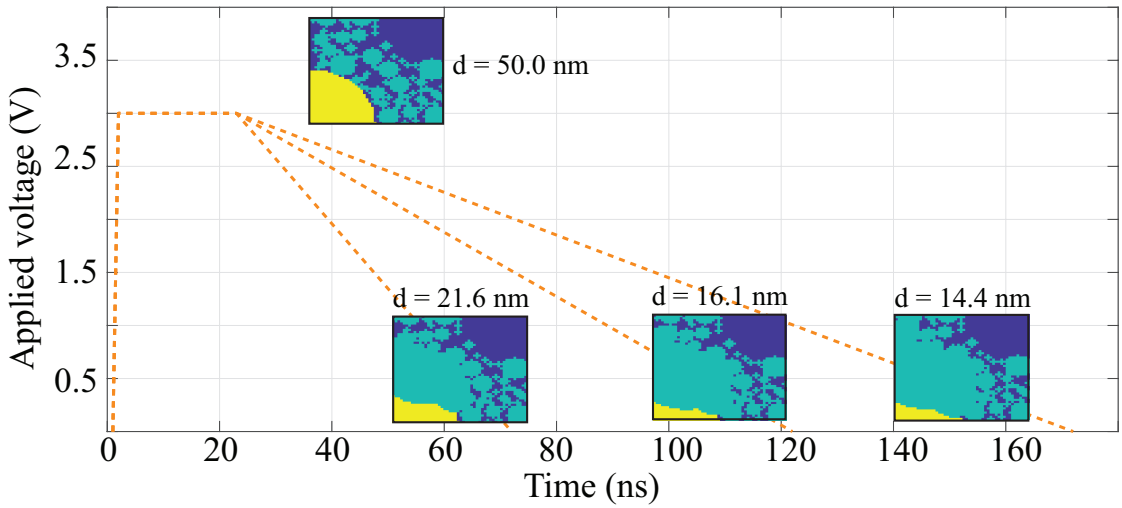

Figure 2.19: Crystal nuclei cluster distributions are given before and after various SET pulses. Red dashed lines demonstrates three different SET scenarios. Reduced amorphous region is achieved by longer SET pulses.

In Fig. 2.19, d describes the shortest path that current can take through the amorphous region, which is more descriptive of amorphous volume than commonly used u_A, the radius of amorphous region [79]. Decreasing d with increasing SET pulse duration shows that staying longer in crystallization temperature region leverage crystallization effect as expected. The observable growth rates for SET tests, which are calculated by $\Delta d/t_{SET}$, are $0.6, 0.3, 0.2\ m/s$ for $50, 100$ and 150 nm long pulses. These results are very close agreement with previously reported amorphous region shrink velocities [53, 79]. This is a remarkable result for two main reasons:

- This model does not assume perfect semi-round amorphous region during SET operation.
- It also can explain from first principles that experimentally observed growth rates can be calculated by individual growths of tens of crystal nuclei clusters whom radius follows exponential distribution between 2-10 nm.

Another key result of SET tests is that during experimenting different SET pulses on various crystallization distributions, we have not encountered a single nucleation event. Because transient nucleation rate is extremely low until ~ 0.1 milliseconds (see Fig. 2.5), even a heterogeneous nucleation event on GST did not take place. Hence, we confirmed that crystallization in GST is a growth dominant rather than nucleation dominant mechanism.

Chapter 3

Modeling Drift of PCM Based Selector Devices

The second part of this thesis captures my research at Advanced Technology Development Team (TD) and Computer Aided Engineering Team (CAE) of Samsung Electronics Co., Ltd. in Korea. This part focuses on the modeling of drift in phase change material based selector devices.

As phase change material based non-volatile memory devices shrink to sub 10 nm region, a couple of problems emerged in the engineering of densely packed crossbar arrays. One of the major issues is "sneaky path problem", where WRITE operation of one cell, may disturb neighbor cells with residual leakage currents or obstruct READ operation as shown in Fig. 3.1. To suppress parasitic currents, one solution is to add a selector device with a highly non-linear current-voltage (IV) characteristics, series with each memory cell.

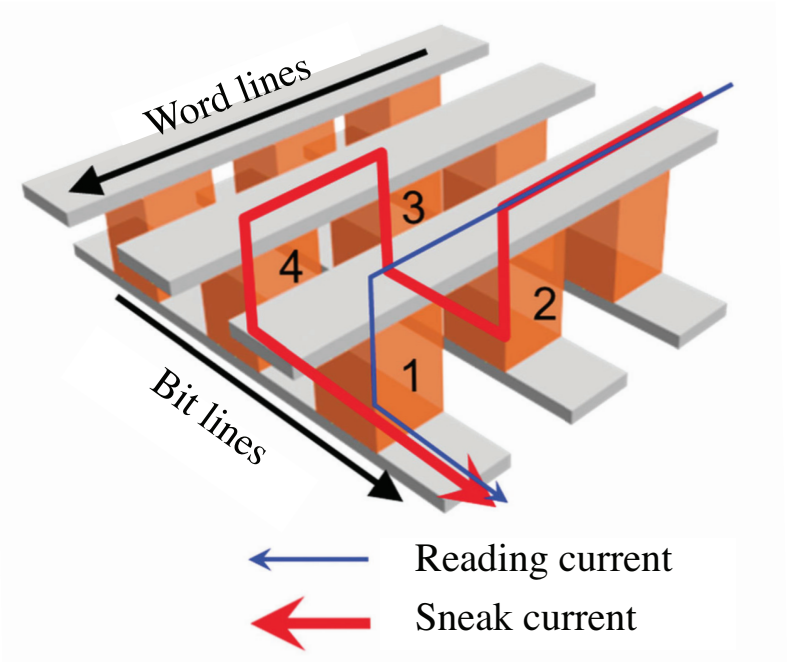

Figure 3.1: A diagram showing the read disturbance problem by the presence of sneak current: reading current (thin blue line), sneak current (thick red line). Taken from [82].

There are several selector implementations in the literature which offer both high current density with good IV nonlinearity, low capacitance and back-end-of-line (BEOL) compatibility, such as:

1. Transistors
2. Diodes (Si or oxide based)
3. Volatile switching selectors
4. Ovonic threshold switching (OTS) devices
5. Mixed electronic and ionic conduction (MIEC)

3.1 Ovonic Threshold Switching (OTS) Selectors

OTS devices are two-terminal amorphous chalcogenide materials, whom electrical conductivity can rapidly change from a high resistive state (HRS) to low resistive state (LRS) by applying a large potential exceeding a specific threshold voltage value [38]. The conductivity difference between switched LRS and HRS can be as high as six orders of magnitude; nevertheless device immediately switches back when the applied voltage is cut.

OTS devices and PCM based memory cell that is studied in Chapter 2 are both based on chalcogenide materials. Hence, OTS devices can crystallize and melt as well. However, OTS materials are chosen in selector applications such that they have lower ionicity and higher hybridizations, which leads to more directed covalent bonds which significantly slow crystallization process [83]. In fact, once crystallization observed in a selector device, it is not feasible by device operations to melt and change its phase back to fully amorphous state, therefore crystallized selectors are always assumed to be non-operational.

3.2 Resistance Drift in OTS Device

Resistance drift is a widely observed physical phenomenon due to rearrangements of atoms in amorphous materials [84]. In chalcogenide materials, whether it is the amorphous phase of PCM or OTS material, resistance drift manifests itself as monotonic increasing of resistance through time [71, 85, 86]. The actual physical reason of the resistance drift is still not clear, but recently Raty et al., Gabardi et al. and Zipoli et al., demonstrated with *ab-initio* simulations that energetically unstable homopolar bonds and defects exist in melt-quenched amorphous [84, 87, 88]. As these unstable defects naturally disappear with time, the distance between traps increases as the structure evolves into a more crystalline-like state, however without the necessary long-range order.

The increase of selector device resistance is a significant problem regarding crossbar array technology. The main problem comes through increase of threshold voltage (V_{th}) as resistivity drifts [86, 89]. READ and WRITE operations requires a known V_{th} level of OTS. If V_{th} increases and applied READ/WRITE pulses could not pass threshold value, then selector device stays in HRS. Resistance drift of V_{th} may be addressed with determining new V_{th} with various READ voltages and detecting the voltage value which certain threshold current level is reached [25]. However, all currently proposed solutions increase time and power required to READ and WRITE operations and add more support circuitry; therefore, they are ideally unfavorable. On the other hand, physical modeling of time-dependent resistance drift can offer a much faster solution.

It has been experimentally observed that resistance drift follows power law [71], given by:

$$R(t) = R(t_0)(\frac{t}{t_0})^{\nu}, \tag{3.1}$$

where $R(t)$ is time-dependent amorphous resistivity, $R(t_0)$ is an observed resistivity at $t = t_0$, and ν is drift coefficient. Even though it is widely used in the literature to forecast resistance of amorphous region Eq. 3.1, falls short explaining the temperature dependence of the drift [90–92]. Ciocchini et al. later proposed a connection of temperature dependent electrical transport and drift mechanism by increasing of activation energy of conduction by time. However they assumed a constant inter-trap distance during the drift, which is proven not to be the case [84, 89].

Recently, Sebastian et al. developed a temperature dependent structural relaxation(SR) model which links structural relaxation to the activation energy of low-field conduction [90]. This work, later improved by Le Gallo et al., to connect activation energy and inter-trap distance changes with 3D Poole-Frenkel based electrical transportation in Eq. 2.4 [52]. Although this simple but powerful model has been validated experimentally across a wide range of time (10 orders of magnitude) and temperature (180-400 K), it does not support one unique drift

feature that we observed in our OTS devices, which is the saturation of the drift.

Drift saturation of PCM material is rarely reported physical phenomenon in the literature, and it is critically important for understanding and developing OTS device technology [93, 94]. In the second part of the thesis, we improved the model proposed by Le Gallo et al. [91], by proposing that two identical, drift saturated devices at different temperatures should have similar inter-trap distance levels as consumption of defects are the limiting factor of the drift.

3.3 Modeling Resistance Drift with Saturation

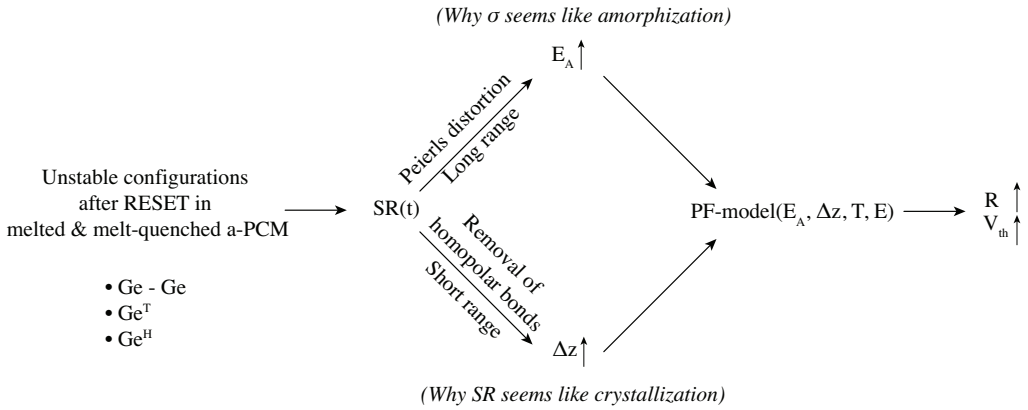

Figure 3.2: From left to right: Homopolar bonds in amorph are energetically unstable hence disappears with time. This mechanism is called structural relaxation(SR) and affects activation energy and trap density. Change in these two parameters are enough to model drift since we assume Poole-Frenkel model captures electrical transport behavior of ovonic threshold switching material.

The model of resistance drift of PCM based devices proposed by Le Gallo et al., [91] describes the simplified dynamics of structural relaxation and how SR changes activation energy of conduction, E_A, and inter-trap distance, Δz as the annihilation of traps proceeds. Figure 3.2 illustrates the causal effects leading to resistivity increase with time. Interestingly, this model can predict experimentally observed resistivity and threshold voltage values by only altering E_A and Δz in Poole-Frenkel model.

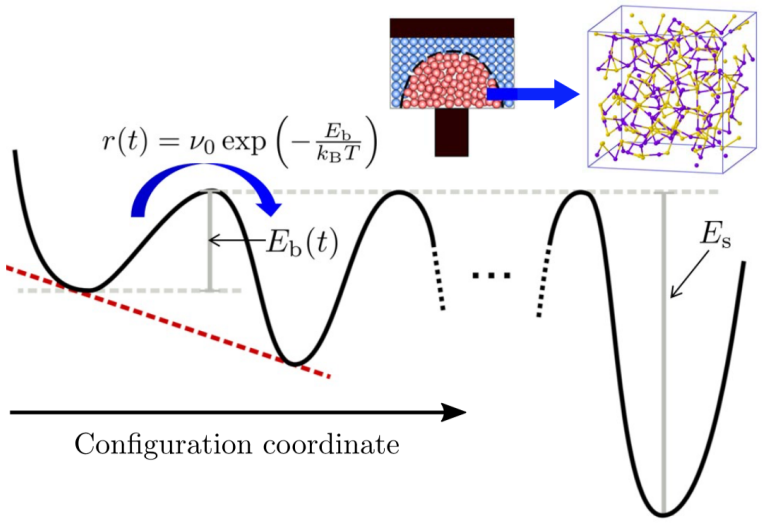

Figure 3.3: Structural relaxation model developed by Le Gallo et. al [91]. After programming, amorphous state is energetically unstable and proceeds towards more stable crystalline-like state with rate $r(t)$, without requiring long range order.

The structural relaxation model denotes PCM's network state with an order parameter Σ. Σ is a normalized parameter and takes values between 1 (low-ordered highly-stressed amorphous state) and 0 (ideal, energetically favorable relaxed state). Whenever $V > V_{th}$ is applied to OTS device, amorphous network state is initialized with $\Sigma(0) = \Sigma_0$. As network state collectively relaxed through more relaxed states, energy barrier required to overcome, E_b, is assumed to be linearly dependent to Σ :

$$E_b(t) = E_s(1 - \Sigma(t)), \tag{3.2}$$

where E_s is the final energy barrier to reach most relaxed state at $\Sigma = 0$. With an Arrhenius behavior, this relaxation events occur at rate $r(t) = \nu_0 \exp(-E_b(t)/k_B T)$, where ν_0 is an attempt-to-relax frequency. If each relaxation event with $E_b(t)$ energy barrier, changes Σ by Δ_Σ, the evolution of Σ as a function of time and temperature can be calculated by:

$$\begin{aligned}\frac{d\Sigma(t)}{dt} &= -v_0\Delta_\Sigma \exp\left(-\frac{E_b}{k_BT(t)}\right) \\ &= -v_0\Delta_\Sigma \exp\left(-\frac{E_s}{k_BT(t)}\right)\exp\left(\frac{\Sigma(t)E_s}{k_BT(t)}\right).\end{aligned} \tag{3.3}$$

At constant temperature, Eq. 3.3 can be solved analytically to track progress of Σ, such that:

$$\Sigma(t) = -\frac{k_BT}{E_s}\log\left(\frac{t+\tau_0}{\tau_1}\right), \tag{3.4}$$

where $\tau_1 = (k_BT/v_0\Delta_\Sigma E_s)\exp(E_s/k_BT)$ and $\tau_0 = \tau_1\exp(-\Sigma_0 E_s/k_BT)$. Once Σ is calculated by Eq. 3.4 at constant temperature, an empirical linear link connecting structural relaxation to activation energy and inter-trap distance can be written as:

$$\begin{aligned}E_{a0}(t) &= E^* - \alpha\Sigma(t) \\ s(t) &= s_0/\Sigma(t)\end{aligned} \tag{3.5}$$

The temperature dependence of activation energy of electrical transportation, is assumed to follow Varshni Rule,

$$E_a = E_{a0} - \xi T^2$$

since optical bandgap is experimentally shown as temperature dependent [59, 95, 96].

Once temperature and time-dependent E_A and Δz determined, 3D Poole-Frenkel model in Eq. 2.4 is used to calculate resistivity of OTS device. However, we did not put to use field dependent version of mobility in our model as suggested by Le Gallo et al., since constant mobility shows better agreement with our experimental data [52].

3.3.1 Experimental Validation of Proposed Model

Figure 3.4 shows experimentally observed resistance drift data of the same device at two different temperatures. The OTS device fabricated for experiment has bottom electrode size of 8 nm × 20 nm, and the thickness of OTS material is 30 nm. The READ voltage values are 2.48 V and 2.64 V respectively for 25 °C and 85 °C experiments. The resistance difference between two temperatures is due to thermally excited Poole-Frenkel emission effect.

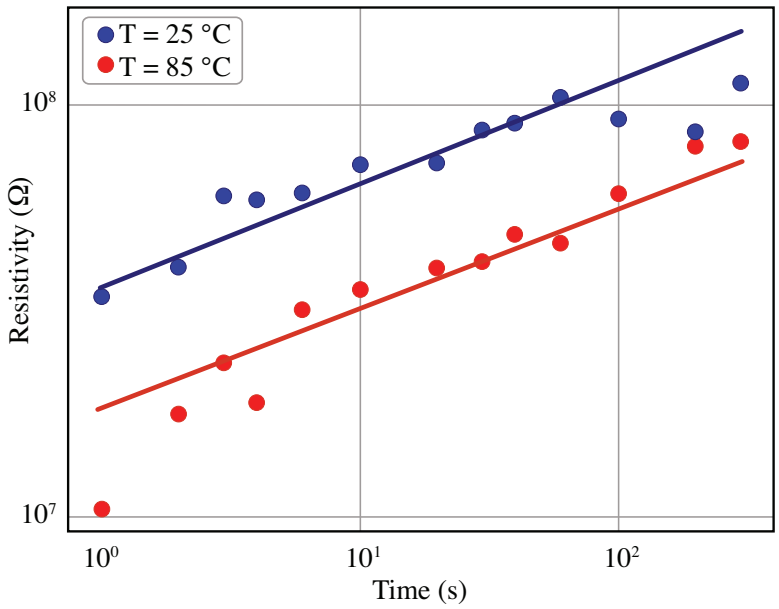

Figure 3.4: Two resistivity measurements of the same OTS device for different temperature values are presented. The fitted models to describe drift behaviors differ only in temperature input and experimentally used READ voltages.

Parameters of the model used to fit two different measurement case are entirely same except temperature information and slightly different READ voltage values which is used to approximate electrical field inside OTS material by $F = V/h_{OTS}$, where h_{OTS} is the thickness of the device.

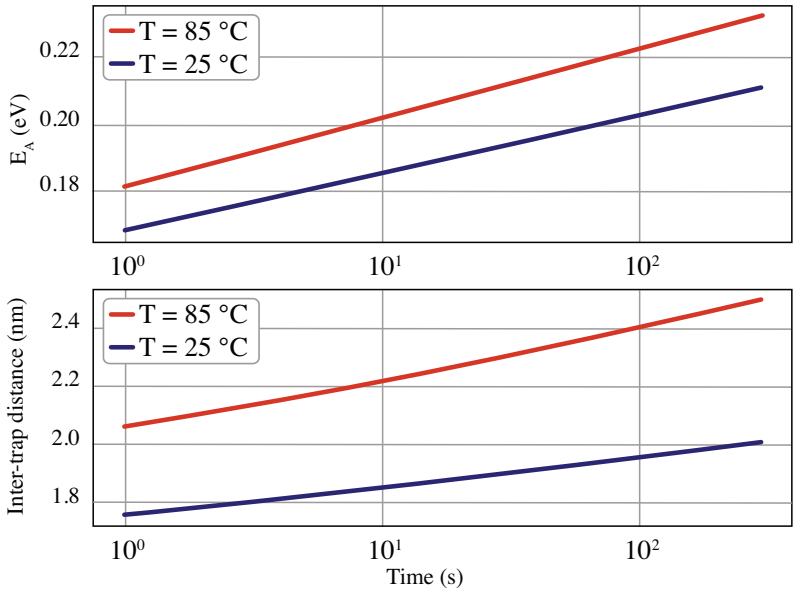

Figure 3.5: Activation energy and inter-trap distance calculated by drift model for OTS devices used in Fig. 3.4.

Once the model is to fit experimental OTS device characteristics, the evolution of immeasurable device properties such as activation energy of conduction and inter-trap distance can be calculated. Fig. 3.5 shows that activation energy of OTS device in 85 °C ambient temperature is higher. This result is well aligned with the experimentally found temperature dependence of optical bandgap. The bottom figure illustrates temperature dependence of inter-trap distance, which is more distant in high ambient temperature due to its annealing effect but increases with time due to structural relaxation.

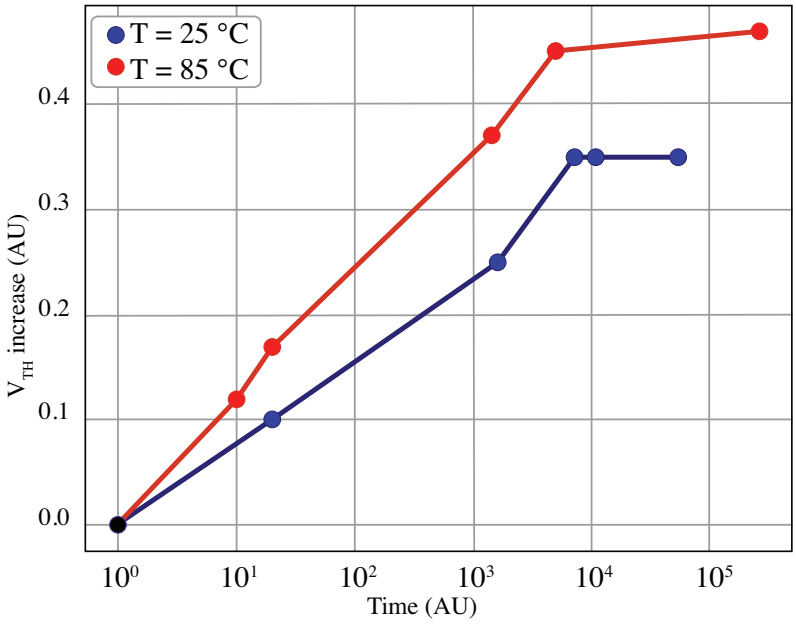

Figure 3.6: Resistance drift saturation measurements of OTS device with 380 nm^2 bottom area and 20 nm thickness. Saturation times are determined to be 10800 seconds and 4980 seconds for 25 °C and 85 °C ambient temperatures respectively.

In some prototype OTS devices that fabricated with different chalcogenide alloys, resistance drift saturates at some point in time, coherently with V_{th}. Fig. 3.6 illustrates that V_{th} increase over time until saturation point is a temperature dependent phenomena. In the strong form of the drift model proposed by Le Gallo et al., the evolution of the device resistance can be predicted; however it falls short predicting this saturation point. To support saturation in Eq. 3.3, we proposed that if we have two identical devices at different temperatures, although one saturates first, eventually they will have the same inter-trap distance and activation energy at the point drift saturated. This proposition requires, $\Sigma(t)$ to be constant after saturation, which requires the condition:

$$\frac{\partial \Sigma(t)}{\partial t} = -r(t)\Delta_{\Sigma} = 0 \tag{3.6}$$

Hence, declaring a new boundary condition $\Sigma\left(t \geq t_{sat}\right) = 0$, for Eq. 3.3, enables model to predict the resistance saturation time.

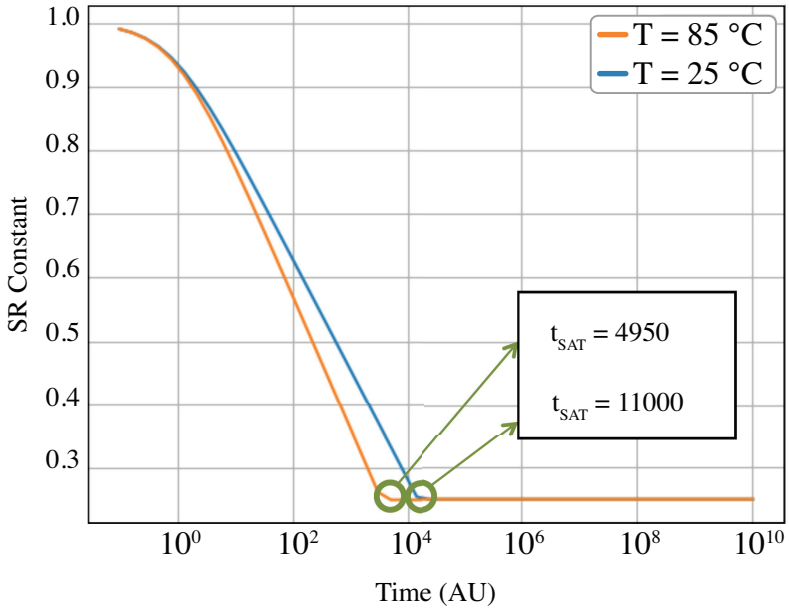

Figure 3.7: Calculated structural relaxation constant Σ is given for both measurement data at Fig. 3.6. $\Sigma = 1$ corresponds to the most disturbed state.

Fig. 3.7 demonstrates the evolution of Σ, when the model is tuned specifically for determined saturation points of measurement shown in Fig. 3.6. The model prediction of resistance - therefore V_{th} - slope is steeper in higher ambient temperatures due to faster annihilations of defects. Once resistance drift model with saturation is tuned for OTS device, time and temperature dependent IV characteristics can be inferred. Fig. 3.8, illustrates IV characteristics of OTS device measured at 300^{th} second, and proposed model prediction. It is clear that drift model captures Poole, Poole-Frenkel, and Ohmic regions reasonably well for this measurement. The only mismatch is present in $V_{th} = 2.1$ V, which is presumed to be due to impact ionization effect.

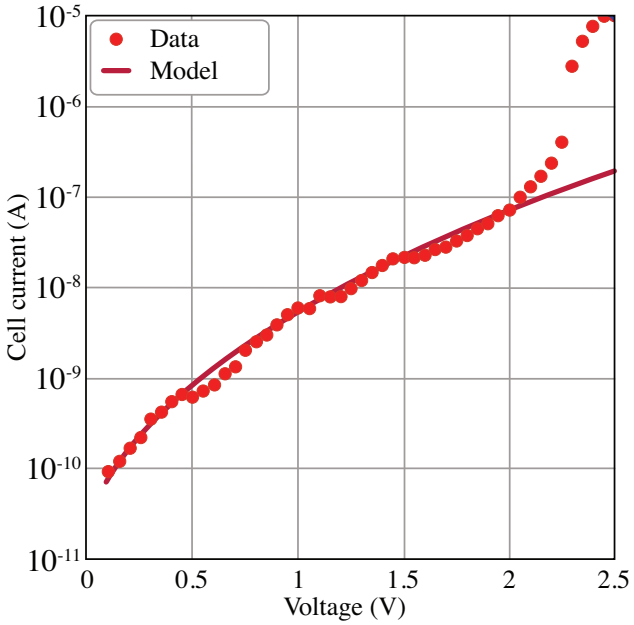

Figure 3.8: IV measurement of OTS device at 85 °C ambient temperature and previously tuned drift model used to predict IV characteristics of the device at 300^{th} second.

As a case study for describing threshold switching behavior of OTS device, several models based on the high field-induced avalanche of carriers are proposed in the literature [97,98]. The empirical Okuto-Crowell impact ionization method is selected based on its good agreement with the OTS switching data (see Fig. 3.10). Combination of Poole-Frenkel subthreshold switching and impact ionization avalanche generation model is given in Fig. 3.9. The important point of this combination is that V_{th} can be calculated by determining the point of abrupt slope change of IV curve. Hence, not only resistance drift but V_{th} drift can be predicted as well.

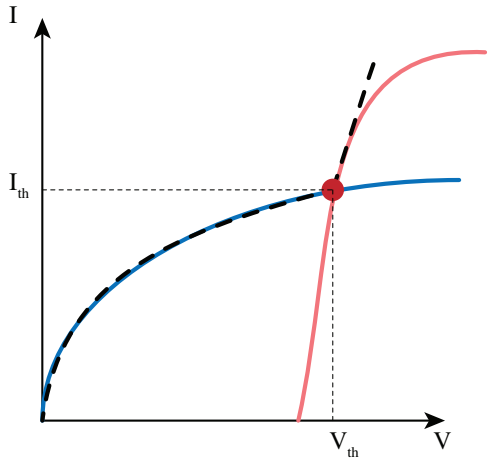

Figure 3.9: Blue line is general Poole-Frenkel behavior for subthreshold conduction, whereas red line is the typical behavior of impact ionization. By combining both Poole-Frenkel and impact ionization, the complete IV curve showed with black dashed line can be obtained.

The implemented Okuto-Crowell impact ionization model is given by:

$$\alpha(F) = a\left(1 + c\left(T - T_0\right)\right) F^{\gamma} \exp\left[-\left(\frac{b\left[1 + d\left(T - T_0\right)\right]}{F}\right]^{\delta}\right], \tag{3.7}$$

where a, b, c, d, γ and δ are empirical constants, T_0 is 300 K and F is electrical field. The avalanche factor $\alpha(F)$ is combined with free carrier charge density calculated via Poole-Frenkel Model to obtain generation rate with following formulation:

$$G = n(F,T)\alpha(F)\mu F. \tag{3.8}$$

Then new free carrier charge density is calculated by

$$n' = n + G\tau, \tag{3.9}$$

where τ is the carrier lifetime.

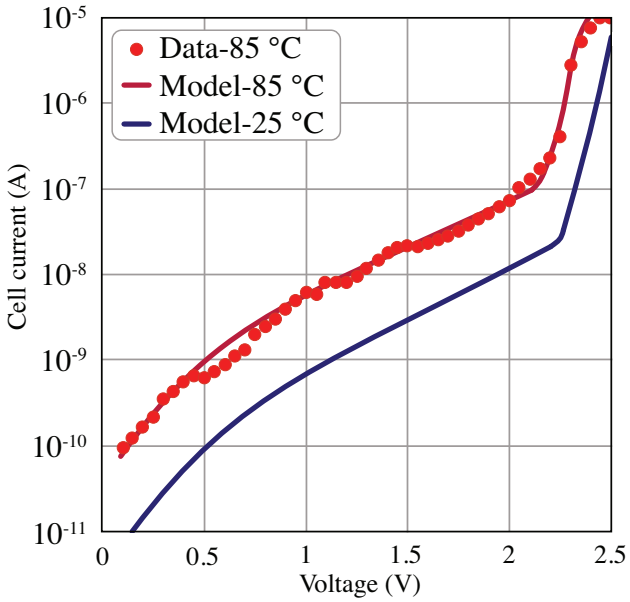

Figure 3.10: Prediction of OTS device IV curves at 300th second for 25 °C and 85 °C with impact ionization is enabled.

Fig. 3.10 shows the implemented Okuto-Crowell impact ionization model, combined with Poole-Frenkel subthreshold conduction mechanism. The new model can predict V_{th} successfully. Model prediction of room temperature device characteristics is also shown as a reference.

3.4 Model Optimization Techniques

To utilize optimization methods to tune model parameters for experimental measurements automatically, model input/output is designed such that it takes the same inputs with the fabricated device (voltage, ambient temperature) and returns the same measurable quantity (current or resistivity). As shown in Fig. 3.11, fabricated OTS device can be modeled as a black box with physical characteristics represented by a multidimensional parameter set, θ.

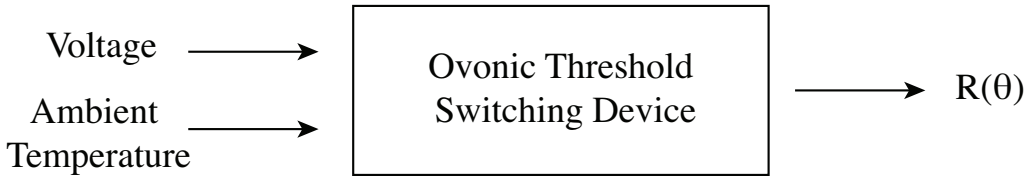

Figure 3.11: For OTS device, the control parameters are ambient temperature and applied voltage.

In proposed drift saturation model illustrated in Fig. 3.12, there are 17 parameters that should be tuned in order to represent the internal dynamics of the fabricated device. In an ideal situation, using well-grounded parameters, both real-world device, and simulated device outputs the same current when we apply same voltage level at same ambient temperature. Therefore, the aim is to minimize the difference between measured resistivity level of the fabricated device, $R(\theta)$ and estimated resistivity by model, $\hat{R}(\theta)$, by tuning model parameters, θ.

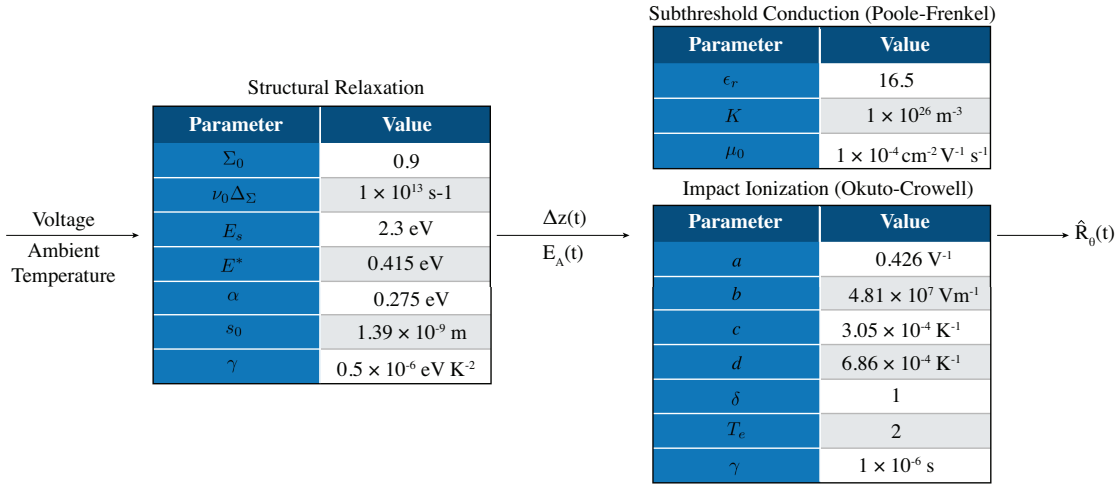

Figure 3.12: At drift simulation, voltage pulse and constant ambient temperature is applied to model and observed parameter dependent resistivity value, $\hat{R}_\theta(t)$.

3.4.1 Least Square Methods

Without boundaries:

$$x = \arg\min_{\theta} \frac{1}{2} \sum \left(R(t) - \hat{R}_{\theta}(t) \right)^2. \tag{3.10}$$

First optimization method used is Trust Region Reflective algorithm of *least_squares* method with Cauchy loss, of *scipy* library of Python [99]. The downside of this method is that tuned parameters could not have lower and upper bounds as shown in Eq. 3.10, hence resulted in physically unrealistic device parameters such as negative activation energy, etc.

With boundaries:

$$x = \arg\min_{\theta} \frac{1}{2} \sum \left(R(t) - \hat{R}_{\theta}(t) \right)^2, \text{ subject to LB} < \theta_i < UB. \tag{3.11}$$

Second optimization attempt is to bound each parameter in a physically expected range via utilizing *leastsq* method of *scipy* library of Python. *leastsq* supports limiting every parameter with one upper and one lower bound as is shown in Eq. 3.11, however, this method resulted in extremely low inter-trap distance, even though all parameters are limited to be positive values.

Simulated Annealing:

$$x = \arg\min_{\theta} \frac{1}{2} \sum \left(R(t) - \hat{R}_{\theta}(t) \right)^2, \text{ subject to } LB_{\text{i}} < \theta_i < UB_i. \tag{3.12}$$

In the last optimization attempt to limit every parameter with different upper and bottom bounds as in Eq. 3.12, simulation annealing method is utilized among other candidate methods such as evolutionary algorithms or gradient-based search algorithms due to its ease of implementation [100]. Despite its computation heavy search, obtained set of parameters were in the order of what is expected.

Chapter 4

Conclusion and Future Work

4.1 Summary of Achievements

The achievements of this thesis include the modeling effort of PCM based memory, and modeling of PCM based selector cell, which together describe a single synaptic device. In the first part of the thesis, a simulation framework using implementation of novel thermoelectrical and phase change models for GST based synaptic device is proposed. In the second part of the thesis, electrical modeling and resistance drift saturation mechanism for PCM based selector devices are proposed.

Modeling of PCM Cell:

We proposed a comprehensive, FEM-based simulation tool for modeling electrical, thermal and phase change response of PCM based synaptic devices. Coupling COMSOL Multiphysics® via with MATLAB® using LiveLink™ interface allows user to investigate and optimize SET operation of the device, which was otherwise, inapplicable. Proposed novel simulation framework with its implemented models, is validated with various previously reported experimental data.

We demonstrated that previously reported temperature dependent amorphous region shrink rates can be decomposed to growth rates of different cluster sizes whom allocation inside GST follows an exponential distribution.

We also successfully demonstrated that commonly practiced SET scheme controls growth dominant crystallization rather than nucleation. Although heterogeneous nucleation rate is higher than homogeneous nucleation rate inside GST, simulation results showed that experimentally observed temperature-dependent crystallization relationship is due to Crystallization Nucleation Theory based growth theory, not related to nucleation.

We proposed a mathematical model, Eq. 2.20, for calculating millisecond long transient nucleation rate with very small FEM simulation time steps. Nucleation rate calculation as it is proposed initially, requires constant temperature during long incubation time; however our model shows inside PCM, the temperature distribution can change at a rate up to $1 \times 10^{11}\,\mathrm{K\,s^{-1}}$. Proposed mathematical method discretizes transient nucleation rate for small simulation time steps, which was otherwise untrackable.

Modeling of Selector Device:

We demonstrated that subthreshold conductivity of small OTS selector device fabricated with 8nm node follows 3D Poole-Frenkel behavior with field-independent mobility. From the insights provided by the model, activation energy and inter-trap distance information of the device is obtained.

We demonstrated that previously developed resistance drift model by Le Gallo et al., which was validated on GST and GeTe, can also describe the drift characteristics of small OTS devices. The implemented model is validated at two different ambient temperature, 25 °C and 85 °C up to wide range of time, $10^0 - 10^3$ seconds.

We proposed a method to predict saturation time of resistance drift for OTS selector devices. Modeling the drift and its saturation together is an important

requirement for PCM based NVM technologies as the threshold voltage of READ and WRITE operations are heavily dependent on the drift behavior. Proposed drift saturation model is validated on two different temperatures (25 °C and 85 °C) and wide range of time (up to 10^5 seconds).

We also reported an ultrafast saturation of the resistance drift in OTS selector devices, observed for the first time in the literature. Previously reported fastest resistance drift saturation time is on the order of $10^5 - 10^6$ seconds. From the technology point of view, $10^3 - 10^4$ second saturation time is a remarkable device property which obligates a threshold voltage look-up table implementation to a memory device.

We implemented a parameter optimizer based on simulated annealing method to tune model parameters within the range of physically expected boundaries.

4.2 Impact of This Research

The proposed model for drift saturation which successfully captured time and temperature dependent resistance drift of OTS selector devices is going to built into Samsung Electronics' semiconductor model library. Being the first successful OTS drift model developed at Samsung Electronics, proposed model paves the way for understanding the device operations and advancing PCM based NVM device technology. Additionally, the growth dominant crystallization implementation at the first part of this thesis is requested by Samsung Electronics to improve currently used models.

4.3 Future Work

The development of promising PCM based synaptic device technology relies on a strong understanding of device operation principles. Particularly following simulation ideas are suggested to investigate to build upon the research conducted in this thesis:

Combination of memory and selector simulations: First chapter of this thesis approach the modeling of the memory cell via FEM simulations, whereas second part takes an analytical approach to model OTS selector device. Next improvement would be designing a single FEM simulation which includes connected OMS and OTS devices, to enable temperature and field interaction between for more realistic results.

Faster iteration requirement: Currently one 50 ns RESET simulation takes approximately 10 hours of simulation time on modern hardware with 16 CPUs. The main bottleneck comes from to reinitialization of COMSOL variables at the beginning of each time step. Reimplementing proposed algorithm on another software such as TCAD Synopsis, etc. would be a good candidate for solving the problem of slow iteration speed.

Implementation of thermoelectrical properties: Peltier, Seebeck and Thomson thermoelectrical effects are present and can impact on the temperature distribution of the device. The implementation of these thermoelectrical properties could improve the understanding of electrical and thermal transportation processes.

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