A GATE MODULATED DIGITALLY CONTROLLED MODIFIED CLASS-E AMPLIFIER FOR ON-COIL APPLICATION IN MRI

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By Bismillah Nasir Ashfaq
March, 2018

We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

A Gate Modulated Digitally Controlled Modified Class-E Amplifier for On-Coil Application in MRI

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The switch-mode RF power amplifiers, known for their high output power capability and good efficiency, have proved valuable for on-coil applications in MRI hardware. The class-D and class-E amplifier topologies have been demonstrated to be promising candidates to replace the conventional inefficient linear RF power amplifiers used in MR hardware which are placed away from the scanner room. Conventionally, the amplitude modulation of the output waveform in such switch-mode RF power amplifier applications is achieved either by implementing an amplitude modulation block at the drain of the amplifier, or by encoding the amplitude modulation information in the phase of the carrier signal at the gate of the amplifier. Both these approaches require additional hardware, thus increasing the cost and complexity of the system.

Considering the aforementioned background, a novel technique of modulating both the amplitude and frequency of the output waveform, without the need for any additional hardware other than the driver circuitry for the amplifier itself, is presented and implemented for class-E amplifier topology. At 64 MHz (1.5 T), the analytical models of the amplifier for both the switch-on and switch-off cases are first derived and implemented in software. The period of the digital carrier signal at the gate of the amplifier is then divided into k bits, where k is greater than 2. It is then noted that both the amplitude and frequency of the output waveform can be controlled by altering this digital input in a certain manner. For a typical 2 ms 1.5 T MRI RF pulse, the digital carrier bitstream would consist of $\mathrm{k} \times 128000$ bits. This would require testing $2^{\mathrm{k}\times 128000}$ bitstream combinations to achieve the desired output waveform, requiring infeasible computational power. It is however shown that by

intelligently programming the bitstream patterns for a selected number of periods, and by repeating those patterns for a chosen duration of time, the desired amplitude and frequency modulation of the output waveform can be achieved. The normalized root mean square error (NRMSE) for a 2 ms sinc pulse designed using such an approach is calculated to be 11%. The designed bitstreams are tested on hardware as well, both in bench-top and MRI experiments. Bench-top experiment results correlate well with the software predictions. The amplifier shows a peak drain efficiency of 89% at 50 W input power. The MR images obtained at 50 W input power using a 2 ms sinc pulse designed using the presented approach show no artifacts.

The ultimate goal of the current research is to design a 32-channel transmit array coil for the MRI, capable of delivering a total of approximately 10 kW output power. Each amplifier element should therefore be able to deliver about 300 W output power. In this regard, further research needs to be conducted to achieve such output power level using the presented modulation approach. Nonetheless, the approach is general and can be implemented to other switch-mode RF power amplifier topologies as well. It promises to provide a performance equivalent to the other modulation approaches while reducing the overall cost and complexity of the system at the same time.

Keywords: RF Power Amplifiers, Class-E Amplifier, Modulation Techniques, Gate Modulation, Digital Modulation, Parallel Transmission, MRI Hardware.

ÖZET

MRG'de Bobin Üzeri Uygulama için Kapı Kiplemeli Sayısal Kontrollü Değiştirilmiş Sınıf-E Güç Yükselteci

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Yüksek çıkış gücü kapasitesi ve iyi verimliliği ile tanınan anahtarlamalı RF güç yükselteçleri, MRG donanımındaki bobin uygulamaları için değerli olduğunu kanıtladı. Sınıf-D ve sınıf-E güç yükselteci topolojilerinin, MR donanımında kullanılan ve tarayıcı odasının dışına yerleştirilen geleneksel verimsiz doğrusal RF güç yükselteçlerinin yerine ümit verici adaylar olduğu kanıtlanmıştır. Geleneksel olarak, bu tür anahtar özellikli RF güç amplifikatör uygulamalarında çıkış dalga formunun genlik kiplemesi, ya güç yükseltecinin kanalında bir genlik kipleme bloğu uygulanarak ya da genlik kipleme bilgisinin, taşıyıcı sinyalin fazındaki genlik kipleme bilgisinin yükseltecinin kapısında kodlanmasıyla elde edilir. Her iki yaklaşım da ek donanım gerektirir, böylece sistemin maliyetini ve karmaşıklığını arttırır.

Yukarıda bahsedilen önbilgi göz önüne alındığında, güç yükseltecinin kendisi için sürücü devresinden başka herhangi bir ek donanıma ihtiyaç duymadan çıkış dalga formunun hem genliğini hem de frekansını kiplemeye yönelik yeni bir teknik, E sınıfı amplifikatör topolojisi için sunulmakta ve uygulanmaktadır. 64 MHz'de (1.5 T), hem açma-kapama durumları için güç yükseltecinin analitik modelleri ilk olarak yazılımda türetilir ve uygulanır. Güç yükseltecinin kapısındaki dijital taşıyıcı sinyalin periyodu daha sonra k'nin 2'den büyük olduğu k bitlerine bölünür. Daha sonra çıkış dalga formunun genliğinin ve frekansının bu dijital girişin uygun bir şekilde değiştirerek kontrol edilebileceğine dikkat çekilir. Tipik bir 2 ms 1.5 T MRG RF darbesi için, dijital taşıyıcı bit akışı k × 128000 bitten oluşacaktır. Bu, istenen çıktı dalga formunu elde etmek için $2^{(k \times 128000)}$ bit akışlı birleşimlerinin test edilmesini gerektirebilir ve bu da olası hesaplama güçlüğü gerektirir. Bununla birlikte, seçilen devirler için bit akış desenlerinin

akıllıca programlanmasıyla ve bu desenlerin seçilen bir süre boyunca tekrarlanmasıyla, çıkış dalga formunun arzu edilen genlik ve frekans kiplemesinin gerçekleştirilebileceği gösterilmiştir. Böyle bir yaklaşım kullanılarak tasarlanmış bir 2 ms sinc darbesi için normalleştirilmiş kök ortalama kare hatası (NRMSE) %11 olarak hesaplanmıştır. Tasarlanan bit akışları, hem tezgâh üstü hem de MRG deneylerinde donanımda da test edilir. Tezgâh üstü deney sonuçları, yazılım tahminleriyle iyi bir ilgileşim göstermektedir. Amplifikatör 50 W giriş gücünde %89'luk bir tepe kaynak verimi gösterir. Sunulan yaklaşımı kullanarak tasarlanmış bir 2 ms sinc darbesi kullanılarak 50 W giriş gücünde elde edilen MR görüntüleri hiçbir artifakt olmadığını göstermektedir.

Mevcut araştırmanın nihai amacı, toplam yaklaşık 10 kW çıkış gücü sunabilen, MRG için 32 kanallı bir iletim dizisi bobini tasarlamaktır. Her amplifikatör elemanı bu nedenle yaklaşık 300 W çıkış gücü sunabilmelidir. Bu bağlamda, sunulan modülasyon yaklaşımını kullanarak böyle bir çıktı gücü seviyesine ulaşmak için daha fazla araştırma yapılması gerekmektedir. Bununla birlikte, yaklaşım geneldir ve diğer anahtarlamalı RF güç amplifikatörü topolojilerine de uygulanabilir. Sistemin genel maliyetini ve karmaşıklığını aynı anda azaltırken diğer kipleme yaklaşımlarına eşdeğer bir performans sağlamayı vaat ediyor.

Anahtar Kelimeler: RF Güç Yükselteçleri, Sınıf-E Güç Yükselteci, Kipleme Teknikleri, Kapı Kiplemesi, Sayısal Kipleme, Paralel Yayın, MRG Donanımı.

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CHAPTER 1

INTRODUCTION

In conventional applications of the switch-mode radio-frequency (RF) power amplifiers, the amplitude/envelope modulation is achieved by applying the modulating signal at the drain of the amplifier [1] while the frequency modulation is achieved by a carrier signal applied at the gate of the amplifier. The implementation of such an amplitude modulation block requires additional hardware at the drain of the amplifier and the approach is often referred to as the supply modulation approach. One method of implementing such an amplitude modulation block is detailed in [2, 3] where the duty cycles of the digital input signals applied to the amplitude modulation block were controlled in order to obtain various envelope shapes of the modulating signals at its output. The resulting modulating signals were then low-pass filtered and applied at the drain of the amplifier to achieve the envelope modulation of the desired output signal.

In other applications namely delta-sigma based transmitter applications [4, 5], the time varying baseband modulating signal is encoded to a bi-level constant envelope signal using a technique called the delta-sigma modulation (DSM) [6]. The resulting signal is then frequency modulated using a frequency up-converter and fed to the input of the gate of the power amplifier (PA). The aim is to contain all the information only in the phase of the signal while maintaining a constant envelope for the signal. A few of the drawbacks of this approach include the need for a high clock speed to oversample the data to achieve good signal quality,

and the problem of the quantization noise which forms most part of the signal at the output of the DSM, affecting the signal quality. For more details on these issues and how they are dealt with, the reader is referred to [4].

An emerging application that the switch-mode RF power amplifiers are recently finding is in the hardware of Magnetic Resonance Imaging (MRI). MRI is a non-invasive imaging technique that utilizes a constant magnetic field B_0, a radiofrequency magnetic field B_1, and multiple gradient magnetic fields (G) to produce high quality images of different parts of the body [7] including brain, chest, abdomen, etc. One of the important building blocks of the MRI system is the RF transmit chain which consists of a frequency synthesizer, a modulator, an amplifier and a transmit coil. The frequency synthesizer generates a continuous sinusoidal carrier wave at the Larmor frequency [7]. The modulator then modulates this carrier wave with a desired envelope signal to obtain the desired pulse shape in the order of milliseconds. The amplifier amplifies the resulting modulated pulse to the required level to achieve certain flip angle. And finally, the transmit coil transmits the modulated pulse to excite the body part under examination.

The commercially available MRI scanners employ linear, low efficiency power amplifiers which are placed in the systems room (situated behind the scanner room) and require cooling systems due to their high power loss. The amplifiers are situated away from the transmit coils which are either located within the inner walls of the scanner or as free-standing devices near or on the patient. This distance between the amplifiers and the transmit coils requires that long transmission cables be used, increasing in turn the overall complexity and cost of the system while further decreasing its overall efficiency.

For the excitation purposes, the birdcage coil [8] has widely been used as the standard transmit coil in MRI due to its high efficiency and homogeneity. Its performance, however, has been reported to be degraded and resulting in lower SNR (signal-to-noise ratio) in case of higher filed strengths (greater than 3 T). Multi-channel transmit array systems (also referred to as parallel transmit systems) are therefore proposed as an alternative to such conventional systems. The several advantages of the parallel transmit systems [9] include

more degree of freedom in terms of controlling each transmit element separately, local area excitation, and multiple slice selectivity. B_1 field uniformity and homogeneity are reported to be improved [10-12], and the system has also shown to be advantageous in terms of improving RF shimming and increasing the imaging speed [13-15]. Additionally, parallel transmit systems have shown to be advantageous in terms of SAR (Specific Absorption Rate) reduction as the applied RF power and the region of excitation can both be controlled more precisely [16, 17]. RF heating on long metallic implants is also shown to be reduced by being able to control and steer the electric field in parallel transmit systems [18, 19]. Despite its enormous advantages, there are however some challenges that arise when it comes to the implementation of a parallel transmit system. Increasing the number of coil elements in the system inherently increases its complexity as the required amount of cabling for separate power lines and control signals for each element increases. Another concerning issue is the unnecessary coupling among the adjacent elements which not only causes a decline in the efficiency but also artifacts in the images resulting from the undesired B_1+ fields in the neighboring coils.

In an attempt to simplify the RF chain design to be more compatible with the parallel transmit systems, the different components of the RF chain including the pulse modulator, the amplifier, and the transmit coil are worked on to be integrated into a single unit. This is the point where the applications of switch-mode RF power amplifiers come into play in MRI. Several novel designs of on-coil RF power amplifiers have been proposed in this regard with the aim that all three functions, i.e., the pulse modulation, signal amplification, and the RF excitation, are performed at one place. The pulse modulation techniques that are usually employed in such designs include the more conventional supply modulation approach or the recently emerging delta-sigma based transmitter approach. Gudino proposed a current-mode class-D amplifier configuration in her work and tested her design at 1.5 T as well as higher field strengths [20-22]. The research group at UMRAM chose to work on class-E amplifier configuration as it is even more suited for on-coil amplifier applications due to its desirable topology and ability to achieve theoretically 100% efficiency [23].

The class-E amplifier topology was initially proposed by Sokal and Sokal [23], with further work on developing the design equations performed by Raab [24, 25] and other authors [26, 27] over the years. The conventional class-E amplifier configuration consists of a switch, an RF choke inductor, and a load network consisting of a shunt capacitance, a series resonance circuit (or a parallel resonance circuit (shunt filter) as presented in [28]), and the load. This topology is considered ideal for MRI applications as the transmit coil itself can be modeled as the load network of the amplifier. By tuning the coil to the Larmor frequency and matching it to the optimum load impedance of the amplifier, the need for any additional 50 ohm matching is removed. Additionally, as an on-coil configuration, the need for long transmission cables carrying the RF power from the amplifier to the transmit coil is also eliminated.

For the past few years, extensive research has been carried out at UMRAM for developing and implementing a feasible model of the class-E amplifier that is both compatible with the MRI and capable of achieving the desired output power at high efficiency [2, 3, 29-32]. In these works, the RF choke inductor was replaced by an equivalent transmission line for MR compatibility and the transmit coil was implemented as the load network of the amplifier. An output power of 100 W from a single amplifier was first reported at an efficiency of 88%. Later, 300 W output power was achieved from a single amplifier at 84% efficiency. The amplifier's performance under several constraints including its performance in 1 MHz bandwidth and at high temperature, and the effects of load variation on the efficiency of the amplifier were also studied. The effects of increasing the number of coil elements to two and the resulting coupling performance of the system were also analyzed. In all these works, however, the primary approach used for modulating the envelope of the pulse shape over the carrier frequency was the supply modulation approach.

An alternative approach to modulating the envelope of the desired pulse shape, named as the digital modulation approach, was first presented in [2]. The idea was to remove the supply modulation block altogether and to achieve both the amplitude and frequency modulation of the output signal only be controlling the digital input bit-stream at the gate of the transistor. The expected benefits of such an approach would include reduced cost and

complexity of the circuit while striving to achieve an equivalent performance. In this work, the idea of digital modulation for switch-mode RF power amplifiers is revisited and redeveloped from a new perspective, drawing on the concepts of pulse width modulation for non-linear systems and delta-sigma based transmitters. The technique is named as the gate modulation approach based on its implementation method, and though could be implemented to other non-linear switch-mode RF PA configurations as well, the class-E topology is chosen to work on based on its promising applications as an on-coil amplifier configuration in the MRI.

Chapter 2 of this work starts with a brief account of the conventional class-E amplifier topology and the earlier modifications done for making it compatible with the MRI. The concept of gate modulation is then introduced followed by a detailed account of the analytical modelling of the amplifier to develop its complete software model. In chapter 3, the methods used for the implementation of the amplifier model in software are presented, and the gate modulation algorithm is explained in detail. The methods used for software and hardware implementation of the technique are then presented while highlighting the important challenges along the way. In chapter 4, the associated results of the amplifier's software model implementation and of the gate modulation algorithm implementation both in software and hardware (including bench-top and MRI experiments) are presented, while the discussion on those results and the final conclusion points are presented in chapter 5.

CHAPTER 2

THEORY

This chapter starts with a brief overview of the conventional class-E amplifier design and its working principles. The earlier proposed design modifications to make the amplifier compatible for use in MRI are then highlighted, including replacing the RF choke inductance with a transmission line as well as integrating the transmit coil as a part of the load network of the amplifier. The implemented driver circuitry is then briefly explained along with the conventional modulation approach implemented previously. After explaining this essential background information, the concept of gate modulation, a novel method developed to modulate both the amplitude and frequency of the desired radiofrequency pulse (RF-pulse) without the need for supply modulation, is introduced. Implementation of this method involves several steps, from analytical modelling of the amplifier to running simulations and hardware tests. In this chapter, the analytical modelling of the amplifier is presented while the implementation of these models and further details on gate modulation algorithm are left to be discussed in later chapters.

2.1. Conventional Class-E Amplifier Design

The class-E power amplifier is a highly efficient, tuned, switched-mode power amplifier consisting of a load network and a single transistor that operates at the carrier frequency of the output signal. The load network consists of a shunt capacitance C_{shunt} connected in

parallel to the transistor (this includes the internal drain-to-source capacitance C_{ds} of the transistor as well as an externally connected shunt capacitance C_1), and a series-tuned output circuit which may have a residual reactance as well. The amplifier diagram is shown in Fig. 2.1 which shows the DC supply voltage V_{DD}, the RF-choke inductor L_1 which ensures a constant DC current from the supply voltage, the transistor Q which in ideal case acts as a switch, the external shunt capacitance C_1, the series-tuned LC resonance circuit consisting of an inductor L_2 and a capacitor C_2, and finally the load impedance R.

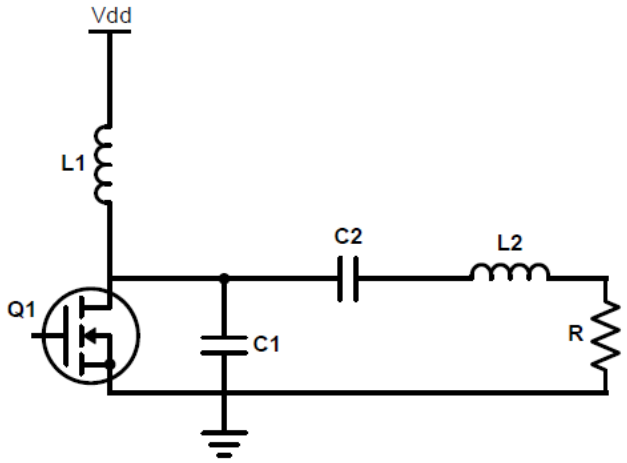


Fig. 2.1 – Conventional class-E amplifier

The ideal optimum operation of the class-E amplifier requires that both the voltage across the switch and its time-derivative be equal to zero at the time of switching (the conditions which are formally known as ZVS (Zero-Voltage Switching) and ZVDS (Zero-Voltage Derivative Switching) conditions), ensuring that there is no power loss in the switch. Provided that the on-resistance of the transistor (R_{ds_on}) is zero (ideal switch condition) and the load network is perfectly tuned and lossless as well, the class-E amplifier can theoretically achieve 100% efficiency in its optimum operation. On the other hand, if the voltage across the switch or its time-derivate are not equal to zero at the time of switching, it will lead to suboptimum operation of the amplifier [24]. In this work, at the stage of deriving the amplifier's model and implementing it in software, the circuit parameters are going to be derived considering 50% duty cycle and optimum operation conditions of the amplifier. But later, when the gate modulation algorithm will be introduced and implemented, the amplifier's operation would

become suboptimum as the amplifier would then be working at multiple duty cycles. Since the circuit parameters were initially derived based on 50% duty cycle operation and would not be updated as the duty cycle changes, it would ultimately result in affecting the efficiency of the amplifier. This can be considered as a conscious trade-off that was kept in mind while proceeding with the algorithm.

Following assumptions have been made while deriving the design equations for the initial implementation of the amplifier circuit parameters:

1) The switch is considered ideal, meaning that R_{ds_on} is equal to zero.
2) The switch operates at 50% duty cycle.
3) The value of the RF choke inductor L_1 is high enough to block the RF signal.
4) The value of the quality factor is assumed high enough to ensure a strictly sinusoidal output current.
5) All the components in the circuit are considered ideal (lossless).

Based on these assumptions, the loaded quality factor (Q_L) based design equations as found in the literature [27, 33-35], that will be used in this work to obtain the initial values for R, C_1, C_2 and L_2, are presented below:

$$R = \left(\frac{(V_{DD})^2}{P_{out}}\right) 0.58 \left(1 - \frac{0.45}{Q_L} - \frac{0.4}{{Q_L}^2}\right) \tag{2.1}$$

$$C_1 = \frac{1}{34.2fR}\left(1 + \frac{0.9}{Q_L} - \frac{1}{{Q_L}^2}\right) + \frac{0.6}{(2\pi f)^2 L_1} \tag{2.2}$$

$$C_2 = \frac{1}{2\pi fR}\left(\frac{1}{Q_L - 0.1}\right)\left(1 + \frac{1}{Q_L - 1.8}\right) - \frac{0.2}{(2\pi f)^2 L_1} \tag{2.3}$$

$$L_2 = \frac{Q_L R}{2\pi f} \tag{2.4}$$

Where P_{out} is the output power desired to be delivered to the load, Q_L is the loaded quality factor of the load network, V_{DD} is the supply voltage at the drain of the amplifier, and *f* is the frequency of operation of the amplifier (1.5 T scanner).

In the case that the switch is non-ideal, the power loss in the switch due to the non-zero on-resistance of the switch, as analyzed by Sokal and Raab in [25], can be written as follows:

$$P_{R_{ds\_on}} = 1.37 \frac{R_{ds\_on}}{R_L} P_{out} \tag{2.5}$$

In this case, the maximum drain efficiency can be calculated as follows:

$$\eta = \frac{R_L}{R_L + 1.37 R_{ds\_on}} \tag{2.6}$$

2.1.1. The Chosen RF Power Transistor Device for Hardware

Considering again the ideal (lossless) switch case, and the 50% duty cycle operation of the amplifier, the relationship between the output power P_{out}, the DC supply voltage V_{DD}, and the load impedance R, as described in [24], can be written as follows:

$$P_{out} = \frac{(V_{DD})^2}{1.74R} \tag{2.7}$$

Also, the relationship between the peak value of the switch voltage V_{C1_peak} and the DC supply voltage V_{DD}, again at 50% duty cycle operation of the amplifier, can be written as follows:

$$V_{C1\_peak} = 3.56 V_{DD} \tag{2.8}$$

Now, as is evident from (2.7) and (2.8), both P_{out} and V_{C1_peak} are directly proportional to V_{DD}. This means that in order to achieve a higher value of the output power at 50% duty cycle operation of the amplifier, V_{DD} should be increased, but increasing V_{DD} would cause the peak value of the switch voltage to increase as well as is evident from (2.8). Based on the specifications of the MOSFET, there's an upper limit to the peak value of the switch voltage, exceeding which would cause damage to the device; this should be kept in mind while

selecting the device. Additionally, as can be seen from (2.6), the drain efficiency of the amplifier is inversely proportional to the on-resistance of the MOSFET (R_{ds_on}). It can also be observed from (2.6) that the value of R_{ds_on} must be lower than the load impedance R_L in order to avoid any degradation in the efficiency. A MOSFET with higher limiting value of V_{C1_peak} and a lower value of R_{ds_on} is therefore desired.

Before this work, other members of the research group at UMRAM had already been working on the conventional supply modulation based class-E amplifier prototypes for the prospective applications in MRI [2, 3]. The ultimate aim of the research group has been to construct a 32-channel transmit array with on-coil amplifiers, capable of transmitting a total of approximately 10 kW power to the body coil, thus requiring each amplifier prototype to provide an output power of 300 W. Based on the points explained in the earlier passages and the requirements of the MRI just mentioned, a 300 W LDMOS RF power transistor (Ampleon, BLF573, Nijmegen, The Netherlands) had already been selected and was being tested in simulations and on hardware. Four-layered PCB prototypes had been designed and fabricated in the lab and were being tested for on-coil applications in MRI. After the gate modulation algorithm was developed in software, it was therefore possible to use the same PCBs for the associated hardware experiments in this work.

It must be noted here that the selected transistor model BLF573 has an R_{ds_on} = 0.09 ohm, and V_{C1_peak} = 110 V. Based on the load-pull analysis performed in [3] and on the value of the load impedance measured on hardware, the value of R_L = 1.5 ohm. From (2.6), the calculated efficiency therefore comes out to be approximately 92.4%. Considering the DC supply voltage V_{DD} equal to 30 V, the value of V_{C1_peak} comes out to be 106.8 V which is well under the limiting value of 110 V. It shall be kept in mind, however, that these calculations have been performed keeping in mind 50% duty cycle operation of the amplifier. Once the gate modulation algorithm is introduced and implemented, the efficiency and V_{C1_peak} will be affected.

2.2. Earlier Proposed Design Modifications

The points explained in this section have been worked on in quite detail in previous works [2, 3]. The reader is therefore referred to the mentioned references to develop a detailed understanding on the subject. Here, a brief overview on the subject is provided. In order to make the amplifier compatible with the MRI, the conventional class-E amplifier design had been modified as shown in Fig. 2.2.

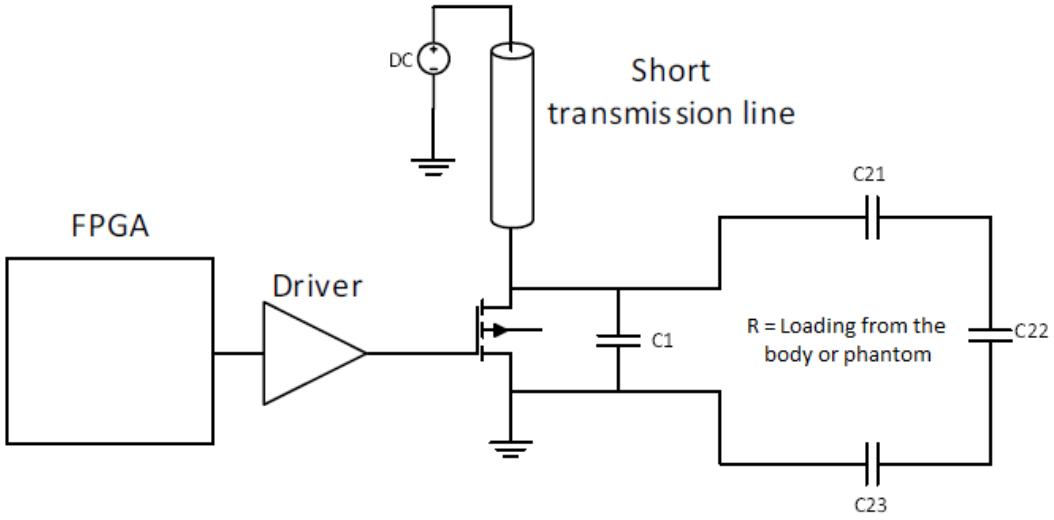


Fig. 2.2 – Modified class-E amplifier design. The RF choke inductor had been replaced with an equivalent transmission line. The transmit coil was designed such that it served as the load network of the amplifier as well. The driver and FPGA blocks are also shown. [2]

The RF choke inductor L_1 had been replaced with an equivalent short coaxial transmission line, which in later designs was also integrated on the amplifier PCB. The detailed analysis on replacing the RF choke inductor with an equivalent transmission line can be found in [2, 3]. Also, the transmit coil used for the excitation purposes had been designed such that it served as the load network of the amplifier as well. The inductance of the coil served as the equivalent of L_2 from Fig. 2.1, i.e., the inductance of the resonance circuit of the amplifier. The three distributed capacitors C_{21}, C_{22}, and C_{23}, used for tuning of the coil, also collectively served as the equivalent of C_2 from Fig. 2.1, i.e., the capacitance of the resonance circuit of the amplifier. The load inductance R was provided by the loading of the coil by either phantom or the body.

The advantages of designing such an on-coil amplifier configuration have also been mentioned in [2, 3]. First, in such design, the coil serves as both the tuning element of the load network of the amplifier and the RF excitation element for the load in the MRI. Second, as detailed in [3], by using the load pull analysis, the input impedance of the coil is designed so as to match with the optimum load impedance of the amplifier, thus achieving the highest efficiency point. And finally, being an on-coil amplifier structure significantly reduces the transmission line losses which otherwise, in conventional configurations where the amplifiers are placed in the systems room away from the coil, would be significant.

The amplifier is fully digitally controlled by the FPGA, which transmits the designed carrier bit-streams to the gate of the transistor via a driver circuitry. The details on the design of and modifications in the driver circuitry can be found in [2, 3]. Here, a brief overview of the driver circuit is presented as follows.

2.3. Driving the Amplifier – A Brief Overview

To drive the LDMOS transistor BLF573, a 3-stage wideband digitally controlled driver had been designed and implemented. The designed bit-streams were transmitted from KCU105 FPGA evaluation board (Xilinx Inc., California, USA) to the driver circuitry as low voltage differential signals (LVDS). LVDS signaling shows better noise performance as compared to single ended signals. Fig. 2.3 shows the block diagram of the designed driver.

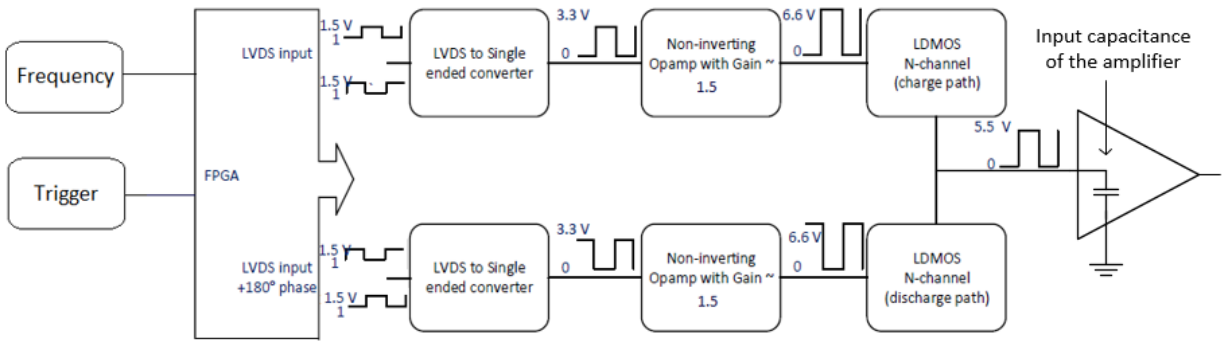


Fig. 2.3 – Three-stage wideband driver design [2, 3]

The FPGA takes as its input a trigger signal and a frequency signal from the signal generator. The value of the frequency signal is set based on the implementation of the FPGA code and may vary from implementation to implementation. The FPGA then transmits the programmed carrier bit-stream (the details on which will be provided later) to the driver circuit in the form of LVDS signals. Two LVDS signals are transmitted with a 180^{o} phase shift in order to control the high and low sides of the driver. At first stage of the driver circuit, these LVDS signals are converted to single ended signals. At second stage, these single ended signals are sent to the non-inverting current-feedback op-amp configuration whose gain is set to approximately 1.5. In the third and final stage, the output signals from the second stage drive the push-pull MOSFETs which in turn drive the main transistor of the class-E amplifier configuration by charging and discharging its gate capacitance. Delay control between the high-side and low-side of the push-pull driver circuit was achieved using the FPGA.

2.4. The Conventional Supply Modulation Approach and Introducing the Concept of Gate Modulation

In order to excite the load in MRI, the output pulse of the amplifier must have a specific shape. In small angle approximation, the flip angle is proportional to the magnitude of the FT (Fourier transform) of RF pulse shape. Therefore apodized sinc pulses are commonly used but other RF pulse designs also exist. In conventional applications of the class-E amplifier, while the frequency modulation is achieved through the gate of the transistor, the amplitude/envelope modulation is achieved via an additional supply modulation block implemented at the drain of the transistor. The details on the implementation of such a supply modulation block can be found in [2, 3]. In this work, the gate modulation approach is suggested as an alternative approach to achieve both the amplitude and frequency modulation of the desired output pulse.

Conceptually speaking, the aim is to remove the supply modulation block at the drain of the amplifier, and to achieve both the amplitude and frequency modulation of the output waveform by only controlling the digital gate input signal of the transistor. In typical 50% duty cycle operation of the amplifier, the digital gate signal of the transistor can be considered as

a uniform sequence of ones and zeros, where each one or zero represents the half duration of the entire period at the frequency of operation. Thus a bit-stream sent by the FPGA in case of such nominal 50% duty cycle operation would be 101010···. The idea of manipulating the carrier bit-stream to a pattern other than 101010··· in order to achieve the amplitude and frequency modulation was first introduced in [2], but at that stage, each cycle was still considered to be consisting of only two bits, not allowing enough flexibility for design.

In this work, the idea of manipulating the carrier bit-stream was revisited and reconstructed, and as will be explained in detail in the next chapter, it was observed that by dividing each cycle of the carrier waveform into more than two bits per cycle, and by manipulating those bits in a certain manner and transmitting them to the gate of the transistor, it was possible to achieve various amplitude levels of the output waveform in addition to achieving the frequency modulation (concept illustrated in Fig. 2.4). In order to realize such a concept, however, both the switch-on and switch-off modes of the class-E amplifier operation needed to be analytically modelled and implemented in software like MATLAB (The MathWorks, Inc., Natick, Massachusetts), so that different carrier bitstream patterns could be designed and tested by running them on such amplifier models.

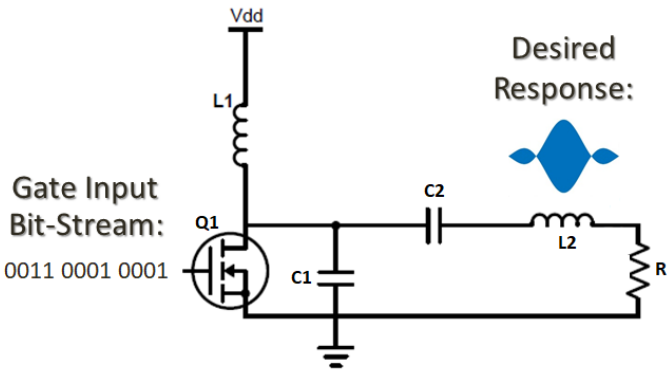


Fig. 2.4 – The gate modulation concept illustrated. By removing the supply modulation block, and by controlling the digital input of the gate of the amplifier, it is aimed to achieve both the amplitude and frequency modulation of the output waveform.

The following section presents, therefore, a detailed account of the mathematical analysis and derivations of the amplifier waveform equations necessary to implement the amplifier models in software. Two different amplifier models are considered at this stage.

2.5. Analytical Modeling of the Amplifier Waveforms

Before digging into the gate-modulation algorithm in detail in the next chapter, the task at hand is to derive and implement a working model of the class-E amplifier in software, and verify that model by performing and comparing simulations using standard circuit simulator software (e.g. Advanced Design System (ADS)).

Two different models of the class-E amplifier were considered for this purpose. In the first model (model 1), a constant-current source assumption was made at the drain of the amplifier for reducing complexity. For reasons explained in later chapters, this amplifier model necessitated to be updated to include the RF choke inductor at drain (model 2), replacing the constant-current source assumption made in case of model 1.

For both models, the switch was considered ideal (zero loss), and the amplifier operation was broken down to two modes: switch-on and switch-off. State-space matrix representations were written for both these modes, from which the essential waveform equations were derived. The mathematical workflow for both models is detailed in the following subsections, while their implementation will be explained in the next chapter.

2.5.1. Model 1: Constant-Current Source Assumption at Drain

Fig. 2.5 shows the schematic of this model. A constant-current source I_{DC} is assumed at the drain of the amplifier. The switch is considered ideal. The unknown state-variables of interest are $i_{L2}(t)$, $v_{C2}(t)$ and $v_{C1}(t)$. Let's start our analysis with the switch-on case as follows.

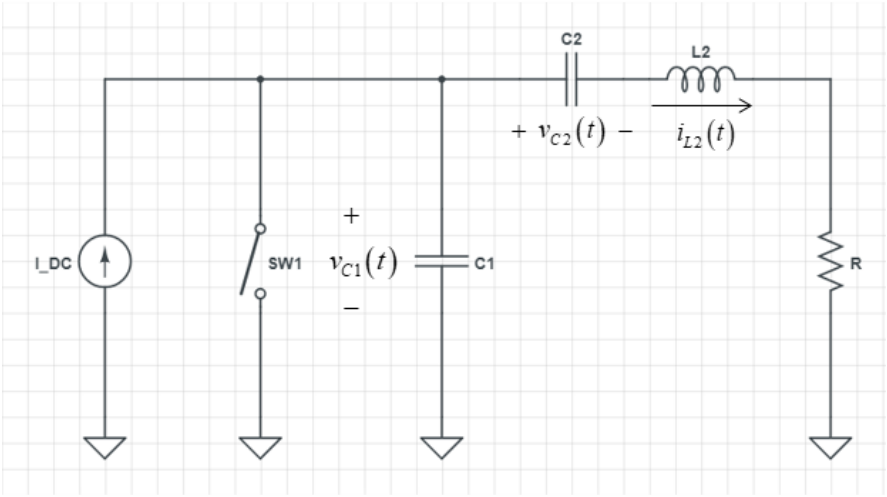


Fig. 2.5 – Amplifier model 1 schematic. An ideal constant-current source is assumed instead of the RF choke inductor at the drain of the amplifier. The transistor is replaced by an ideal switch with zero internal losses.

2.5.1.1 Switch-On Case:

Fig. 2.6 shows the schematic for the switch-on case for the amplifier model 1.

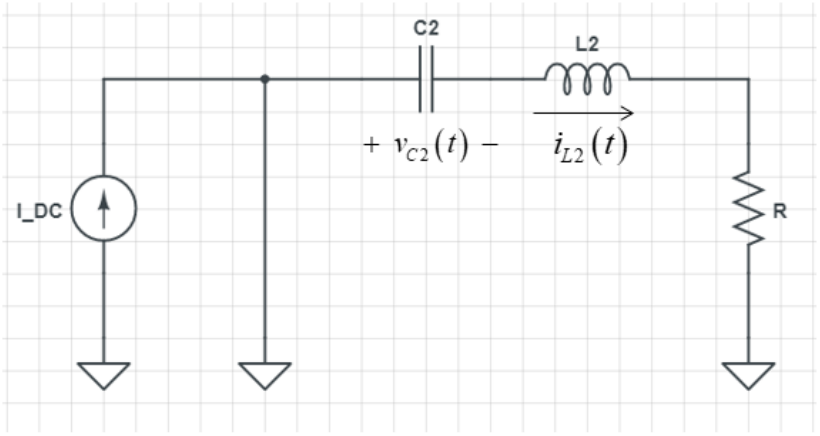


Fig. 2.6 – The schematic diagram for the switch-on case of the amplifier model 1

It can be observed from Fig. 2.6 that the circuit for switch-on case is source-free, which means that we will be investigating the natural response of the circuit in this case. Let's start our analysis by writing the state-space matrix representation for this case. By Kirchhoff's Voltage Law (KVL), we can write:

$$v_{C2}(t) + v_{L2}(t) + v_R(t) = 0 \qquad (2.9)$$

$$\Rightarrow \quad v_{C2}(t) + L_2 \frac{di_{L2}(t)}{dt} + R i_{L2}(t) = 0 \tag{2.10}$$

$$\Rightarrow \quad \frac{di_{L2}(t)}{dt} = -\frac{R}{L_2} i_{L2}(t) - \frac{1}{L_2} v_{C2}(t) \tag{2.11}$$

where $$i_{L2}(t) = i_{C2}(t) = C_2 \frac{dv_{C2}(t)}{dt} \tag{2.12}$$

$$\Rightarrow \quad \frac{dv_{C2}(t)}{dt} = \frac{1}{C_2} i_{L2}(t) \tag{2.13}$$

Here, we note that during the time when the switch is on, voltage across the switch, or equivalently, across the shunt capacitor C_1 is equal to zero (ideal switch assumption).

$$v_{C1}(t) = 0 \tag{2.14}$$

Combining (2.11), (2.13), and (2.14), we can write the state-space matrix representation as follows:

$$\frac{d}{dt}\begin{bmatrix} i_{L2}(t) \\ v_{C2}(t) \\ v_{C1}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R}{L_2} & -\frac{1}{L_2} & 0 \\ \frac{1}{C_2} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L2}(t) \\ v_{C2}(t) \\ v_{C1}(t) \end{bmatrix} \tag{2.15}$$

Now, let's derive the explicit expressions for state-variables $i_{L2}(t)$ and $v_{C2}(t)$. From the state-space matrix representation above, we can write:

$$\frac{di_{L2}(t)}{dt} + \frac{R}{L_2} i_{L2}(t) + \frac{1}{L_2} v_{C2}(t) = 0 \tag{2.16}$$

Taking derivative on both sides of the above equation, we get:

$$\frac{d^2 i_{L2}(t)}{dt^2} + \frac{R}{L_2}\frac{d i_{L2}(t)}{dt} + \frac{1}{L_2}\frac{d v_{C2}(t)}{dt} = 0 \tag{2.17}$$

Combining (2.13) and (2.17), we get:

$$\frac{d^2 i_{L2}(t)}{dt^2} + \frac{R}{L_2}\frac{d i_{L2}(t)}{dt} + \frac{1}{L_2 C_2} i_{L2}(t) = 0 \tag{2.18}$$

Equation (2.18) is a second-order differential equation of the type:

$$\frac{d^2 y(t)}{dt^2} + 2\zeta\omega_0 \frac{dy(t)}{dt} + \omega_0^2 y(t) = 0 \tag{2.19}$$

where $y(t)$ is the unknown variable, ω_0 is the **undamped natural frequency** with dimensions of radians/second, and ζ is the **damping ratio**, a dimensionless parameter [36]. Comparing (2.18) with (2.19), ω_0 and ζ in our case can be defined as follows:

$$\omega_0 = \frac{1}{\sqrt{L_2 C_2}} \tag{2.20}$$

$$\zeta = \frac{1}{2} R \sqrt{C_2 / L_2} \tag{2.21}$$

The associated characteristic equation can be written as follows:

$$s^2 + 2\zeta\omega_0 s + \omega_0^2 = 0 \tag{2.22}$$

The roots of the characteristic equation (2.22), also known as the **natural frequencies,** the **characteristic frequencies,** or the **critical frequencies** of the circuit, can be written as follows:

$$s_{1,2} = \left(-\zeta \pm \sqrt{\zeta^2 - 1}\right)\omega_0 \tag{2.23}$$

Inserting in (2.21) the optimum values of R, C_2 and L_2 that we obtained in Section 2.1, we find that $0 < \zeta < 1$, meaning that the circuit for switch-on case has an **underdamped natural response**, in which case $\sqrt{\zeta^2 - 1} = j\sqrt{1 - \zeta^2}$ $\left(j = \sqrt{-1}\right)$ and the roots of the characteristic equation become:

$$s_{1,2} = \alpha \pm j\omega_d \tag{2.24}$$

where

$$\alpha = -\zeta\omega_0 \tag{2.25}$$

and

$$\omega_d = \omega_0\sqrt{1 - \zeta^2} \tag{2.26}$$

Here, α is called the **damping coefficient,** and ω_d is called the **damped natural frequency.** Inserting the values of ω_0 and ζ from (2.20) and (2.21) into (2.25) and (2.26), we get:

$$\alpha = -\frac{R}{2L_2} \tag{2.27}$$

$$\omega_d = \frac{\sqrt{\frac{4L_2}{C_2} - R^2}}{2L_2} \tag{2.28}$$

And finally the solution to the equation (2.18) for the case of underdamped natural response can be written as follows:

$$i_{L2}(t) = A\exp(\alpha t)\sin(\omega_d t + \theta) \tag{2.29}$$

where A and θ are the initial condition constants, and can be derived as follows:

At time t = 0, we have from equation (2.29):

$$i_{L2}(0) = A\sin\theta \Rightarrow A = \frac{i_{L2}(0)}{\sin\theta} \tag{2.30}$$

By taking derivative of (2.29) and inserting t = 0, we get:

$$\frac{di_{L2}(0)}{dt} = A(\alpha \sin\theta + \omega_d \cos\theta) \tag{2.31}$$

Inserting t = 0 in (2.11), and combining it with (2.31), we get:

$$A(\alpha \sin\theta + \omega_d \cos\theta) = -\frac{R}{L_2} i_{L2}(0) - \frac{1}{L_2} v_{C2}(0) \tag{2.32}$$

Inserting the value of A from (2.30) and solving for θ, we get:

$$\theta = \cot^{-1}\left\{\frac{\frac{-Ri_{L2}(0) - v_{C2}(0)}{L_2} - \alpha i_{L2}(0)}{\omega_d i_{L2}(0)}\right\} \tag{2.33}$$

The expression for $v_{C2}(t)$ can either be derived from the state-space matrix representation of (2.15) or we can write from (2.10) as follows:

$$v_{C2}(t) = -Ri_{L2}(t) - L_2 \frac{di_{L2}(t)}{dt} \tag{2.34}$$

Inserting in the above equation the expression for $i_{L2}(t)$ from (2.29), and solving for $v_{C2}(t)$ results in the following expression:

$$v_{C2}(t) = -(R + \alpha L_2) i_{L2}(t) - \omega_d A L_2 \exp(\alpha t) \cos(\omega_d t + \theta) \tag{2.35}$$

Now let's derive the expressions for $i_{L2}(t)$, $v_{C2}(t)$ and $v_{C1}(t)$ for switch-off case as follows.

2.5.1.2 Switch-Off Case:

The schematic for the switch-off case of the amplifier model 1 is the same as shown in Fig. 2.5 earlier. It can be observed from Fig. 2.5 that the circuit for switch-off case has a DC forcing element I_{DC}, which means that we will be investigating the transient response of the circuit in this case. Let's start by deriving the state-space matrix representation. By Kirchhoff's Voltage Law (KVL), we can write:

$$v_{C1}(t) = v_{C2}(t) + v_{L2}(t) + v_R(t) \tag{2.36}$$

$$\Rightarrow \quad v_{C1}(t) = v_{C2}(t) + L_2 \frac{di_{L2}(t)}{dt} + Ri_{L2}(t) \tag{2.37}$$

$$\Rightarrow \quad \frac{di_{L2}(t)}{dt} = -\frac{R}{L_2} i_{L2}(t) - \frac{1}{L_2} v_{C2}(t) + \frac{1}{L_2} v_{C1}(t) \tag{2.38}$$

where $$i_{L2}(t) = i_{C2}(t) = C_2 \frac{dv_{C2}(t)}{dt} \tag{2.39}$$

$$\Rightarrow \quad \frac{dv_{C2}(t)}{dt} = \frac{1}{C_2} i_{L2}(t) \tag{2.40}$$

By Kirchhoff's Current Law (KCL), we can write:

$$i_{C1}(t) = C_1 \frac{dv_{C1}(t)}{dt} = I_{DC} - i_{L2}(t) \tag{2.41}$$

$$\Rightarrow \quad \frac{dv_{C1}(t)}{dt} = -\frac{1}{C_1} i_{L2}(t) + \frac{1}{C_1} I_{DC} \tag{2.42}$$

Combining (2.38), (2.40), and (2.42), the state-space matrix representation can be written as follows:

$$\frac{d}{dt}\begin{bmatrix} i_{L2}(t) \\ v_{C2}(t) \\ v_{C1}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R}{L_2} & -\frac{1}{L_2} & \frac{1}{L_2} \\ \frac{1}{C_2} & 0 & 0 \\ -\frac{1}{C_1} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L2}(t) \\ v_{C2}(t) \\ v_{C1}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{1}{C_1} \end{bmatrix} I_{DC} \tag{2.43}$$

Now, let's derive the explicit expressions for state-variables $i_{L2}(t)$, $v_{C2}(t)$ and $v_{C1}(t)$. From the state-space matrix representation above, we can write:

$$\frac{di_{L2}(t)}{dt} + \frac{R}{L_2} i_{L2}(t) + \frac{1}{L_2} v_{C2}(t) = \frac{1}{L_2} v_{C1}(t) \tag{2.44}$$

Taking derivative on both sides of the above equation, we get:

$$\frac{d^2 i_{L2}(t)}{dt^2} + \frac{R}{L_2}\frac{di_{L2}(t)}{dt} + \frac{1}{L_2}\frac{dv_{C2}(t)}{dt} = \frac{1}{L_2}\frac{dv_{C1}(t)}{dt} \tag{2.45}$$

Incorporating (2.40) and (2.42) into (2.45), we get:

$$\frac{d^2 i_{L2}(t)}{dt^2} + \frac{R}{L_2}\frac{di_{L2}(t)}{dt} + \frac{1}{L_2 C_2} i_{L2}(t) = \frac{1}{L_2 C_1}\{-i_{L2}(t) + I_{DC}\} \tag{2.46}$$

$$\Rightarrow \quad \frac{d^2 i_{L2}(t)}{dt^2} + \frac{R}{L_2}\frac{di_{L2}(t)}{dt} + \frac{1}{L_2 C_{eq}} i_{L2}(t) = \frac{1}{L_2 C_1} I_{DC} \tag{2.47}$$

where $$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \tag{2.48}$$

The solution to the second-order differential equation (2.47) will be consisting of two components: a transient component and a steady-state component, and will be of the following form [36]:

$$i_{L2}(t) = i_{L2_{trans}} + i_{L2_{ss}} \tag{2.49}$$

Here, the expression for the transient component depends on the value of ζ (defined in Subsection 2.5.1.1), and since in our case $0 < \zeta < 1$ (see Subsection 2.5.1.1), the transient component can be written as follows:

$$i_{L2_{trans}} = A\exp(\alpha t)\sin(\omega_d t + \theta) \tag{2.50}$$

where α and ω_d are the **damping coefficient** and the **damped natural frequency** respectively, and are defined as follows for the switch-off case:

$$\alpha = -\frac{R}{2L_2} \tag{2.51}$$

$$\omega_d = \frac{\sqrt{\frac{4L_2}{C_{eq}} - R^2}}{2L_2} \tag{2.52}$$

Additionally, A and θ are the initial condition constants which we will be deriving in a moment. But before that, let's define the steady-state solution $i_{L2_{ss}}$ as a constant 'c'. Inserting this steady-state solution in (2.47), we get:

$$i_{L2_{ss}} = c = \frac{C_{eq}}{C_1} I_{DC} \tag{2.53}$$

Combining (2.49), (2.50), and (2.53), we can write the solution to (2.47) as follows:

$$i_{L2}(t) = A\exp(\alpha t)\sin(\omega_d t + \theta) + c \tag{2.54}$$

where c is defined in (2.53). Now let's derive the expressions for the initial condition constants A and θ. At time t = 0, we have from the equation (2.54):

$$i_{L2}(0) = A\sin(\theta) + c \Rightarrow A = \frac{i_{L2}(0) - c}{\sin\theta} \tag{2.55}$$

By taking derivative of (2.54) and inserting t = 0, we get:

$$\frac{di_{L2}(0)}{dt} = A(\alpha \sin\theta + \omega_d \cos\theta) \tag{2.56}$$

Inserting t = 0 in (2.38), and combining it with (2.56), we get:

$$A(\alpha \sin\theta + \omega_d \cos\theta) = -\frac{R}{L_2} i_{L2}(0) - \frac{1}{L_2} v_{C2}(0) + \frac{1}{L_2} v_{C1}(0) \tag{2.57}$$

Inserting the value of A from (2.55) and solving for θ, we get:

$$\theta = \cot^{-1}\left\{\frac{\frac{-Ri_{L2}(0) - v_{C2}(0) + v_{C1}(0)}{L_2} - \alpha\{i_{L2}(0) - c\}}{\omega_d\{i_{L2}(0) - c\}}\right\} \tag{2.58}$$

Let's now derive the expression for $v_{C1}(t)$. From the state-space representation (2.43), we can write:

$$\frac{dv_{C1}(t)}{dt} = \frac{1}{C_1}\{I_{DC} - i_{L2}(t)\} \tag{2.59}$$

Inserting in the above equation the expression for $i_{L2}(t)$ from (2.54), and integrating both sides from time 0 (the instant the transistor was switched off) to any time t during switch-off, we get:

$$\begin{aligned} v_{C1}(t) = \frac{1}{C_1}\Big[&(I_{DC} - c)t \\ &- \frac{A}{\alpha^2 + {\omega_d}^2}\exp(\alpha t)\{\alpha \sin(\omega_d t + \theta) \\ &- \omega_d \cos(\omega_d t + \theta)\}\Big] + v_{C1}(0) \end{aligned} \tag{2.60}$$

where under the ZVS (zero-voltage switching) condition, $v_{C1}(0) = 0$.

We can now conveniently derive the expression for $v_{C2}(t)$ using the equation (2.37). By inserting the expression for $i_{L2}(t)$ from (2.54) into (2.37) and evaluating the corresponding time-derivative, and by solving the resulting equation for $v_{C2}(t)$, we get the following result:

$$v_{C2}(t) = \{v_{C1}(t) - Ri_{L2}(t)\} - AL_2\exp(\alpha t)\{\omega_d \cos(\omega_d t + \theta) + \alpha \sin(\omega_d t + \theta)\} \quad (2.61)$$

where $v_{C1}(t)$ is already defined in (2.60).

2.5.2. Model 2: Inductor Assumption at Drain

Fig. 2.7 shows the schematic of this model where the constant-current source I_{DC} is now replaced with an RF choke inductor L_1. The unknown state-variables of interest in this case are $i_{L2}(t)$, $v_{C2}(t)$, $v_{C1}(t)$ and $i_{L1}(t)$.

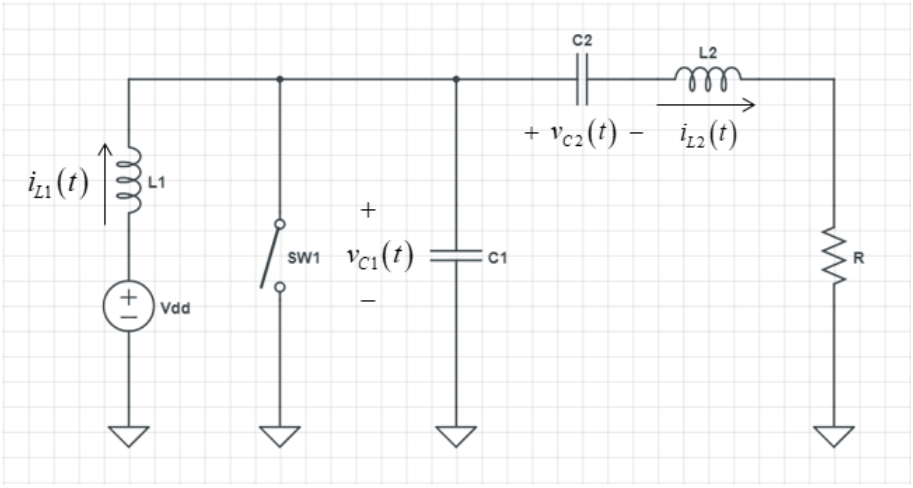


Fig. 2.7 – Amplifier model 2 schematic. The previous ideal constant-current source assumption in model 1 is now replaced by an RF choke inductor assumption at the drain of the amplifier. Again, an ideal, lossless switch is considered in place of the transistor.

Including this inductor inherently increases the order and therefore the mathematical complexity of the model. But this can be reduced by expressing the current through the inductor L_1 ($i_{L1}(t)$) as a linear expression as follows:

$$i_{L1}(t) = at + b \quad (2.62)$$

This assumption/approximation for $i_{L1}(t)$ is not arbitrary. Running simulations in ADS2016 (Advanced Design System, Keysight, Santa Rosa, CA) for this model result in a waveform shape as shown in Fig. 4.3 (b). Such a higher order waveform can be approximated by a linear ramp

function (equation (2.62)) for a large value of inductor L_1, thereby reducing the overall complexity of the model to second-order. The slope 'a' and the y-intercept 'b' are calculated and updated during each iteration of the switch operation for both switch-on and switch-off cases as will be shown in the following subsections.

Let's start our analysis for this model with the switch-on case as follows.

2.5.2.1 Switch-On Case:

Fig. 2.8 shows the schematic for the switch-on case for the amplifier model 2.

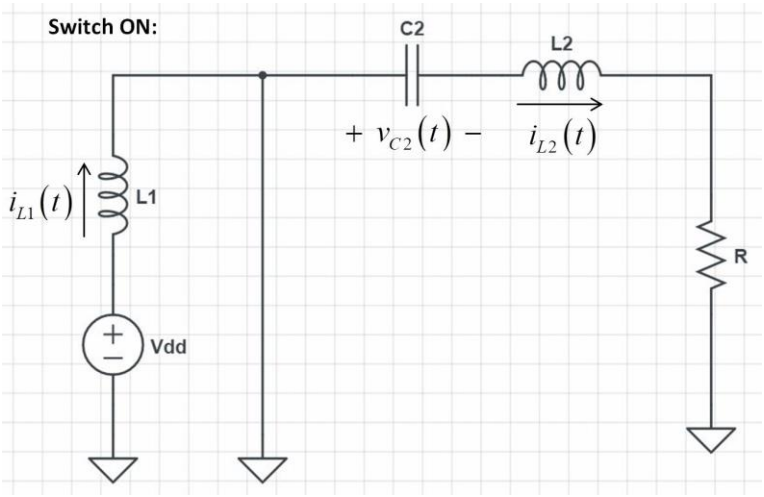


Fig. 2.8 – The schematic diagram for the switch-on case of the amplifier model 2

As can be observed from Fig. 2.1, the right side of the circuit is source-free similar to the switch-on case circuit for model 1, meaning its analysis will be identical to the analysis done in Subsection 2.5.1.1. In addition, from the left side of the circuit, we can write the following:

$$V_{DD} - 0 = L_1 \frac{di_{L1}(t)}{dt} \tag{2.63}$$

$$\Rightarrow \quad \frac{di_{L1}(t)}{dt} = \frac{V_{DD}}{L_1} \tag{2.64}$$

Combining (2.11), (2.13), and (2.14) from Subsection 2.5.1.1 with (2.64) above, we can write the state-space matrix representation for the switch-on case of model 2 as follows:

$$\frac{d}{dt}\begin{bmatrix} i_{L2}(t) \\ v_{C2}(t) \\ v_{C1}(t) \\ i_{L1}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R}{L_2} & -\frac{1}{L_2} & 0 & 0 \\ \frac{1}{C_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L2}(t) \\ v_{C2}(t) \\ v_{C1}(t) \\ i_{L1}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{1}{L_1} \end{bmatrix} V_{DD} \tag{2.65}$$

The expressions for $i_{L2}(t)$, $v_{C2}(t)$ and $v_{C1}(t)$ in this case are exactly the same as derived in Subsection 2.5.1.1, and are summarized as follows:

$$i_{L2}(t) = A\exp(\alpha t)\sin(\omega_d t + \theta) \tag{2.66}$$

$$v_{C2}(t) = -(R + \alpha L_2)i_{L2}(t) - \omega_d A L_2 \exp(\alpha t)\cos(\omega_d t + \theta) \tag{2.67}$$

$$v_{C1}(t) = 0 \tag{2.68}$$

where α is the damping coefficient and is defined in (2.27), ω_d is the damped natural frequency and is defined in (2.28), and A and θ are the initial condition constants and are defined in (2.30) and (2.33) respectively.

Finally, let's derive the expression for $i_{L1}(t)$. Taking the integral on both sides of (2.64) from time 0 (the instant the transistor was switched on) to any time t during switch-on, we get:

$$i_{L1}(t) = \frac{V_{DD}}{L_1}t + i_{L1}(0) \tag{2.69}$$

where $i_{L1}(0)$ is an initial condition constant. By comparing the above equation with (2.62), we get $a = \frac{V_{DD}}{L_1}$ and $b = i_{L1}(0)$. The value for b (or equivalently $i_{L1}(0)$) can be assigned arbitrarily for the first iteration of the model and then needs to be updated during each iteration.

2.5.2.2 Switch-Off Case:

Fig. 2.9 shows the schematic for the switch-off case for the amplifier model 2.

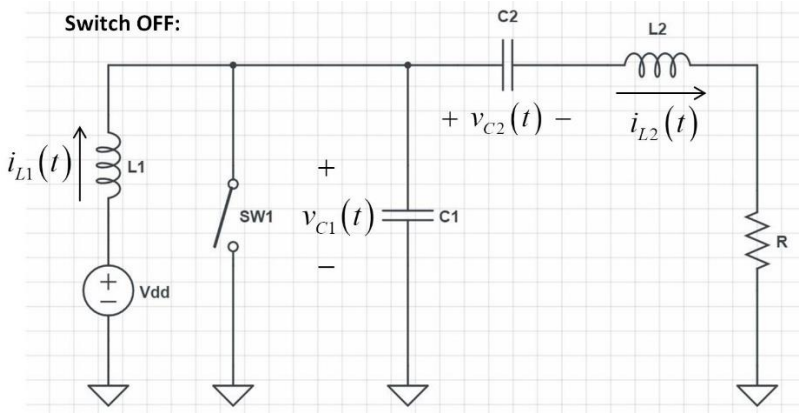


Fig. 2.9 – The schematic diagram for the switch-off case of the amplifier model 2

By using Kirchhoff's Voltage Law (KVL) and by following the same steps as in Subsection 2.5.1.2, we can write:

$$\frac{di_{L2}(t)}{dt} = -\frac{R}{L_2} i_{L2}(t) - \frac{1}{L_2} v_{C2}(t) + \frac{1}{L_2} v_{C1}(t) \tag{2.70}$$

$$\frac{dv_{C2}(t)}{dt} = \frac{1}{C_2} i_{L2}(t) \tag{2.71}$$

Now, by Kirchhoff's Current Law (KCL), we can write:

$$i_{C1}(t) = C_1 \frac{dv_{C1}(t)}{dt} = i_{L1}(t) - i_{L2}(t) \tag{2.72}$$

$$\Rightarrow \quad \frac{dv_{C1}(t)}{dt} = -\frac{1}{C_1} i_{L2}(t) + \frac{1}{C_1} i_{L1}(t) \tag{2.73}$$

Also, we can see from the circuit in Fig. 2.9 that:

$$V_{DD} - v_{C1}(t) = L_1 \frac{di_{L1}(t)}{dt} \tag{2.74}$$

$$\Rightarrow \qquad \frac{di_{L1}(t)}{dt} = -\frac{1}{L_1} v_{C1}(t) + \frac{1}{L_1} V_{DD} \tag{2.75}$$

Combining (2.70), (2.71), (2.73), and (2.75), we can write the state-space matrix representation as follows:

$$\frac{d}{dt}\begin{bmatrix} i_{L2}(t) \\ v_{C2}(t) \\ v_{C1}(t) \\ i_{L1}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R}{L_2} & -\frac{1}{L_2} & -\frac{1}{L_2} & 0 \\ \frac{1}{C_2} & 0 & 0 & 0 \\ -\frac{1}{C_1} & 0 & 0 & \frac{1}{C_1} \\ 0 & 0 & -\frac{1}{L_1} & 0 \end{bmatrix} \begin{bmatrix} i_{L2}(t) \\ v_{C2}(t) \\ v_{C1}(t) \\ i_{L1}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{1}{L_1} \end{bmatrix} V_{DD} \tag{2.76}$$

The task at hand now is to derive the explicit expressions for state-variables $i_{L2}(t)$, $v_{C2}(t)$, $v_{C1}(t)$ and $i_{L1}(t)$. Starting with the derivation of $i_{L2}(t)$ and by following the similar steps as in Subsection 2.5.1.2, keeping in mind that I_{DC} is now replaced with $i_{L1}(t)$, we can write the following differential equation:

$$\Rightarrow \qquad \frac{d^2 i_{L2}(t)}{dt^2} + \frac{R}{L_2}\frac{di_{L2}(t)}{dt} + \frac{1}{L_2 C_{eq}} i_{L2}(t) = \frac{1}{L_2 C_1} i_{L1}(t) \tag{2.77}$$

where $$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \tag{2.78}$$

By defining $i_{L1}(t)$ as a linear expression as in (2.62), the equation (2.77) can be reduced to a second-order differential equation, and by following the similar steps as in Subsection (2.5.1.2), we can write the solution to the equation (2.77) as follows:

$$i_{L2}(t) = i_{L2_{trans}} + i_{L2_{ss}} = A\exp(\alpha t)\sin(\omega_d t + \theta) + ct + d \tag{2.79}$$

where $i_{L2_{trans}} = A\exp(\alpha t)\sin(\omega_d t + \theta)$ is the transient solution while $i_{L2_{ss}} = ct + d$ is the particular steady-state solution when $i_{L1}(t) = at + b$. Here, α and ω_d are the same as

defined in (2.51) and (2.52) respectively, and, A and θ are the initial condition constants that we will be deriving in a moment. But first, let's derive the expressions for constants c and d. By inserting $i_{L1}(t) = at + b$ and $i_{L2}(t) = ct + d$ in the differential equation (2.77), evaluating the time-derivatives, and re-arranging, we get:

$$\frac{1}{L_2 C_{eq}} ct + \frac{R}{L_2} c + \frac{1}{L_2 C_{eq}} d = \frac{1}{L_2 C_1} at + \frac{1}{L_2 C_1} b \tag{2.80}$$

By comparing the corresponding coefficients of the first-degree and zero-degree terms in the above equation, we get:

$$\frac{1}{L_2 C_{eq}} c = \frac{1}{L_2 C_1} a \Rightarrow c = \frac{C_{eq}}{C_1} a \Rightarrow a = \frac{C_1}{C_{eq}} c \tag{2.81}$$

And,

$$\frac{R}{L_2} c + \frac{1}{L_2 C_{eq}} d = \frac{1}{L_2 C_1} b \Rightarrow d = \left(\frac{b}{C_1} - Rc\right) C_{eq} \tag{2.82}$$

Here, we have not yet defined the expressions for constants 'a' and 'b'. We will be defining those as we derive the expression for $i_{L1}(t)$ later in the subsection. But let's now evaluate the expressions for the initial condition constants A and θ.

At time t = 0, we have from the equation (2.79):

$$i_{L2}(0) = A \sin(\theta) + d \Rightarrow A = \frac{i_{L2}(0) - d}{\sin \theta} \tag{2.83}$$

By taking derivative on both sides of the equation (2.79) and inserting t = 0, we get:

$$\frac{d i_{L2}(0)}{dt} = A(\alpha \sin \theta + \omega_d \cos \theta) + c \tag{2.84}$$

Inserting t = 0 in (2.70), and combining it with (2.84) above, we get:

$$A(\alpha \sin \theta + \omega_d \cos \theta) = -\frac{R}{L_2} i_{L2}(0) - \frac{1}{L_2} v_{C2}(0) + \frac{1}{L_2} v_{C1}(0) \tag{2.85}$$

Inserting the value of A from (2.83) and solving for θ, we get:

$$\theta = \cot^{-1}\left\{\frac{\frac{-Ri_{L2}(0) - v_{C2}(0) + v_{C1}(0)}{L_2} - \alpha\{i_{L2}(0) - d\} - c}{\omega_d\{i_{L2}(0) - c\}}\right\} \tag{2.86}$$

Let's now derive the expression for $v_{C1}(t)$. From the state-space representation (2.76), we can write:

$$\frac{dv_{C1}(t)}{dt} = \frac{1}{C_1}\{i_{L2}(t) - i_{L2}(t)\} \tag{2.87}$$

Inserting in the above equation the expressions for $i_{L1}(t)$ and $i_{L2}(t)$ from (2.62) and (2.79), and integrating both sides of the resulting equation from time 0 (the instant the transistor was switched off) to any time t during switch-off, we get:

$$\begin{aligned} v_{C1}(t) = \frac{1}{C_1}\Bigg[\left(\frac{C_1}{C_{eq}} - 1\right)\frac{c}{2}t^2 + (b-d)t \\ - \frac{A}{\alpha^2 + {\omega_d}^2}\exp(\alpha t)\{\alpha\sin(\omega_d t + \theta) \\ - \omega_d\cos(\omega_d t + \theta)\}\Bigg] + v_{C1}(0) \end{aligned} \tag{2.88}$$

where under the ZVS (zero-voltage switching) condition, $v_{C1}(0) = 0$.

Next, by inserting the expression for $i_{L2}(t)$ from (2.79) to (2.70) and evaluating the corresponding time-derivative, and by solving the resulting equation for $v_{C2}(t)$, we get the following expression:

$$\begin{aligned} v_{C2}(t) = \{v_{C1}(t) - Ri_{L2}(t)\} \\ - L_2[A\exp(\alpha t)\{\omega_d\cos(\omega_d t + \theta) \\ + \alpha\sin(\omega_d t + \theta)\} + c] \end{aligned} \tag{2.89}$$

And finally, by taking the integral on both sides of the equation (2.75) from time 0 (the instant the transistor was switched off) to any time t during switch-off, and solving for $i_{L1}(t)$, we get:

$$i_{L1}(t) = \frac{1}{L_1}\left\{V_{DD} - \frac{1}{t}\int_0^t v_{C1}(t)dt\right\}t + i_{L1}(0) \tag{2.90}$$

where $i_{L1}(0)$ is the initial condition constant. By comparing the above equation with (2.62), we get:

$$a = \frac{1}{L_1}\left\{V_{DD} - \frac{1}{t}\int_0^t v_{C1}(t)dt\right\} \tag{2.91}$$

$$b = i_{L1}(0) \tag{2.92}$$

Here, the value of b (or equivalently $i_{L1}(0)$) is easy to evaluate. It can be assigned arbitrarily during the first iteration of the model and then it simply needs to be updated during each iteration. But the real deal here is to find the value of the constant 'a'. In the expression for the constant 'a' above, we can see that there is an integral expression involved of the voltage $v_{C1}(t)$ whose own expression in (2.88) involves the unknown constant 'c' which in turn is related to the constant 'a' by the equation (2.81). This riddle of unknown constants can be solved by approximating the value of the voltage $v_{C1}(t)$ during the switch-off duration as a constant v_{C1_eff}, which is essentially the effective value of the voltage $v_{C1}(t)$ during the entire switch-off duration of the model. The expression for v_{C1_eff} is defined as follows:

$$v_{C1\_eff} = \frac{1}{\Delta t}\int_0^{\Delta t} v_{C1}(\Delta t)dt \tag{2.93}$$

where Δt is the switch-off duration of the model. Here, $v_{C1}(\Delta t)$ is defined using (2.88) as follows:

$$v_{C1}(\Delta t) = \frac{1}{C_1}\left[\left(\frac{C_1}{C_{eq}} - 1\right)\frac{c}{2}\Delta t^2 + (b-d)\Delta t - \frac{A}{\alpha^2 + {\omega_d}^2}\exp(\alpha\Delta t)\{\alpha\sin(\omega_d\Delta t + \theta) - \omega_d\cos(\omega_d\Delta t + \theta)\}\right] \quad (2.94)$$

Inserting the expression for v_{C1_eff} from (2.93) into (2.91) and since $a = \frac{C_1}{C_{eq}}c$, we can write:

$$\frac{C_1}{C_{eq}}c = \frac{1}{L_1}\left(V_{DD} - v_{C1\_eff}\right) \quad (2.95)$$

$$\Rightarrow \quad \frac{C_1 L_1}{C_{eq}}c - V_{DD} + v_{C1\_eff} = 0 \quad (2.96)$$

By inserting the expression for $v_{C1}(\Delta t)$ from (2.94) into (2.93), and by symbolically evaluating the integral expression in (2.93), we can find the expression for v_{C1_eff}. Then, by inserting this resulting expression for v_{C1_eff} into the equation (2.96), and by solving the resulting equation for the value of c, we can finally obtain the expression for and hence the value of the constant 'c'. The value of 'a' can now be easily evaluated using (2.81).

Following is a step-by-step method explaining the order in which the initial condition constants A and θ, and the other associated constants a, b, c and d are evaluated:

Step 1: Assume c = 0 at the beginning, and evaluate d, A and θ from their respective expressions.

Step 2: Find the value of c, and consequently the value of a, using the detailed method explained above.

Step 3: Re-evaluate constants d, A and θ, incorporating the value of c in their respective expressions.

Step 4: Repeat steps 2 and 3 until the values of all constants stabilize.

Now that the analytical models of the amplifier have been developed, the next step is to implement these models in software, and compare their performance against the amplifier model run in circuit simulator software. Once the satisfactory performance of these models is achieved, the next step would be to develop and implement the gate modulation algorithm in software, and to test its performance on hardware as well, as explained in next chapter.

CHAPTER 3

METHODS

In this chapter, the methods used to implement the amplifier models in software, and a detailed account of the gate modulation algorithm along with its implementation in software and hardware is provided. The software implementation of the amplifier models is first verified by running simulation in ADS2016 (Advanced Design System, Keysight, Santa Rosa, CA), and then, after providing the details on gate modulation algorithm, the methods used to design the desired RF pulses in software are explained. Next, the details on the hardware used to test the generated carrier bit-streams are provided. The experimental setup for bench-top experiments is then explained in detail along with the reasons and methods used to re-optimize the carrier bit-stream on hardware. Finally, the experimental setup for MR experiments, the associated challenges and problems, and the methods used to resolve those problems are explained.

3.1. Amplifier Model Implementation

Now that the essential waveform equations for both models of the class-E amplifier (see Section 2.5) are derived, these models can be implemented to compare the resulting waveforms with the simulations.

3.1.1. Implementation

Both models (i.e., model 1 as well as model 2) of the class-E amplifier which were derived in Section 2.5 are implemented in MATLAB in a similar way. So instead of explaining the implementation of both models separately, the essential blocks into which the entire code is subdivided for both models, is explained as follows.

1. Timing and Frequency Parameters: The working frequency of the amplifier is set to f = 64 MHz (T = 1/64 MHz = 15.625 ns). The time-point resolution is set to 20 points per one time period T. The simulation can be run for 200 μs, 2 ms, or any other time duration based on the requirements of the waveform to be designed.

2. Amplifier Design Parameters: In this block, the values for input parameters (V_{DD}, I_{DC} in case of model 1) are defined. A high value of L_1 is defined in case of model 2 to block the RF signal. The duty cycle is set to 50% and the quality factor (Q) is set to 64 based on the specifications of the hardware. The values for R, C_1, C_2 and L_2 are then calculated using Equations (2.1-2.4). During the implementation of both models, after calculating the initial values for the circuit parameters from Equations (2.1-2.4), the emphasis is put on tuning those values so as to achieve both the ZVS and ZVDS conditions. Following figure is used as a reference while tuning the component values [35]:

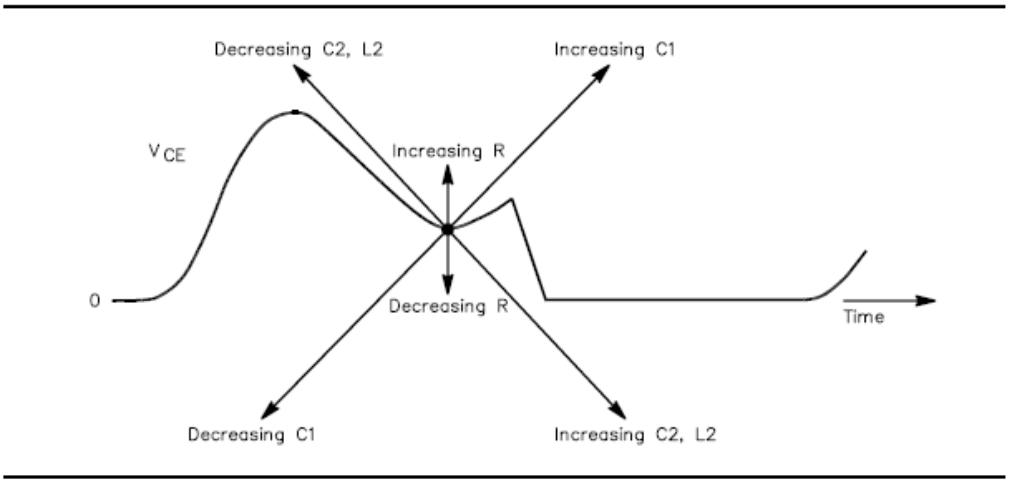


Fig. 3.1 – The effects of adjusting the load network components on the switch-voltage waveform [35]

3. Model Implementation: In this block, the equations derived for both the switch-on and switch-off cases of the model are implemented. The initial condition constants and other involved constants for both switch-on and switch-off cases are evaluated in separate functions during each half-cycle of operation.

4. Plotting: Finally, the essential waveforms are plotted. The waveforms of special interest are the switch-voltage $v_{C1}(t)$ and output current $i_{L2}(t)$ waveforms for both models, while the RF choke inductor current $i_{L1}(t)$ waveform is also essential to be plotted for model 2.

3.1.2. Simulations in Circuit Simulator for Comparison and Verification

In order to confirm the validity of the analytical models, a realistic model of the class-E amplifier was implemented in the circuit simulator. The schematic diagram of the circuit simulator model is shown in Fig. 3.2.

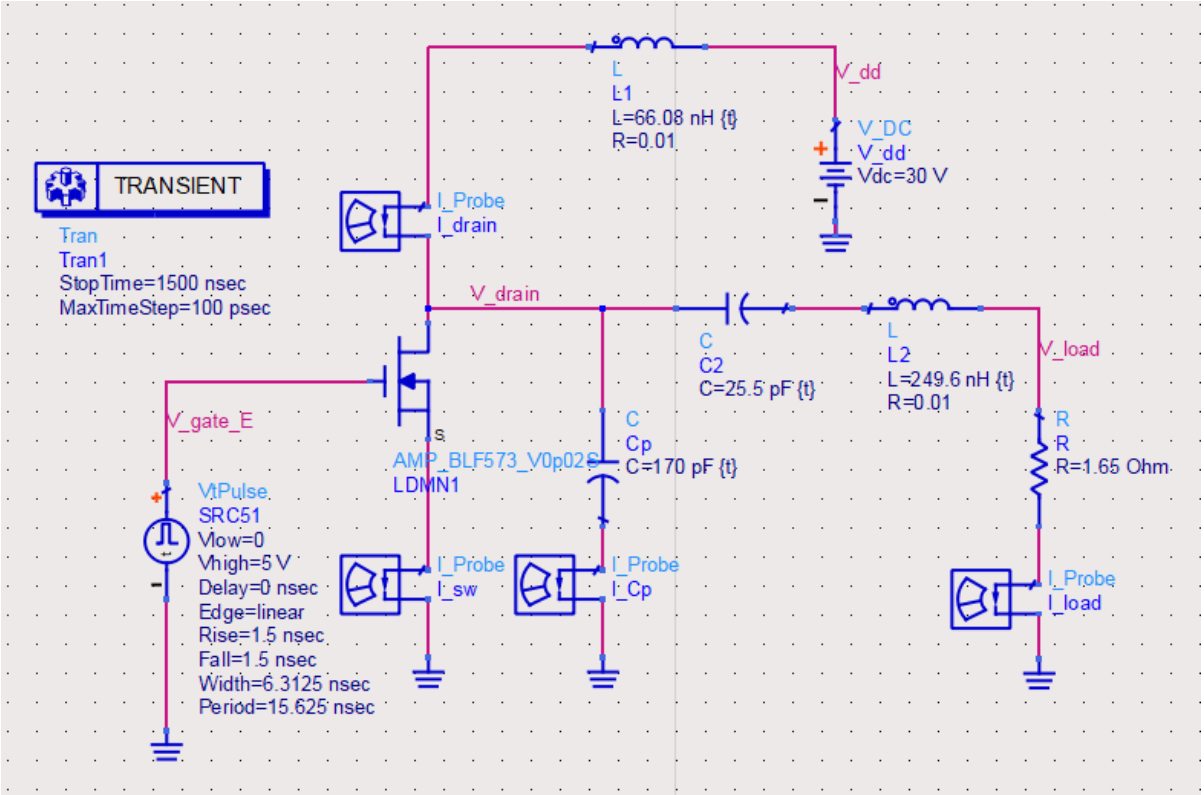


Fig. 3.2 – Schematic diagram of the class-e amplifier model with realistic switch

As shown in the schematic above, a realistic LDMOS RF power transistor model (Ampleon, BLF573, Nijmegen, The Netherlands) is used as the main transistor of the amplifier. The characteristic parameters of this transistor are shown in Table 3.1 below.

Table 3.1 – Characteristic parameters of BLF573	
Output Power (W)	300
Drain-Source On Resistance $R_{DS(on)}$ (mΩ)	90
Feedback Capacitance C_{rs} (pF)	2.3
Input Capacitance C_{iss} (pF)	300
Output Capacitance C_{oss} (pF)	103
Maximum V_{ds} (V)	110
Threshold Voltage V_{th} (V)	2

Here in the circuit simulations, the gate of the amplifier is driven by a 64 MHz square wave signal with rise and fall times of 1.5 ns each. The RF choke inductor is included in the model. The load network values are set as found during the implementation of analytical models of the amplifier. Finally, the resulting essential waveforms are compared with their counterparts from the analytical implementation, and the circuit parameters are tuned accordingly to achieve the ZVS (Zero Voltage Switching) and ZVDS (Zero Voltage Derivative Switching) conditions in all implementations. Fig. 3.3 shows the screenshot of the tuning environment set in the circuit simulator for this purpose.

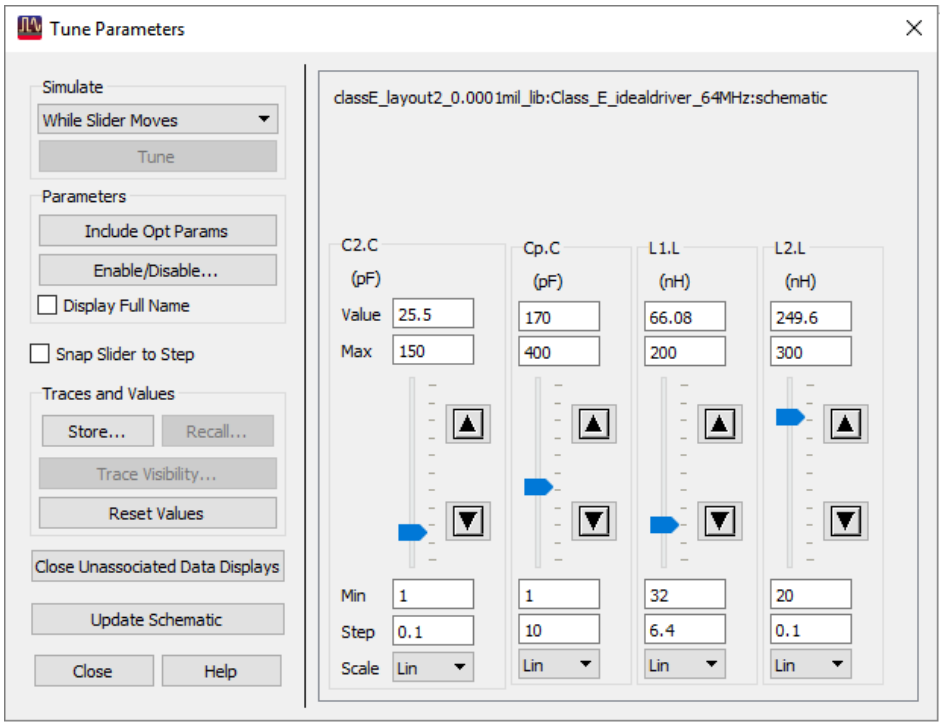


Fig. 3.3 – The load-network tuning environment in the circuit simulator

3.2. The Gate Modulation Algorithm

Now that we have implemented and tuned the analytical models of the amplifier, the next step is to design and implement the gate modulation algorithm. The idea was briefly introduced in Section 2.5. The goal here is to remove the conventional supply modulation block and achieve both the amplitude and frequency modulation of the output waveform by digitally controlling the duty cycle and phase of the carrier frequency applied to the gate of the transistor. The gist of the algorithm is summarized in the following two paragraphs while further details regarding several aspects of the algorithm and its implementation in MATLAB are provided in the consequent subsections.

Working at $f = 64$ MHz, we associate each cycle (T = 15.625 ns) of the carrier frequency with k bits, where in our case, k = 4. An RF pulse of duration s = 2 ms would require a carrier signal of the same duration, consisting of s/T cycles and consequently $n = (k \times s/T)$ bits. In order to achieve the desired pulse shape at the output, 2^n combinations for the carrier frequency exist to choose from, requiring infeasible computational power.

At this point, the carrier bit-stream is divided into multiple subsections. In each subsection, Q number of cycles are needed to be designed where Q is the quality factor of the system. Considering Q = 50, $k \times Q$ bits (200 bits in our case) are needed to be designed and repeated in each subsection. This still requires 2^{200} combinations to choose from, still requiring infeasible computational power. The presented solution to the problem is as follows.

In each subsection, $k \times m$ number of bits (where m is an integer ranging from 1 to 16, and equals the number of cycles being controlled per each subsection) are controlled and repeated over the entire subsection (for m = 16, sampling rate equals $T \times m = 0.25\ \mu s$ at 64 MHz, providing a bandwidth of 4 MHz), and the amplifier model is run for that subsection. A set of only three bit-stream patterns (0000 = 0%, 0001 = 25%, 0011 = 50%) is used for controlling each cycle. The resulting output waveform for each subsection is compared in amplitude with the desired pulse for that subsection. Once the amplitude match is obtained, the bit-stream elements are shifted left or right to achieve the phase match. This process is repeated for all subsections until a customized carrier bit-stream, with least error between the desired and predicted waveforms, is generated.

3.2.1. Running the Amplifier's Circuit Simulator Model at Different Duty Cycles

The last two paragraphs above explain the gist of the algorithm. In order to elaborate further on how the idea was initially pitched, let's get back to the amplifier's implementation in the circuit simulator explained earlier in Subsection 3.1.2. We know that class-E amplifier is a non-linear amplifier, meaning that it has a non-linear gain. In order to further understand the behavior of this non-linearity, the amplifier's circuit model was run at different duty-cycles from 6.25% to 93.75% with a step-size of 6.25% and the resulting output waveform's amplitude levels were observed. It was based on these observations that the earliest concept of the currently implemented gate modulation algorithm was realized. The effects of changing the duty cycle on input and output power, and the associated drain efficiency were also observed.

3.2.2. Running the Amplifier's Analytical Models at Different Duty Cycles

The obvious next step was to test the amplifier's analytical models at different duty cycles as well and see if their performance correlated with the observations from running the circuit simulator model at different duty cycles. This is when, in MATLAB code, the idea of breaking one cycle of operation into four bits was conceptualized. Till this point in the development of analytical models, the duty-cycle was kept fixed at 50%. One complete cycle of operation was represented by only two bits: '0' and '1' where '0' represents the switch-off case, and '1' represents the switch-on case. In conventional operation of the amplifier, the switch is on half of the period and it is off in the other half. Therefore, bitstream of '01' represented one full period. In this implementation, before the execution of the switch-on case equations, the values for initial condition constants were obtained from the final values of the previous execution of switch-off equations, and vice versa.

But now, in order to test the analytical models at different duty cycles, each cycle needed to be broken to k bits, least possible value for k being 4, so that the models could be tested for different duty cycles (for example 0001 = 25%, 0011 = 50%, 0111 = 75%). Worth noting here is the fact that the initial condition values would still be updated only at the transition from switch-off to switch-on and vice versa. Meaning, if, for example, the amplifier model would be running at 25% duty cycle (0001), the first three zeros will be grouped together and the switch-off case would run for all those zeros. Then, at the transition from the third zero to one, the initial condition values would be updated, and finally the switch-on case would run for the last bit '1' in 0001.

This is the point where analytical model 1 (constant-current source assumption at the drain of the amplifier) failed. This model worked well for 50% duty-cycle operation of the amplifier, but when duty cycles other than 50% were introduced into the model, the constant-current source assumption at the drain of the amplifier caused the initial condition constants to show unstable behavior. This was in contrast to the analytical model 2 where more practical RF choke inductor assumption was made at the drain of the amplifier. In this model, the drain

current (the current through the RF choke inductor) was set to be a variable itself ($i_{L1}(t)$) and it was observed that the initial condition constants were updated without showing unstable behavior for cases other than 50%. It must be kept in mind now that further developments in the algorithm are done using the analytical model 2.

As will be shown in the next chapter, running the amplifier's circuit simulator model for duty cycles higher than 50% resulted in higher switch losses and consequently lower efficiency. Similar observations were observed by running the analytical model 2 at higher duty cycles as well. Therefore, further development of the algorithm from this stage onwards necessitated to be working under and up to 50% duty cycle.

3.2.3. Achieving Amplitude Modulation Using Only k = 4 Bits per Cycle

In order to achieve more amplitude levels using only 4 bits per cycle, different duty cycle combinations were combined and repeated over certain durations of time. For example, we know that 0000 will provide a 0% duty cycle while 0001 will provide a 25% duty cycle, each resulting in their own associated amplitude levels at the output waveform. What can be done here is to combine these two bit-stream patterns (i.e., 0000 and 0001) and repeat these over for multiple number of cycles to observe their effect on the amplitude of the output waveform. The bit-stream now would like something like: 0000 0001 0000 0001 0000 0001⋯ and so on. As will be shown in the next chapter, it was observed that this new bit-stream pattern provided an amplitude level lower than that provided by 0001 but higher than that provided by 0000. An important point to remember here is that, since the model's quality factor is ~60, it would take about 60 cycles ($15.625\ ns\ \times 60 = 0.9375\ \mu s$) for the output waveform amplitude to reach steady-state.

Now, in order to ultimately modulate a sinc pulse, a lot more amplitude levels of the output waveform were required. This was achieved by designing a bit-stream pattern consisting of multiple number of cycles (the number of cycles to be designed was defined as an integer 'm', where it was observed that sufficient amplitude variation could be achieved using values of 'm' from 1 to 16), and by using any of the bit-stream patterns 0000, 0001, and 0011 while

designing each cycle of the entire bit-stream pattern. The resulting example patterns for three different values of 'm' are shown in Table 3.2 below.

Table 3.2 – Examples of different bit-stream patterns for m = 2, 4, 6

Number of Cycles to be Designed	**Examples**	
m = 2	0000 0001	0001 0011
m = 4	0000 0001 0001 0011	0001 0011 0011 0011
m = 6	0000 0000 0001 0001 0001 0011	0001 0001 0011 0011 0011 0011

These bit-stream patterns were then repeated for certain durations of time and the resulting amplitudes of the output waveform were observed.

3.2.4. The Effect of Shifting the bits and Achieving Phase-Modulation

Till now, we have only been considering three bit-stream patterns: 0000 = 0%, 0001 = 25%, 0011 = 50%, and their combinations over multiple cycles (m = 1, 2, 3, etc.) to achieve multiple amplitude levels of the output waveform. But the amplitude match isn't the only goal. We need to match the phase and frequency of the output waveform as well. This can be achieved in two ways: either 1) by applying a circular shift to the entire designed bit-stream pattern and then repeating the resulting bit-stream pattern over the specified duration of time, or 2) by shifting the position of bits in a specific cycle of the entire designed bit-stream pattern (this is applicable when $m > 1$, because when $m = 1$, this is equivalent to applying a circular shift) and then repeating the resulting bit-stream pattern over the specified duration of time. Both these cases are explained in more detail in the following passages.

Applying a circular shift to the entire bit-stream pattern will simply shift the entire output waveform by a phase of $\pi/2$ (since k = 4). Thus applying a circular shift four times (when k = 4) will result in the same phase as without applying any circular shift at all, while the amplitude of the waveform will remain unaffected throughout. This is shown by an example in the Table 3.3 below.

Table 3.3 – The effect of applying circular shift to the designed bit-stream pattern on the amplitude and phase of the output waveform			
Original Example Bit-stream Pattern (m = 4): 0000 0001 0001 0011 (repeated…)			
Number of Circular Shifts Applied to the Original Pattern	**Resulting Pattern**	**Effect on Phase**	**Effect on Amplitude**
1	1000 0000 1000 1001	π/2	Nil
2	1100 0000 0100 0100	π	Nil
3	0110 0000 0010 0010	3π/2	Nil
4	0011 0000 0001 0001	2π (or zero)	Nil

At first glance, it appears as if there should be an effect on the amplitude as well by applying the circular shift as shown in the table above. At this point, two things must be remembered in order to understand why that is not the case. First is that the designed bit-stream pattern is not applied only once. Rather it is being repeated continuously for a certain duration of time for which we need a particular amplitude and phase match between the desired and predicted waveform. This means that the original bit-stream from the above example will be applied like 0000 0001 0001 0011, 0000 0001 0001 0011, and so on… And after one circular shift, it will appear like 1000 0000 1000 1001, 1000 0000 1000 1001⋯ Now second thing to remember, and this is really important, is that the algorithm first accumulates all the consecutive zeros (or ones) in a given pattern, and then runs the amplifier model for those zeros (or ones) without updating the initial conditions between consecutive zeros (or ones). In other words, the initial conditions are updated only during the transition from zero to one or vice versa. Understanding these two facts makes it clear that applying a circular shift to the entire waveform doesn't cause any effect on the amplitude.

On the other hand, shifting the bits positions in one particular cycle of the entire designed bit-stream pattern (when $m > 1$) will have more complicated effects. This will not only affect the phase of the output waveform but also its amplitude. Consider again for example the bit-stream pattern 0000 0001 0001 0011 that we used earlier. Now, let's only change the

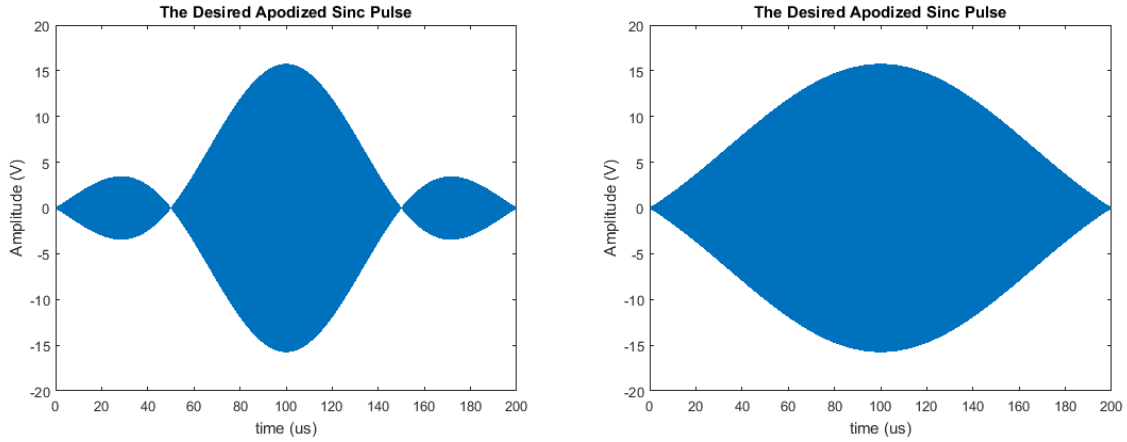
positions of bits in the third cycle such that the modified bit-stream pattern becomes 0000 0001 0010 0011. It can be observed in the modified bit-stream pattern that the 1 in third cycle is occurring after two consecutive zeros whereas it was occurring after three consecutive zeros in the original bit-stream pattern. This means that the amplifier is switching on earlier now in the third cycle than it was in the original bit-stream pattern. Hence such shifting of the bits will cause not only the phase shift in the output waveform but also the amplitude change. This fact is not disadvantageous at all. We can in fact leverage it to our benefit and can design the bit-stream more accurately, achieving better amplitude and phase modulation of the output waveform.

3.2.5. Meaning of 0101 and when it should be used…

We are currently operating at a frequency of 64 MHz, where each cycle (time period) is divided into four bits. Applying a bit-stream pattern of 0011 0011 0011⋯ means that the amplifier is operating at 64 MHz with a 50% duty cycle. But the bit-stream pattern 0101 0101 0101⋯ means that the amplifier is switching on and off twice as fast as in the case of 0011 0011 0011⋯ In other words, the amplifier is now operating at a frequency of not 64 MHz, but 128 MHz! This should normally be avoided as the amplifier's loading network is tuned to 64 MHz and not 128 MHz. Now, the designer might not be using the bit-stream pattern 0101 on purpose but if, for example, while adjusting the phase, the patterns 0001 and 0100 are used together, that essentially means that we are having a bit-stream pattern 0001 0100 0001 0100⋯ Having a closer look, it is evident that there is a 0101 sequence hiding in there, which will increase the harmonic content of 128 MHz and will affect the amplifier's performance. The pattern 0101 should be used only when the designer purposefully wants to degrade the amplitude of the output waveform.

3.3. The Desired Amplitude and Frequency Modulated Waveform

Now that we have learnt to manipulate the carrier bit-stream to achieve both the amplitude and frequency modulation of the output waveform, it is time to generate a desired sinc pulse waveform in MATAB that we can use as standard while designing the bit-stream. For initial simulations, to keep the initial application of the algorithm easier and faster, the simulation time was set to 200 μs. In the start, two different versions of the sinc pulse were considered – one consisting of a main lobe and two side lobes, while the other consisting of only one main lobe (Fig. 3.4). Later, the sinc pulse with only one main lobe was set as standard.



(a) (b)

Fig. 3.4 – The desired sinc waveforms each of duration 200 μs. a) The desired sinc waveform with one main lobe and two side lobes. b) The desired sinc waveform with one main lobe.

Now that we have developed some knowledge about the gate modulation algorithm and created the desired output waveforms, let's dive into the methods used to implement the algorithm in software to design the carrier bit-stream patterns that could predict the desired output waveforms with least possible errors. Methods used to test the resulting bit-streams on hardware (both bench-top and MR) and tackle the associated challenges would also be explained.

3.4. Algorithm Implementation in Software

In this section we are going to discuss the methods used to design the carrier bit-streams to obtain the desired output waveforms. The method is divided into four steps as follows:

Step 1: The desired sinc pulse waveform is divided into multiple subsections.

Step 2: Based on the points explained in Section 3.2, bit-stream patterns are designed and repeated for each subsection and the amplifier model is run for that subsection. As we already know, the goal is to achieve both the amplitude and phase match of the predicted output waveform with the desired output waveform. In order to facilitate the process, the predicted output waveform is plotted on top of the desired output waveform and the effect of designing and altering the bit-stream pattern on the predicted waveform is observed.

Step 3: An error function is defined and plotted simultaneously while designing the bit-stream pattern for each subsection. This error function is defined as the root mean square error (RMSE) per cycle between the predicted and the desired output waveforms for each subsection. The error plots are used as an aid in the process of designing the carrier bit-stream patterns such that the amplitude and phase differences between the desired and the predicted output waveforms are minimized. The normalized root mean square error (NRMSE) for the entire waveform is also calculated using the formula as mentioned below:

$$NRMSE = \frac{\sqrt{mean(desired - predicted)^2}}{\sqrt{mean(desired)^2}} \tag{3.1}$$

NRMSE for different subsections of the entire waveform are also calculated in order to have an additional insight into the accuracy of the algorithm.

Step 4: The FFT (Fast Fourier Transform) of the predicted output waveform, for each subsection as well as the entire waveform, is plotted and observed simultaneously. This is done in order to keep a continuous check on the harmonic content of the predicted output waveform while designing the bit-stream patterns for each subsection.

3.4.1. The MATLAB GUI (Graphic User Interface)

In an attempt to speed up the design process, a MATLAB GUI was developed that incorporated and facilitated the application of all four steps described above. Users could enter the start and end timings of the subsection to be designed in the interface. They could then design and simulate the bit-stream pattern for that specific subsection while observing 1) the overlap of both the desired and predicted output waveforms for that subsection, 2) the error profile for that subsection, and 3) the FFT results for that subsection. Once the users had finished designing the bit-stream pattern for a particular subsection, they could then hit the save button and the bit-stream pattern for that subsection along with the start and end timings was saved in a separate text file. The GUI also provided an option to call the MATLAB function in which a previously designed bit-stream for the entire waveform was saved. Users could then observe the entire designed waveform (plotted over the desired waveform), as well as its error profile and the FFT response.

Equipped with the method described till now, the following subsections would explain the approach taken to design the earlier 200 μs duration pulses and how later the approach was generalized to design the 2 ms duration pulse.

3.4.2. Designing a Sinc Pulse of Duration 200 μs with a Subsection Duration of 6.25 us

At f = 64 MHz (T = 15.625 ns), a total time duration of 200 μs equals 12800 total cycles (time periods), and 51200 bits (k = 4). Dividing this time duration into multiple subsections each of duration 6.25 μs results in a total of 32 subsections, including 400 cycles and 1600 bits per each subsection. The bit-stream pattern (m = 1 to 16 cycles) is designed for each subsection based on the already explained methods, and the resulting bit-stream pattern (consisting of 4 to 64 bits) is then repeated for the entire subsection.

At this point, it is important to note that in case of symmetric pulse shape, we only need to design the first half of the pulse duration, i.e., we need to design only the first 16 subsections (100 μs duration). For the other 16 subsections, the same patterns need to be repeated but

in descending order. For example, the bit-stream pattern for the 17th subsection would be the same as that for 16th subsection, and the bit-stream pattern for 20th subsection would be the same as that for the 13th subsection, and so on. It must also be kept in mind that the bitstream patterns for the second half of the pulse duration should not be complemented, as complementing (applying binary NOT) to the bit-stream patterns would cause a $180°$ phase shift in the second half of the pulse which is not desired unless otherwise asked.

The sinc pulse shown in Fig. 3.4 (a) was used as reference for this design. Designing 16 subsections on either side of the pulse meant that there were a total of 32 quantization levels in the designed output waveform in this case.

3.4.3. Designing a Sinc Pulse of Duration 200 µs with a Subsection Duration of 3.125 us

The 200 µs pulse duration in this case is subdivided to 64 subsections, each of duration 3.125 µs and consisting of 200 cycles and consequently 800 bits per each subsection. This means that the output waveform will now have twice the number of quantization levels compared to the previous design (64 quantization levels). The bit-stream patterns are now designed and repeated for each subsection similar to the previous case. Again, considering the waveform as symmetric, we only need to design the first 32 subsections of the waveform while the same bit-stream patterns will be repeated for the other 32 subsections but in descending order as explained in the previous subsection. Note that in this design, the sinc pulse shown in Fig. 3.4 (b) was used as reference.

3.4.4. Quantization Levels vs. Subsections – Generalizing the Approach and Designing a Sinc Pulse of Duration 2 ms

By this point, the number of quantization levels to be achieved appear to be dependent on the number of subsections to which the pulse duration is divided. There can be an alternative, more generalized approach to targeting the problem. Instead of dividing the waveform duration to a specific number of subsections, the emphasis should be put to designing and

running a bit-stream pattern for as long as it provides an accurate amplitude and phase match of the output waveform with the desired waveform. The next bit-stream pattern should be designed and applied as soon as the error profile grows above tolerable limit. This way, there is no constraint put on the number of quantization levels that could be designed, or on the duration of a subsection for which a specific bit-stream pattern needs to be run. With this approach in mind, the designed bit-stream for the previous case (sinc pulse of duration 200 μs with a subsection duration of 3.125 us) was updated and the total simulation time was increased to 2 ms in order to obtain a sinc pulse of duration 2 ms at the output.

3.5. Hardware Implementation

Fig. 3.5 shows the block diagram of the hardware implemented to test the designed carrier bit-streams on class-E amplifier.

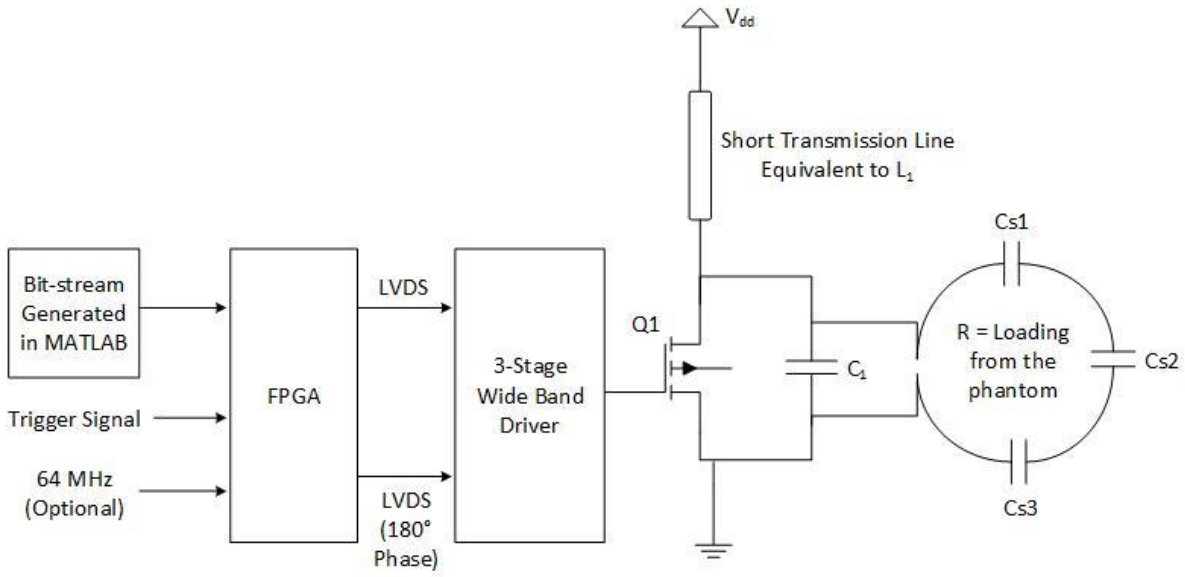


Fig. 3.5 – Block diagram of the hardware implemented to test the designed bit-streams

The designed bit-stream in MATLAB is first saved in the FPGA (XILINX Inc., KCU105, California, USA) ROM, later to be transmitted to the driver of the amplifier through Low-Voltage Differential Signaling (LVDS). The FPGA takes an external trigger signal from the signal generator which can be set to either active-low or active-high, and is required to continuously transmit the bit-stream from the FPGA to the driver at regular intervals (repetition times).

The frequency of operation is f = 64 MHz, but since the number of bits per each cycle (time period) is set to k (k = 4 in our case), the FPGA needs to transmit the bit-stream at a rate k times higher than the operating frequency, i.e., in our case, at 256 MHz. This frequency can either be generated inside the FPGA using the FPGA's internal oscillator, or the FPGA can take an external 64 MHz signal from the signal generator as reference to generate this frequency.

3.5.1. Driver Implementation

The FPGA transmits the saved bit-stream to the amplifier PCB (consisting of both the amplifier and its driver) via a CAT-7 Ethernet cable. As mentioned earlier, this transmission is done in the form of Low-Voltage Differential Signaling (LVDS). The driver of the amplifier is a three-stage wideband driver. At first stage, the LVDS signals are converted to single-ended signals using the IC DS90LT012A. At second stage, these single-ended signals are amplified by a current feedback amplifier configuration using the IC THS3202. The gain of these amplifiers is set uniquely as is explained in [3]. At third stage, the ICs MRF1513 MOSFETS are used to provide the adequate current to charge and discharge the gate capacitance of main MOSFET which is a 300 W LDMOS RF power transistor (Ampleon, BLF573, Nijmegen, The Netherlands). The reason for using this transistor model as the main switch of the amplifier has already been explained in Subsections 2.1.1 and 3.1.2. The driver part of the PCB is provided with an 8-9 V DC voltage via a power supply, which is then converted to 3.3 V and -3.3 V by LF33ABDT and MAX1861 to provide the input voltage to different ICs on the board. The block diagram displaying all the components of the driver circuit is shown in Fig. 3.6 below.

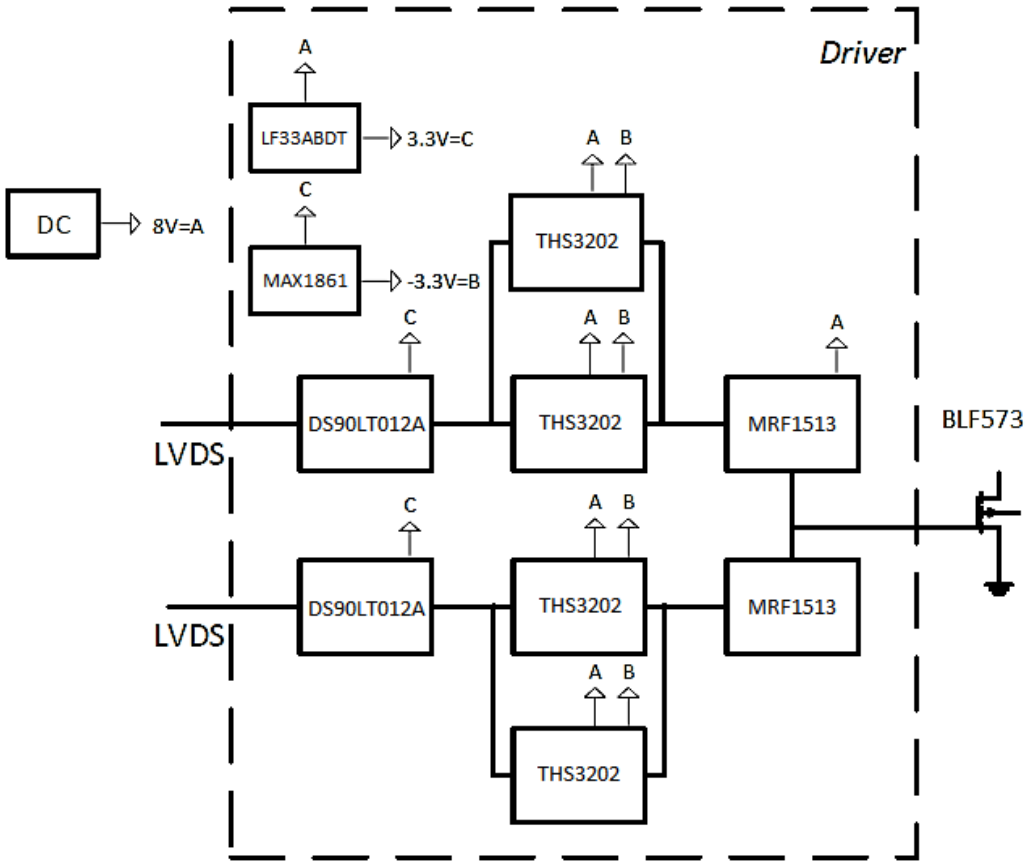


Fig. 3.6 – The block diagram showing different components of the 3-stage driver circuit [2, 3]

3.5.2. Class-E Amplifier Implementation

Through the driver circuitry, the carrier bit-stream is fed to the gate of the transistor which is the main switch of the class-E amplifier. In the implementation of the amplifier, the RF choke inductance L_1 has been replaced with an equivalent transmission line for MR compatibility. The detailed analysis on designing this equivalent transmission line can be found in [2, 3]. The amplifier's load network needs to be designed such that it matches with the optimum output load impedance of the amplifier, required to achieve maximum power with highest possible efficiency [3]. In order to find this optimum load impedance and tuning point of the amplifier, load-pull analysis was performed in ADS2016 (Keysight, Santa Rosa, CA) as detailed in [3]. The optimum load impedance value was found to be approximately $1.2 - j0.9$ ohm at which the amplifier could deliver maximum power (300 W) with highest efficiency.

In hardware, the load network consists of the transmission coil and phantom. The transmission coil acts as the necessary series resonance circuit of the class-E amplifier as well as, combined with the phantom, provides the optimum load impedance required for the efficient operation of the amplifier. The transmission coil thus acts as both the tuning and matching element of the amplifier, eliminating the need for an additional matching network. Our transmission coil has a series inductance value of $\sim 256\ \mathrm{nH}$ (L_2) with a quality factor of ~60, and the coil is tuned to 64 MHz using three distributed tuning capacitors each of value $\sim 70\ \mathrm{pF} \pm 1\ \mathrm{pF}$. The series inductance of the coil (L_2) combined with the equivalent value of tuning capacitors (C_2) constitute the series resonance circuit of the amplifier. The load is then added and the coil is retuned to achieve the desired load impedance value. The achieved load impedance value in hardware was approximately $1.25 - \mathrm{j}1$ ohm. The value of shunt capacitance C_1 is also tuned in order to achieve the ZVS and ZVDS conditions and is set to $60\ \mathrm{pF}$ (it should be kept in mind that the MOSFET BLF573 has its own output capacitance of 103 pF as well, as shown in Table 3.1).

3.5.3. Amplifier PCBs Used for the Experiments

Two already fabricated amplifier PCBs were used for the experiments. The first PCB (dimensions 65 mm by 50 mm) did not have an integrated transmission line on board so an external custom-made transmission line needed to be connected as shown in Fig. 3.10.

The design layout for this PCB was modified to include an integrated micro-strip transmission line on board. The new design layout is shown in Fig. 3.7, having the same physical dimensions as the PCB shown in Fig. 3.10.

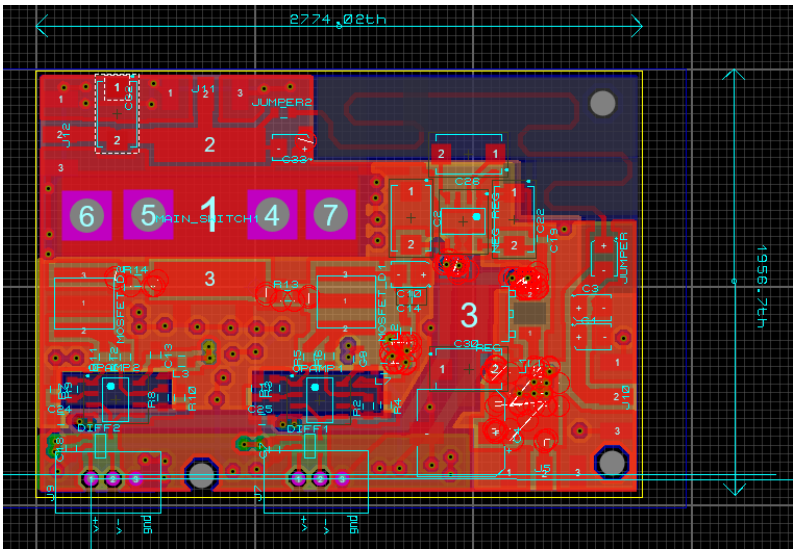


Fig. 3.7 – Modified design layout of the amplifier PCB to include the equivalent micro-strip transmission line integrated on board (dimensions: 65 mm by 50 mm)

This new design was not fabricated for the reason that there was yet another fabricated PCB (presented in [2, 3], dimensions: 100 mm by 50 mm) being used by other research members of the group which included an integrated micro-strip transmission line as well as a supply modulation block. By disconnecting the jumper that provided power to the supply modulation block, this PCB could be used for our purposes as well, and that's what was done. The design layout for this second PCB is shown in Fig. 3.8 below [2].

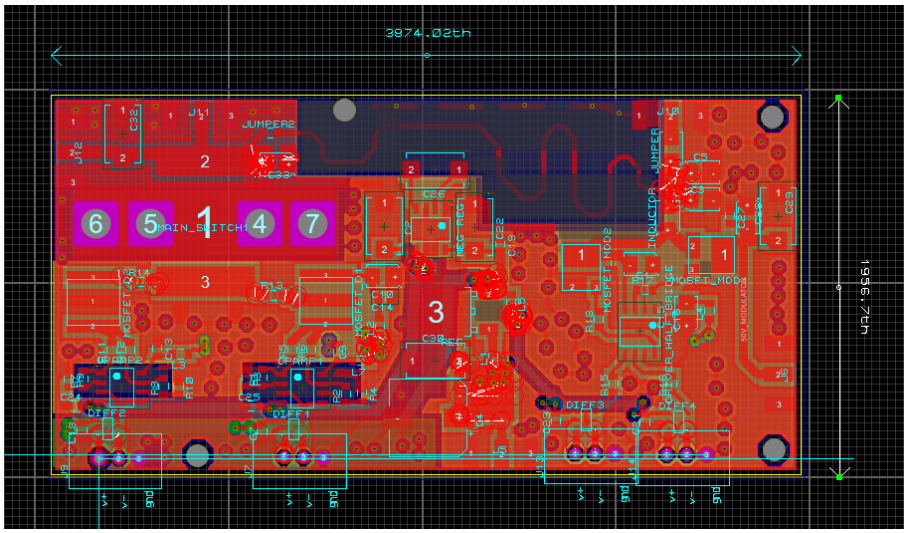


Fig. 3.8 – The design layout of the amplifier PCB including the supply modulation block as well as the integrated micro-strip transmission line (dimensions: 100 mm by 50 mm) [2]

3.6. Experimental Setup for Bench-top Experiments

The block diagram of the experimental setup used for bench-top experiments, including the output waveform measurement experiments, power and efficiency measurement experiments, and the re-optimization of the carrier bit-stream on hardware, is shown in Fig. 3.9 below.

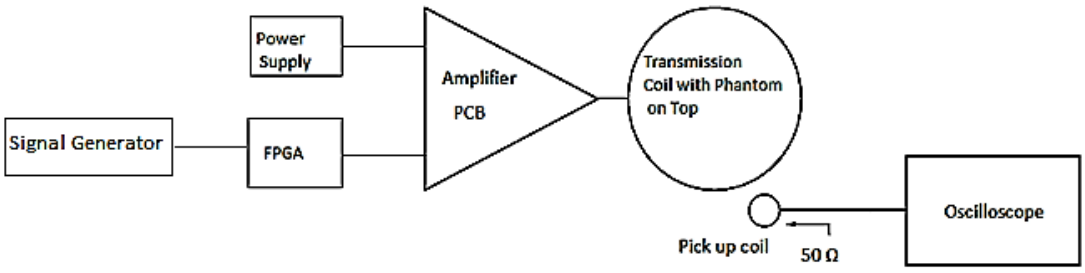


Fig. 3.9 – The block diagram of the experimental setup for bench-top experiments [3].

The amplifier PCB connected at drain end to both the external transmission line and to the transmit coil of diameter 12 cm with three distributed capacitors is shown in Fig. 3.10. A small pick-up coil tuned and matched to 64 MHz and 50 ohm respectively, placed near the transmit coil, is also shown.

The experiments were performed at power levels of up to 80 W. The resulting output waveform was observed on the oscilloscope while the drain current profile was monitored using the active current probe. The power and efficiency measurements were made using the method as detailed in [3].

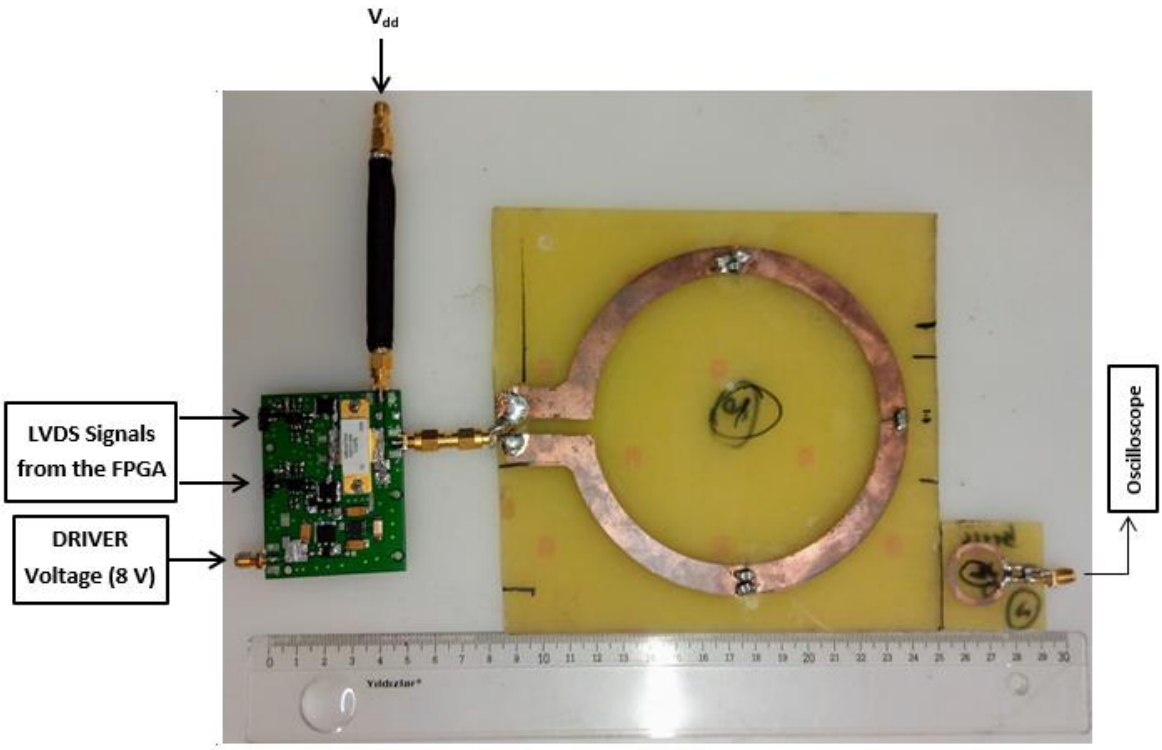


Fig. 3.10 – The hardware setup for bench-top experiments. The FPGA sends the LVDS signals to the amplifier PCB (consisting of the driver and amplifier circuitry). An external transmission line equivalent to RF choke inductor is shown connected at the drain of the amplifier. The output waveform is monitored on the oscilloscope via a 2 cm diameter receiver coil placed near the transmit coil loaded with phantom.

3.6.1. Carrier Bitstream Re-optimization on Hardware

Since the analytical model assumed an ideal switch, a few of the quantization levels in the output waveform obtained in hardware did not match precisely with their software counterparts when software-optimized carrier bit-stream was first implemented on hardware. Hence additional adjustments for some subsections of the bit-stream were required which were performed as explained below.

The observed output waveform on the oscilloscope was recorded and the associated data points were stored in .csv format. The .csv file was then imported in MATLAB where the waveform was plotted again, over the desired and previously designed waveforms. All three waveforms were carefully analyzed and the bit-stream patterns for the subsections of the hardware waveform which showed significant differences from the previously designed

waveform were redesigned. The newly designed carrier bit-stream was then tested again on hardware. If required, the process of re-optimization of the carrier bit-stream was repeated until the desired output waveform was obtained on hardware as well.

3.7. Experimental Setup for MRI Experiments

After the carrier bit-stream re-optimization on hardware, an MRI experiment was conducted in 1.5 T (Scimedix Inc., Incheon, South Korea) Scanner to test the slice selective capability of the generated radiofrequency pulse. Fig. 3.11 shows the block diagram of the experimental setup.

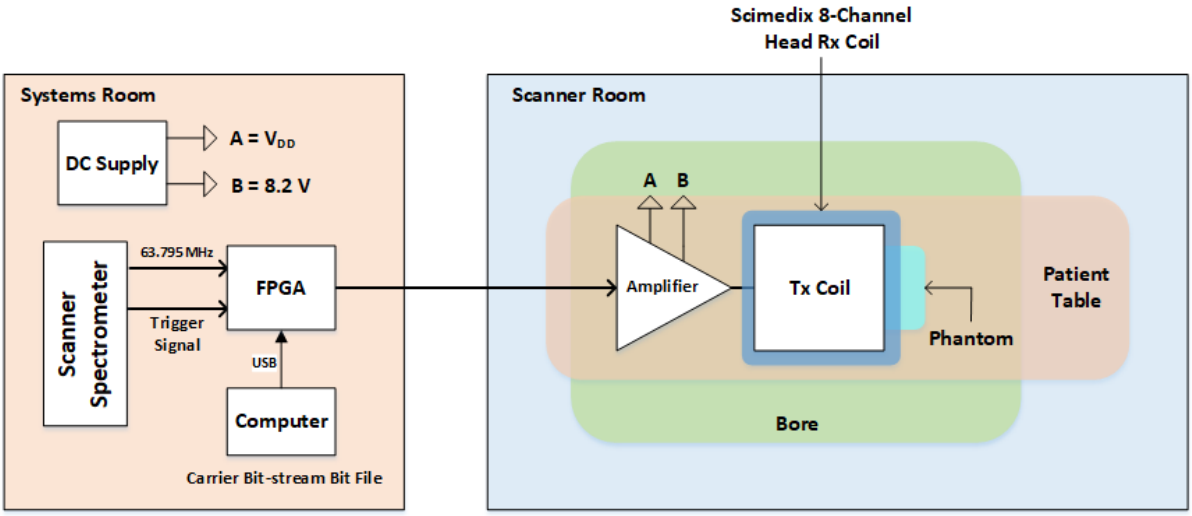


Fig. 3.11 – The block diagram of the experimental setup for MRI experiments

Before explaining the setup, it should be noted here that the operating frequency of our scanner is about two hundred kilohertz below 64 MHz. The precise value, accurate to three decimal places, is reported to be 63.795 MHz. The MATLAB and the FPGA codes were therefore updated accordingly.

As shown in Fig. 3.11, the FPGA, the programming PC and the DC power supplies were placed in the systems room situated on the back side of the scanner room. The FPGA was programmed using the USB cable connected to the PC on which the designed carrier bit-stream was saved. In the initial experiments, the FPGA was provided with the trigger signal and the frequency signal (63.795 MHz) via the spectrometer module of the scanner. The FPGA

then performed the multiplication operation and produced a frequency four times higher than the operating frequency ($4 \times 63.795\ \mathrm{MHz} = 255.18\ \mathrm{MHz}$) to transmit the carrier bitstream to the PCB. The carrier bit-stream was then transmitted from the FPGA to the amplifier PCB via a CAT-7 Ethernet cable. The necessary DC signals were provided to the amplifier PCB via DC filters in order to reduce the noise flow inside the scanner.

Inside the scanner room, under the bore, the amplifier PCB was connected to a custom designed square-loop transmit coil (built in-house) placed on top of the 8-channel receiver head coil. A cylindrical standard Siemens plastic phantom was used as load and was placed under the head coil (Fig. 3.11, Fig 3.12). Gradient echo sequence was used for imaging with 250 mm FOV (field of view), 5 mm slice thickness, and TE/TR = 15/200 ms (TE = Echo Time, TR = Repetition Time). The phantom was excited with our custom designed 2 ms sinc pulse while the scanner's main transmit system was off.

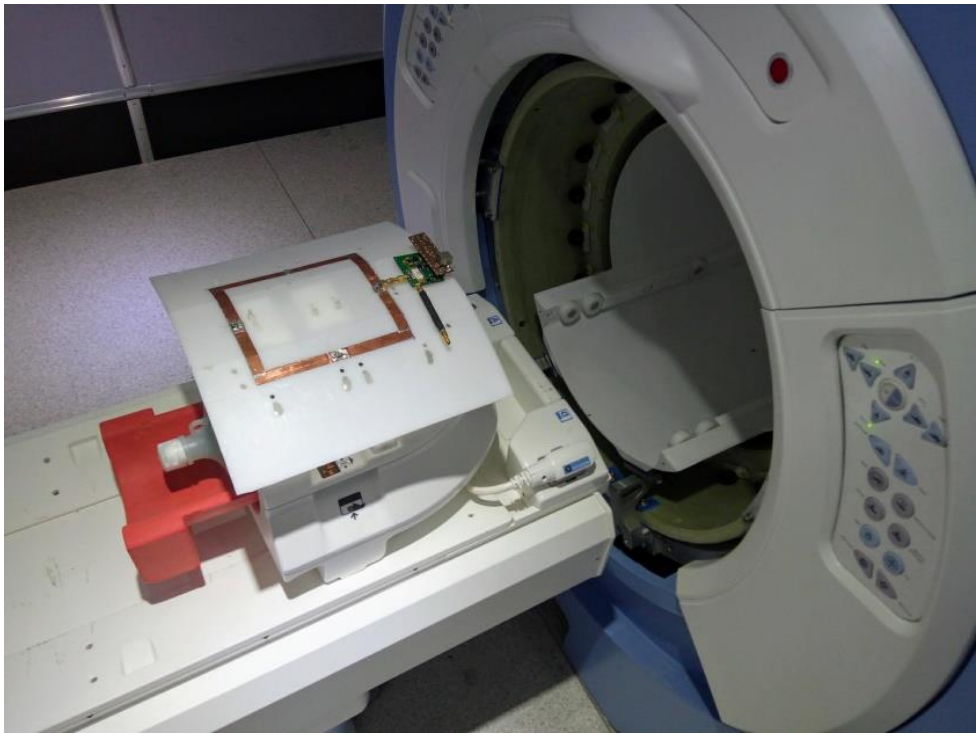


Fig 3.12 – MRI experiment setup: Inside the scanner room – The amplifier PCB was connected to the custom made square-loop transmit coil placed on top of the 8-channel receiver head coil, and the cylindrical phantom placed under the head coil was excited with the custom generated 2 ms sinc pulse while the scanner's transmit system was off.

3.7.1. FPGA Implementation Errors and Synchronization Issues – Identifying the potential problems and methods used to resolve them

The resulting MR image from the initial experiment, as will be revealed in the next chapter, showed ghosting artifacts in the phase-encoding direction. In an attempt to locate the source of the problem, an MR scan was performed with phase encoding turned off while other parameters were kept the same, and the k-space data for the entire scan (256 repetitions) was obtained and analyzed. Magnitude and phase of the k-space data were plotted and it was inferred from the magnitude plot (shown in Fig 3.13) that there was a repeated discontinuity in the transmission of the RF pulse to the phantom in a few of the 256 repetitions. The discontinuity occurred randomly and approximately seven to eight times on average per the entire scan, represented by an absence of the expected bright line in the magnitude plot.

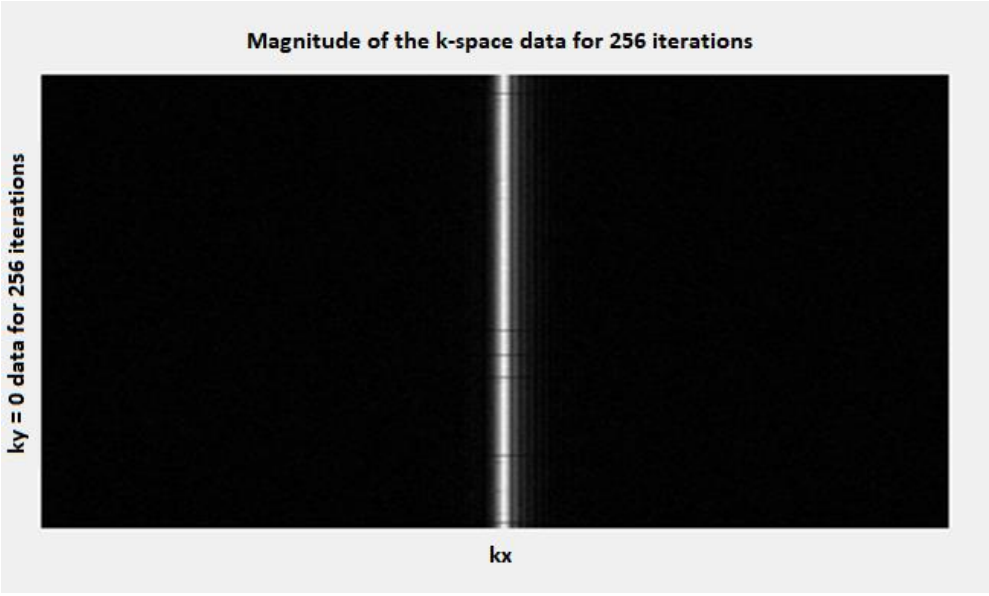


Fig 3.13 – The k-space magnitude of the data from a single receive channel obtained from the MRI experiment conducted with phase encoding turned off. It can be observed from the diagram that the discontinuity occurs in the transmission of the RF pulse a total of six times in this specific case.

In an attempt to resolve this problem, the bench-top experiments were conducted again using the method explained in Section 3.6. This time, the LVDS signals transmitted from the FPGA, the carrier bit-stream waveform at the gate of the amplifier, and the output waveform of the amplifier were observed carefully on the oscilloscope using its 'Segmented Sampling

Mode'. The sampling mode settings can be found in the 'Acquisition Setup' tab of the oscilloscope, and a screenshot of these settings is shown in Fig 3.14. The number of segments was set to 128, sampling rate was set to 1.25 GSa/s, and the number of samples per segment was set to maximum possible value. The goal of this approach was essentially to record the 128 consecutive instances of the LVDS signals, the gate input waveform, and the output waveform of the amplifier.

Fig 3.14 – The 'Acquisition Setup' settings implemented for the 'Segmented Sampling Mode' of the oscilloscope, used to record the consecutive gate and output waveforms of the amplifier

Two kinds of phase inconsistencies were observed in the LVDS signals transmitted from the FPGA. One of these phase inconsistencies caused the MOSFETs in the third stage of the driver to switch-on simultaneously. This caused the output waveform of the third stage of the driver (which is the same as the waveform at the input of the amplifier's gate) to degrade. This in turn resulted in an erroneous waveform at the output of the amplifier (this problem occurred three to four times on average in 128 instances, confirming in a way the seven to eight times occurrence of the inconsistency observed in 256 repetitions of the MR scan). The other phase inconsistency caused a certain phase shift in the LVDS signals which contributed to an

equivalent phase shift to the other successive signals as well. In an attempt to solve the problem, the FPGA code implementation method was repeatedly updated and the resulting bitstream files were constantly tested on hardware, until eventually both kinds of phase inconsistencies in the LVDS signals were resolved. The phase inconsistency that caused a constant phase shift in all signals was entirely resolved, while the phase inconsistency that caused the output waveform to become erroneous either did not occur at all or occurred only once in 128 instances.

Another MR experiment was then performed using the same method and parameters as explained earlier (GRE sequence, 250 mm FOV, 5 mm slice thickness, TE/TR = 15/200 ms). The MR image now contained an even more pronounced ghosting artifact in the phase encoding direction. The MR experiment was repeated with phase encoding turned off and the k-space data was obtained. As shown in Fig. 3.15, there were now one, two, or no discontinuities at all observed in the magnitude plot of the k-space data (the shown figure has zero discontinuities), hence confirming the solution to the FPGA's implementation errors that was achieved in bench-top experiments.

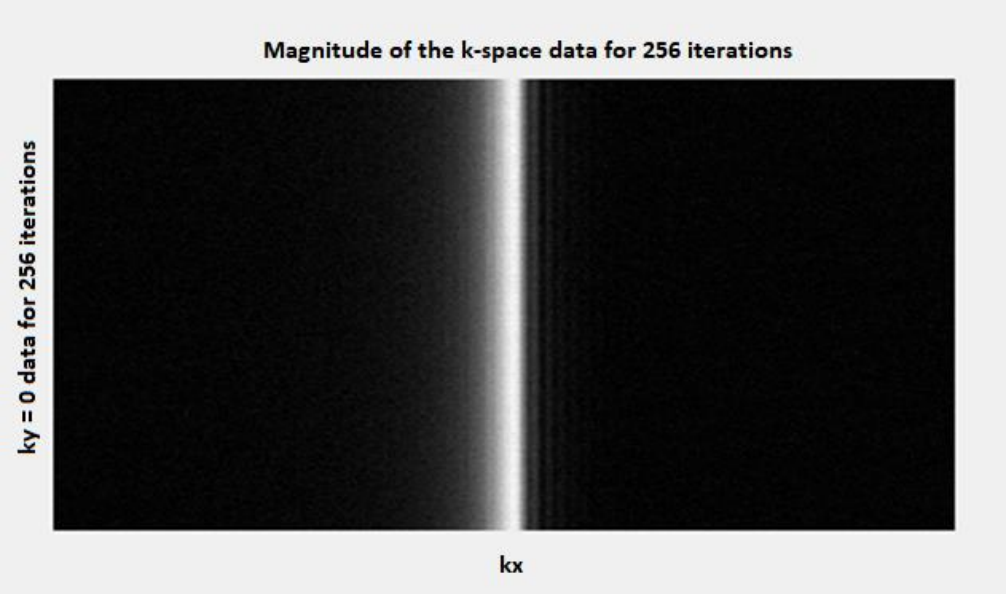


Fig. 3.15 - The k-space magnitude of the data from a single receive channel obtained from the MRI experiment conducted with phase encoding turned off after the implementation errors in the FPGA code were resolved. It can be observed from the diagram that no discontinuities occur in the transmission of the RF pulse.

The phase plot of the k-space data was also analyzed from which it was inferred that the scanner and the FPGA were not working in synchronization with each other. The implementation of the FPGA code was further updated with two significant changes. First, the frequency signal that the FPGA got now from the signal generator was a 255.18 MHz signal instead of 63.795 MHz signal. The FPGA sampled and utilized this frequency signal to transmit the carrier bit-stream to the PCB at the same rate without needing to perform any additional multiplication operations inside. Second, and this was the most significant step in synchronizing the scanner with the FPGA, a 10 MHz signal was generated from the FPGA and was provided to the scanner and also to the signal generator for reference purposes. As the MRI experiment was repeated (GRE sequence, 5 mm slice thickness, TE/TR = 15/200 ms), ghost-free MR images were finally obtained. The images were obtained at up to 50 W input power. The updated setup in the systems room is shown in Fig. 3.16.

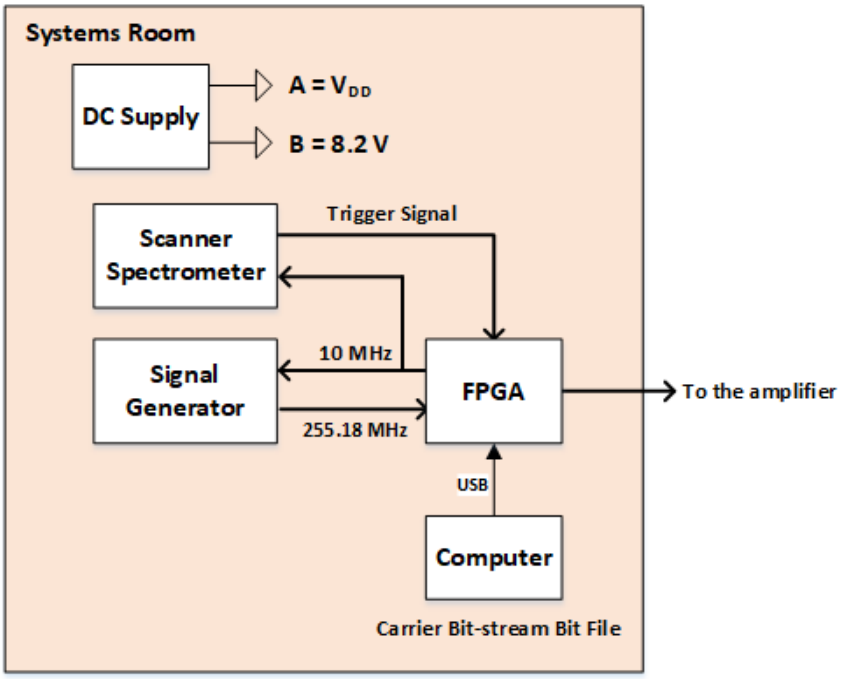


Fig. 3.16 – The updated setup in the systems room. A 10 MHz signal is generated by the FPGA and is fed to the signal generator and the scanner spectrometer for synchronization

CHAPTER 4

RESULTS

4.1. Amplifier Models' Implementation – Simulation Results

In this section, the simulation results for amplifier's analytical models implemented in MATLAB and of simulations run in circuit simulator are presented. We start with the results for model 1 which assumed a constant-current source at the drain end of the amplifier.

4.1.1. Model 1 – Constant-Current Source Assumption at Drain

The switch voltage $v_{C1}(t)$, the switch current, the output current $i_{L2}(t)$ and the output voltage ($i_{L2}(t) \times R$) waveforms (versus time) are all shown in Fig. 4.1. It must be recalled that at this stage, the amplifier model is run at 50% duty cycle. It can be observed from the switch voltage waveform in Fig. 4.1 (a) that both the ZVS and ZVDS conditions are satisfied. Also, since the switch is considered ideal, there is no recorded loss in the system and hence the model shows an ideal-case efficiency of 100%.

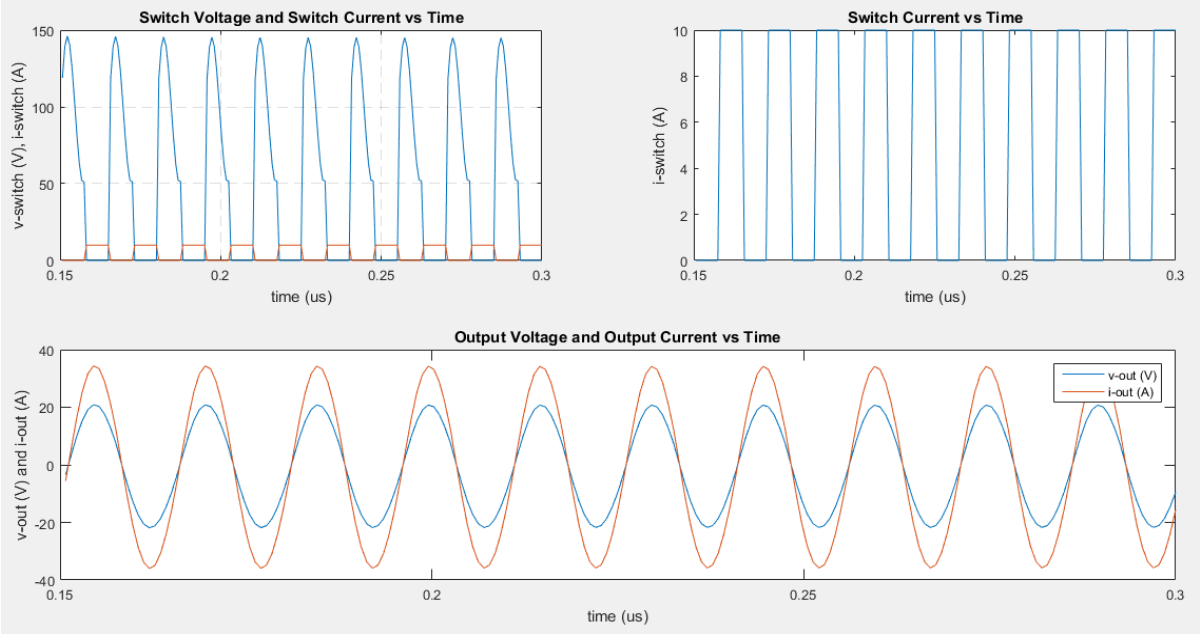


Fig. 4.1 – The amplifier model 1 implementation results. a) Switch voltage and switch current vs. time. b) Switch current vs. time. c) Output voltage and output current vs. time.

4.1.2. Model 2 – Inductor Assumption at Drain

Fig. 4.2 shows the steady-state results for the implementation of model 2 of the amplifier at 50% duty cycle operation. Fig. 4.2 (a) shows the switch voltage $v_{C1}(t)$ versus time. Fig. 4.2 (b) shows the output voltage and output current versus time. Fig. 4.2 (c) shows the drain current $i_{L1}(t)$ versus time, while Fig. 4.2 (d) shows a zoomed-in version of the drain current $i_{L1}(t)$ versus time.

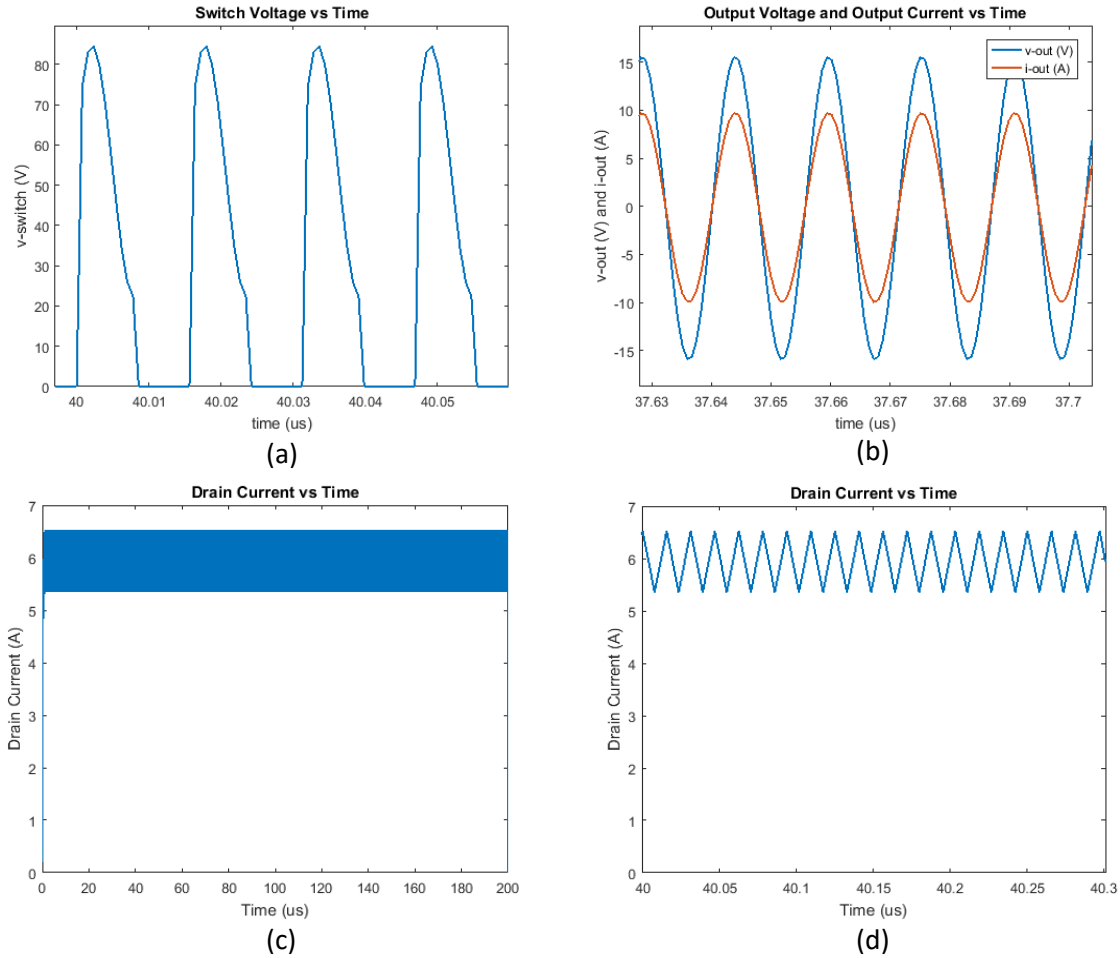


Fig. 4.2 – The amplifier model 2 implementation results. a) Switch voltage vs. time. b) Output voltage and output current vs. time. c) Drain current vs. time (Zoomed-out). d) Zoomed-in version of the drain current vs. time at steady-state.

It must be noted that the peak-to-peak magnitude of the ramp in $i_{L1}(t)$ waveform is dependent on the value of the inductor L_1. A higher inductor L_1 value will result in a lower peak-to-peak magnitude of the ramp. However, the characteristic impedance and the length of the equivalent transmission line to be used in hardware are directly proportional to the value of this inductor ($L_1 = Z_o l/v$, where Z_o and l are respectively the characteristic impedance and length of the transmission line, while v is the speed of propagation of the wave inside the transmission line). Therefore, the value of the inductor L_1 was set accordingly in simulations, keeping in mind the hardware limitations. Another point to be noted is that the magnitude of the drain current that the amplifier pulls from the voltage supply also depends on the tuning circuit (comprising of C_2 and L_2) of the amplifier.

The values of C_2 and L_2 can be tuned in order to achieve a higher magnitude of the drain current $i_{L1}(t)$ but it should be noted that the switch voltage waveform is also dependent on the values of C_2 and L_2 as shown earlier in Fig. 3.1. Hence a balance must be struck while tuning this analytical model in order to achieve the desired waveforms conditions.

Finally, as will be demonstrated in the following subsection, the drain current profile in MATLAB simulations is in fair agreement with its counterpart in circuit simulator simulations.

4.1.3. Circuit Simulator Model Results – Comparison and Verification of the Implementation of Analytical Models

The circuit simulator results at steady-state are shown in Fig. 4.3. The gate voltage is shown in Fig. 4.3 (a). The zoomed-in version of the drain current profile is shown in Fig. 4.3 (b) which verifies the drain current profile obtained for analytical model 2 of the amplifier. The switch voltage waveform is shown in Fig. 4.3 (c) and it can be seen that the ZVS and ZVDS conditions are satisfied. The output voltage and current versus time are shown in Fig. 4.3 (d).

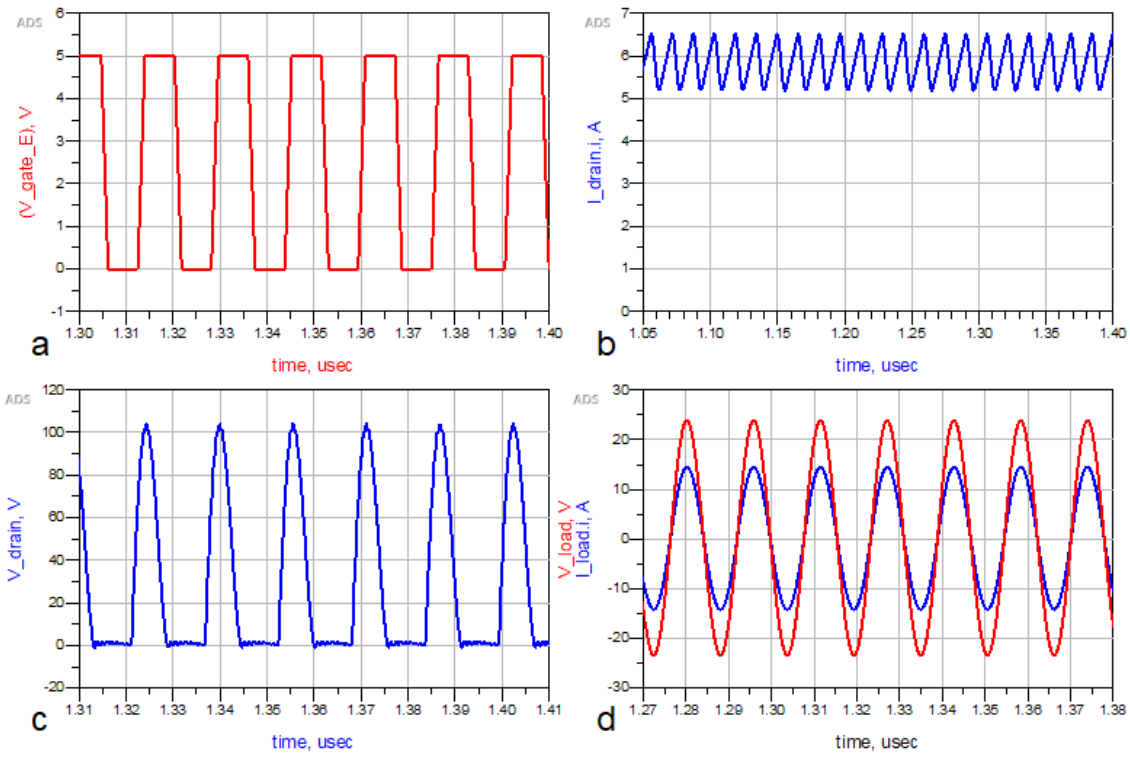


Fig. 4.3 – The circuit simulator implementation results. a) Gate voltage vs. time. b) The drain current vs. time. c) The switch-voltage vs. time. d) The output voltage and output current vs. time.

4.2. Circuit Simulator Results at Multiple Duty Cycles

Fig 4.4 shows the peak amplitude of the output voltage plotted against the duty cycle of operation for the circuit simulator model of the amplifier. Though not a linear function, it can be observed that the amplitude of the output waveform can be modulated by varying the duty cycle of the gate signal of the amplifier. It can be observed that the amplitude of the output waveform increases from about 6 V to about 32 V as the duty cycle increases from 6.25% to 50%, but doesn't change much as the duty cycle increases beyond 50%. This means that there is a possibility of achieving a lot of amplitude levels by varying the duty cycle (especially in the first half, i.e., from 0% to 50%). This idea served as the basis for developing the gate modulation algorithm: by controlling the digital carrier bit-stream input to the gate of the amplifier, it was possible to achieve multiple amplitude levels of the output waveform without the need to deploy a separate supply modulation block.

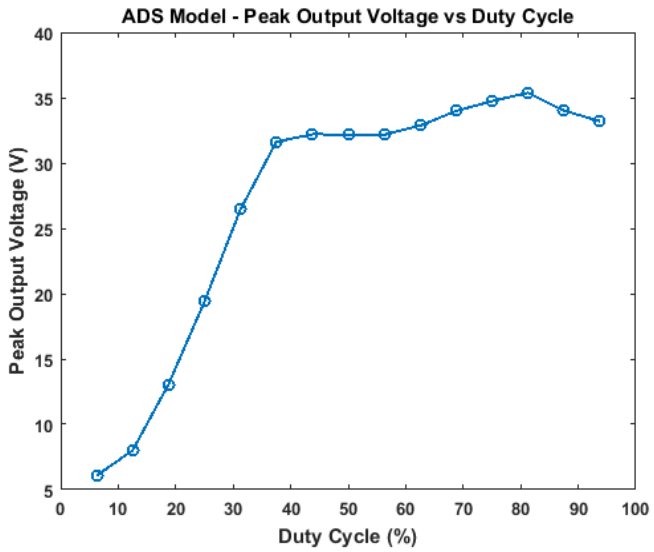
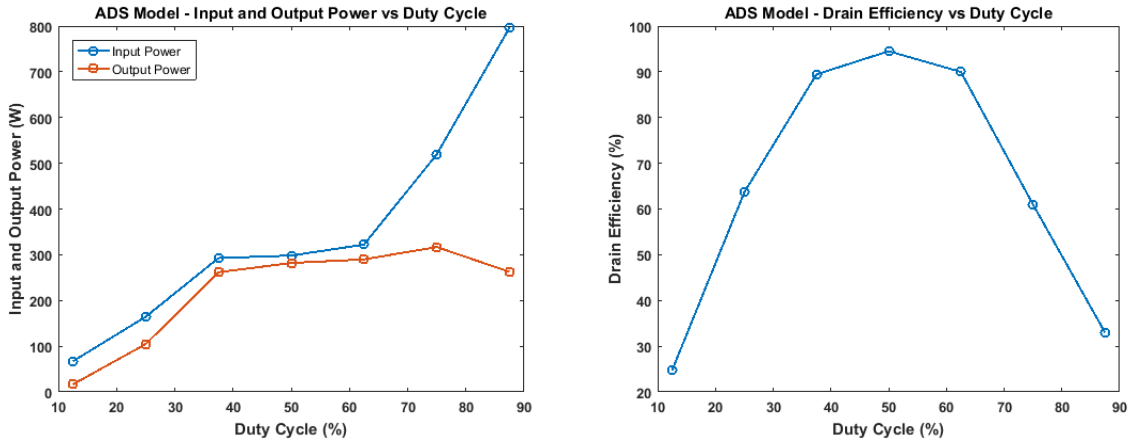


Fig 4.4 – Peak output voltage vs. the duty cycle of the gate input signal for the ADS model of the class-E amplifier

One concern however in approaching the problem this way is the question of efficiency. Fig. 4.5 (a) shows the input and output power contours plotted against the duty cycle (step-size: 12.5%) for the ADS model of the class-E amplifier while the associated drain efficiency versus duty cycle plot is shown in Fig. 4.5 (b). It can be observed that the difference between the input and output powers is lowest and consequently the drain efficiency is highest at and near the 50% duty cycle operation (37.5% to 62.5%). But as the duty cycle decreases or increase beyond this optimum region, the difference between the input and output power increases, and consequently the efficiency decreases.

It should be noted especially in the higher duty cycle region that the input power levels increase dramatically while the output power levels don't change much. The reason for this dramatic increase in the input power at higher duty cycles is that the switch is open for longer durations of time and hence draws more and more current which may practically result in dangerously high power dissipation in the switch causing permanent damage. Combining this information with the fact that output voltage level doesn't change much beyond 50% duty cycle (as shown in Fig 4.4), we learn that bit-stream patterns involving higher duty cycle (0111) must be used less frequently. This is because 1) they will not result in any higher amplitude levels than desired, since the highest desired amplitude levels can readily be

achieved by 50% duty cycle bitstream pattern (0011), and 2) they can result in dangerously higher power dissipation in the switch which is not desired.



(a) (b)

Fig. 4.5 – a) Input and output power vs. the duty cycle of the gate input signal for the ADS model of the class-E amplifier. b) Associated drain efficiency vs. the duty cycle.

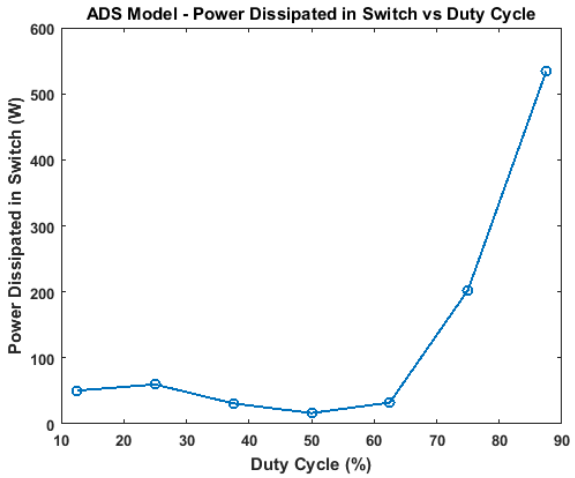


Fig. 4.6 – Power dissipated in the switch vs. the duty cycle of the gate input signal for the ADS model of the class-E amplifier

4.3. Gate Modulation Algorithm – Simulation Results

The intricate details regarding different aspects of the gate modulation algorithm and the methods employed to achieve both the amplitude and frequency modulation of the output waveform were elaborated in Sections 3.2 and 3.4. In this section, the simulation results of running the amplifier's analytical model (model 2) with the designed carrier bit-streams for achieving several desired output waveforms are presented.

4.3.1. Sinc Pulse of Duration 200 μs (Subsection Duration: 6.25 μs)

Fig. 4.7 shows the desired and predicted output waveforms for the sinc pulse of duration 200 μs. The total time duration in this design is divided into 32 subsections, each of duration 6.25 μs. Fig. 4.8 (a) shows the predicted output waveform plotted on top of the desired output waveform while Fig. 4.8 (b) shows a zoomed-in version from one of the subsections of this overlapped plot. It can be observed in Fig. 4.8 (b) that both the amplitude and phase of the predicted output waveform (orange) are made to follow, as precisely as possible, the amplitude and phase of the desired output waveform (blue). The NRMSE (normalized root mean square error) for the entire waveform is calculated to be 20.5% in this case. The FFT plots of the desired and the predicted output waveforms are shown in Fig. 4.9.

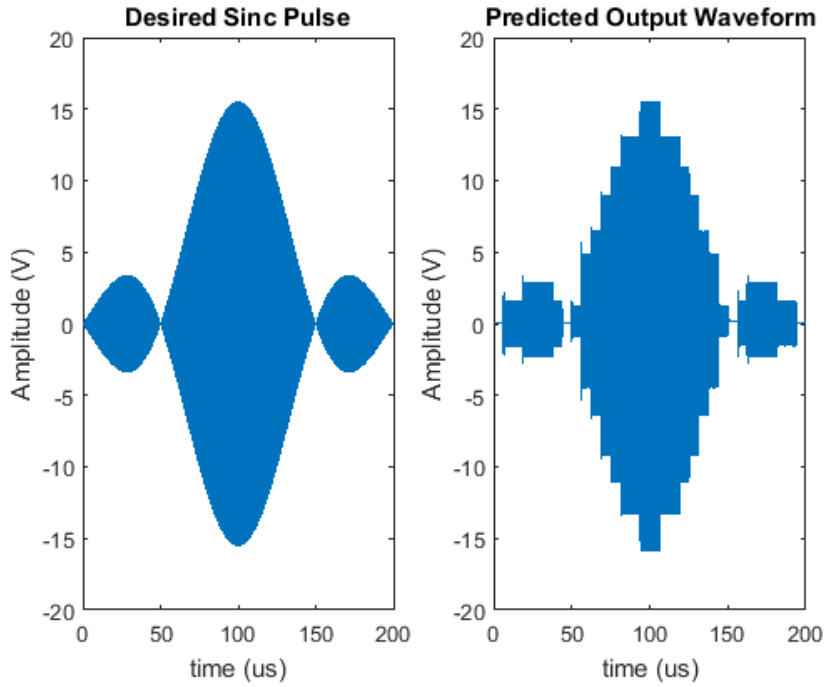
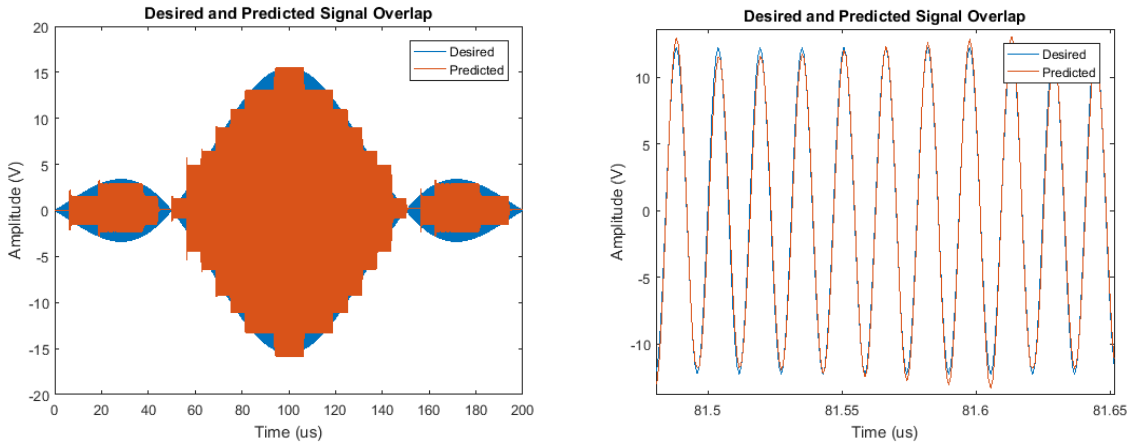
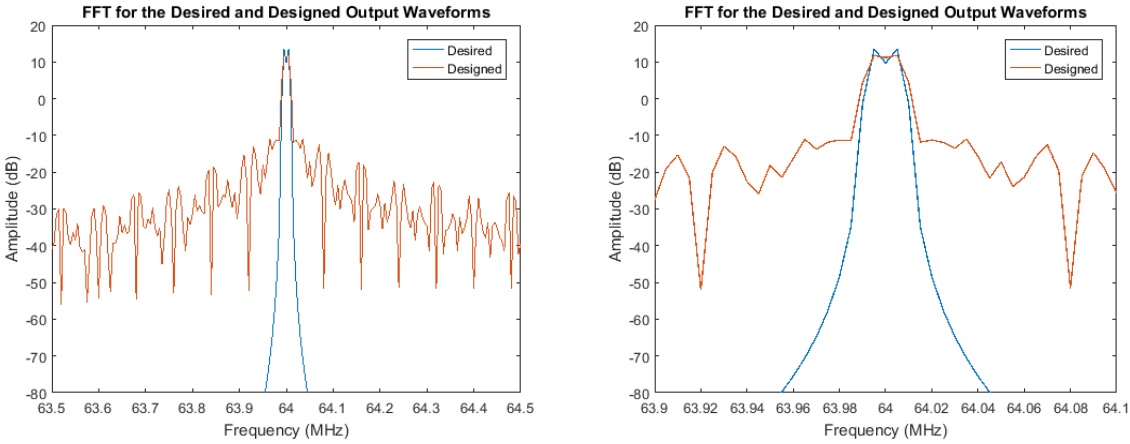


Fig. 4.7 – The desired (left) and predicted (right) output waveforms for the sinc pulse of duration 200 μs with a subsection duration of 6.25 μs.



(a) (b)

Fig. 4.8 – (a) The predicted output waveform plotted on top of the desired output waveform for the sinc pulse of duration 200 μs with a subsection duration of 6.25 μs. (b) Zoomed-in version of the same plot for one of the subsections.



(a) (b)

Fig. 4.9 – The overlapped FFT plots of the desired and predicted output waveforms. (a) The FFT plots in 1 MHz bandwidth show no harmonic peaks. (b) The FFT plots in 0.2 MHz bandwidth are shown. The FFT plots of the desired and designed output waveforms show 9.7 dB and 11.2 dB amplitude respectively at the center frequency (64 MHz).

4.3.2. Sinc Pulse of Duration 200 μs (Subsection Duration: 3.125 μs)

Fig. 4.10 shows the desired and predicted output waveforms for an apodized sinc pulse of duration 200 μs. In this case, the number of subsections and consequently the number of quantization levels are doubled compared to the previous case. The total time duration is now divided into 64 subsections, each of duration 3.125 μs.

It should be noted here that it takes about Q (Q for Quality Factor) cycles for the output waveform to reach the transient state in each subsection. Shifting from one bit-stream

pattern to another in a new subsection causes amplitude spikes in the transient state of that particular subsection. The bit-stream patterns are therefore designed such that the amplitude spikes in the transient state of each new subsection are minimized.

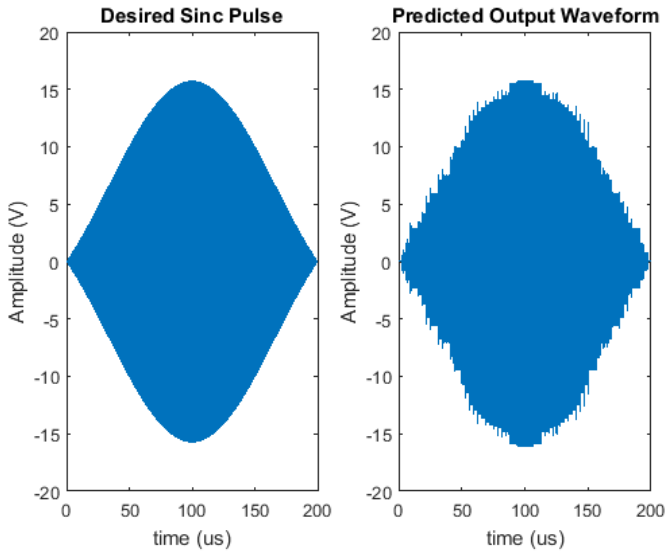
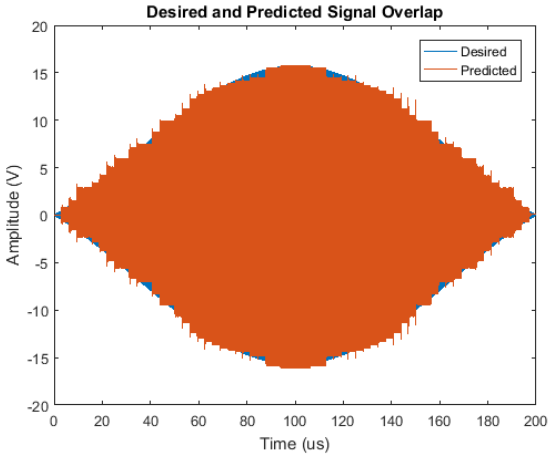
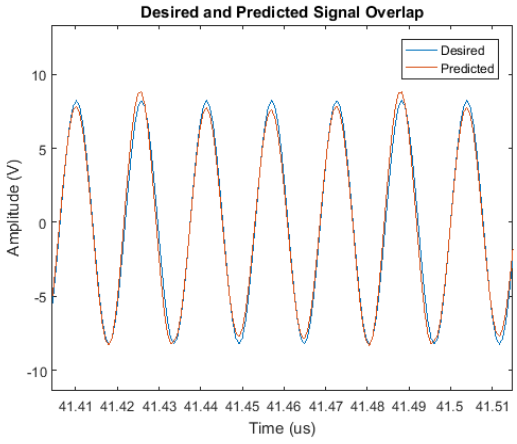


Fig. 4.10 – The desired (left) and predicted (right) output waveforms for the sinc pulse of duration 200 μs with a subsection duration of 3.125 μs. The spikes observed in the amplitudes of the predicted output waveform (right) correspond to the transient states of each subsection and are minimized based on careful designing of the bit-stream patterns.

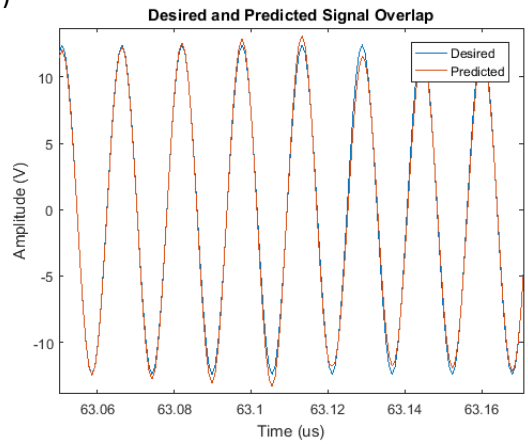
Fig. 4.11 (a) shows the predicted output waveform plotted on top of the desired output waveform while Fig. 4.11 (b-c) show zoomed-in versions from two of the subsections of the overlapped plot. It can be observed from these plots that both the amplitude and phase of the predicted output waveform (orange) are made to follow, as precisely as possible, the amplitude and phase of the desired output waveform (blue). The NRMSE for the entire waveform is calculated to be 14.8% in this case. The FFT plots of the desired and the predicted output waveforms are shown in Fig. 4.12. The FFT plots of the desired and predicted output waveforms show 26.6 dB and 19 dB amplitude respectively at the center frequency (64 MHz).



(a)

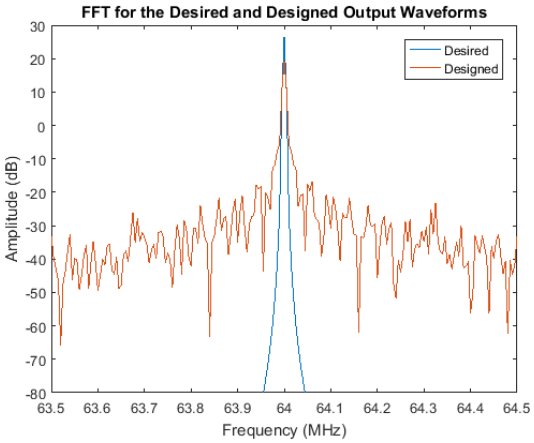


(b)

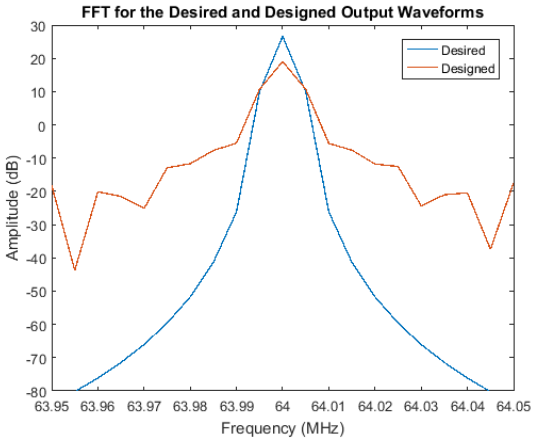


(c)

Fig. 4.11 – (a) The predicted output waveform plotted on top of the desired output waveform for the sinc pulse of duration 200 μs with a subsection duration of 3.125 μs. (b-c) Zoomed-in versions of the same plot for two of the subsections.



(a)



(b)

Fig. 4.12 – The overlapped FFT plots of the desired and predicted output waveforms. (a) The FFT plots in 1 MHz bandwidth show no harmonic peaks. (b) The FFT plots in 0.1 MHz bandwidth are shown. The FFT plots of the desired and designed output waveforms show 26.6 dB and 19 dB amplitude respectively at the center frequency (64 MHz).

4.3.3. Sinc Pulse of Duration 2 ms

Following the points explained in Subsection 3.4.4 of the previous chapter, an apodized sinc pulse of duration 2 ms was designed as shown in Fig. 4.13. Similar carrier bit-stream patterns were used for designing the sinc pulse in this case as were used in designing the sinc pulse of duration 200 μs with a subsection duration of 3.125 μs. The desired and predicted output waveforms in this case are shown in Fig. 4.13 while the associated FFT plots are shown in Fig. 4.14. The FFT plots of the desired and predicted output waveforms show 26.4 dB and 19 dB amplitude respectively at the center frequency (64 MHz). The NRMSE for the entire waveform in this case is calculated to be 11%.

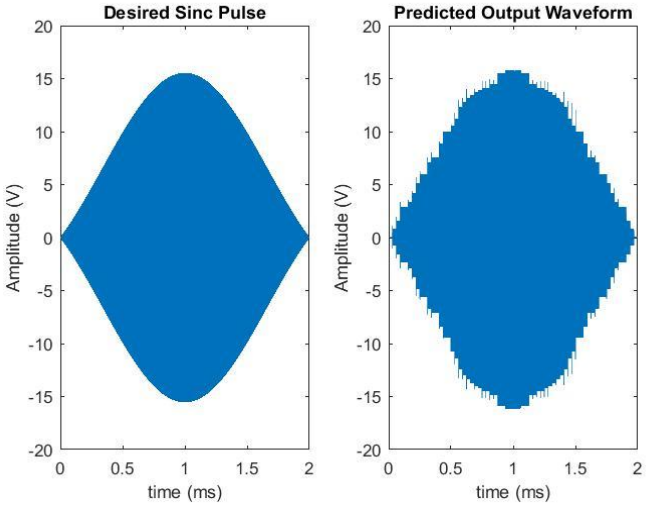


Fig. 4.13 – The desired (left) and predicted (right) output waveforms for the apodized sinc pulse of duration 2 ms

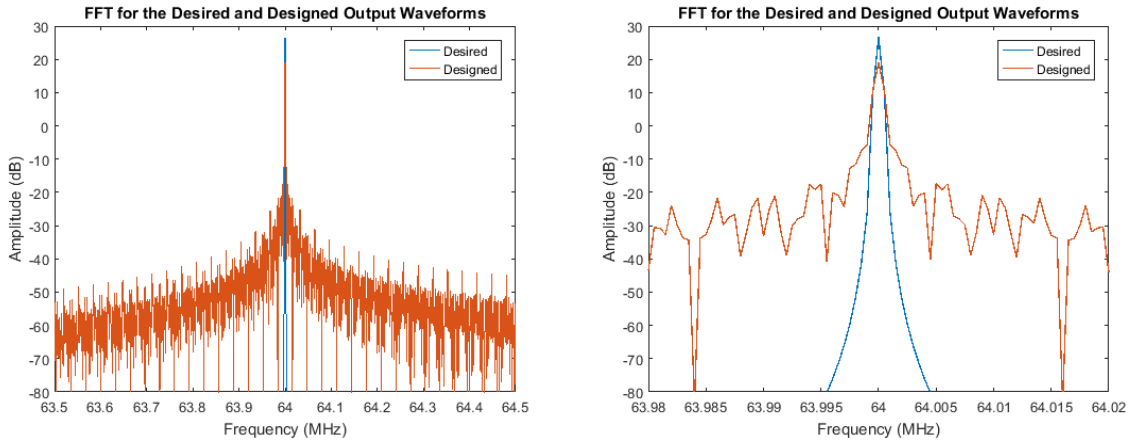


Fig. 4.14 – The overlapped FFT plots of the desired and predicted output waveforms. (a) The FFT plots in 1 MHz bandwidth show no harmonic peaks. (b) The zoomed-in version is shown. The FFT plots of the desired and designed output waveforms show 26.4 dB and 19 dB amplitude respectively at the center frequency (64 MHz).

4.4. Hardware Implementation Results

The methods used for the amplifier's implementation on hardware were detailed in Section 3.5. In this section, the associated essential waveform results are presented. It must be noted here that the gate modulation algorithm is not yet implemented on hardware. Meaning, the FPGA is not sending the custom designed carrier bit-stream to the PCB at this point. It is instead sending a 50% (0011) duty cycle bit-stream to the PCB. This is done in order to perform the pre-tuning of the amplifier in order to achieve ZVS and ZVDS conditions and obtain the most efficient operation of the amplifier at 50% duty cycle. Fig. 4.15 (a) shows the LVDS signals that the FPGA sends to the amplifier's PCB, as an input to the driver circuit of the amplifier. Fig. 4.15 (b) shows the driver circuit's output signal (the signal at the input of the gate of the amplifier). The rise and fall times of this signal are measured to be approximately 1.8 ns. And finally, Fig. 4.15 (c) shows switch voltage waveform. It can be seen that the ZVS and ZVDS conditions are satisfied.

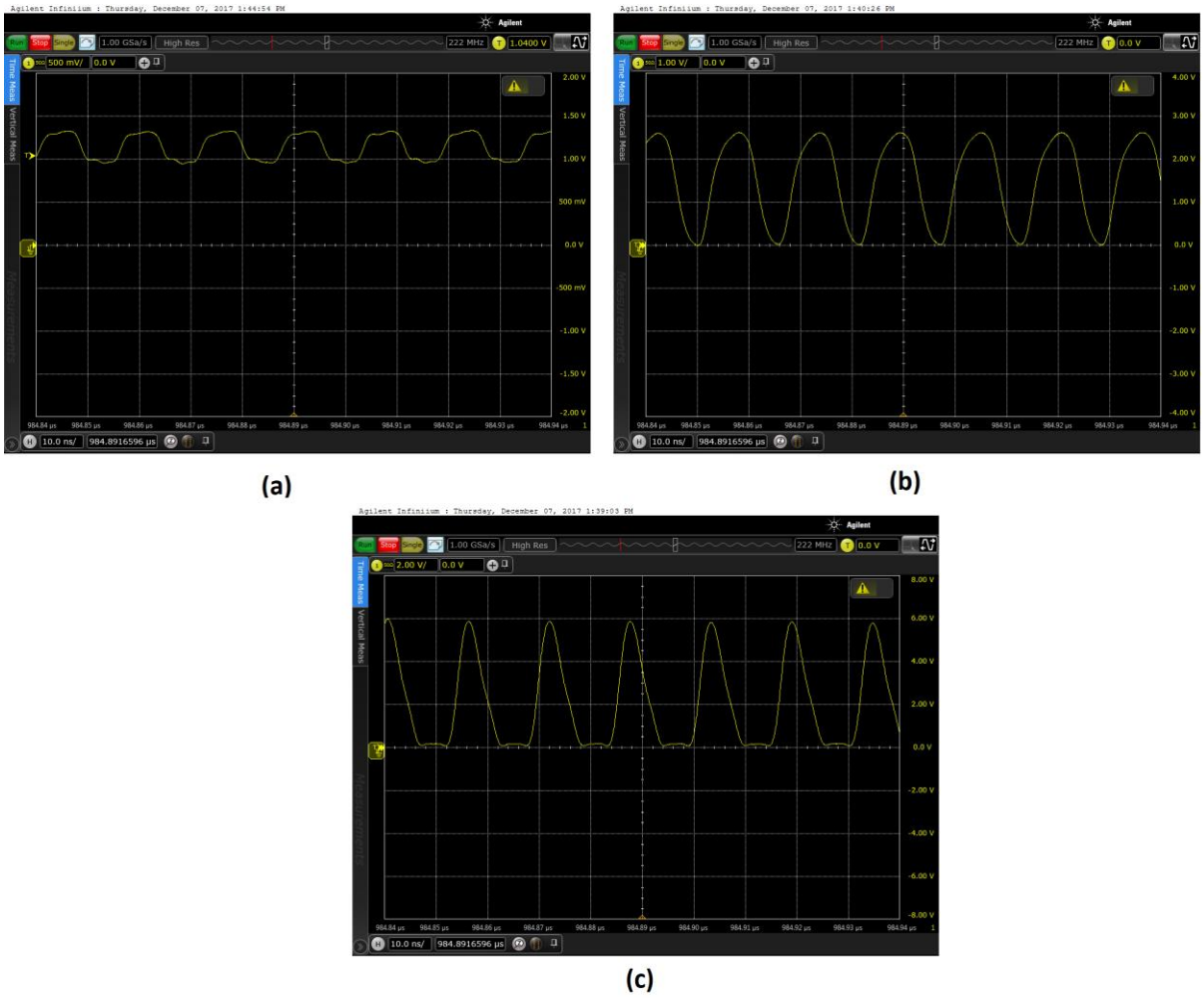


Fig. 4.15 – Hardware implementation results when the amplifier PCB is run with a 50% duty cycle signal at the gate of the amplifier (0011). a) LVDS signals sent by the FPGA to the driver part of the amplifier PCB. b) The signal at the output of the driver part and input to the gate of the amplifier. c) Switch-voltage vs. time. ZVS and ZVDS conditions are satisfied.

4.5. Gate Modulation Algorithm – Experimental Results

In this section, the results of implementing the gate modulation algorithm on hardware, i.e., the results of running the amplifier PCB with the designed carrier bit-streams in both the bench-top and MR experiments are presented.

4.5.1. Bench-top Experiments Results

The FPGA was programmed with the designed carrier bit-streams and the setup was arranged as described in Section 3.6. Following are presented the results for the implementation of two carrier bitstreams.

4.5.1.1. Sinc Pulse of Duration 200 μs (Subsection Duration: 6.25 μs)

Fig. 4.16 shows the amplifier's gate modulated output waveform when the carrier bit-stream designed for obtaining a sinc pulse of duration 200 µs with a subsection duration of 6.25 µs was implemented.

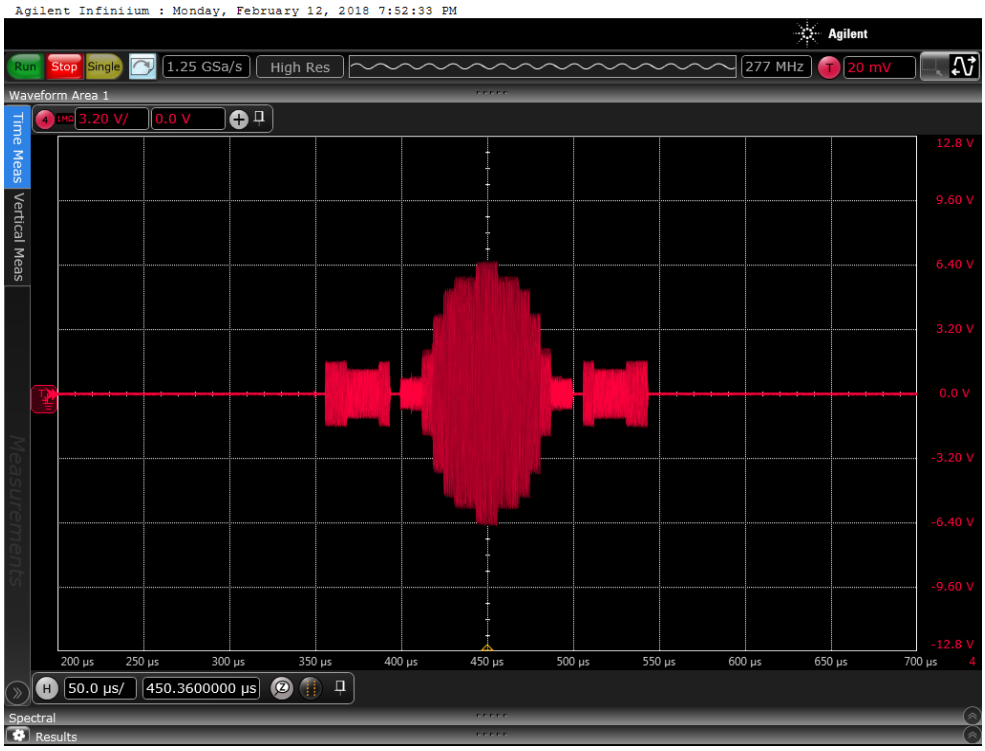


Fig. 4.16 – Gate modulated output waveform of the amplifier when the carrier bit-stream designed for a duration of 200 µs with a subsection duration of 6.25 µs is implemented.

It can be seen from the figure above that the amplitude levels of the side lobes of the sinc pulse don't match with their software counterparts. This can be explained by the fact that the amplifier's analytical model assumes an ideal switch and therefore a few of the amplitude levels in the hardware implementation would not always precisely match with their software counterparts. This fact was kept in mind while implementing the later carrier bit-streams on hardware, and a re-optimization method as explained in Subsection 3.6.1 was implemented in order to obtain the closest match between the software and hardware waveforms. The FFT of the output waveform is shown in Fig. 4.17.

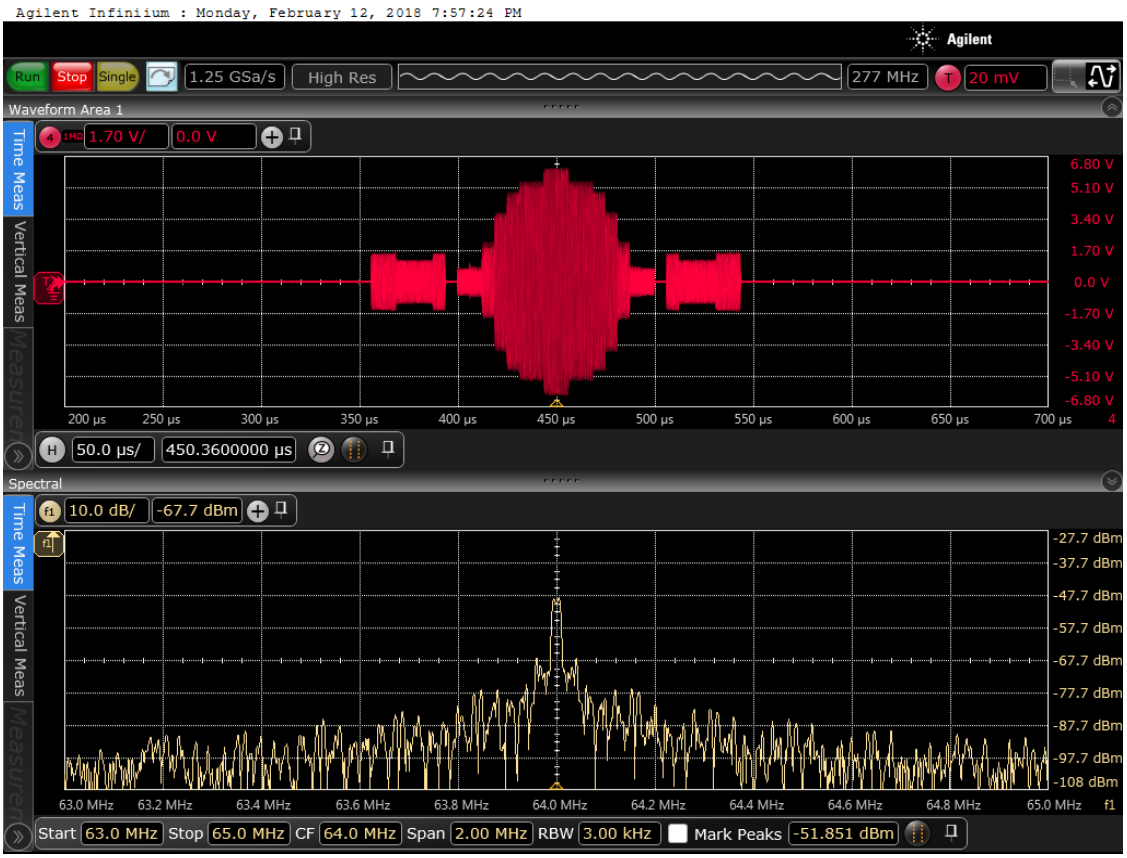


Fig. 4.17 – Gate modulated output waveform of the amplifier (200 µs, subsection duration 6.25 µs) and the associated FFT in 1 MHz bandwidth.

4.5.1.2. Sinc Pulse of Duration 2 *ms*

Fig. 4.18 shows the amplifier's gate modulated output waveform when the carrier bit-stream designed to obtain a sinc pulse of duration 2 ms was implemented. It must be noted here that certain sections of the carrier bit-stream were re-optimized using the method explained in Subsection 3.6.1 in order to obtain the closest match between the software and hardware waveform. Fig. 4.18 (right) shows the drain current waveform (yellow) on top of the received output waveform (red). The experiment was conducted at 30 W input power and the peak drain efficiency was recorded to be 89%. The FFT of the output waveform is shown in Fig. 4.19. The FFT shows a 14.1 dBm peak value at the central frequency (64 MHz) with a 10 dB difference in magnitude to the nearest harmonic components under a bandwidth of 2 MHz.

Fig. 4.18 – Gate modulated output waveform (red) of the amplifier when the carrier bit-stream designed for a duration of 2 ms is implemented. The overlapped drain current profile (yellow) is also shown (right side).

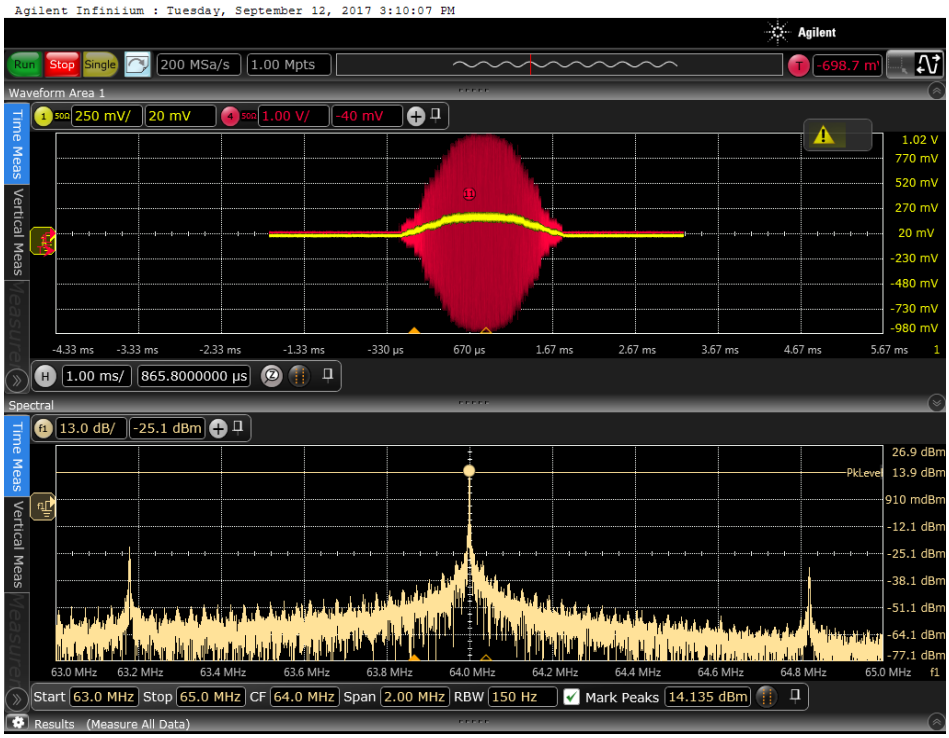


Fig. 4.19 – Gate modulated output waveform of the amplifier (2 ms) and the associated FFT in 2 MHz bandwidth. The FFT shows a 14.135 dBm peak value at the central frequency (64 MHz) with a 10 dB difference in magnitude to the nearest harmonic components under a bandwidth of 2 MHz.

4.5.2. MRI Experiments Results

The initial MR image obtained at 50 W input power (GRE sequence, 5 mm slice thickness, TE/TR = 15/200 ms) is shown in Fig. 4.20 The ghosting artifacts observed in the phase

encoding direction (left to right) were associated with the phase inconsistencies and synchronization issues as described in Subsection 3.7.1.

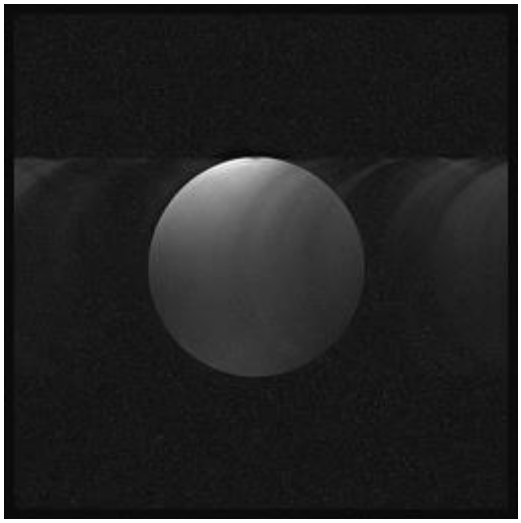


Fig. 4.20 – MR image obtained at 50 W input power (TE/TR = 15ms/200ms). The ghosting artifacts observed in the phase encoding direction (left to right) are associated with the phase inconsistencies and synchronization issues.

After resolving those issues as explained in Subsection 3.7.1, the resulting MR images at 50 W input power (GRE sequence, 5 mm slice thickness, TE/TR = 15/200 ms) and at different FOV (fields of view) are shown in Fig. 4.21 below.

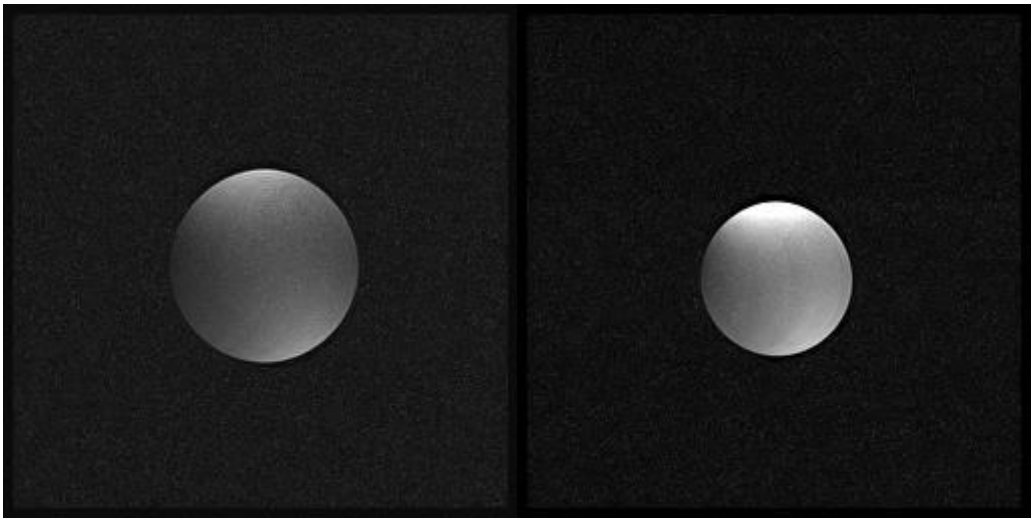


Fig. 4.21 – MR image obtained at 50 W input power (TE/TR = 15ms/200ms) at different FOV (Field of Views) after the phase inconsistencies and synchronization issues have been resolved.

CHAPTER 5

DISCUSSION AND CONCLUSION

In this work, a novel technique of modulating the amplitude and frequency of the output waveform in a class-E configuration and the application of such technique to the on-coil amplifier configuration for RF excitation in MRI is presented. The analytical modelling of the class-E amplifier was performed using two different assumptions at the drain of the amplifier, and the resulting equations for both those models were implemented in MATLAB. One of the models, where an ideal constant-current source assumption was made at the drain of the amplifier, worked well at 50% duty cycle operation but provided false results as the duty cycle was varied and therefore was not utilized further. The gate modulation algorithm was developed with the other model (model 2) of the amplifier where an inductor was assumed at the drain of the amplifier. However, since the MATLAB model assumed an ideal switch, a few of the quantization levels in the hardware tests didn't match precisely with their software counterparts and hence further re-optimization of certain sections of the carrier bit-stream needed to be performed.

During developing the Gate Modulation algorithm, each period of the carrier waveform was divided into k bits where k was set to 4 in our case. This required that the FPGA transmitted the bit-stream at a rate k times higher than the operating frequency. In our case, the operating frequency was 64 MHz, so the FPGA transmitted the bitstream at 256 MHz. Though increasing the number of bits per period would allow for a better design and control over the output waveform while designing the carrier bit-stream in software, it would also mean that

on hardware, the FPGA would be required to transmit the bit-stream at an even higher rate. For example, 8 bits per period with an operating frequency of 64 MHz would require the FPGA to transmit the bit-stream at $64\ \mathrm{MHz} \times 8 = 512\ \mathrm{MHz}$. Such hardware limits must be kept in mind if a higher number of bits per period are to be pursued in future.

The process of designing the bit-stream patterns for obtaining both the amplitude and phase match between the desired and predicted output waveforms was carried out manually. The amplitude and phase of the desired and predicted output waveforms were visually observed on top of each other for the subsection being designed, alongside observing the error plot between the predicted and desired waveforms and their corresponding FFT plots as well. Based on the experience and understanding of the way different bit-stream patterns affected the waveform, an entire carrier bit-stream could be designed in approximately thirty minutes to two hours. A point of interest however is to automate the process of designing the bitstream. But even if only four bitstream patterns were to be considered for the entire design process (0000, 0001, 0010, 0011), and 16 cycles were chosen to be designed at a time, it would mean that there are $4^{16} = 4{,}294{,}967{,}296$ available bit-stream patterns to choose from while designing each subsection. Generating such huge number of patterns in MATLAB and then testing each of them for designing each subsection of the bit-stream is practically infeasible. One suggested approach to addressing the problem is to consult the domains of neural networks and deep learning algorithms. By generating an array of all the bitstream patterns of interest, and by running the amplifier model for all those bitstream patterns for a small duration of time, the resulting output waveform data could be utilized as the training data for the neural networks. With the desired output waveform already known, the neural network could then learn to find the optimum carrier bitstream patterns for all the sections of the waveform.

The ultimate goal of the research group has been to design a 32-channel transmit array using integrated on-coil amplifiers, replacing the need for conventional low-efficiency MRI RF amplifiers placed in the systems room away from the excitation coil. In pursuing that goal, each individual amplifier has been required to provide 300 W output power so that an array

of 32 such amplifiers could collectively provide about 10 kW of output power which would be sufficient enough to excite the whole body, thus the goal of the previous works has primary been to achieve 300 W output power from an individual amplifier while achieving the highest possible efficiency. Before this work, the main emphasis of the group had been to use the conventional supply modulation approach in obtaining the amplitude modulation of the output pulse. In an attempt to remain consistent with the overall goal of the group, the same PCBs with the same MOSFET models as fabricated earlier were utilized for the current work as well. There were, however, a few problems that were encountered when an attempt to achieve higher power levels (above 50-80 W) was made using the current approach. It was observed both in simulations and hardware experiments that certain bitstream patterns caused the peak value of the switch voltage (V_{C1_peak}) to increase beyond the typical value (typical value being 3.56 times that of the supply voltage V_{DD} according to equation (2.8)). The ZVDS condition were also observed to be violated in certain instances, indicating that the amplifier was operating in the suboptimum region in those sections of the waveform. In order for the amplifier to achieve about 300 W output power, the supply voltage needed to be increased to about 30 V, but this meant that V_{C1_peak} would increase beyond the limiting value (110 V) which could damage the transistor. Further research needs to be conducted in this aspect of the project to achieve the required output power. Techniques described in [37-39] could be utilized to reduce and limit the value of V_{C1_peak} in an attempt to solve this problem.

It is also suggested to combine the presented modulation technique with the conventional supply modulation approach in an attempt to achieve higher dynamic range. One way of achieving this is to first divide the supply voltage waveform (V_{DD}) into multiple levels using the supply modulation approach. Then, the gate modulation approach could be implemented in different parts of the waveform using different available values of V_{DD}. Sections of the waveform with lower desired amplitude values could be assigned lower values of V_{DD}, while those sections where higher amplitude is required, higher values of V_{DD} could be assigned. The waveform could be divided to a greater number of quantization levels in lower amplitude parts in order to achieve smoother envelope modulation, while less number of quantization levels could be used in parts of the waveform where the amplitude is not changing abruptly.

In conclusion, the gate modulation technique presented in this work opens up a new dimension in the field of achieving the amplitude and phase modulation of the output waveforms with demonstrated application in MRI and expected applications in wireless power transfer and other transmitter applications. The technique is general in its implementation. Though not proven, the theory and methods presented in this work, from analytical modelling of the amplifier to implementing the gate modulation technique, are general in nature and could be applied to other switch-mode RF power amplifier topologies as well like class-D, class-F, inverse class-E etc. The presented technique is novel in nature but not entirely perfect at this stage. Further improvements can be made in analytical modelling of the amplifier by including a non-ideal model of the switch. By introducing further developments to the algorithm and by overcoming the currently presented challenges of the hardware, the gate modulation technique could provide an equivalent performance as the conventional supply modulation approach while reducing the overall cost and complexity of the circuit at the same time.

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