A 94-GHZ PHASE INVERTER-VARIABLE GAIN AMPLIFIER IN SiGe BiCMOS

A THESIS

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MASTER OF SCIENCE

By

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July, 2017

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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July, 2017

Phased array radar systems are capable of steering the beam of radio waves electronically by adjusting the gain and phase of each antenna element as desired. In order to achieve that, each element has to have gain/phase control and these parameters have to be controlled separately. In W-Band designs, constant gain-360° phase control is difficult to achieve due to parasitic effects of high frequencies which may quickly differ across different settings. Dividing the phase control task into different blocks in system eases the design difficulties. A well developed W-Band technology SiGe BiCMOS is also crucial to achieve high frequencies and system control.

In this thesis, a 94-GHz SiGe BiCMOS phase inverter with variable gain amplifier is developed. Single bit-180° phase inversion enables to use multiple bit-180° phase shifter which is easier to design in W-Band. In addition to that, variable gain amplifier allows to use this circuit in phased array systems for amplitude tapering to achieve desired beam forming.

Keywords: phased array, phase inverter, variable gain amplifier, SiGe BiCMOS, W-Band.

ÖZET

94-GHZ SIGE BICMOS TEKNOLOJİSİNDE FAZ EVİRECİ-DEĞİŞTİRİLEBİLİR KAZANÇLI YÜKSELTEÇ

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Faz dizili radar sistemleri her anten elemanının kazancını ve fazını istenilen şekilde ayarlayarak radyo dalgalarının yönünü elektronik olarak kontrol etme özelliğine sahiptirler. Bunu yapabilmek için, her elemanın kazanç/faz kontrolü olması ve bu parametrelerin birbirlerinden ayrı olarak kontrol edilebilmesi gerekmektedir. W-Bant tasarımlarda, yüksek frekansların farklı ayarlarda değişebilen parazitik etkilerinden dolayı sabit kazanç-360° faz kontrolü elde etmek zordur. Faz kontrol görevini sistemdeki farklı bloklara bölmek, tasarım zorluklarını kolaylaştırmaktadır. İyi geliştirilmiş W-Bant SiGe BiCMOS teknolojisi de yüksek frekans ve sistem kontrolü icin hayati önem taşımaktadır.

Bu tezde, 94-GHz SiGe BiCMOS tabanlı değiştirilebilir kazançlı faz evireci geliştirilmiştir. Tek bit-180° faz evirme işlemi W-Bant'ta daha kolay tasarlanabilen çoklu bit-180° faz kaydırıcı kullanımını sağlamıştır. Buna ek olarak, istenilen sinyal hüzmesini ve yönünü elde edebilmek için değiştirebilir kazanç yükselteci bu devrenin faz dizili sistemlerde kullanılabilmesini sağlamıştır.

Anahtar sözcükler: faz dizili, faz evireci, değiştirebilir kazanç yükselteci, SiGe BiCMOS, W-Bant.

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Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 General Introduction

Phased arrays can be defined as circuits that enable to steer the beam electronically and rapidly. This operation is done by adjusting the phase and amplitude of the signals of the individual elements. Many advantages of phased arrays made them popular such as not moving the structures to beam to different directions, fast-electronically controlled beam forming and high yield numbers since systems can tolerate single element failures [1].

System components inside of the phased arrays should provide different key features. In this thesis, one of them is addressed and tried to be solved; constant gain 360° phase inversion. At system level, one can calculate the phase and amplitude of each element to achieve desired beam forming. Constant gain 360° phase control separates phase and gain parameters from each other and provides precise phase control to system level designers. Gain control is usually done by multi-bit controlled attenuators and sometimes by adjusting the gain of amplifiers. Reliable phase and gain control of the integrated circuit enables to get high quality images from different directions in small intervals.

Between the commercially avaliable technologies, SiGe BiCMOS is a reliable

technology considering it's maturity (other circuits are already developed at lower frequencies as in [2], [3], [4]), high frequency performance and capability of producing complementary metal oxide semiconductors (CMOS) on chip to build analog/digital control circuitry.

1.2 mm-waves

mm-wave frequencies are defined as the frequency range between 30 and 300 GHz. Its getting more and more popular due to high demand of higher data rate communications such as 5G. In terms of data rate, mm-wave designs present capability of achieving 1 Gb/s communication rates [5] thanks to higher operating frequency and open a new era of communication systems. In addition to that, mm-waves are also popular in imaging systems since it provides higher resolution. Increased resolution attracted developers from different majors and mm-wave enters in different areas such as medical, adaptive cruise control and aircraft landging surveillance systems [6]. Also higher frequencies enable us to build smaller and closer antennas which can be directly integrated on package [7].

At the mm-wave spectrum, attenuation of a signal usually increases with frequency due to water vapor and oxygen. At some frequencies attenuation increases due to resonance behaviour of these particles [8]. This can be desirable for indoor applications to limit the range but also might be undesirable for the outdoor applications such as surveillance radars. Particularly 94-GHz is popular among imaging applications and used in different circuits such as transmitters, receivers or sensors as in [6], [9], [10] since there is not any extra resonance behaviour of particles in air and the frequency is high enough to benefit from it's advantages. The circuit in this thesis is going to be used in such application therefore 94 GHz is selected as operating frequency.

1.3 SiGe BiCMOS Technology

Silicon-germanium (SiGe) BiCMOS technology is first developed at 1996 providing the capability of producing heterojunction bipolar transistors (HBTs) with CMOS transistors on the same substrate which is SiGe. High f_T and f_{max} valued bipolar transistors are used in RF/mm-wave circuits while CMOS technology which contains NMOS and PMOS transistors is used in analog/digital circuitry. Particularly in civilian applications, SiGe BiCMOS is desired over III-V technology since it provides higher integration level which leads to build unique system architectures and lower cost. Although new technology solutions such as GaN HEMTs, GaAs HEMTs and InP HBTs have capability of work on mm-wave frequencies their cost and integration level haven't reached SiGe BiCMOS yet [11]. Reliability level is one of the most important factors in complex integrated circuit designs. Without well-established process and design kit it is impossible to achieve simulated performance on real life.

In this thesis, IBM's 130 nm SiGe BiCMOS 8XP technology is used (IBM sold the foundry to GlobalFoundries during to development stages of 8XP). At 1.7 V operation 260 GHz f_T and 320 GHz f_{max} values are reported for HBTs which is adequate for 94-GHz designs[8]. 8XP technology is recently became commercially available and provided reliable HBT performance. The circuit in this thesis produced through multi-project wafer fabrication of MOSIS IC Fabrication Service Provider.

1.4 Thesis Outline

In this thesis, design and measurement of a 94-GHz phase inverter-variable gain amplifier in SiGe BiCMOS is presented. In chapter 2, some of the key features and techniques of mm-wave designs are explained. Design steps and simulation results are presented in chapter 3. Measurement setup and results are explained in chapter 4.

Chapter 2

mm-wave Design Fundamentals

Since mm-wave band is the frequency spectrum just above the microwave band, typical RF/microwave design techniques are still valid. However, due to increased parasitic effects designer should only use stable and mathematically well established procedures such as impedance transformations, input/output matching of transistor and bias point calculations. At the same time, designer should avoid not well calculated procedures as much as possible such as EM analysis, single transistor amplifiers due to parasitic collector-base capacitance and interconnections which are not modeled. Some solutions of the problems above may reduce the performance, however stable first-time-right design is the most important feature to achieve considering high production costs. In this thesis, these solutions and their effects on performance are discussed time to time with possible more risky solutions and reasons of their risk.

In this chapter, the techniques where mm-wave designs differ from standard RF/microwave designs are discussed. Simulation flow is also reviewed to give the impression of what should be done to start and complete a mm-wave design.

2.1 Crucial Elements to Achieve First-Time-Right Design

First-time-right design can be defined as achieving desired/simulated performance at measurement of first run of produced chips. Satisfying this goal is important in terms of cost and time, since every other iteration requires significant amount of time and money to be spent. Some of the items in this section is also valid for RF/microwave circuits but some of them are special for mm-wave or has to be considered more carefully.

2.1.1 Well Modeled Technology

From the lowest frequencies to mm-wave probably the most important factor to build successful design is model-to-hardware correlation. Most of the immature technologies and foundries cannot provide well modeled technologies. Because of that, even if they offer high performance technology and show their capability of producing it, hardware must be modeled correctly so that designer can trust simulations.

The circuit in this thesis is one of the very first designs produced with 8XP technology. However, 8XP technology can be seen as the updated version of 8HP technology (f_T f_{max} values are slightly greater, noise figure is slightly lower) where successful designs are already reported at mm-wave [12][13].

2.1.2 High Performance Technology

When the technology performance is higher, designer can apply techniques such as matching according to reflections rather than noise or power, to make the design more robust in case models are slightly off. Since this frequency range is not as popular as microwave band, obtaining a robust working design is more important than pushing the limits of technology.

2.1.3 Good Parasitic Extraction Decks and Tools

In order to achieve good simulation-hardware correlation, designer should pay attention to use design kit models as much as possible especially at RF signal line. However, some interconnections must be drawn without using design kit models in layout such as transition from upper layer metal to lower layers. Furthermore, transistor performance can be directly affected from adjacent metals or other layout layers. Therefore, parasitics at these areas must be extracted carefully by designer and a design tool should be capable of doing it. Considering all of the features of an electronic design automation (EDA), extraction tool is the most expensive feature since it calculates lots of effects together and provide correct parasitic parameters to designer to be work on.

2.1.4 Bug-free Design Kit

Design kits usually contain bugs; some of them are minor and solvable but some of them are major and make the design unworkable. Of course, decreasing the number of bugs always in favor of designers, however in mm-wave complex circuitries there are two important tools that have to be as much bug-free as possible; DRC (Design Rule Check) and LVS (Layout Versus Schematic).

Usually foundry provides Design Rules to tell designers what they can produce and what they cannot according to their production capabilities. These rules divided into three sections; Class A, B and C rules. Class C rules can be considered as notifications to designers telling that foundry can produce the layout as it is however designer should be aware of the situation which affect the performance or reliability. Class B rules can still be omitted however foundry does not approve to produce them since the corresponding layout area carry high risk to affect performance. Class A rules mean foundry cannot produce the layout in that form, designer should change it. These rules have to be defined correctly so that designer can know what is producible and what is not. In addition to that, well-defined Class B and C errors provide designer to capability of manipulating layout to achieve desired performance and completing final layout with

some possible errors.

LVS is a tool that compares layout and schematic netlists and show if the layout completely corresponds to the schematic. A single or few-layer desings such as MMICs usually do not require LVS since all connections can be checked easily. However, when the number of layers increases, it is difficult to keep track of all connections especially in large designs. Although the operation of this tool seems easy, it can still carry bugs. Removing those bugs will assure designer that he is simulating exactly what he is going to produce. A single small error may end up with wrong produced IC which costs a lot.

2.1.5 Good Interaction with Foundry

As designers try to improve their designs, technology development teams in foundries also try to improve their processes and design kits. Routinely they release updates for design kits and try to improve hardware-model correlation and decrease the number of bugs. However, new updates can bring new bugs or some features that result in different simulation results compared to previous kit. If designer is in close interaction with foundry these problems can be addressed quickly and he/she can continue to work rather than spend extra time to understand and solve that problem. The importance of this item further increases if the technology used is relatively new such as in 8XP technology.

2.1.6 Corner Simulations

In research based works, usually people tend to present the performance of single chip/circuit. However in real life, the performance of chips may differ according to different parameters, the most significant ones are process variation, temperature and voltage supply value. Although temperature and voltage supply value can be kept as constant at measurements, process variation is out of control. Designer should keep in mind that his design may encounter with some variation and he should adjust his design to satisfy the requirements independent of variation.

When a design turns into a real life product and starts to be used in different locations, temperature and voltage supply value also come into picture. Design can be expected to work at sunny weather and snowy weather at the same time. Voltage supply value may also change to some degree.

In order to consider all of these effects together, simulating all combinations of these parameters may not be feasible. Thus, a designer can define corners which are combinations of these parameters and complete simulations at those corners. The corner parameters defined for this thesis will be explained in Chapter 3.

2.1.7 Reliable Test Environment

Even if designer pays attention to all other parameters and foundry produces exactly the design in simulations, it has to be verified correctly to ensure it is working properly. At mm-wave frequencies all of the components used in test setup have to be very-well defined. Even a small bend at a cable may affect the performance and change the measured gain. The details of test setup of this thesis will be explained in Chapter 4.

2.2 Key Design Features Where mm-wave Differs From Microwave

Besides the points mentioned in previous section, there are few design differences at mm-wave compared to microwave circuits. These differences enable to build more reliable circuits and also help to achieve first-time-right design.

2.2.1 Transmission Lines

At microwave frequencies, commonly microstrip lines are used as transmission lines rather than CPW (co-planar waveguide) lines. In Fig. 2.1 and 2.2, pictures

of a microstrip and a CPW line can be seen.

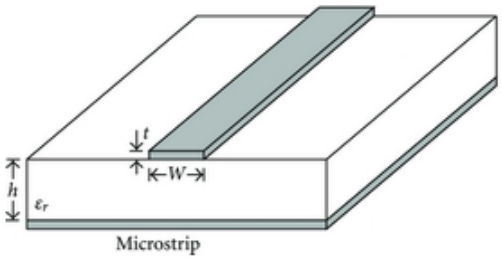

Figure 2.1: A microstrip line

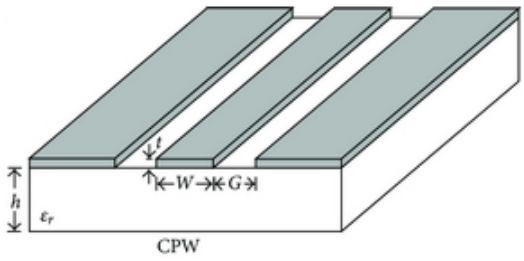

Figure 2.2: A CPW line

When microstrip lines are used, there will be some electro magnetic (EM) coupling effect between the transmission line and circuit elements since signal can radiate freely. In order to capture that, EM analysis should be performed with a CAD tool such as HFSS. However, since this analysis solves a large number of equations the required time increases exponentially when the number of layers increases. More importantly, when a mm-wave circuit is designed on multi layer IC, these EM coupling effects became out of control and they might cause oscillations. Thus, it is almost impossible to reflect hardware on software correctly. To overcome this issue, a designer can waive advantages of microstrip lines and use so called half-CPW half-microstrip line which can be seen at figure 2.3.

At this configuration, RF signal line is surrounded by ground plane by 180 degree so that EM lines will end up at well defined ground plane rather than coupling to unrelated design components. The vertical ground connection between the lower and upper layer at Figure 2.3 is done by densely manufactured vias.

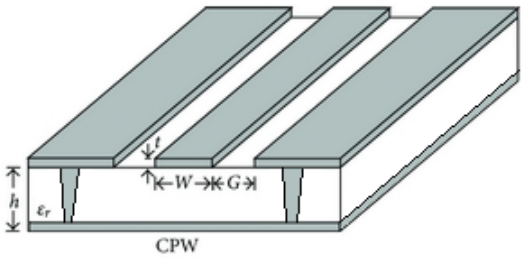

Figure 2.3: A half-CPW half-microstrip line

Surrounding RF line from upper side is not necessary if RF line is at highest level of metal. If it is not it, has to be surrounded from both sides due to reasons explained.

As it is described in previous pages, this configuration of transmission line has to be well defined by foundry so that designer can use it safely at mm-wave. Removing the effort of EM analysis and possible further tuning operations will save tremendous amount of time and improve the hardware-software correlation.

2.2.2 Cascode Structure

In Fig. 2.4, a common-emitter common-base configuration can be seen. The advantage of this configuration compared to single common-emitter amplifier is the increased isolation between output and input ports. Due to this reason it is very popular among mm-wave designs as in [14], [15], [16]. The transistor that is used as common-base form reduces the multiplication effect of the Miller capacitance at common-emitter transistor and makes the circuit easier to stabilize. This multiplication effect comes from the gain of the transistor, however in cascode form the transistor at common-emitter configuration presents low gain therefore small capacitor is obtained at base to collector. At 94 GHz, unwanted feedback loops can be formed if a common-emitter amplifier is used. Thus, this configuration is desired although it carries other disadvantages such as requirement of two transistors.

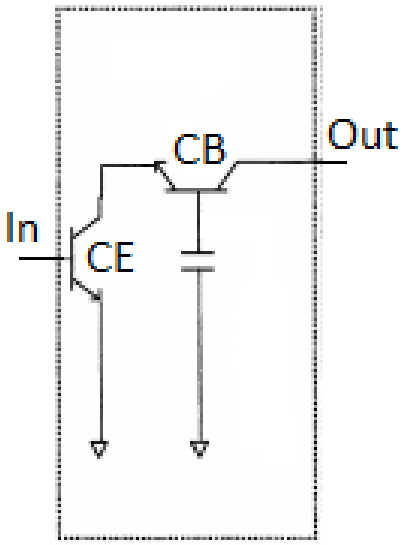

Figure 2.4: Common-emitter common-base cascode configuration

2.2.3 Simulation Flow

Correct simulation flow is also important to realize the desired design and it carries slight differences in mm-wave. Firstly, conventional schematic simulations has to be done. Secondly, EM analysis should be performed if the transmission lines are somewhat interacting each other due to design requirements. For instance, in Fig. 2.5, two transmission lines are crossing each other at different layers and their half-cpw half-microstrip structure is sacrificied. Areas like this require EM analysis.

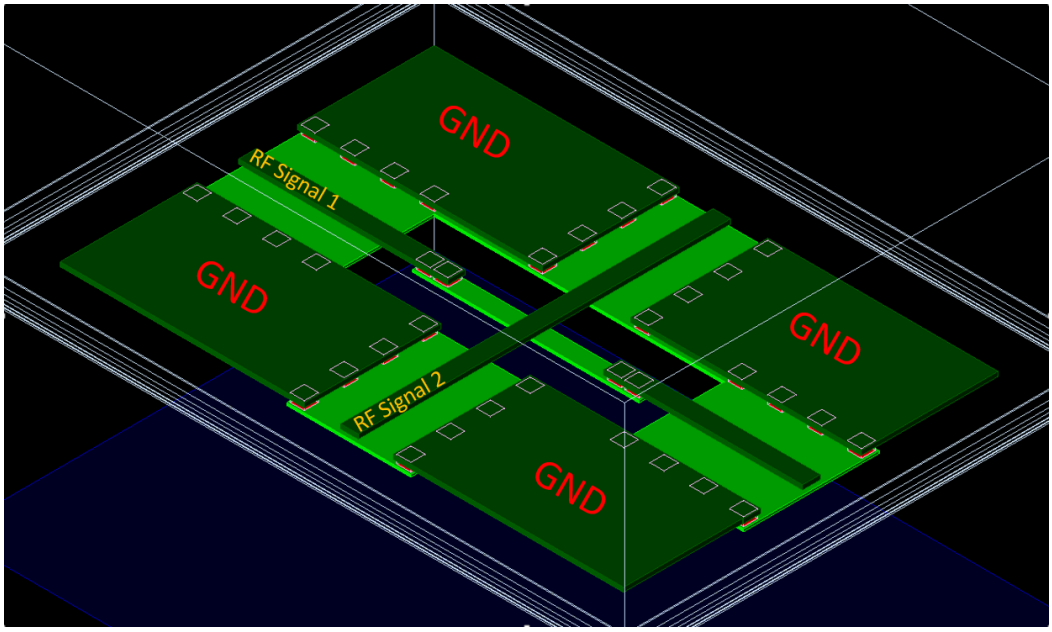

Figure 2.5: Crossing of two signals at different layers

After that, device-level parasitic extraction (with QRC tool) has to performed, especially at areas that can affect the circuit performance. Parasitic extraction is mainly used for capturing the parasitics around the active devices since EM analysis cannot be performed around active devices and improving software-hardware correlation on the areas where only passive design kit models are used. As a final step, via inductances has to be added manually since QRC tool we used correctly extracts only resistances and capacitances not inductances. As a rule of thumb, 1 pH inductance is placed for a μm via length.

Chapter 3

A 94-GHz SiGe BiCMOS Phase Inverter-Variable Gain Amplifier Design

In this chapter, the design of a 94-GHz SiGe BiCMOS phase inverter with variable gain amplifier is discussed. This circuit was fabricated on 0.13 μm gate length silicon germanium BiCMOS 8XP technology from GLOBALFOUNDRIES (formerly IBM's). This thesis work aimed to achieve constant gain single-bit 180° phase control and three-bit gain variation across all corners. All simulations and layout design were completed using Cadence software package.

8XP technology was at it's beta version when this circuit is designed. Foundry released many design kit updates during and after the design process. These updates on design kit models significantly affected the resulting performance, especially at 94 GHz. In this chapter, all simulations are given with latest design kit which is V.1.6.2.3 since foundry claims it is more accurate for representing hardware although the circuit is initally designed at V.1.6.1.0. This damages the effort of achieving first-time-right design, however it did not destroy completely.

3.1 Single-bit 180° Phase Control

In order to achieve a single-bit phase control, a switching structure can be implemented. By this structure, the input signal sees a low impedance at one branch, a high impedance at the other and tends to flow through low impedance one. Switching operation is usually done by PIN diodes, FET transistors or BJT transistors. There are different switch implementations named according to connection of switching elements such as series, shunt, series-shunt. Each of them has different advantages and disadvantages on parameters of switches mainly as insertion loss, isolation and bandwidth. In Fig. 3.1, a shunt configuration can be seen. When switching element is OFF, low impedance is transformed as high impedance to the input thanks to $\lambda/4$ transmission line and signal flows through the branch where the switching element is ON.

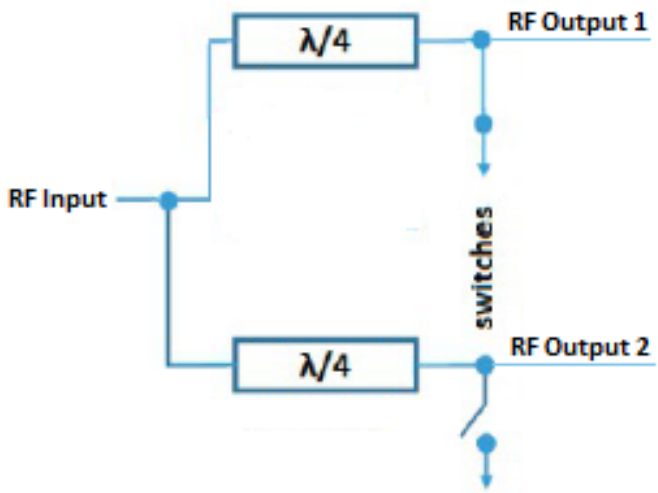

Figure 3.1: Shunt switching structure

This configuration provides good performance on insertion loss since there is no series element, good performance on isolation since it presents low impedance to output port of OFF branch. On the other hand, it has narrow bandwidth since $\lambda/4$ transmission line is defined at single frequency. Since there is no bandwidth requriement in our work, this configuration is selected.

In order to create the 180° phase difference between branches, two more $\lambda/4$ transmission lines are added to one of the branches as shown in Fig. 3.2. This addition won't change the impedance transformations of that branch since the length of total addition is $\lambda/2$ meaning a full rotation in Smith chart. Furthermore, since the addition is done at left side of switching elements and output side of branches are identical including switches, next block can be designed together with switches at both branches.

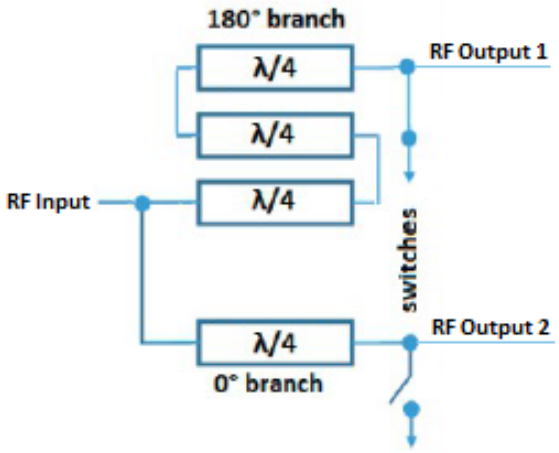

Figure 3.2: Shunt switching structure with additional $\lambda/4$ tlines

Main advantage of this technique is using a design kit elements. Other structures such as balun may also provide phase inversion however their performance is always questionable at these frequencies and even more questionable when package effects come into picture. The drawback is extra loss at longer branch due to requirement of travelling longer transmission line. According to simulations, difference is around 0.2 dB which can be considered as acceptable.

Although this theory sounds great in theory, it needs a slight modification. The 'short' state of switching elements is not perfectly short due to via inductances from transistor layers to signal layer and transistor parasitics at 94 GHz. s_{11} can be seen in Fig. 3.3 and 3.4 for a short switching element. Poor short is transformed to poor open at input and due to this desired high impedance at OFF branch can not be achieved.

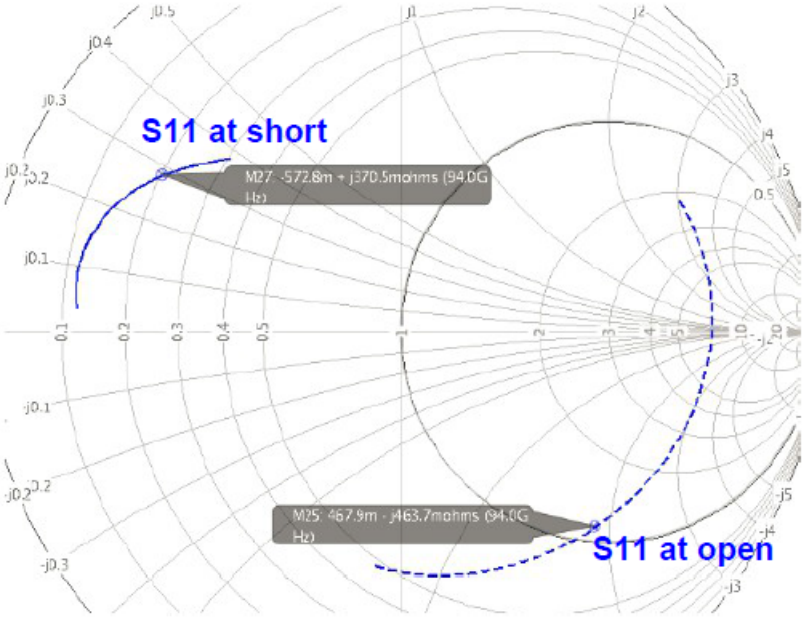

Figure 3.3: Short and open characteristics of 0° branch

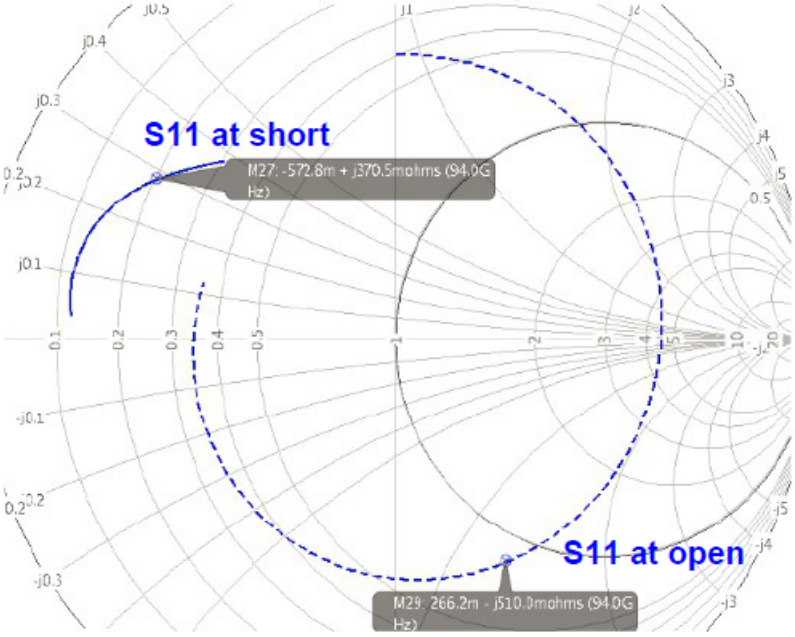

Figure 3.4: Short and open characteristics of 180° branch

To overcome this issue, a $\lambda/4$ transmission line from both branches are shortened to move poor short to a decent open. This length is represented as λ/common in Fig. 3.5. Note that, since one transformation is done by λ/common transmission line and the other is done by λ/common+ $\lambda/2$ transmission line, final s_{11} points are not exactly the same. In order to show similar high impedances for OFF branches in both switching cases, the common length was chosen to place the open impedances on both sides equidistant of the real axis. One can twist this selection in the favor of 180° branch since 0.2 dB additional loss is expected and our aim is to achieve constant gain at both branches. However, in order to be sure of this technique at 94 GHz, that twist is not done. Improved open at input when λ/common lines are used can be seen in Figs. 3.6 and 3.7 for both branches.

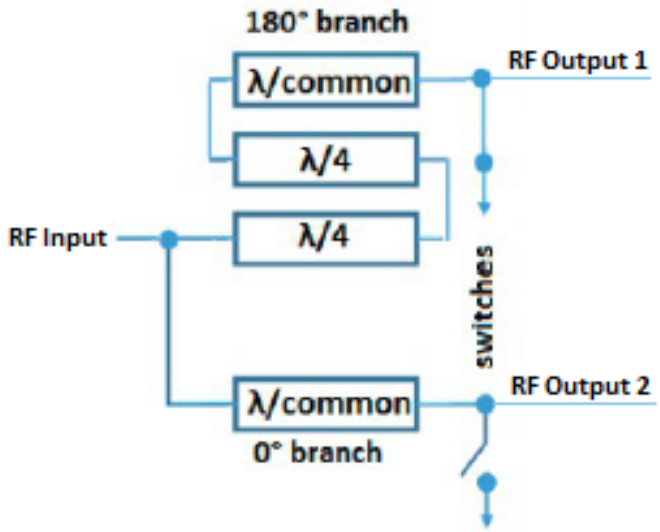

Figure 3.5: Shunt switching structure with additional λ/common tlines

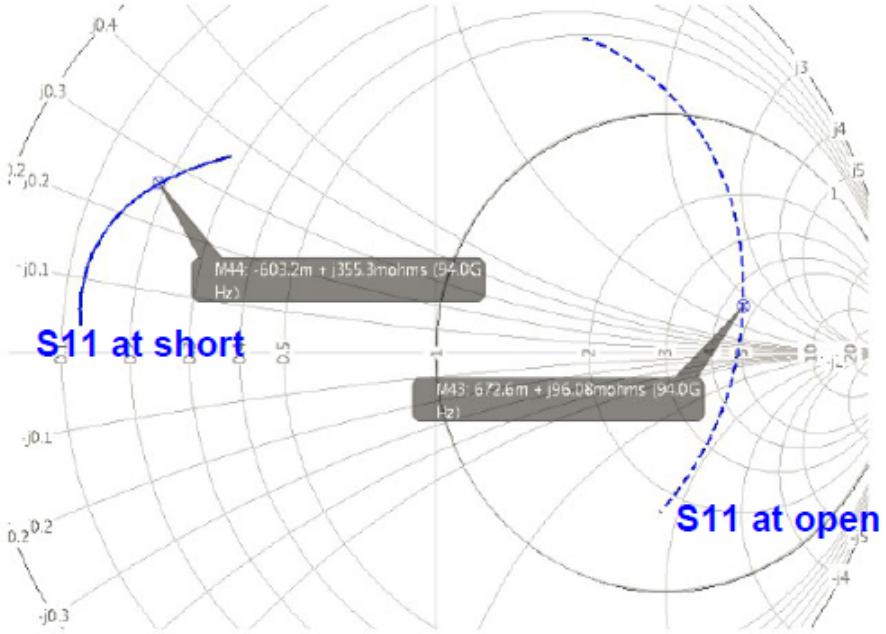

Figure 3.6: Short and improved open characteristics of 0° branch

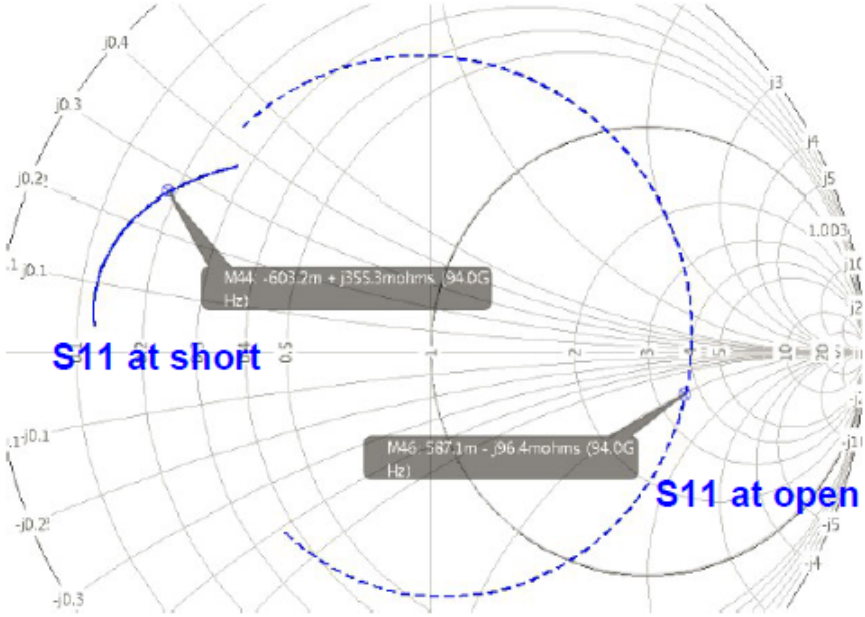

Figure 3.7: Short and improved open characteristics of 180° branch

3.2 Variable Gain Amplifier

Two identical variable gain amplifiers follow the switch that is described at previous section. Depending on which branch of the switch is active, the other variable gain amplifier is turned off with the same setting in order to prevent unnecessary power consumption. As it can be seen from Fig. 3.8, output matching circuit is shared by two branches since off cascode amplifier presents high impedance at its collector.

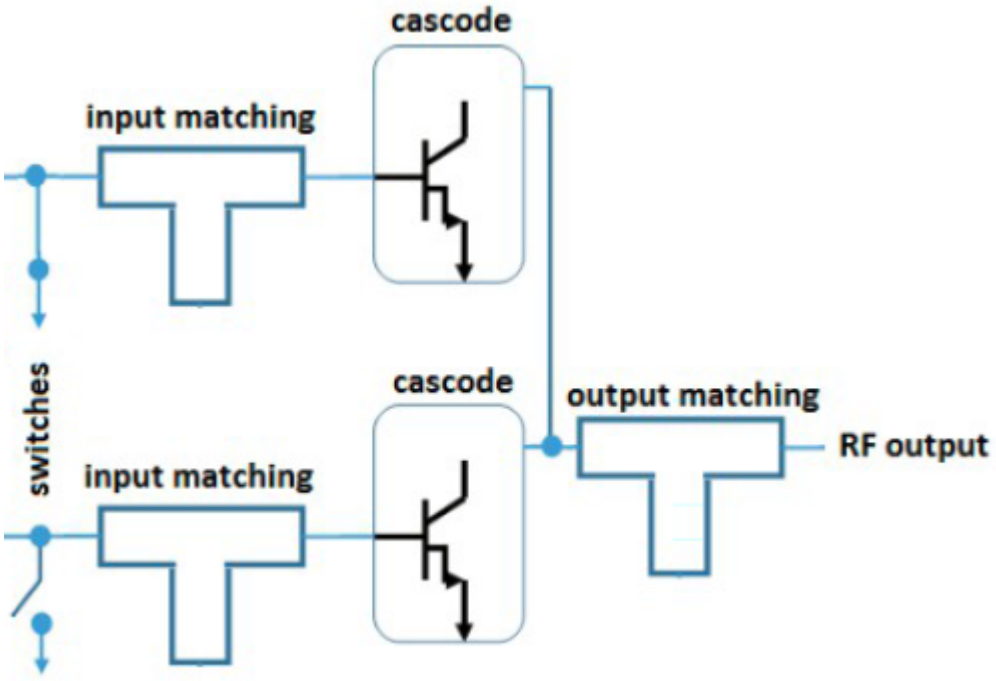

Figure 3.8: Two cascode variable gain amplifiers

In Fig. 3.9 s_{11}, s_{22} and s_{21} values of the circuit in Fig. 3.8 at 94 GHz can be seen. Note that the notch points of both s_{11} and s_{22} are shifted due to design kit updates although they are designed to be appear at exactly 94 GHz. Nevertheless, both reflections are still under -10 dB. Figure 3.10 shows these reflections on Smith chart.

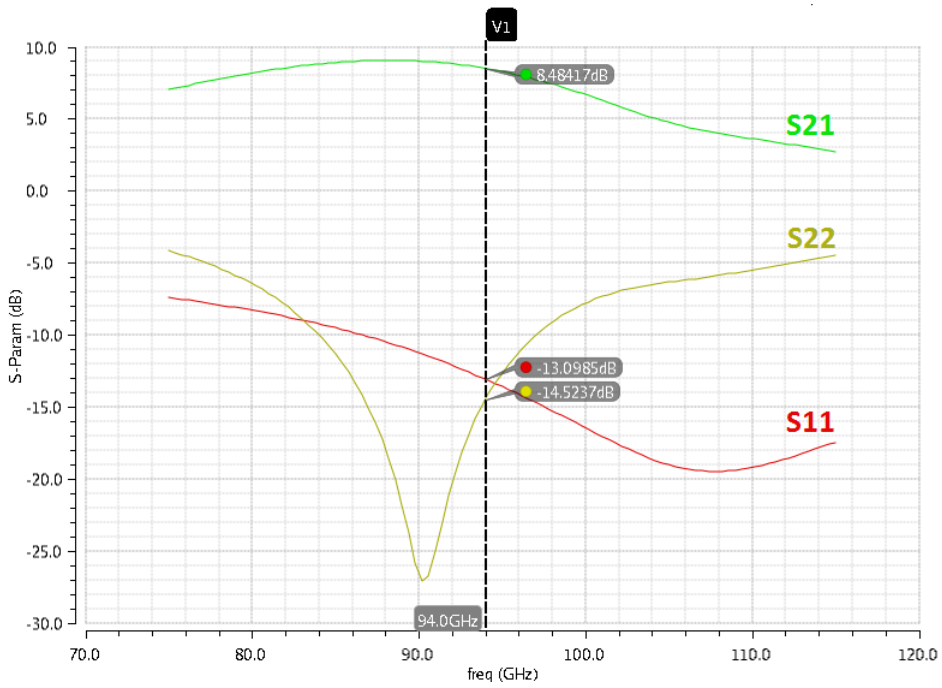

Figure 3.9: s_{11}, s_{21} and s_{22} plots of cascode gain amplifier at rectangular plot in dB

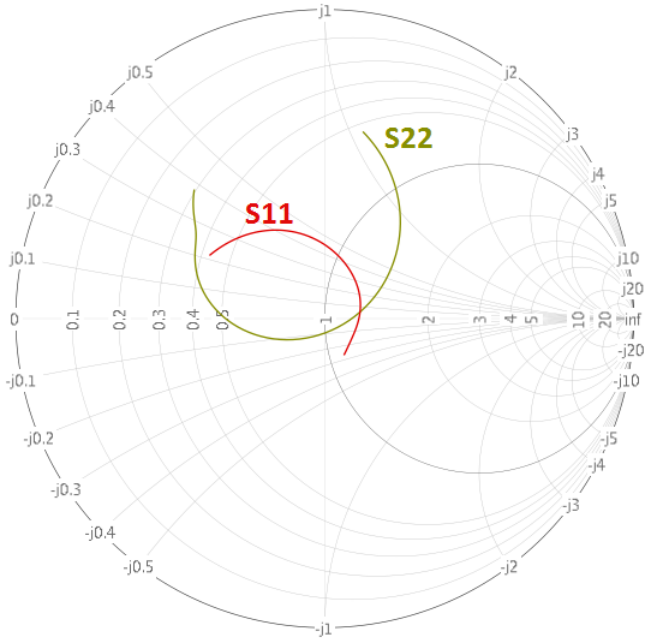

Figure 3.10: s_{11}, s_{22} plots of cascode gain amplifier at smith chart

3.2.1 Biasing and Varying the Gain

Variable gain operation is done by changing the biasing of the amplifier. Cascode gain amplifier is biased through a current mirror (a simple current mirror circuit is shown in Fig. 3.11) which takes 'reference current' and mirrors it with certain ratio to transistor at common-emitter configuration. Reference current is controllable as it can be seen in Fig. 3.12. It is also generated through current mirror which takes 'core reference current' from outside of the circuit. Current mirror bank consists of different sizes of transistors whose on and off states are determined by 3-bits of gain control setting. Thanks to that, constant core reference current is mirrored to reference current which is mirrored again to be used at cascode gain amplifier.

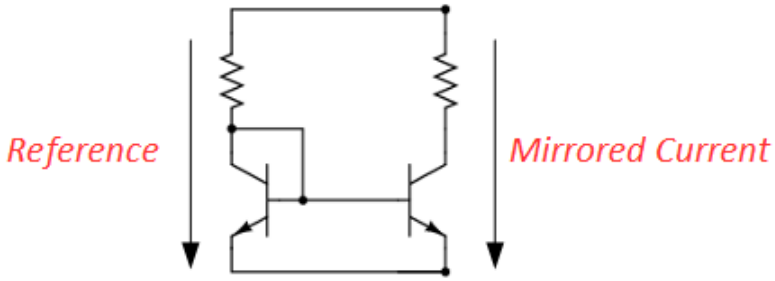

Figure 3.11: Current mirror schematic

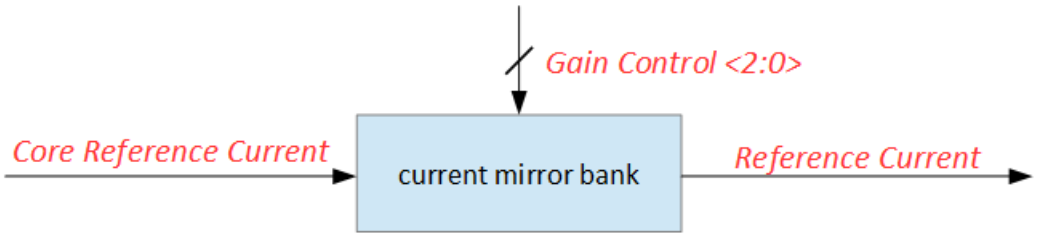

Figure 3.12: Block diagram of biasing

In Fig. 3.13, s_{21} in dB form can be seen according to 8 different possible settings. Gain varies from 5.44 dB to 8.48 dB.

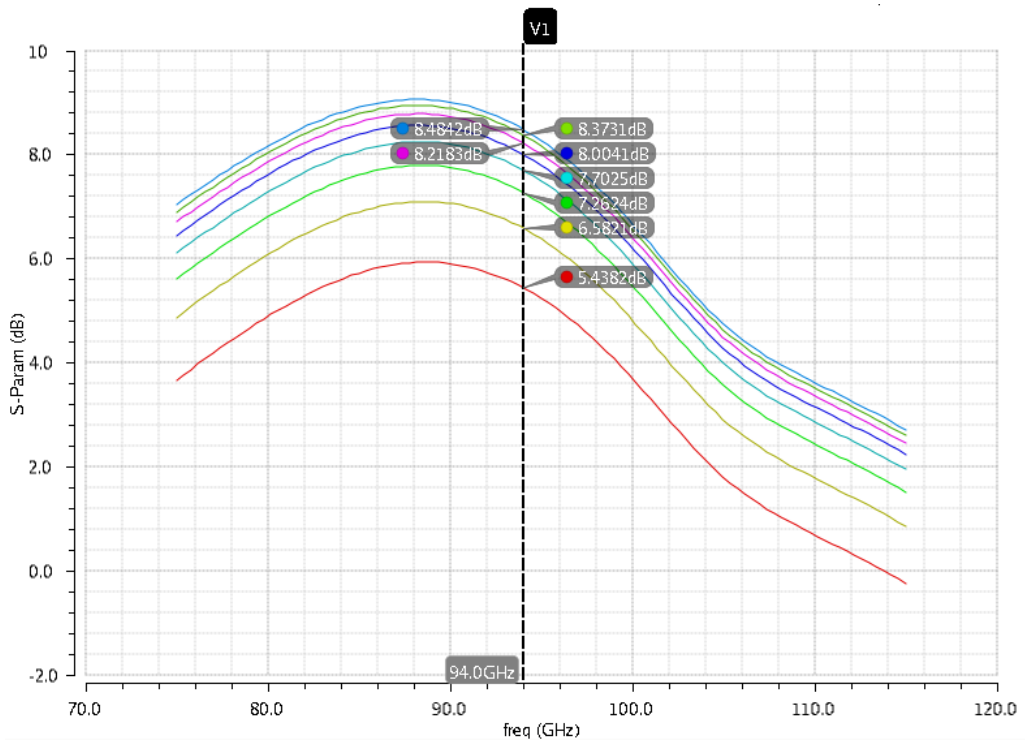

Figure 3.13: s_{11}, s_{22} plots of cascode gain amplifier at smith chart

3.3 Parasitic Modeling and Layout Considerations

Parasitic modeling is essential to achieve good correlation between software and hardware. As it is described before, after conventional schematic simulations, EM analysis, parasitic extraction and manual addition of parasitic inductances should be performed. In this thesis, there is not any region that requires EM analysis therefore that part is skipped. Secondly, surrounding areas of RF transistors are RC extracted as it can be seen from Fig. 3.14 (switch) and 3.15 (cascode gain amplifier). Finally, unmodeled horizontal and vertical interconnections are manually added as parasitic inductors and they are presented with yellow circles in Fig. 3.14 and 3.15.

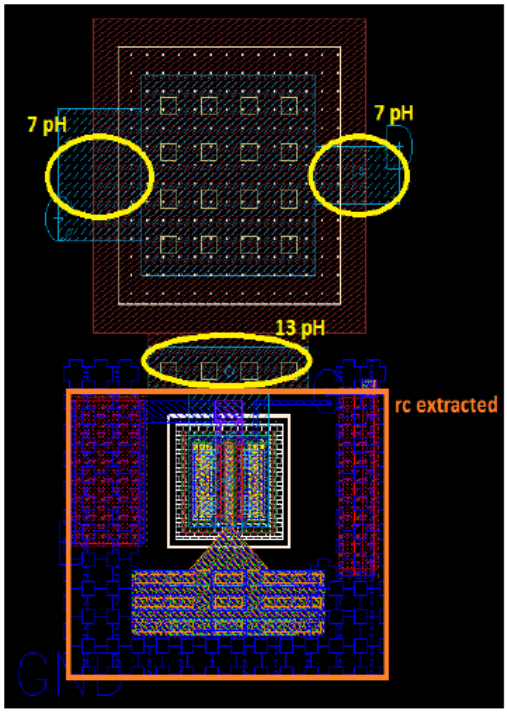

Figure 3.14: Parasitic modeling of switch

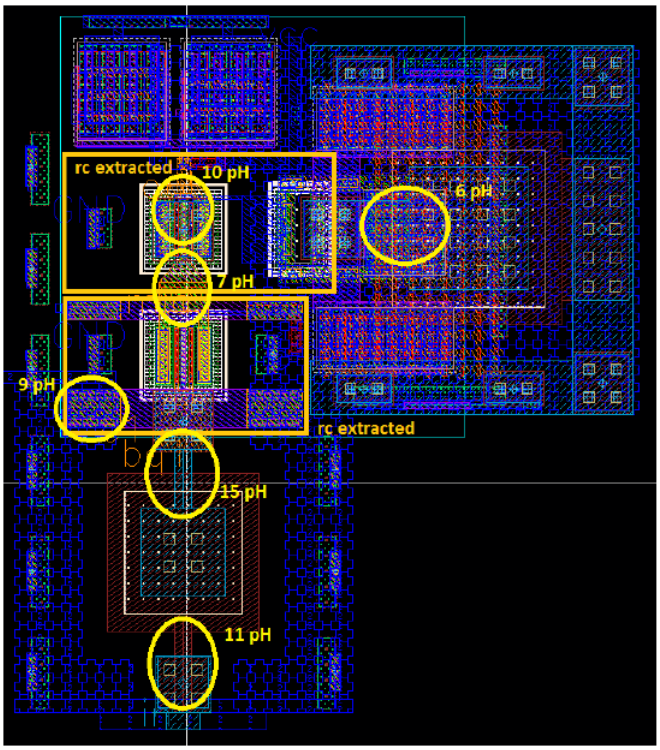

Figure 3.15: Parasitic modeling of layout

In simulations, it is observed that the overall performance is very sensitive to parasitic inductance at the base of common-base transistor of cascode amplifier. It is not possible to shorten that length since base of the transistor is at lowest metal layer while the capacitor is at upper layers. Having a long parasitic interconnect at that node might result in unpredicted results. Therefore, in order to reduce the inductance of vertical connection, that via is surrounded by grounded vias. Thanks to that approach, some kind of vertical transmission lines is formed and overall inductance at that point is reduced.

3.4 Simulation Results for Overall Circuit Across Corners

In this section, simulation results for overall circuit is presented. The block diagram can be seen in Fig. 3.16 which is combination of switching architecture and variable gain amplifier. The schematic and the layout of the circuit simulated are shown in Figs. 3.17 and 3.18, respectively.

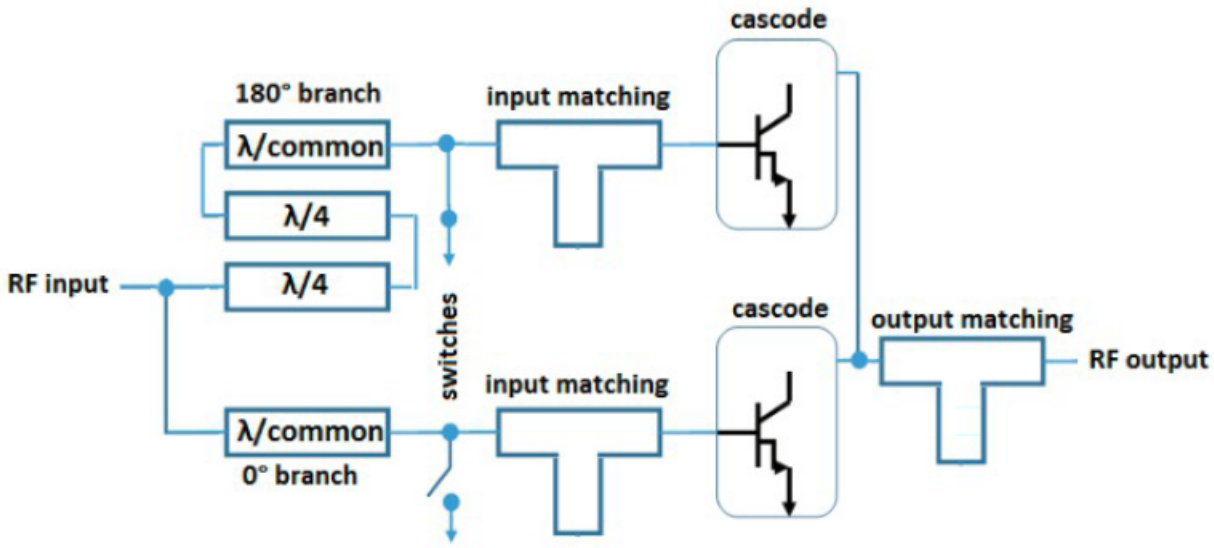

Figure 3.16: Block diagram of phase inverter-variable gain amplifier

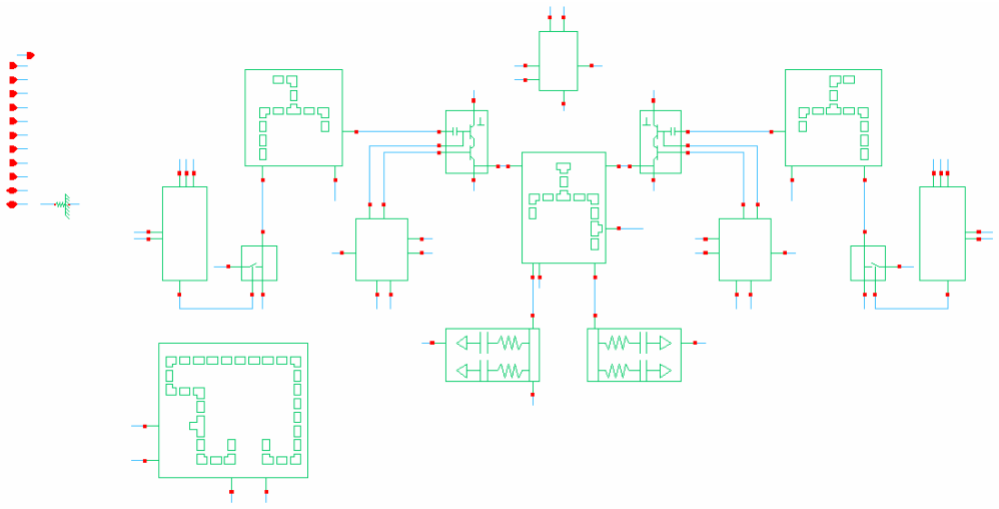

Figure 3.17: Schematic of the simulated circuit

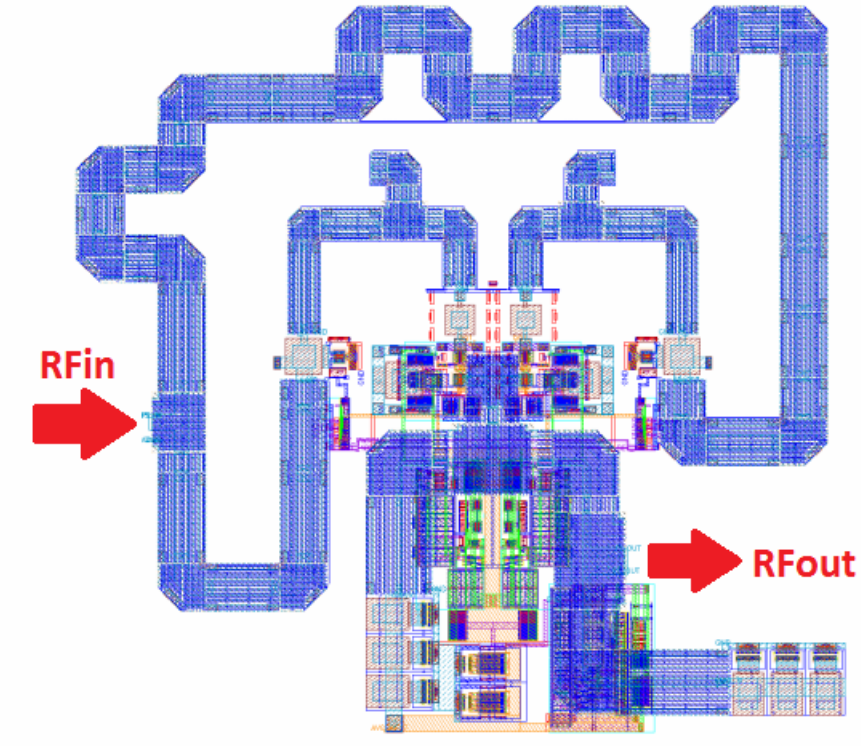

Figure 3.18: Layout of the simulated circuit

Three corners are defined for the simulations; nominal, slow and fast. Basically, slow corner consists of parameter changes that reduces the gain and vice versa for fast corner. Following parameters are adjusted from corner to corner;

- Temperature. As it is stated at [17], gain of a SiGe HBT decreases when the temperature increases if the base voltage is high due to so called Kirk effect. Since the base voltage of HBTs in this design is high enough, gain decreases with increased temperature. By ensuring slow and fast corner, operation between 0° and 85° is also ensured which covers possible real life conditions.

- Power supply. Lower power supply values result in less gain. By ensuring slow and fast corner, operation between 2.55 and 2.85 V is also ensured which covers possible fluctiations at DC supply.

- Device performance. This parameter is defined by foundry which tells the possible production variations on transistors. TT means typical, SS means slow, FF means fast.

Corner name	Nominal	Slow	Fast
Temperature (°C)	25	85	0
Power supply (V)	2.7	2.55	2.85
Device performance	TT	SS	FF

Table 3.1: Simulation corner definition

In what follows, S-parameter and P1 dB simulations are presented at nominal, slow and fast corners for minimum and maximum gain setting. Filled squares represent the 0° phase shift branch while empty circles represent the 180° phase shift branch. In Table 3.2, whole results are represented together.

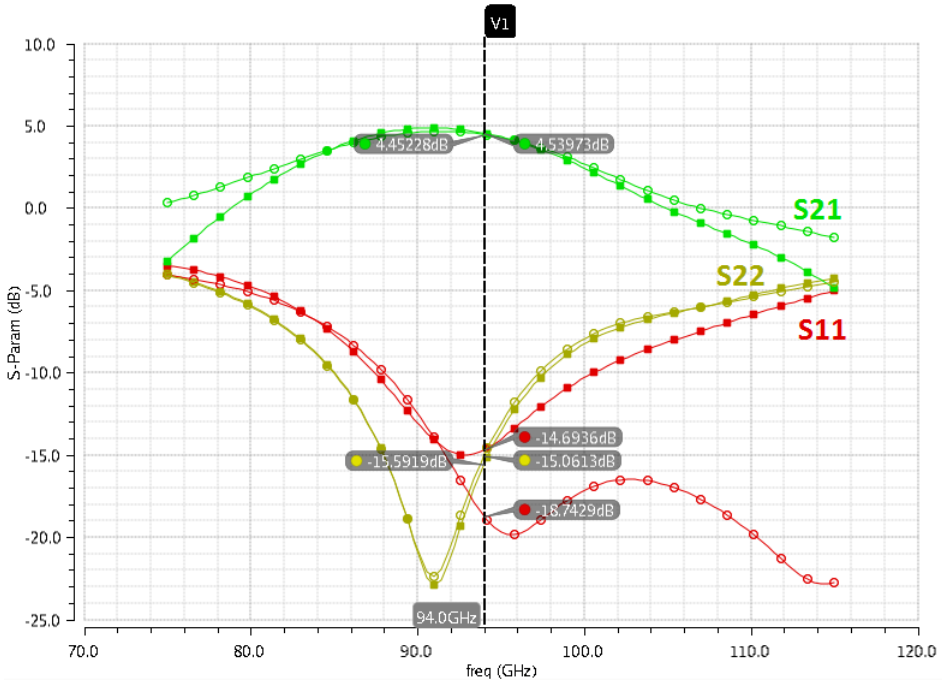

Figure 3.19: Nominal corner, min. gain setting, s-parameters

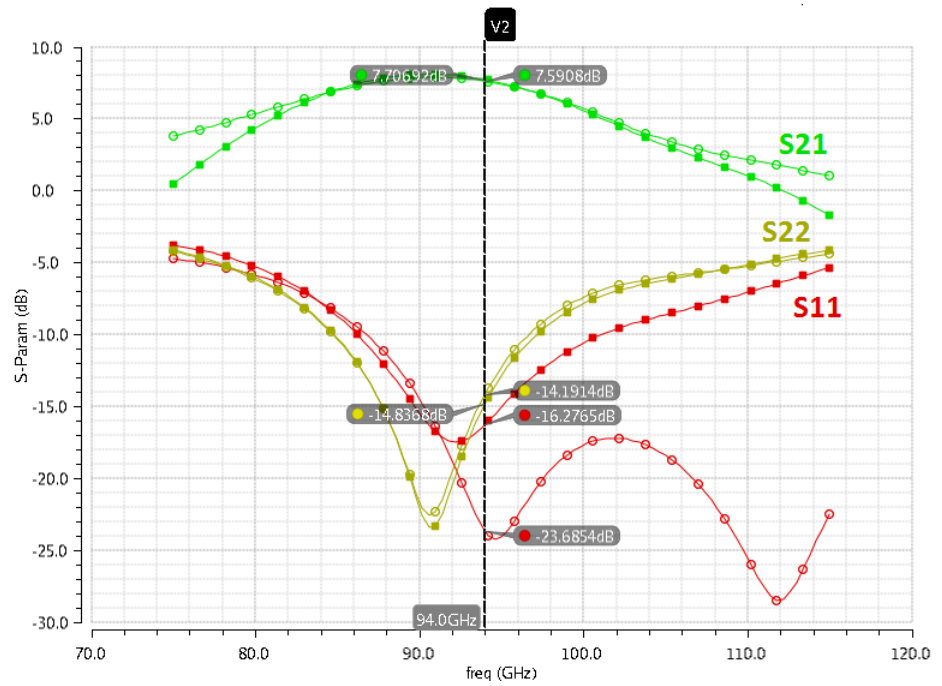

Figure 3.20: Nominal corner, max. gain setting, s-parameters

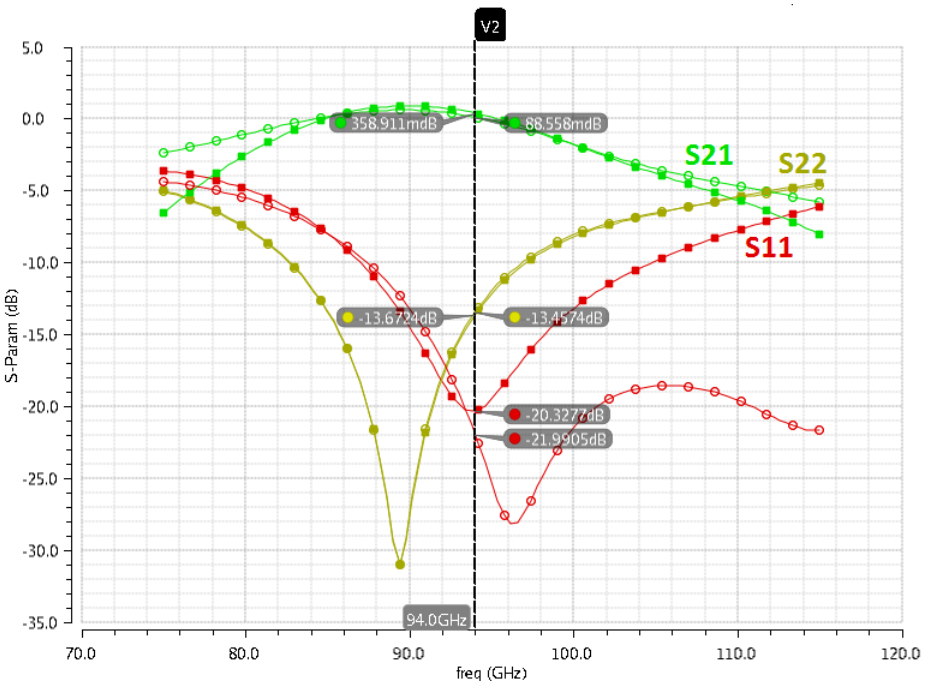

Figure 3.21: Slow corner, min. gain setting, s-parameters

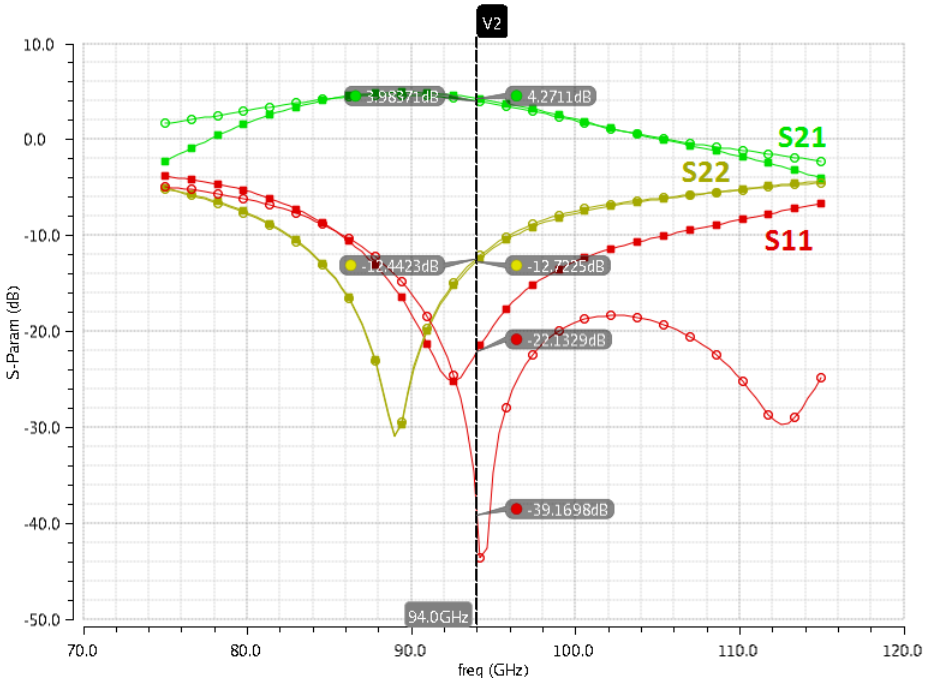

Figure 3.22: Slow corner, max. gain setting, s-parameters

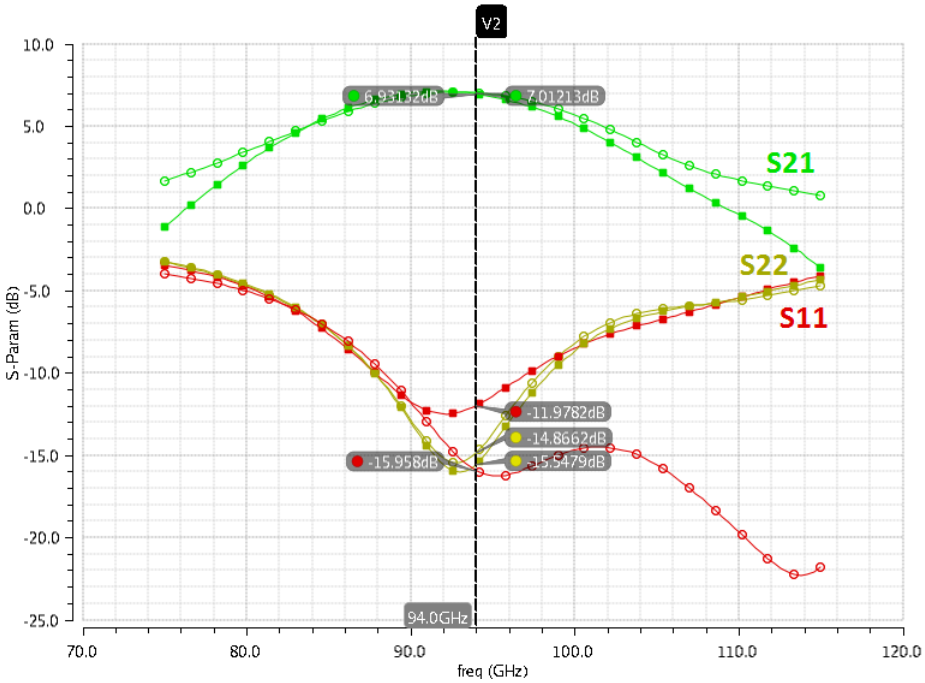

Figure 3.23: Fast corner, min. gain setting, s-parameters

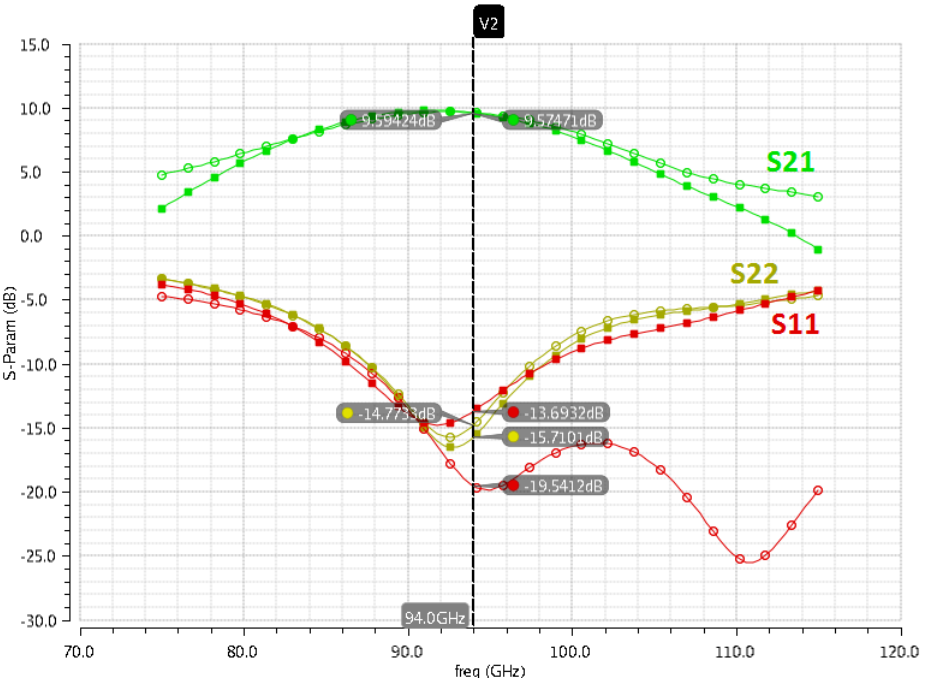

Figure 3.24: Fast corner, max. gain setting, s-parameters

Corner	Gain	PI Setting	s_{21} (dB)	s_{11} (dB)	s_{22} (dB)	P1dB (dBm)
Nominal	Min.	0	4.54	−14.69	−15.59	−6.81
Nominal	Min.	180	4.45	−18.74	−15.06	−6.96
Nominal	Max.	0	7.71	−16.28	−14.84	1.41
Nominal	Max.	180	7.59	−23.69	−14.19	1.40
Slow	Min.	0	0.36	−20.33	−13.67	−8.93
Slow	Min.	180	0.09	−21.99	−13.46	−9.39
Slow	Max.	0	4.27	−22.13	−12.72	−0.27
Slow	Max.	180	3.98	−39.17	−12.44	−0.44
Fast	Min.	0	7.01	−11.98	−15.55	−3.60
Fast	Min.	180	6.93	−15.96	−14.87	−4.42
Fast	Max.	0	9.57	−13.69	−15.71	2.15
Fast	Max.	180	9.59	−19.54	−14.77	2.11

Table 3.2: S-parameters and P1dB simulation results at 94 GHz

Chapter 4

Measurement

4.1 Setup

Measurement setup consists of the blocks that are given in Table 4.1. The diagram of setup can be seen in Fig. 4.1. This setup can perform the small-signal measurement from 10 MHz to 110 GHz.

Model	Explanation	Quantity
Agilent N5227A	Vector Network Analyzer	1
Agilent N5261A	mm-wave Head Controller	1
Agilent N5260-60013	mm-wave Head Module for Freq. Extension	2
Agilent N6700B	Low - Profile MPS Mainframe	1
SHF DCB-100B	DC Block	2
GORE CX0AB0ABC20.0	1mm. cable	2
GGB 110H-GSG-100-P-W	RF Probe (GSG)	2
GGB MCW-25-2487-1	DC Probe (PPGPPGPP)	1

Table 4.1: Blocks at measurement setup

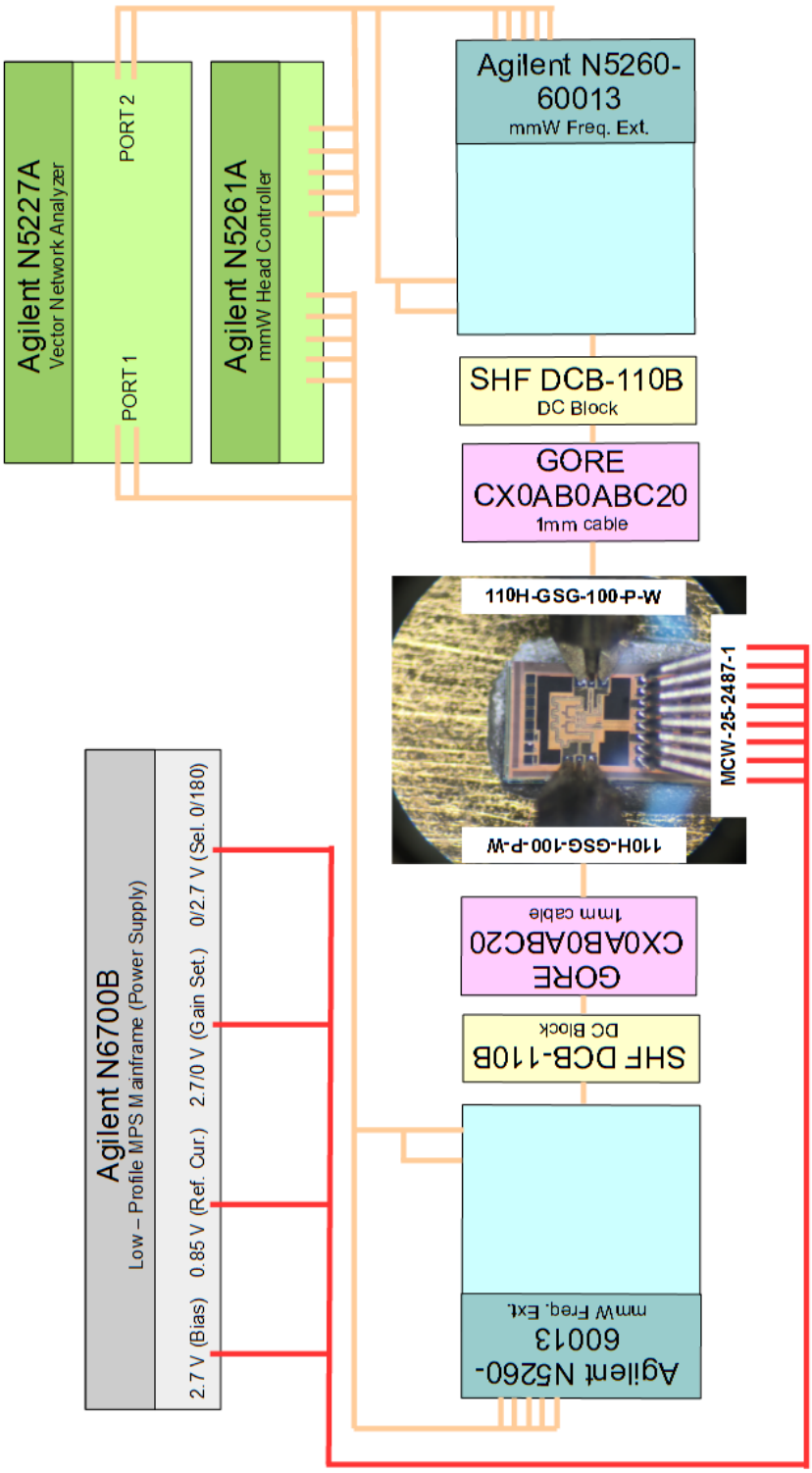

Figure 4.1: Block diagram of measurement setup

Working procedure is as follows; The network analyzer is capable of generating signals up to 67 GHz, therefore another structure is needed for frequencies above. When the frequency is below 67 GHz, network analyzer operates as there is no head modules and controller. When frequency exceeds 67 GHz, higher frequencies are generated at head modules by frequency multiplication controlled by head controller. Network analyzer, head module and head controller is a mm-wave setup solution priovided by Agilent Technologies up to 110 GHz. Generated signal passes through DC block and 1 mm. cable which are both capable of handling 94 GHz signal and presented to chip through GSG (ground-signal-ground) probe (west). The RF probe can be seen in Fig. 4.2 (a). At the output port of the circuit (east) the same RF components are presented.

DC power is supplied from MPS (modular power system) mainframe. It has four outputs; 2.7 V for bias, 0.85 V for generating 50 μA reference current, 0 or 2.7 V for minimizing or maximizing gain setting (3 bits are avaliable for gain setting, they are all connected to this port), 0 or 2.7 V for selecting phase. They are all connected to chip from south side through PPGPPGPP probe (6 power pads; bias, reference current, 3 settings of gain, selecting phase) (P represents power, G stands for ground). The DC probe can be seen in Fig. 4.2 (b).

Calibration of probes is done on the calibration set provided by Picoprobe given in Fig. 4.3. SOLT (short-open-load-through) calibration is completed from 90 to 98 GHz with 200 Hz IF bandwidth.

In Fig. 4.4, the picture of the measured circuit can be seen. Note that on top of the layout given in Fig. 3.18, it has extra pads and transmission lines to pads to land appropriate probes. Produced chips are diced by foundry and glued to the copper carrier using thermal epoxy.

In Fig. 4.5, overall setup is presented. This setup is newly built at ASELSAN-REHIS and it is also used for different circuits/measurements therefore it has other blocks around it to perform different measurements.

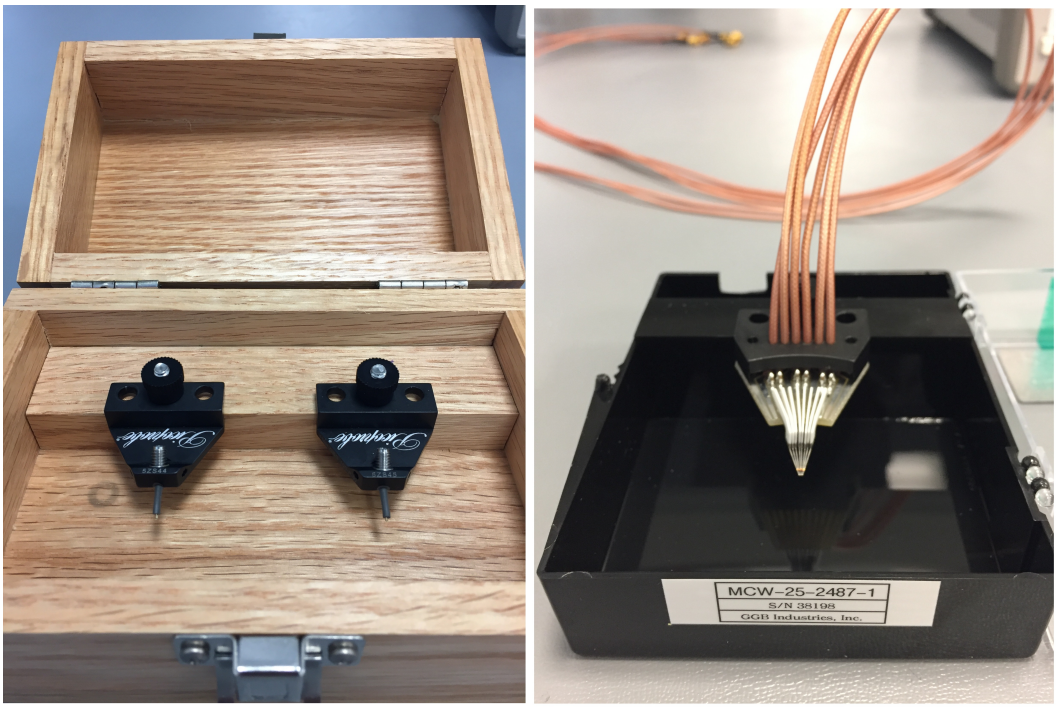

Figure 4.2: RF Probes at left (a), DC probe at right (b)

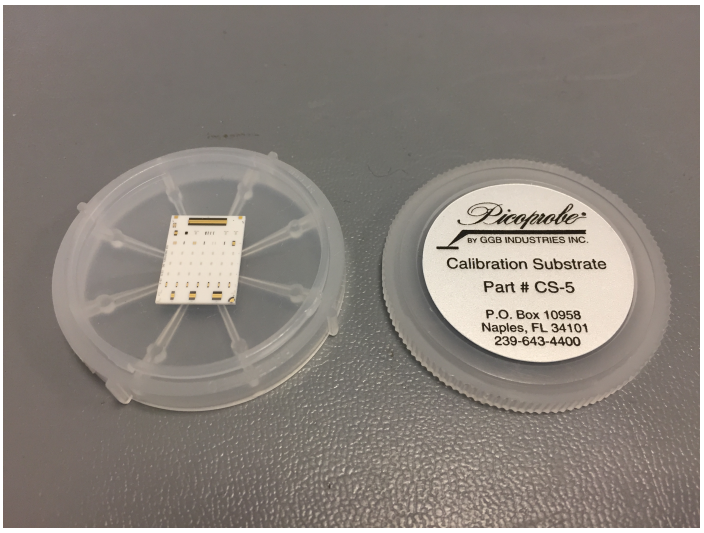

Figure 4.3: CS-5 calibration kit

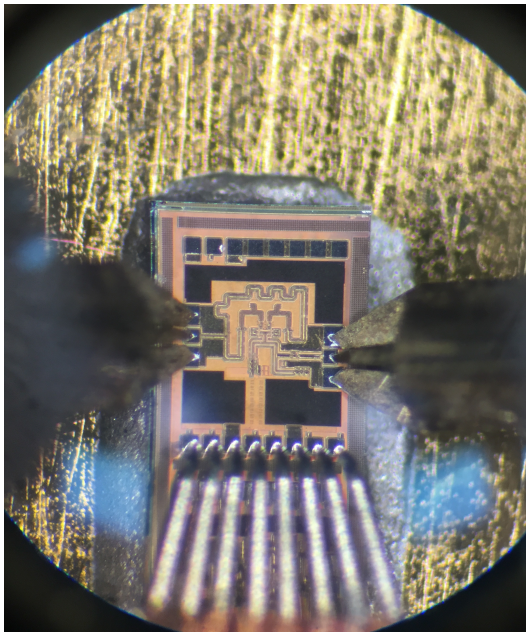

Figure 4.4: Probes are landing on IC

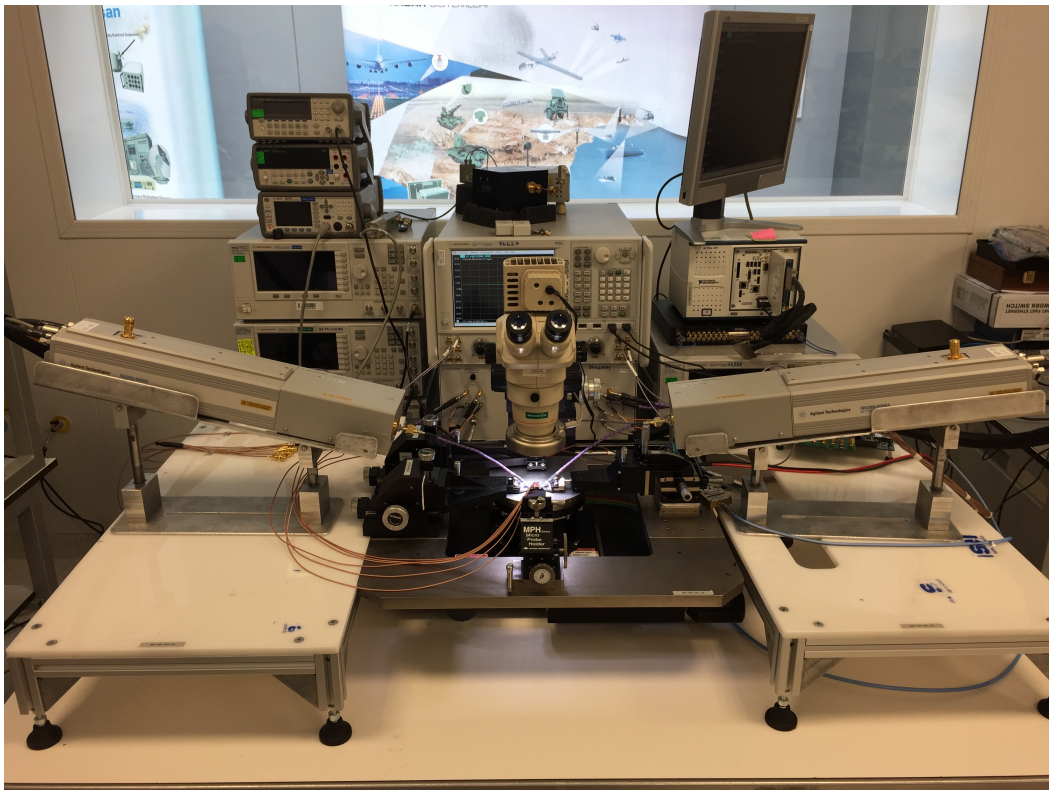

Figure 4.5: 94 GHz setup

4.2 Measurement Results

Remember that all of the simulation results given at Chapter 3 are done with the circuit which has the layout in Fig. 4.6(a). This circuit can be called as "Core PI-VGA" since it is going to be integrated to higher scale IC and it has to provide certain features such as decent input and output return losses. However, in order to make this circuit measurable, pads for probe landing and additional transmission lines to those pads are necessary. Eventually, these additions mainly change the input and output return losses since the pads introduce significant capacitance at 94 GHz. In Fig. 4.6, layouts of simulated and measured circuits can be seen. In Fig. 4.7 simulation results of core PI-VGA, in Fig. 4.8 simulation results of measured circuit are given at nominal corner, maximum gain. Note that as in Chapter 3, the shapes of small-signal results are similar with some shifting behaviors among corners and gain/phase settings therefore only one of the corners at one setting is shown to give the main idea.

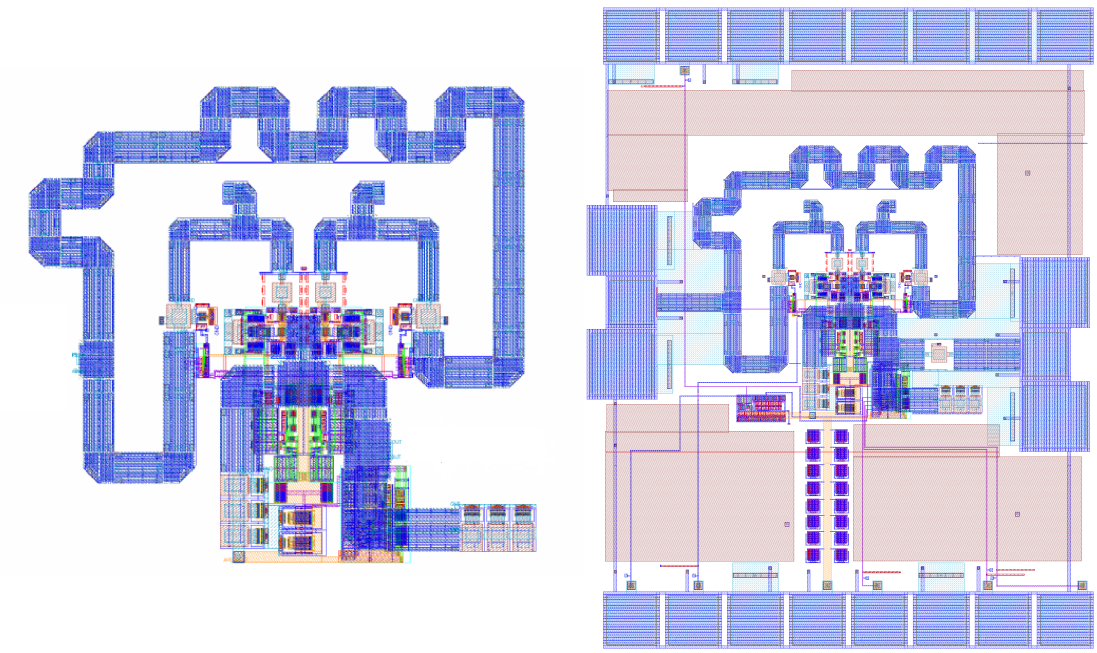

Figure 4.6: Core PI-VGA at right (a), measured circuit (b)

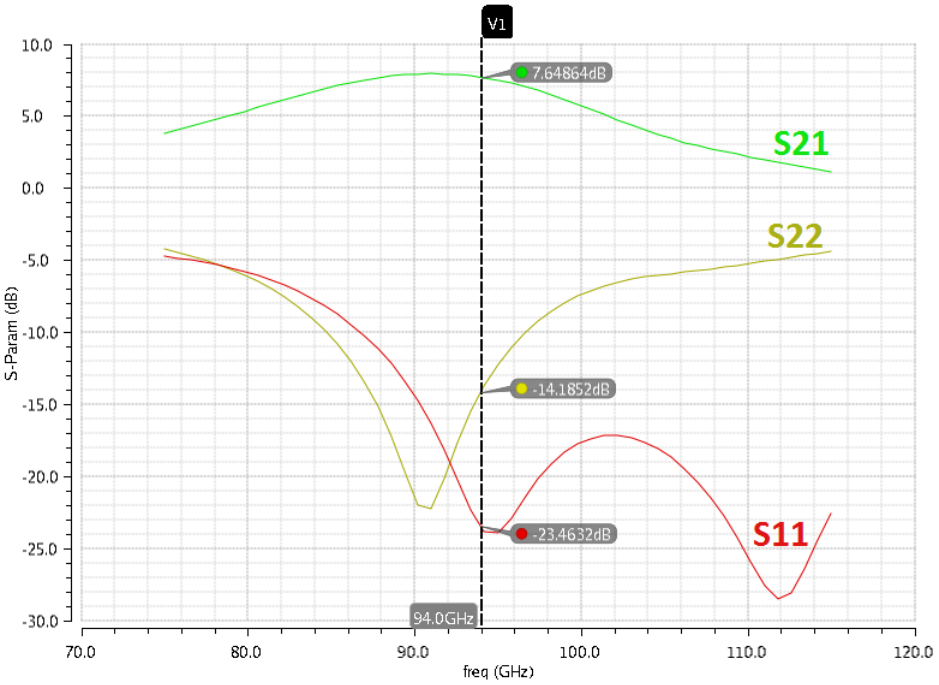

Figure 4.7: Simulation results of core PI-VGA

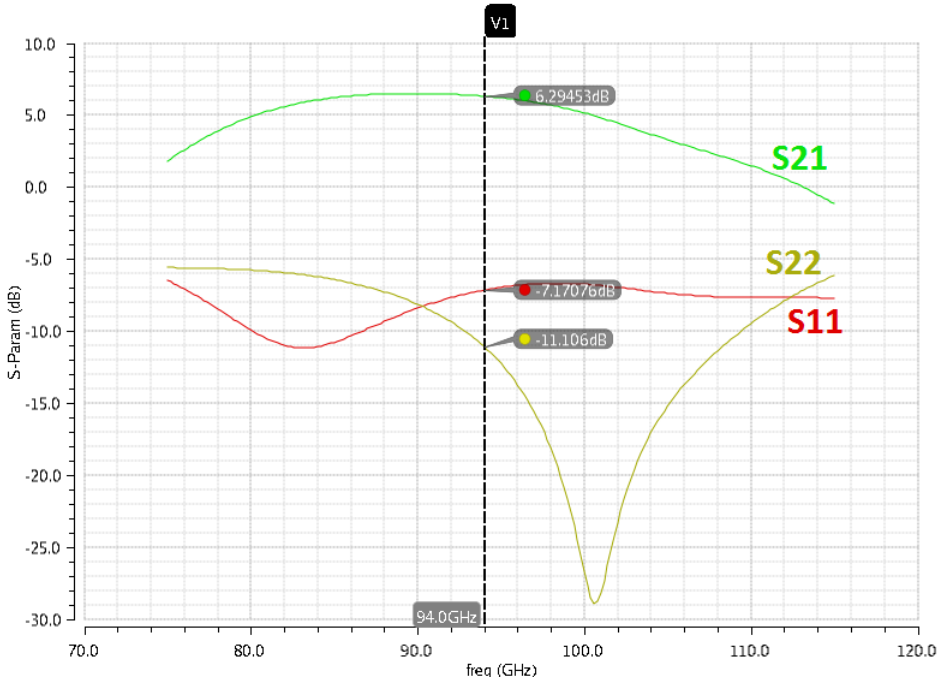

Figure 4.8: Simulation results of measured circuit

Two samples of phase inverter-variable gain amplifier are measured. Their results at 94 GHz are presented at table 4.2.

IC Number	Gain	PI Setting	s_{21} (dB)	s_{11} (dB)	s_{22} (dB)	Phase (°)
1	Min.	0	4.33	−10.49	−17.45	121.94
1	Min.	180	4.00	−10.27	−18.85	−62.39
1	Max.	0	6.84	−10.62	−15.90	117.05
1	Max.	180	7.01	−10.16	−17.44	−67.21
2	Min.	0	4.13	−10.63	−18.22	120.71
2	Min.	180	3.90	−10.44	−19.52	−63.39
2	Max.	0	6.76	−10.66	−16.42	115.72
2	Max.	180	7.02	−10.25	−17.90	−68.27

Table 4.2: Measurement results of two samples

Results above show that PI-VGA works as expected in terms of its most important parameters;

- Phase. For the same sample and gain setting, inverting the phase bit creates a phase difference very close to 180° (it is 184° approximately). This shows that, phase model of $\lambda/2$ transmission line is accurate and 4 degrees can be considered as tolerable. In addition to that, for the same sample and phase setting, minimizing and maximizing the gain creates a phase difference around 5 degrees. If the overall phased array system is considered, this value is acceptable and will not create huge errors at beam directions. Therefore, one can use the variable gain amplifier for tapering purposes safely.

- s_{21} (dB). According to simulation results given at table 3.2, the gain results map somewhere between nominal and slow corner, closer to the nominal. Also the gain difference between minimum and maximum settings is consistent with simulation result which shows that circuit is capable of performing gain adjustment.

In Fig. 4.9, the small-signal analysis of simulation and measurement of two samples from 90 to 98 GHz are shown together where boxes represent the simulation, circles and crosses represent the measurement of two samples. From this figure it can be understood that;

- Results of two samples are very close to each other. This increases the confidence on measurement results.
- s_{21} values match with around 0.5 dB error which is at acceptable level.
- s_{11} values are also close but seem better at measurement (from around -7.2 dB to -10.6 dB).
- s_{22} values show that the frequency of notch is shifted significantly however it turns out that return losses at measurement are better (from around -11.1 dB to 16 dB).

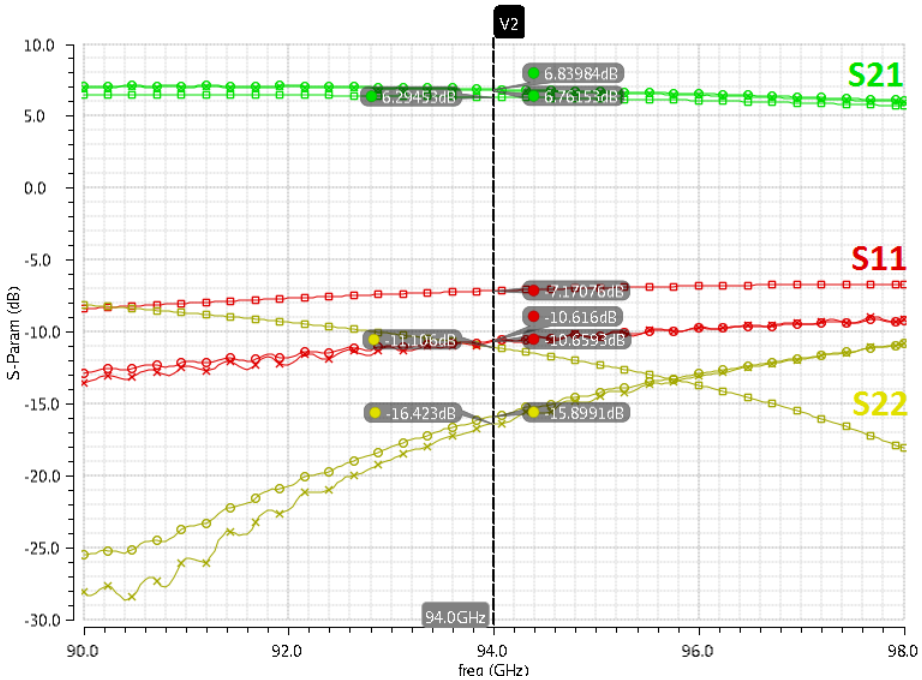

Figure 4.9: Comparison of small-signal analysis of simulation and measurement of two samples from 90 to 98 GHz

Chapter 5

Conclusion and Future Work

In this work, a 94 GHz phase inverter-variable gain amplifier is designed to be used in a 94 GHz phased array structure. Considering the difficulty of a constant gain-360° phase shifter at these frequencies, this circuit is considered to provide constant gain and single bit 180° phase control. Some tapering range is desired to be included since gain of indiviual front ends will be adjusted according to desired beam direction at system level.

Circuit is designed at 8XP technology of GLOBALFOUNDRIES, since it is mainly designed to be used in 94 GHz recevier and transmitter ICs at that technology. During the design, design kit models are tried to be used as much as possible and custom structures are avoided. Nevertheless, some areas at layout couldn't be modeled with design kit such as transistor connections to upper layers, therefore careful parasitic extractions and estimation of parasitic inductances are performed. Overall design is optimized to provide decent gain, input and output return losses at three corners defined.

After the design is completed, in order to measure the circuit at probe station, additional pads and transmission lines are added. Small signal measurements are performed at given setup from 90 to 98 GHz. Measurement results show that circuit operates well in terms of single bit 180° phase shifting, gain values and gain tapering. It also provides good input and output return loss, while the notch

of output return loss is shifted.

As a future work, that shift at output return loss can be investigated. The possible candidate is the modeling of the base of common-base transistor at cascode structure. The reason of it is, that node was sensitive on simulations and a small error at modeling may end up with effecting the circuit. Also, since the shape of s_{11} is somewhat consistent between simulation and measurement while the shape of the s_{22} is not, the problem could be near to the output.

In this thesis, I tried to present not only the circuit but also the important points to pay attention at a mm-wave design. I hope other students can benefit from this thesis in the future if they want to enter this area.

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