X-BAND CPW HIGH POWER AMPLIFIER DESIGN BY GAN BASED MMIC TECHNOLOGY

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By
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We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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The developments in defense industry, telecommunication and satellite systems have gradually increased the necessities for the small and compact Power Amplifiers (PAs) with high output powers and gains. Monolithic Microwave Integrated Circuits (MMICs), that are fabricated by using Gallium Nitride (GaN) on Silicon Carbide (SiC) substrate, achieve the system requirements. GaN based MMIC technology gives chance to produce high power capable and compact PAs. Moreover, suitable Wilkinson Power Dividers (WPDs) with low Insertion Loss (IL) assist in transferring output power of the device with combining MMIC PAs. Presented designs in this thesis work have been fabricated in Bilkent University NANOTAM with GaN on SiC process. Fabricated X-band Coplanar Waveguide (CPW) PA works from 7.9 GHz to 8.4 GHz as intended and its efficiency equals to 40 % at 8.4 GHz under 2.1 dB compression. Measurements of fabricated PA show that output power of the device is equal to 37.8 dBm under 2.1 dB compression and it has 9.8 dB minimum gain in the operating band. Furthermore, equal, three-way WPD device was designed and fabricated with the same process and it works at wide-band range with approximately 0.9 dB IL. It is advantageous that the total dimension of paralleled MMIC PAs can be adjusted by scaling branches of the designed WPD with the aim of performance optimization.

Keywords: Power Amplifier, MMIC, Wilkinson Power Divider, CPW, GaN.

ÖZET

GAN TABANLI MMIC TEKNOLOJİSİ KULLANILARAK X-BANTTA YÜKSEK GÜÇLÜ YÜKSELTEÇ TASARIMI

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Günden güne gelişmekte olan savunma sanayi, telekomünikasyon ve uydu sistemleri; küçük, yekpare ve yüksek güçlü yükselteçlere (PAs) duyulan ihtiyacı arttırmaktadır. Üretimi Silicon Karbit (SiC) üzerine Galyum Nitrat (GaN) alttaşı kullanılarak yapılan, monolitik mikrodalga entegre devre (MMIC) teknolojisi, sanayi ve sistem gereksinimlerini sağlamaktadır. GaN temelli MMIC teknolojisi sayesinde yüksek güce dayanıklı ve kompakt güç yükselteçleri üretilmektedir. Ayrıca uygun ve az kayıplı Wilkinson güç bölücüleri (WPDs) kullanılarak birleştirilen MMIC güç yükselteçleriyle üretilen cihazdan daha fazla çıkış gücü elde edilebilinmektedir. Bunlardan dolayı, bu tez çalışmasında sunulan tasarımlar Bilkent Üniversitesi NANOTAM'da, SiC üzerine GaN işlemiyle üretilmiştir. Eş düzlemli dalga kılavuzu (CPW) yapılarıyla X bandında üretilen güç yükselteçleri, beklenildiği gibi 7.9 GHz - 8.4 GHz aralığında çalışabilmekte olup, 2.1 dB kazanç sıkıştırılması altında % 40 verimliliğe sahiptir. Üretilen güç yükselteçlerinin ölçümlerine göre, 8.4 GHz frekansında, güç yükseltecinin çıkış gücü, 2.1 dB kazanç sıkıştırılması uygulandığında, 37.8 dBm seviyesinde olup, minimum 9.8 dB kazanca sahiptir. Ek olarak, eşit üç kollu WPD tasarımının üretimi aynı üretim prosesiyle gerçekleştirilmiştir ve geniş band aralığında yaklaşık 0.9 dB ek kayıpla (IL) çalışmaktadır. WPD kollarının uzatılıp, kısaltılmasına rağmen güzel bir performans göstermesi; çoklanan MMIC PA'ların toplam boyutunun, WPD kollarının uzunluklarının ayarlanmasıyla, değişiyor olması, avantaj sağlamaktadır.

Anahtar sözcükler: Güç Yükselteci, MMIC, Wilkinson Güç Bölücü , CPW, GaN.

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Chapter 1

Introduction

After long researches on Silicon Semiconductor Technology, the first transistor was discovered in 1947 by John Bardeen and Walter Brattain at Bell Labs [1]. This active component has been used with passive components without any extra wire or connection materials due to developments of semiconductor technology at the earliest 1960's and these solid structures have been called as MMICs by researchers [2]. In 1979, the first PAs were notified and after some improvements on output power, MMIC technology has been started to be in use for PAs [3]. In addition, the advantages of GaN material have been used since 1990 because manufactured PAs based on GaN transistors have relatively high output power, high breakdown voltage and low Radio Frequency (RF) loss [4, 5, 6].

In consideration of MMIC PAs' developments, this thesis introduces a design of X-Band CPW High Power Amplifier (HPA) by GaN based MMIC Technology. This work was done in order to achieve goals which were specified by a government institution. Achieved goals are minimum 9 dB gain and minimum 5 W output power in the operating frequency from 7.9 GHz to 8.4 GHz. Additionally, designed MMIC PA chip size was minimized. Different X-Band MMIC PA designs are placed in the literature. Designed PAs have 4 W output power with output harmonic injection and 6 W output power with power recycling, respectively [7, 8]. However, Dani [7] and Michael [8] do not present manufactured MMIC PA

chip size and their designs work about at 10 GHz. In this thesis, designed MMIC PA's size equals to 2 mm x 4 mm and manufactured device works from 7.9 GHz to 8.4 GHz. Additional structures are not designed to increase output power of MMIC PA because of size limitations.

Design requirements and steps are presented in detail throughout this study. Initially, background and theoretical information about PAs and their classifications (including DC bias conditions) are briefly mentioned. After this short introduction to PAs, design steps of both PA and WPD are explained according to the necessities of MMIC technology, fabrication techniques and limitations by using Advanced Design System (ADS) momentum, which is a 2.5 dimension electromagnetic simulator [9]. Additionally, design of an equal, three-way WPD is presented. After finishing PA and WPD design analyses, mask preparation and fabrication process are evaluated. Finally, performances of manufactured devices are discussed according to indicated measurement techniques. In addition, simulation results will be compared with measured data.

In Chapter 2, general information about RF PAs are mentioned and different class properties are analyzed in detail with formulations and figures by taking into consideration the linearity and the efficiency cases.

In Chapter 3, High Electron Mobility Transistor (HEMT) characterization techniques, including DC-IV measurements, small signal and large signal measurements and MMIC fabrication process, are mentioned after explanations of MMIC technology with its milestones. Then, design considerations and steps are presented via ADS simulations. Moreover, layout and photo-mask design are specified as the last steps before production. Finally, measurements are explained in detail with the comparison of simulation results and measurements. At that point, benchmarking studies on passive elements are performed to show the fabrication accuracy.

In Chapter 4, firstly, introduction about basic properties of WPDs is presented. Then, design steps, including optimization and meandering of objects, are explained in detail. After recording scattering parameters of fabricated WPDs,

measurements are compared with simulation results.

This thesis is ended with the conclusion chapter. In that chapter, final inferences of this study and future work are presented with possible new achievements, designs and findings.

Chapter 2

Power Amplifiers

2.1 Introduction to RF Power Amplifiers

In modern world, the significance of military technologies and telecommunication equipments has been gradually rising. Therefore, lots of countries pay close attention to radars, antennas, and satellite systems. PAs play a crucial role in operation of these devices and systems. The main purpose to use PAs is to increase the signal amplitudes [10]. Besides output power levels, the nonlinearity and the efficiency are important terms that should be considered. If a PA operates in nonlinear region instead of linear region, gain compression is seen at the output of RF PA and available gain goes down [10].

Most of RF devices and systems are designed to achieve high efficiency and good linearity at the same time. If the efficiency of the device is adequately increased, its cost goes down, its performance increases and its life cycle gets longer [10]. However, there is a trade-off between efficiency of the device and the linearity. With increasing efficiency, RF PA moves away from its linear region [10]. As a result, RF PA designers should be aware of this trade-off and carefully analyze the system requirements.

Amplifiers, that are composed of transistors, are activated by DC voltages/currents and amplified RF signal is observed at the output. Furthermore, input and output matching circuits directly affect output RF signal amplitude and characteristic. Therefore, one of the most important design step is to properly construct matching circuits. Finally, after adding direct current (DC) bias networks and RF connectors or RF probe pads for MMIC PAs, amplifier structure is completed. According to DC bias points, output RF signal amplitude and characteristic, output power performance and available gain, amplifiers can be classified as variable gain, linear power, buffer, saturated high-power, and high-efficiency amplifiers [11].

Other important design parameters are gain and large signal characterization of transistors, stability of PA and selecting appropriate DC bias points according to specified amplifier class. These design parameters are analyzed in next chapters in detail.

2.2 Power Amplifier Classes

PA design requirements have been evolved with developments in the technology. Initially, based on the given design requirements, appropriate DC condition for transistor biasing and input/output matching circuits should be determined. If amplifier is designed for microwave frequencies, it can be basically classified as class A, class AB, clas B, and class C based on initial characterization parameters. In addition, E, F and J classes are not analyzed in this work because they operate in relatively nonlinear region. Class A design structure has been generally used for small signal amplifiers and other classes have been used to design HPAs. Although designers have started to classify PAs according to their output waveforms and required measurement techniques; Power Added Efficiency (PAE), stability, gain, bandwidth, linearity, and output power terms also play a significant role in classification of PAs. These terms are directly related to chosen drain/gate currents and input/output impedances [10, 11].

While PA classes' names are changing from A to C in alphabetical order, the linearity of PA reduces and its efficiency increases. Class A operation provides microwave engineers to design easy and linear PA circuits. However, it has low efficiency comparing to other classes. Therefore, class AB operation was discovered to overcome the efficiency disadvantage. However, linearity problems arise in class AB operation. In class AB operation transistor does not spend power continuously in one period, it stays off-state for small time intervals in each period and starts to work more nonlinearly than class A operation [10]. On the other hand, despite its low linearity, class B operation might be preferred rather than class AB in terms of high efficiency of class B. Finally, among these classes, class C has the best efficiency in spite of its very poor linearity characteristic.

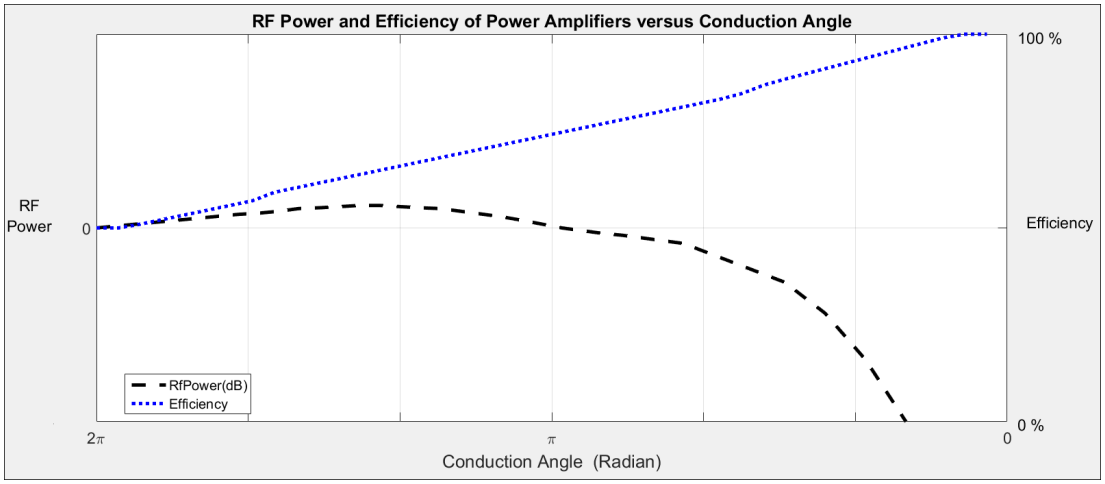

Figure 2.1: RF Power and Efficiency change as a function of Conduction Angle

The RF power and the efficiency change as a function of conduction angle are presented in Figure 2.1 [10, 12]. In Figure 2.1, the efficiency increases from 50 % to 100 %, when conduction angle decreases from 2π to 0. With conduction angle decrease from 2π to 0, RF power decreases too, and class properties of PA changes starting from class A till class C in an alphabetical order [10, 12]. Detailed information about conduction angle are given in next three subsections. As a result, specifying the operation classes of PAs is related to transistor DC biasing condition and the rest of parameter effects such as characterization of transistors and RF performance of the circuit.

2.2.1 Class A Amplifiers

The class A amplifiers always operate in linear region. They just amplify the given input signal that can be observed without any distortion at the output of amplifiers. Used transistors remain open permanently for a full cycle, i.e., conduction angle changing from 0 to 2π, and half of the maximum current is applied to transistor for activating it. Moreover, transistors' loads should be matched properly for obtaining maximum power at the output of designed PA. If the source and the load sides of the transistor are conjugately matched, the PA has high gain and very good reflection performance [10, 11].

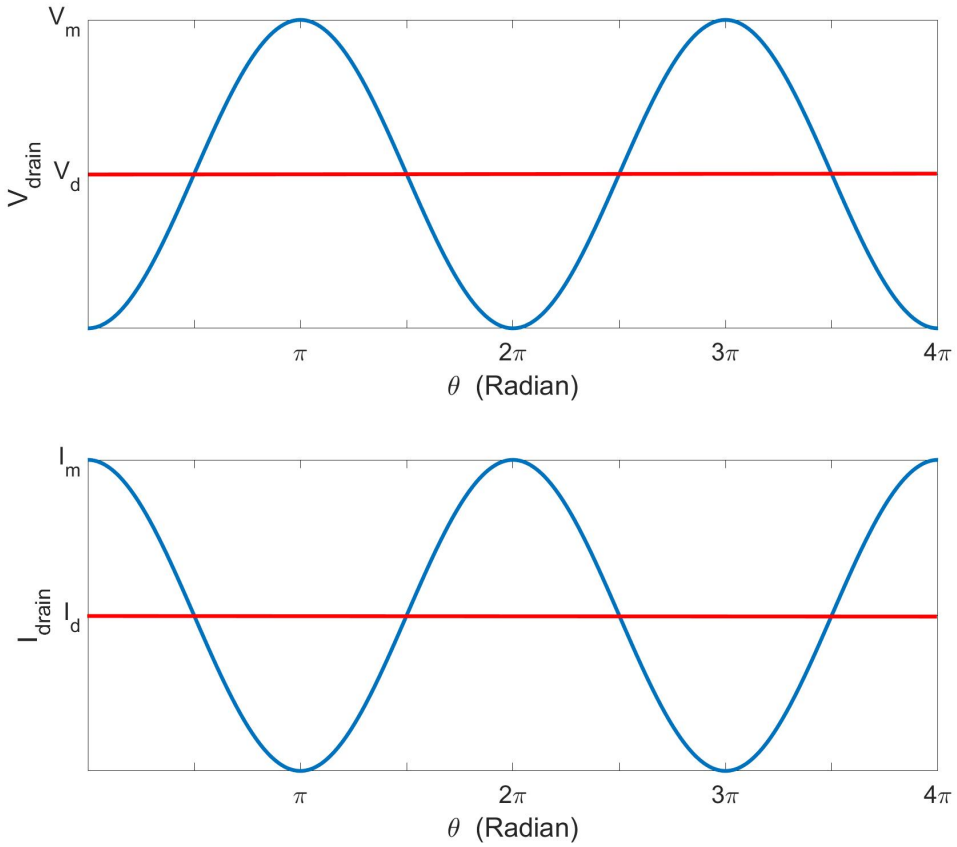

Figure 2.2: Class A Amplifier Waveforms

The conventional class A amplifier's drain voltage and drain current waveforms are seen in Figure 2.2 [10]. V_m and I_m indicate maximum drain voltage and maximum drain current values, respectively. On the other hand, V_d and I_d correspond to average DC-drain values. The ratio of the output power to input DC power can be estimated from the waveform of class A amplifier. By this way, efficiency of the amplifier can be directly calculated [10].

General mathematical formulas for computing the efficiency and PAE of an amplifier are given in Eqs. from (2.1) to (2.7), in which knee voltage is placed on. After a certain source voltage, transistors start to operate in saturation region, where current remains constant despite voltage increases. This voltage transition point between linear and saturation regions is called as knee voltage [10, 13]. Knee voltage can be observed from DC-IV graph of a transistor and it equals to voltage value corresponding to the maximum current point on the graph.

Furthermore, voltage, current and power relations of an RF signal are given below together with the efficiency calculations [10, 11, 13, 14].

$$V_{rms} = \frac{V_{peak}}{\sqrt{2}} = \frac{V_{peak-to-peak}}{2\sqrt{2}} \tag{2.1}$$

$$I_{rms} = \frac{I_{peak}}{\sqrt{2}} = \frac{I_{peak-to-peak}}{2\sqrt{2}} \tag{2.2}$$

$$P_{out} = \frac{I_m}{2\sqrt{2}}\frac{V_m}{2\sqrt{2}} = \frac{I_d}{\sqrt{2}}\frac{V_d}{\sqrt{2}} = \frac{I_d V_d}{2} \tag{2.3}$$

$$P_{out_2} = \frac{I_d(V_d - V_{knee})}{2} \Rightarrow \lim_{V_{knee}\to 0} P_{out_2} = P_{out} \tag{2.4}$$

$$P_{dc} = I_d V_d \tag{2.5}$$

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{\frac{I_d V_d}{2}}{I_d V_d} = 0.5 = 50\,\% \tag{2.6}$$

$$\eta_{Power-Added-Efficiency} = \frac{P_{out} - P_{in}}{P_{dc}} \tag{2.7}$$

Knee voltage term is added to Eq. (2.3) and it is accepted zero in ideal case to be used in subsequent equations. Thus, the efficiency and PAE calculations are done according to ideal case. However, if transistor's additional losses, which can be defined as knee voltage restriction, are taken into consideration, the output power and the efficiency reduce proportionally [11, 15]. In addition, knee voltage can be altered from device to device and effects of it can be reduced by increasing the output impedance of the transistor [16].

As a result, with Eqs. from (2.1) to (2.7) the efficiency of a transistor is found. Notice that in Eq. (2.7), PAE only depends on input power and the efficiency of class A amplifier, is 50 % if there is no additional loss.

2.2.2 Class AB and B Amplifiers

Properties of class A amplifiers were briefly analyzed in the previous subsection together with the other classes including class B, class AB and class C amplifiers. According to Steve [12], conduction angles of class A and class B amplifiers equal to 360° and 180°, respectively. On the other hand, conduction angle takes a value between 360° and 180° for class AB amplifiers.

The basic changes for these classes occur with reducing the DC current, which is applied to the drain of the device. This variation can be achieved in HEMT devices by decreasing the level of device's gate voltage [10].

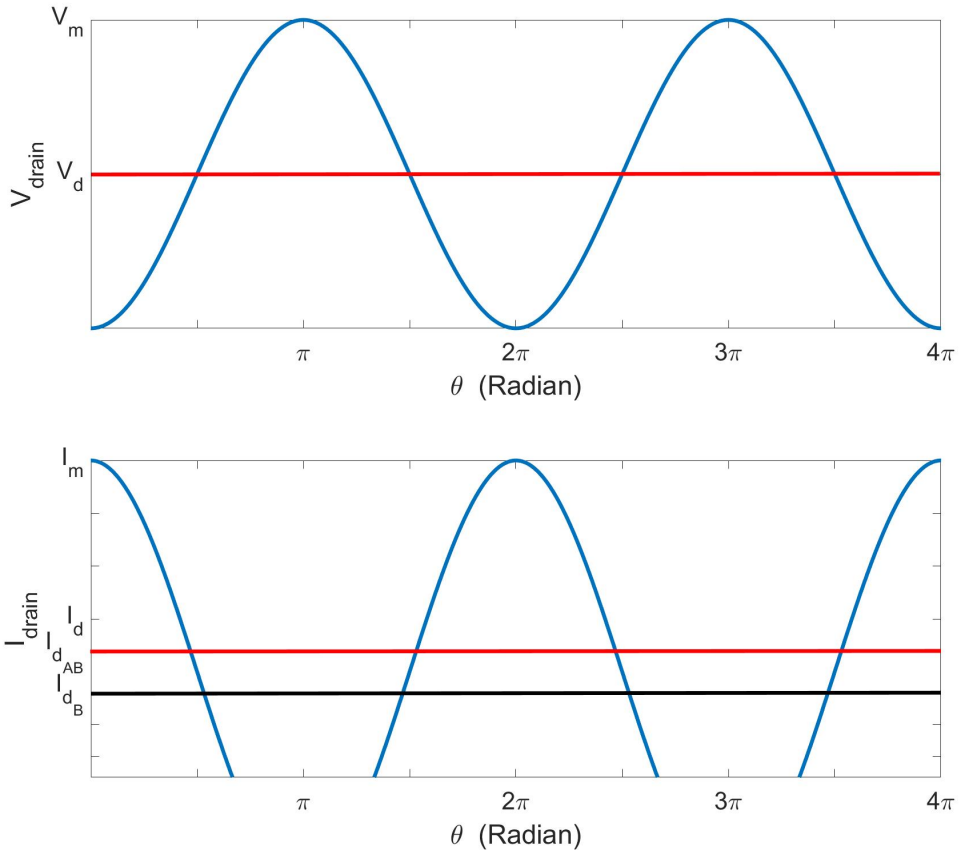

Figure 2.3: Waveforms for Class AB & B Amplifiers

The drain voltage waveform of class AB and B amplifiers are the same with that of class A as it is clearly seen in Figure 2.3 [10]. Additionally, drain current amplitude of class B is a little bit smaller than that of class AB [10].

Eqs. from (2.3) to (2.9) are rearranged according to Bahl [11]. These equations are given below.

$$P_{out} = \frac{I_m}{2\sqrt{2}}\frac{V_m}{2\sqrt{2}} = \frac{I_m}{2\sqrt{2}}\frac{V_d}{\sqrt{2}} = \frac{I_m V_d}{4} \tag{2.8}$$

$$P_{dc} = I_{d_B} V_d = \frac{I_m V_d}{\pi} \tag{2.9}$$

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{\frac{I_m V_d}{4}}{\frac{I_m V_d}{\pi}} = \frac{\pi}{4} = 78.5\,\% \tag{2.10}$$

As a result, it is clear that the efficiency of class B amplifier is 78.5 % (Eq. (2.10)). Additionally, Figures 2.2 and 2.3 [10] show that the efficiency of class AB amplifier is between 50 % and 78.5 %, which is in proportion with conduction angle, because drain current of class AB is between drain current values of class A and B amplifiers.

2.2.3 Class C Amplifiers

Finally, class C amplifiers are briefly mentioned in this subsection. Basic formulas for amplifiers' classifications have been given in the previous subsections. Hence, class C is presented result-oriented.

Class C devices basically work in nonlinear region, their efficiencies directly converges to 100 % in proportion to reduction of conduction angle. Therefore, the linearity vanishes [11, 12]. According to Steve [12], conduction angle of class C amplifiers takes a value between 180° and 0°. Waveform graphs of class C amplifiers are approximately the same with class AB and B waveforms as can be seen in Figure 2.3 [10]. Considerable decrease in drain current of class C is observed comparing to that of other classes and voltage supply problems are become more significant because of short conduction angle and input power related issues [10].

Chapter 3

X-Band Class AB MMIC Power Amplifier Design

3.1 MMIC Technology

Towards the end of 20th century, MMIC technology has been preferred in PA designs because of developments in fabrication of semiconductor material and newly invented device topologies. All active devices (transistors) and passive components (capacitors, inductors and resistors), that are used in RF circuits, can be constructed on a substrate simultaneously with utilizing metals, dielectric and resistive materials in one piece. These materials are compulsory for MMICs fabrication. Furthermore, production cost for each integrated circuit has been decreasing because more than one circuit can be manufactured with a single fabrication run on a single wafer [13].

Different types of semiconductor materials have been used as a substrate material. Choosing the substrate depends on the type of RF device, frequency range of the design and other requirements like gain, power, and so on. At this juncture, Gallium Arsenide, Gallium Nitride on Silicon Carbide, Silicon, Silicon on Sapphire, and Indium Phosphate can be used for the MMICs [13].

Additionally, properties of materials, which are conductivity, permittivity, permeability and resistivity, in MMIC fabrication have been determined according to product line abilities and required circuitry. Usually, gold is used as a conductive material for capacitors, inductors, ground planes and TLINs. Secondly, high relative permittivity and very low loss dielectric materials like Silicon Dioxide and Silicon Nitride are used for capacitors. Finally, suitable resistive materials are chosen [13].

3.2 Characterization of HEMT Devices

Design and analysis of transistors as active devices are significant for the PAs. In this respect, HEMTs have been chosen for this study because RF characteristics of HEMTs are very deterministic for PA behaviors and give adequate chance to estimate final RF results of designed PA. From these points of view, information about DC, small-signal and large-signal characterization of HEMT devices are given in this section. Moreover, the same fabrication process and fabrication steps are used for manufacturing both HEMTs and MMICs.

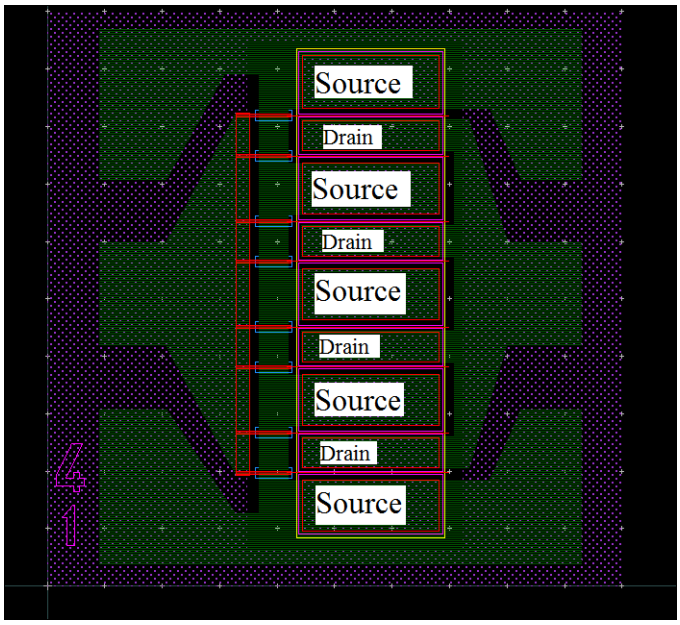

Figure 3.1: A transistor layout from top view

Before characterization information, physical properties and especially dimensions should be shortly presented. A transistor layout from top view that has been used in this study, can be seen in Figure 3.1. The transistor model is called 8x125. Source to drain distance (SDD) is 3 μm and gate widths equal to 125 μm. When SDD increases, maximum available gain decreases and transistor output power goes up. SDD limits the maximum voltage that can be applied between drain and source fingers. Moreover, approximate drain and source active area dimensions are $120x25$ μm^2 and $120x45$ μm^2, respectively. These dimensions are

related to desired frequency band.

Current density, transconductance, breakdown performance, gate leakage flow and pinch-off voltage are determined during DC measurements of HEMT devices, which are performed with B1505A Power Device Analyzer on a probe station. Measurement setup is illustrated in Figure 3.2. Drain and gate voltages are applied to device with a needle and a standard GSG (Ground-Source-Ground) DC probe, respectively.

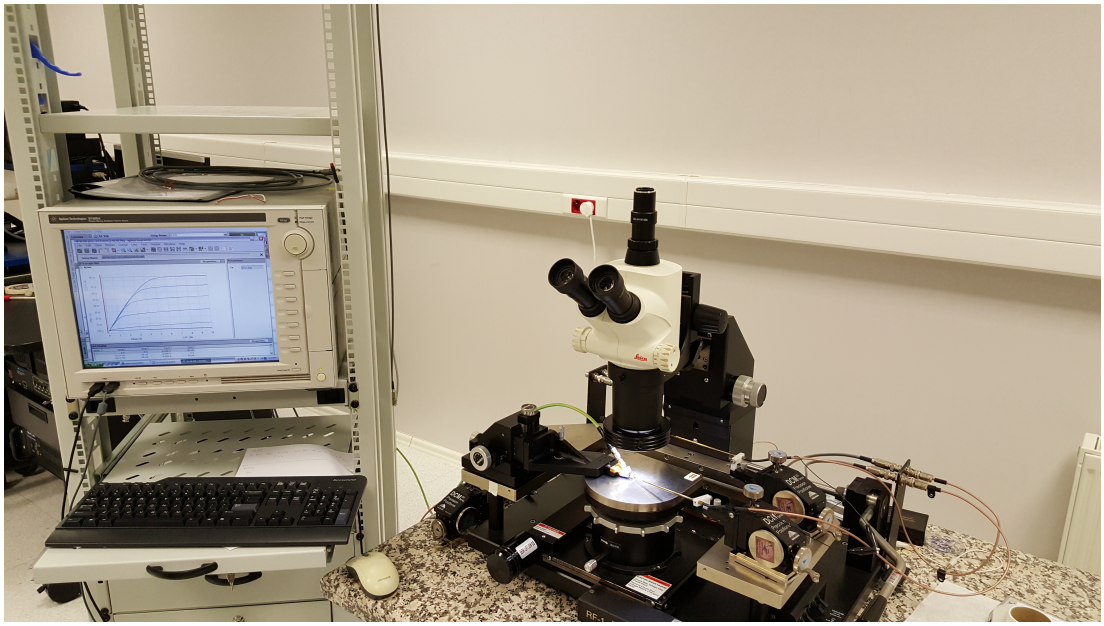

Figure 3.2: DC measurement setup

Required variables are clarified with measurement results, which are presented in Figures 3.3, 3.4 and 3.5. They were recorded via the measurement setup program. Knee voltage that is explained in Section 2.2, can be easily distinguished from IV plot in Figure 3.3. It is marked via circle and approximately equals to 6 V with 770 mA/mm drain current. Furthermore, knee voltage level matches maximum drain current of device but drain voltage was swept from 0 V to 15 V due to 10 W system limitation.

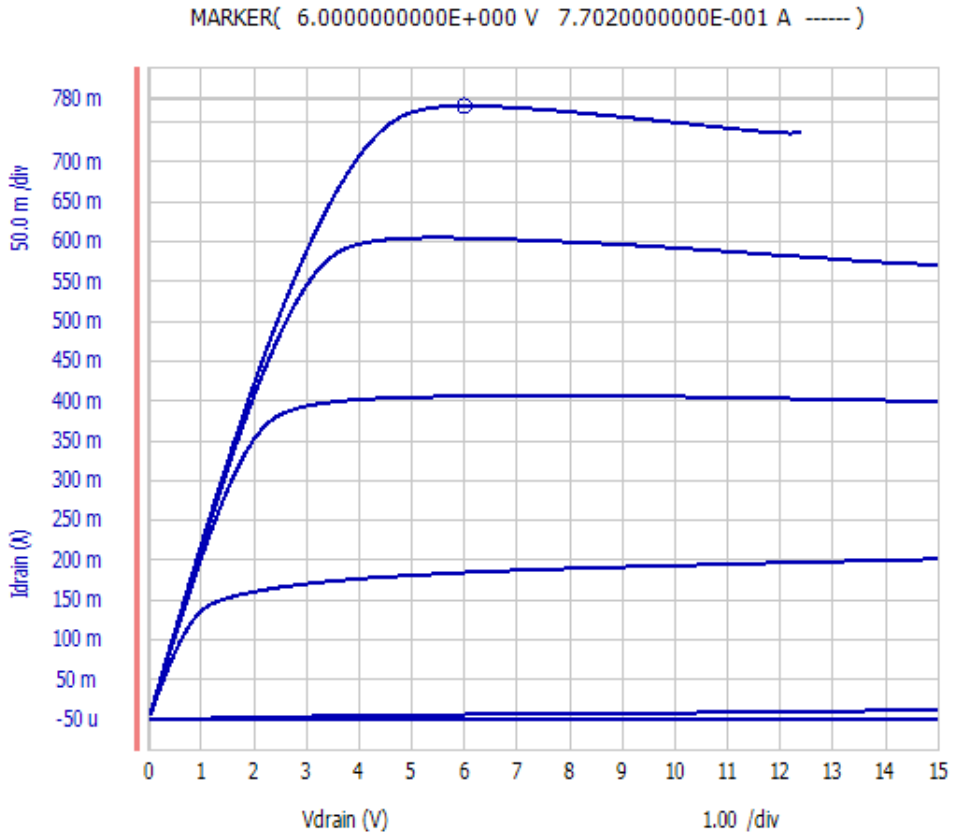

Figure 3.3: DC-IV graph of 8x125 HEMT device

Transconductance (g_m) characteristic of device is shown in Figure 3.4, where g_m value is 213 mS/mm. Additionally, pinch-off voltage is read as approximately $-3.6\ V$. Pinch-off voltage is the voltage level below which transconductance (g_m) is unchanged. On the other hand, drain voltage remains constant and V_{gate} is swept from $-6\ V$ to $1\ V$ to obtain transconductance (g_m) value at maximum current density level. When gate voltage is adjusted to be equal to $V_{pinch-off}$, device current starts to flow. Classic transconductance formula is presented in Eq. (3.1).

$$g_m = \frac{\triangle I_{drain}}{\triangle V_{gate}} \tag{3.1}$$

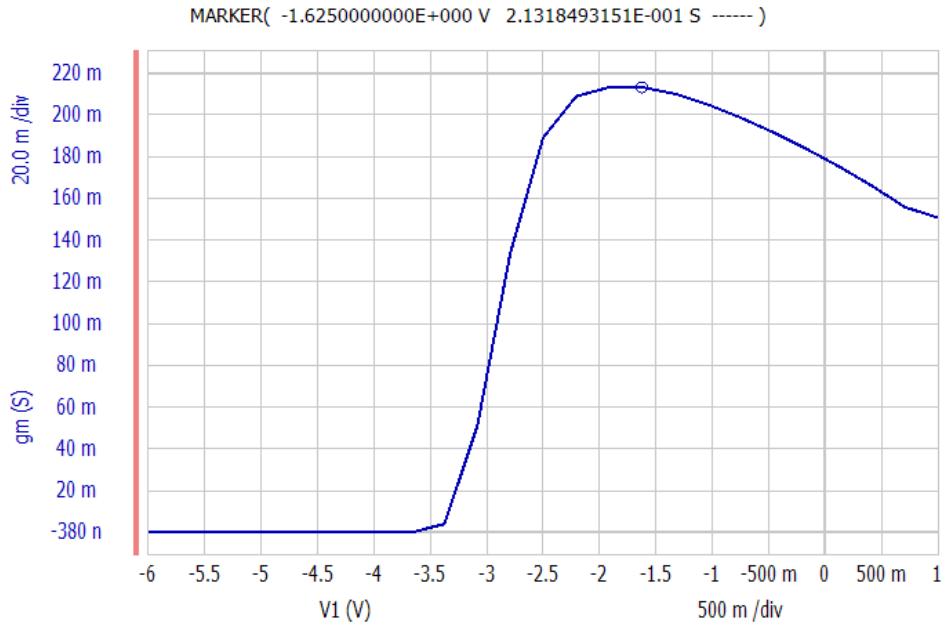

Figure 3.4: Transconductance change of 8x125 HEMT device

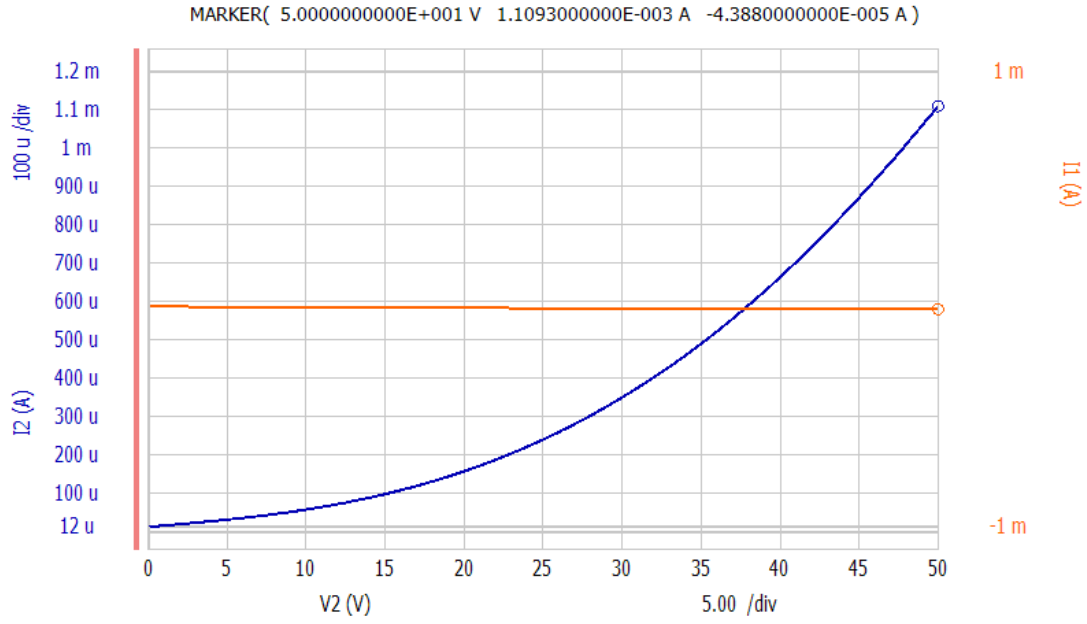

Figure 3.5: Drain Current vs. Breakdown Voltage graph of 8x125 HEMT device

Breakdown voltage is higher than 50 V if applied current is equal to 1.1 mA at -6 V gate voltage as seen in Figure 3.5. Additionally, there is a small gate

leakage current at a level of few μA's.

In this work, drains of transistors are biased with 25 V and they draw approximately 250 mA current in the linear region. It is calculated and verified that the transistors, used in this work, operate in class AB operation. Detailed DC-IV sweep could not be done due to power limitations of the setup.

On the other hand, small-signal characterization of HEMT device is done by calculating cut-off frequencies of current gain (f_t) and power gain (f_{max}). Detailed information about measurement setup are given in Section 3.7. Figure 3.6 illustrates small signal measurement setup.

Figure 3.6: Small Signal measurement setup

In addition, scattering parameters are attained after performing small-signal measurements. f_t and f_{max} values are determined using Eqs. (3.2), (3.3) and (3.4) [17]. In Eq. (3.2), $(H_{21})_{dB}$ equals to 0 at f = f_t. Similarly, $(U)_{dB}$ in Eq. (3.4) is equal to 0 at f = f_{max}. Also, k in Eq. (3.4) represents stability factor of the transistor [17].

$$H_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \tag{3.2}$$

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|} \tag{3.3}$$

$$U = \frac{1}{2} \frac{|\frac{S_{21}}{S_{12}} - 1|^2}{k|\frac{S_{21}}{S_{12}}| - Re(\frac{S_{21}}{S_{12}})} \tag{3.4}$$

Lastly, load-pull characterization of HEMT device is performed for obtaining output power contours with Focus Microwaves' Load-pull Measurement Setup that is seen in Figure 3.7. Detailed information are given in Section 3.8.

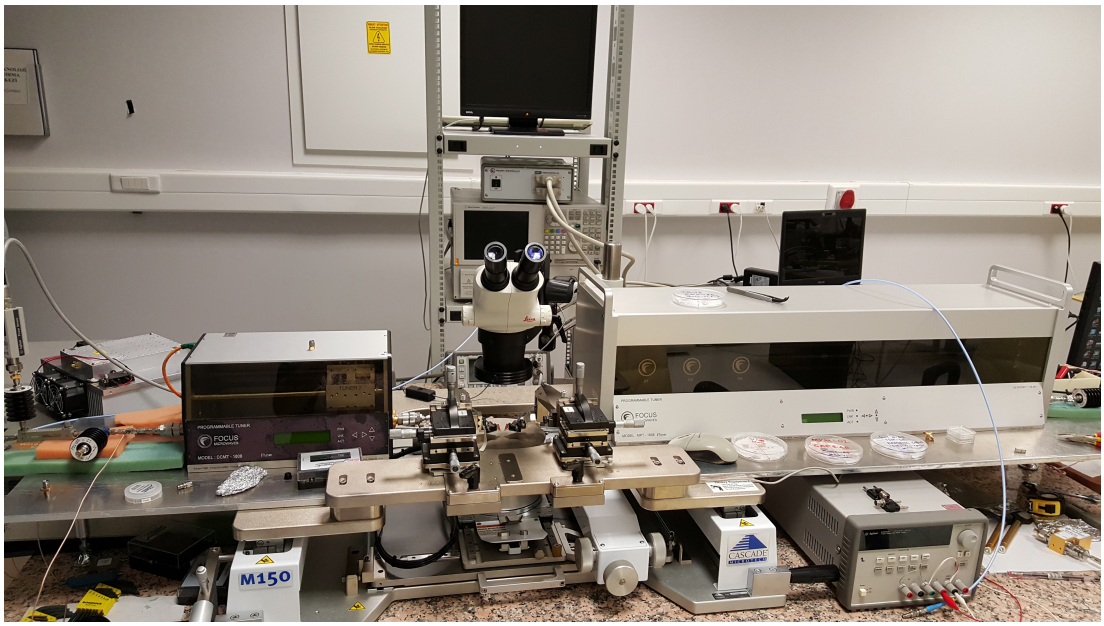

Figure 3.7: Load-Pull measurement setup

Power contours that are obtained by load-pull measurements, are important in terms of giving information about transistor's output power performance at every impedance values in the smith chart. Therefore, designers need to start to PA design at suitable impedances with taking into consideration both output power and gain requirements of a project. Figure 3.8 shows a power contour,

which has roughly the same characteristics with 8x125 transistor that is used in this thesis work. According to Figure 3.8, the transistor provides approximately 35 dBm output power in the red colored area at 8 GHz.

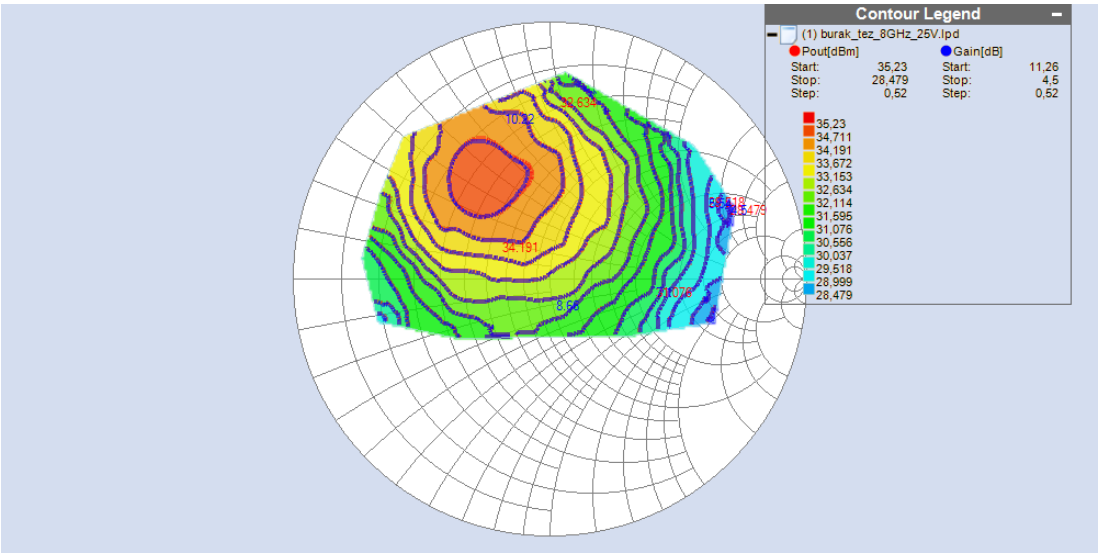

Figure 3.8: Transistor output power contour

3.2.1 Fabrication of HEMT Devices in Bilkent University NANOTAM

Fabrication steps of a HEMT device might differ according to fabrication facilities and design requirements but the main process steps must be the same for all MMIC and HEMT production lines. In this subsection, fabrication process that is performed in Bilkent University NANOTAM, is analyzed and explained with figures.

GaN on SiC substrate structures are used in fabrication. GaN is a semiconductor that provides designing HPAs at high frequencies. Moreover, high voltage can be applied to devices and temperature durability of them increases with GaN based HEMTs and MMICs. Initial lateral section of the structure is shown in Figure 3.9. GaN is an epitaxial layer, which is grown up in NANOTAM, and devices are fabricated with this epitaxial layer.

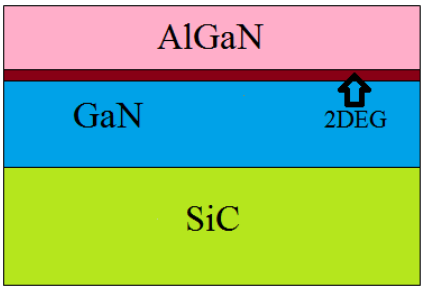

Figure 3.9: General HEMT device structure from side view

During fabrication, first, positive lithography is done to form intended geometrical area of the transistors. Photo-resists are sticked on initial structure as can be seen in the left side of Figure 3.10. After etching process, basic structure of transistors is generated as illustrated in the right side of Figure 3.10.

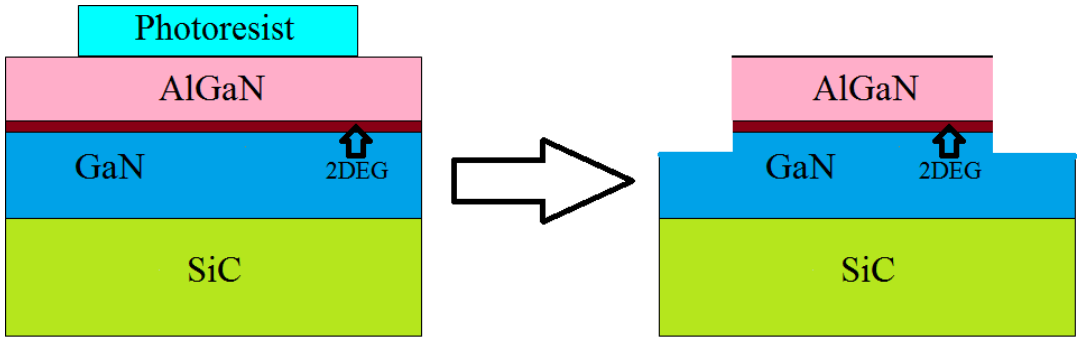

Figure 3.10: Positive lithography step of a transistor

Next, Ti/Al/Ni/Au metals are coated, respectively to form ohmic contacts on transistor to form the source and the drain fingers [18]. In this process, positive lithography with leaving open contact areas is repeated and after coating of metals, etching steps are done again. Thus, required contact areas become coated. In Figure 3.11, yellow parts of the structure represent ohmic contacts and the SEM (Scanning Electron Microscope) view of ohmic contacts from the top is seen in the right side of the figure.

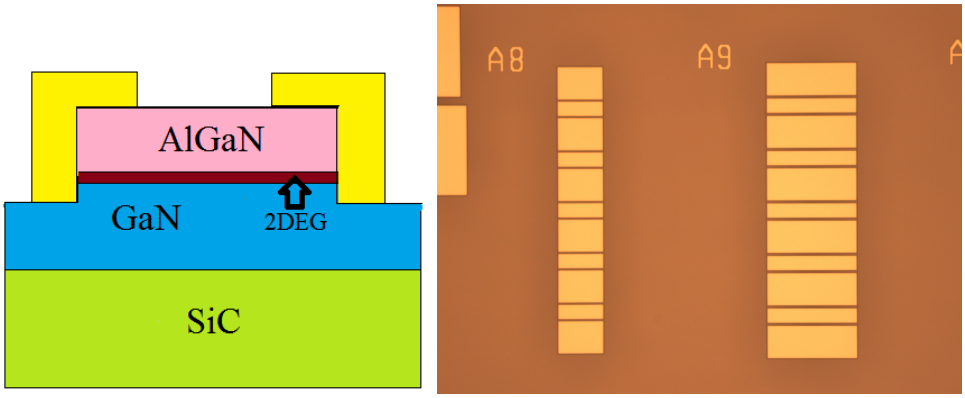

Figure 3.11: Creating of ohmic contacts

Furthermore, after creating transistor drain and source contacts, first metal coating process is done. Bottom metal consists of Ti-Al. It is required for passive elements of PA. Moreover, it is necessary to connect grounds in CPW structures. Other metal coating process is done for gate pads of transistors. Ni-Au metals are used during coating and this time negative lithography is performed. Gate metalization of transistors after e-beam lithography step is presented in Figure 3.12.

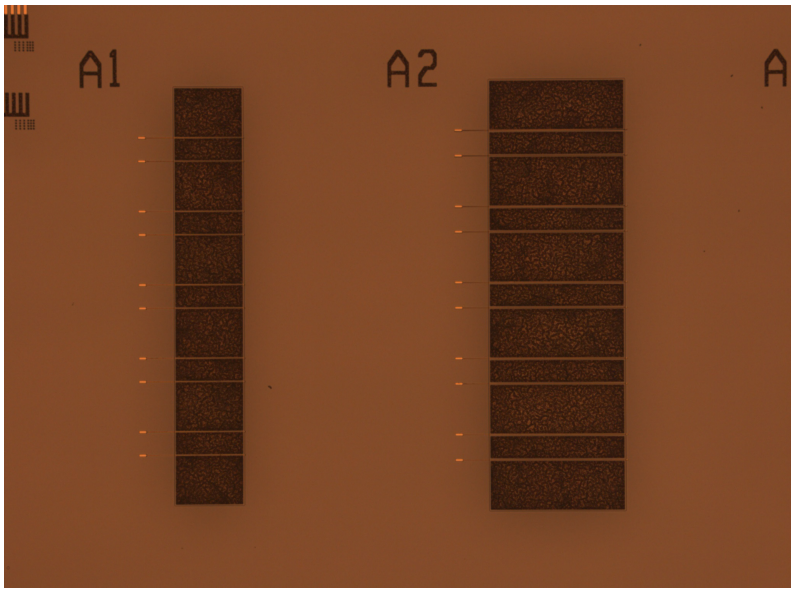

Figure 3.12: Gate metalization of transistors

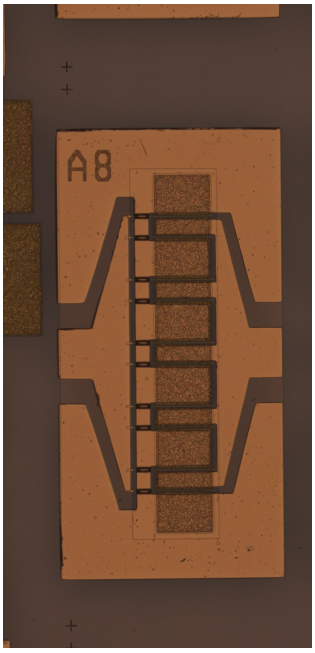

Figure 3.13: Transistor from top view after final stage of fabrication

The fabricated transistor appears as in Figure 3.13. After production, the structured wafer is coated with Silicon-Nitride materials as dielectric whose thickness is nearly equal to 300 nm. Capacitors are generated and transistor areas are passivated performing this step. As the last step, interconnect metal is coated for connecting needed layers. By this way, air bridge structures that can be clearly seen in Figure 3.14, are formed. As a result, designed HEMTs and MMICs are prepared for usage and measurements.

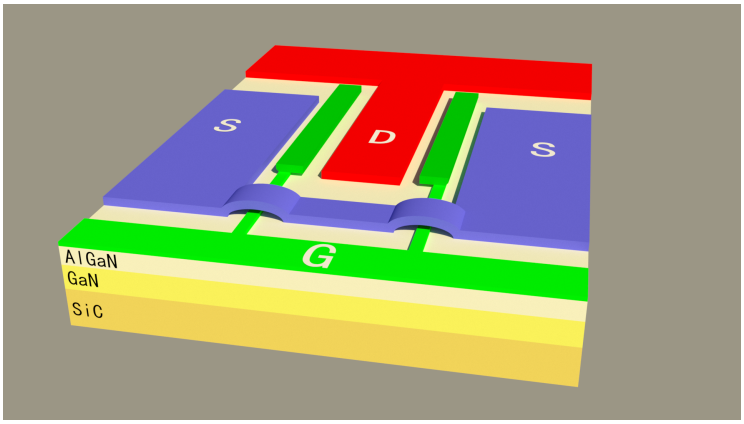

Figure 3.14: A perspective view of transistor after fabrication

Finally, it is crucial that fabrication restrictions of CPW structures should be determined by combining previous experiences and fabrication abilities of the company and the researchers. In this fabrication process, gap, that is between signal and ground plane, and transmission line width should be between 12 μm and 50 μm. Additionally, minimum space of middle gap of meandered inductors should be 70 μm to avoid coupling effects of signal lines to each other.

3.3 Initial Design of HPA with Ideal Elements in ADS

The initial design of HPA with ideal elements is presented in this section. Limitations and design steps are briefly explained. The main purpose of this work is to obtain a relatively small in size X-band HPA. Desired gain is approximately 12 dB in the operation band which is from 7.9 to 8.4 GHz because the gain decreases due to additional losses. Moreover, the output power of manufactured PA is approximately projected as 5 W at 8.2 GHz at 1.5 dB compression point. The compression point is chosen to be 1.5 dB at operating point in order not to increase nonlinearity of fabricated PA.

Physical properties of the HEMTs that are used, small and large signal characteristics of the used HEMTs are clearly explained in Section 3.2. After well defining the devices, DC bias points of the transistors (gate and drain currents) and source/load impedances are chosen for accomplishing both gain and output power specifications.

It is well known that active devices are electrically connected in parallel for increasing the output power and connected in series for getting higher gain from the power amplifier. In this design, two transistors are connected in parallel to achieve power specification. Addition to these, stability of power amplifiers is very significant issue to get a practical device in the operating range. Thus, stability circuits are used to take precaution for this design are clearly examined in this section. Finally, amplifier design is started with ideal elements in ADS.

The matching circuits consist of lumped elements and ideal TLINs, whose parameters can be determined via ADS line calculation tool. Substrate parameters that are used in fabrication process, are entered the line calculation tool's input. Matching circuits that are designed by the designers, can be sometimes inadequate to match the transistor. In that case, the smith chart and impedance matching tools of ADS are preferred to be used [9]. From these viewpoints general track of the design is specified.

DC voltage was not applied to schematic during the simulations because transistors' data were obtained under required DC bias conditions. Thus, accurate RF characteristics of transistor can be directly used during simulations. Additionally, transistors' data that were entered to data items, were chosen from lots of measurement results for the best matching. Source and load impedances approximately equals to $5+j*10$ and $10+j*20$, respectively when the output power is considered according to load pull data, which is described in Section 3.2. The matching circuits were built according to these impedances by using the previously mentioned simulation tools. After bringing impedances via matching circuit design to essential points, input and output isolation of two transistors and stability of the designed power amplifier were checked and necessary elements were added.

Utilization area of ideal transmission lines, inductors, capacitors and resistors are clearly seen in matching circuits. In addition to these, transmission lines can be used instead of inductors (short-stub) and capacitors (open-stub) in the design.

Input matching circuits with ideal elements are shown in Figure 3.15.

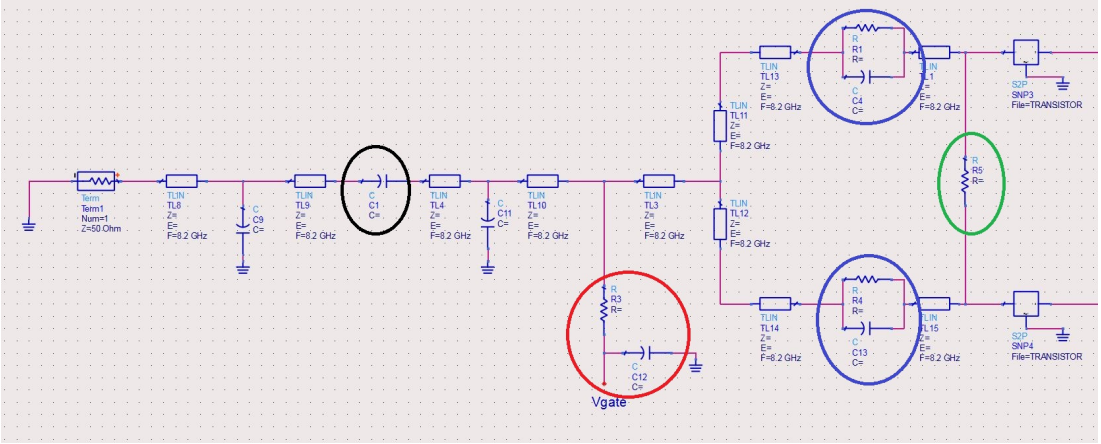

Figure 3.15: Input matching circuit with ideal elements

Resistors and capacitors together with the matching circuits' elements are indicated with circles in the schematic. Capacitor C1 in the black circle is used as DC block and RF short capacitance. It enables safety system measurements against

leakage DC currents because leakage currents might damage the RF measurement setup including network analyzer. This DC block capacitance value is usually chosen very big and it does not affect the RF characteristic of circuit. Red circled circuitry is required to bias gates of the two parallel transistors and reflected RF signals are vanished on the resistor. Unless its value is sufficient to cancel out, reflected waves can be shorted to ground with capacitance. Furthermore, resistor that circled in red is useful against stability problems. A circuitry that consists of a big capacitor and a small resistor connected in parallel is circled in blue. This part is added to input matching circuit for eliminating the stability problems in lower frequencies. For high frequency RF signals, capacitors have been used as transmission path. On the other hand, resistors transmit low frequency signals. Again surplus RF wave, which causes oscillation, is eradicated on this resistor because unstable conditions are mostly observed in the lower frequency band. The last resistor, circled in green, is added to provide better isolation between the two transistors and avoid the oscillation and bias problems especially when there is asymmetry in the transistors or bias circuits which causes odd mode excitation. Therefore, required source impedances can be directly matched to each transistor without any interferences and coupling effects.

On the other hand, output matching circuits with ideal elements are seen in Figure 3.16. Assigned capacitor, which is circled in black, blocks leakage DC currents and circuitry that consists of two capacitors and one resistor in series (green circle), are utilized to isolate two transistors' loads from each other. Drain bias point circuitry that is pointed out with red circle, is different than the gate bias point part. Inductor and capacitor are resonated together in this topology. Length of these elements can be assumed $\lambda/4$, if they are constituted with transmission lines. λ value is determined with respect to required resonance frequency.

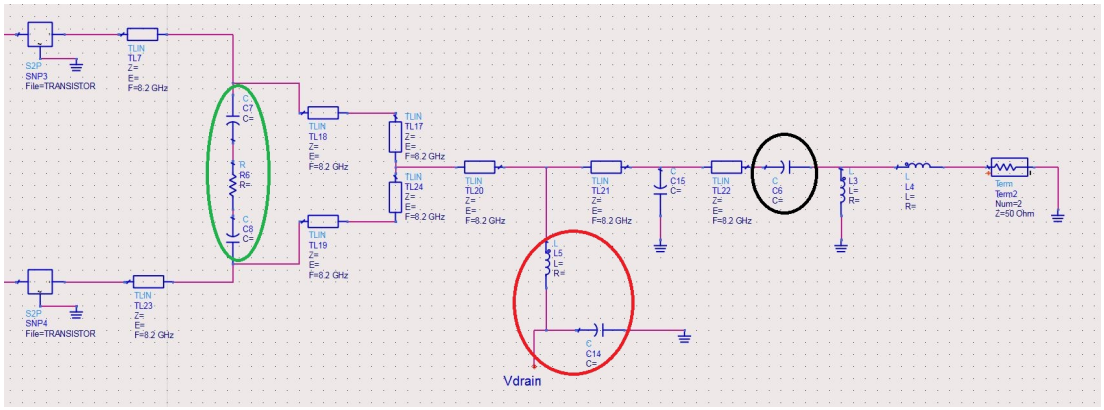

Figure 3.16: Output matching circuit with ideal elements

Initial design of PA is done with approximate element values and lengths. The PA did not perfectly work as it was targeted in the sense of stability, gain and isolation between two devices in frequency range from 7.9 GHz to 8.4 GHz. Therefore, tuning and optimization tools of ADS [9] were used for achieving the projected specifications.

Firstly, proper values of elements were designated with tuning tool to quickly optimize element parameters. Fabrication limitations were explained in Section 3.2.1. Tuning and optimizing the parameters have been performed according to these limitations.

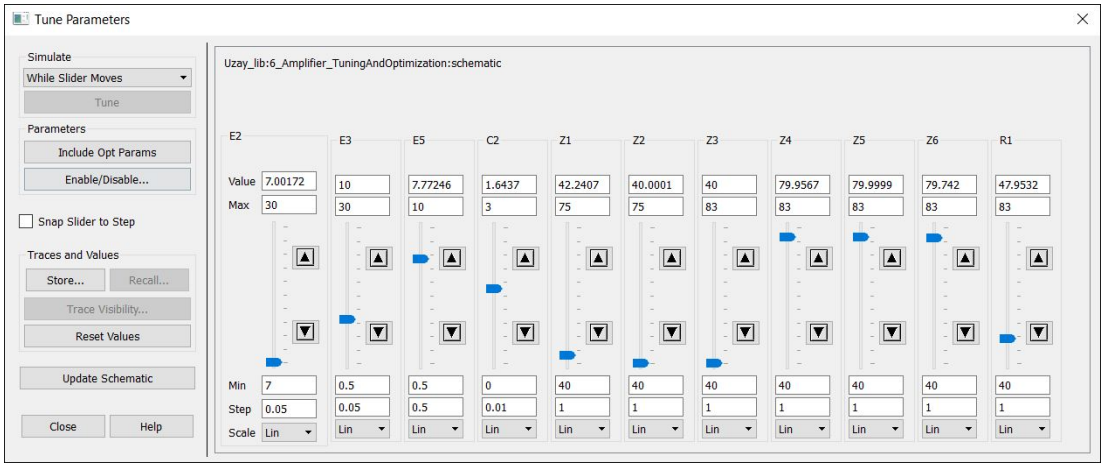

Figure 3.17: A view of Tune Parameters tool

Tune Parameters tool is seen in Figure 3.17. E_i and Z_i values show the electrical length and impedances of TLINs, respectively. Parameters of TLINs and other elements are tuned up to a proper point via this tool in consideration of the limits. In theory, TLIN impedances can be chosen from 43 Ω to 90 Ω. However, as the impedance increases, process becomes more difficult. Therefore, the TLIN impedances are determined to be maximum 80 Ω.

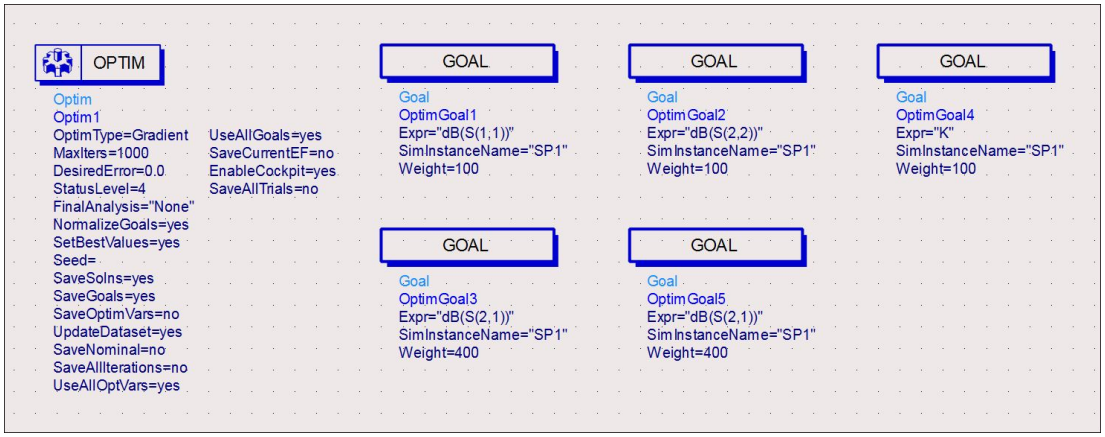

Figure 3.18: Definition of goals for optimization

After tuning the parameters up to useful points, design becomes ready for optimization. Goals that are required for optimization are shown in Figure 3.18. Specifications are defined in the program by using goal functions. They provide designers to manage goals such as input and output reflections, gain and stability factor of the PA. Depending on the defined goals' importance, optimization weight is selected. Concentrating on gain is warranted as it is seen in Figure 3.18, where weight of the gain is maximum. Moreover, default optim function was used during the optimization. Only its type can be taken random instead of gradient, which is quicker but has the problem of finding a local minimum instead of global minimum [9]. Therefore, it can be said that there is a contradiction between time and accuracy of the optimization.

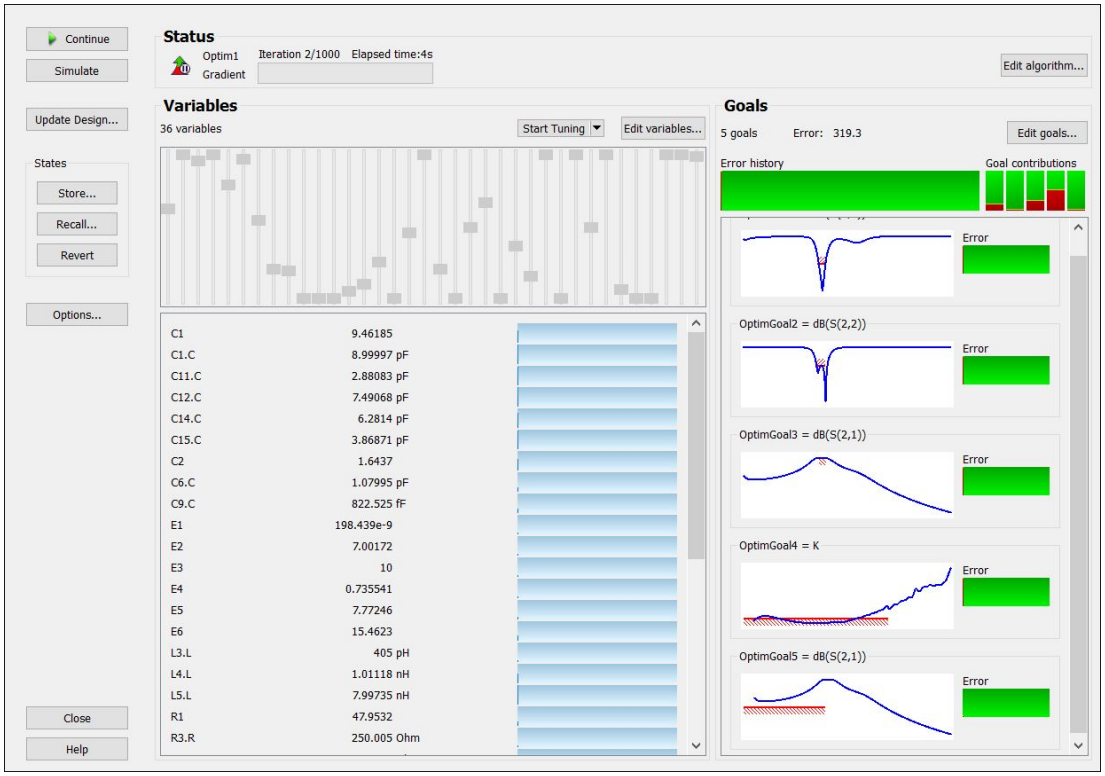

Figure 3.19: A caption from Optimization Cockpit

All adjustable properties of optimization are shown in Figure 3.19. Optimization is automatically ended when all of the defined targets are accomplished. Also, iteration numbers, goal definitions, parameter ranges and algorithm type can be changed during optimization for getting clear results.

Finally, after sufficient optimization, initial design of PA with ideal elements in ADS was finished with projected results that are presented in Figures 3.20 and 3.21.

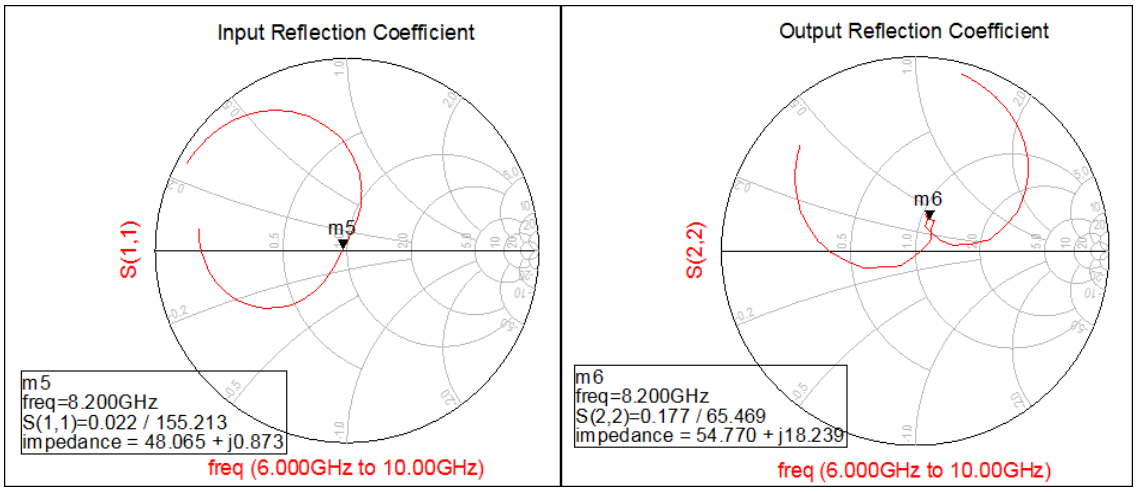

Figure 3.20: Input and output reflection coefficients of the PA (designed with ideal elements)

Input and output reflection coefficient results are shown in Figure 3.20. Graphs are marked at 8.2 GHz, which is approximately midpoint of the band. S(1,1) is matched to approximately 50 Ω. On the other hand, a bow tie is seen on the S(2,2) graph, it means that there are more than one perfectly matching points at output along the band as it can be seen in Figure 3.21 (in dB scale, rectangular plot).

According to simulated gain results, approximately 13.2 dB gain is obtained from designed PA along the operating frequency band. From beginning to the end of the frequency range, reflections at input and output are seen very good. Although minimum reflection value is expected around -12 dB, it equals to approximately -15 dB at 7.9 GHz. These results are clearly seen in Figure 3.21.

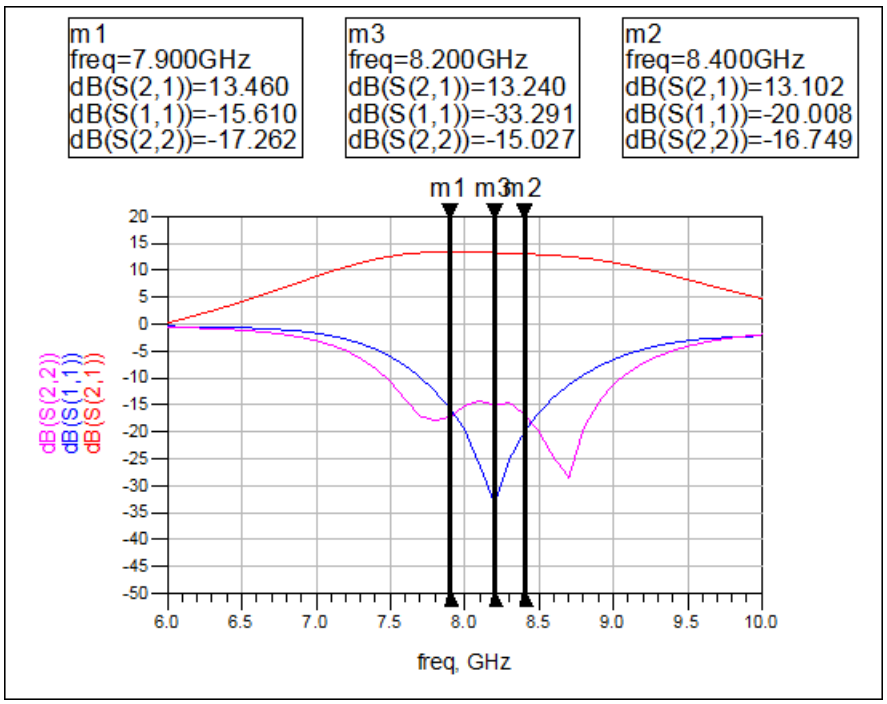

Figure 3.21: Gain and reflection changes with frequency (in dB scale) of the PA (designed with ideal elements)

The last parameter is the stability factor that is presented in Figure 3.22 for the frequency range span from DC to 14 GHz. The minimum point is marked in the figure and it equals to 1.172 at 5.2 GHz. This result shows that stability level of the designed amplifier is enough with ideal elements because it is expected that the matching circuit losses increase if the circuitries are redesigned with CPW technology and realized with respect to entered substrate properties. Thus, stability gets better in the final design. However, while oscillation characteristics are eradicating more clearly, gain of the amplifier unsurprisingly reduces. As a result, it is obvious that there is a trade-off between gain and stability.

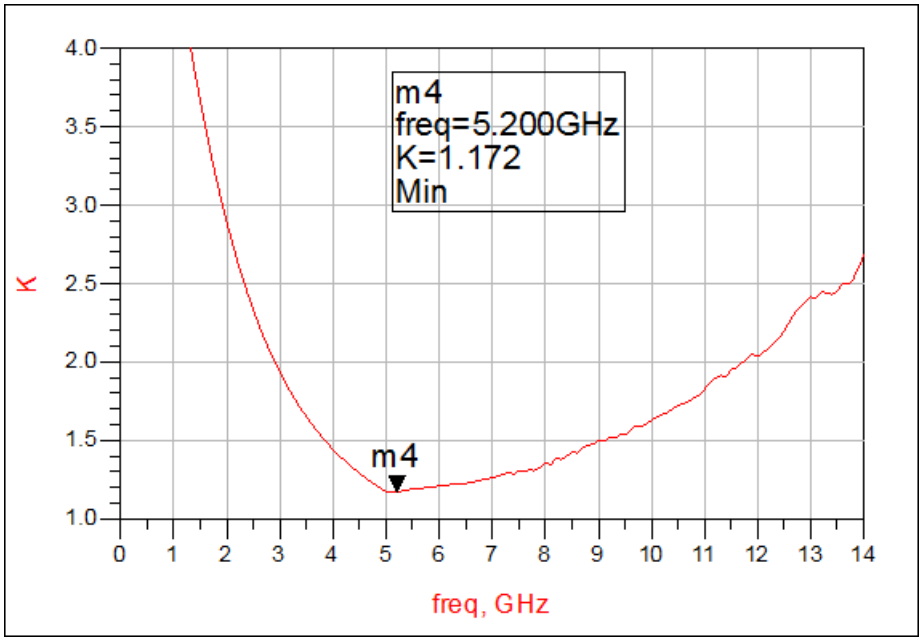

Figure 3.22: Stability of the PA (Designed with Ideal Elements)

Finally, in this section, all of the designs and simulations were done with ideal TLINs and elements as mentioned before. Therefore, frequency characteristic of capacitors, resistors and inductors were not taken into consideration. In addition, TLINs' internal resistance and other parameters do not affect results that are presented here. Importance of that effects are analyzed in the next two sections.

3.4 Transformation of Power Amplifier Design from Ideal Elements to CPW Technology in ADS Momentum

The aim of simulations is to be able to determine the product characterization as good as possible. From this point of view, ideal TLINs are converted to CPW structures for getting results that are more close to these of realized PA. It is expected that gain will reduce and stability factor will increase due to extra losses of CPWs.

Firstly, substrate properties of CPW structures need to be defined. Defined values in the ADS Momentum are shown in Figure 3.23. Width, gap and length variables were calculated by using line calculation tool [9] and corresponding results were used in the matching circuits as CPW.

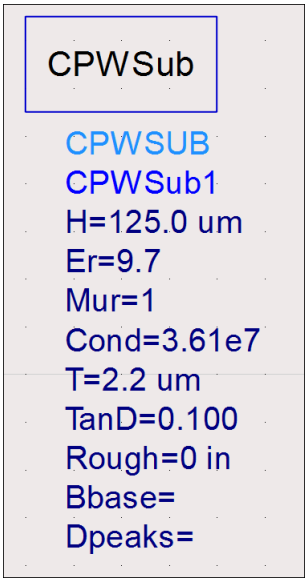

Figure 3.23: Substrate parameters defined in ADS Momentum for CPW structures

After performing the transformation of ideal TLINs to CPWs, circuit schematics for source and load parts of the device are shown in Figures 3.24 and 3.25,

respectively. At this point, it should be reminded that fabrication limits for width and gap variables were again taken into consideration during the transformation.

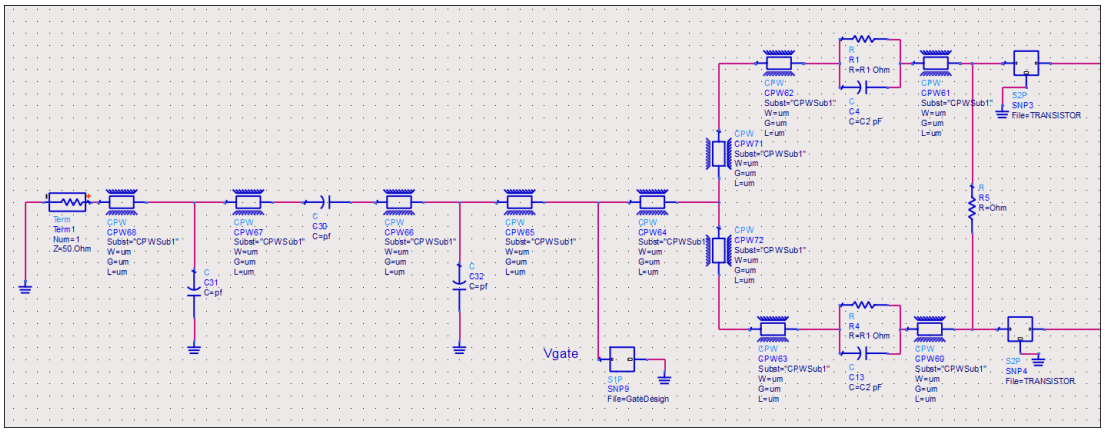

Figure 3.24: Input matching circuit with CPW structures

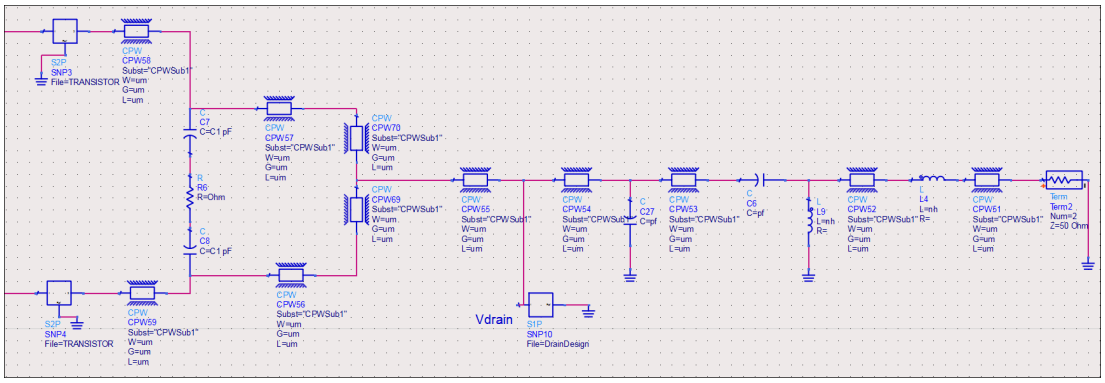

Figure 3.25: Output matching circuit with CPW structures

Missions of additional isolation and stability circuitries to matching elements that are seen in Figures 3.24 and 3.25, were explained in section 3.3. As seen in Figures 3.24 and 3.25, after finalization of the layout designs gate and drain structures were embedded in data items. Finally, CPW variables and other lumped elements were tuned and optimized to obtain more accurate simulation data.

Gate and drain structures of the designed PA are presented in Figures 3.26 and 3.27. There is a shunt capacitor and a resistor in gate side for the stability, as it was stated before. On the other hand, a capacitor and an inductor resonate at desired frequency, which coincides with the drain point.

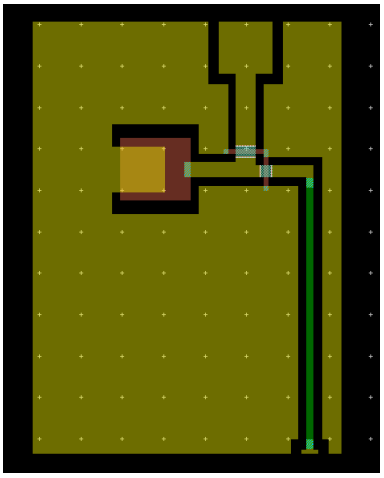

Figure 3.26: Gate structure of the PA

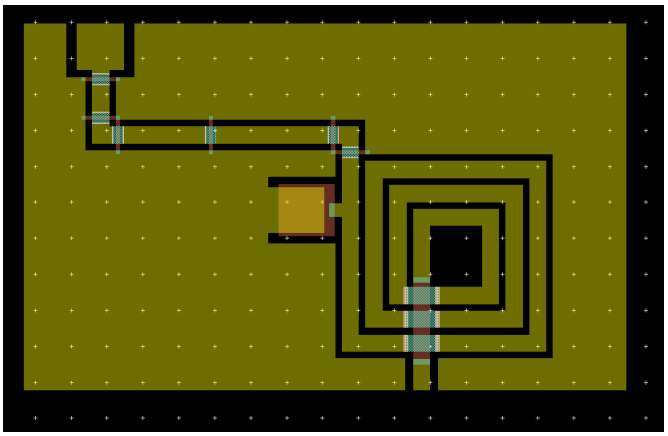

Figure 3.27: Drain structure of the PA

Only gate and drain structures were realized in this design step. The main reason is to take into consideration their real effects in simulation results. Gate and drain structures are very critical for efficiently feeding the active devices.

After transformations, input and output reflection coefficient results for CPW technology are shown in Figure 3.28. The response did not change at referenced points although corresponding marked values were changed a little bit.

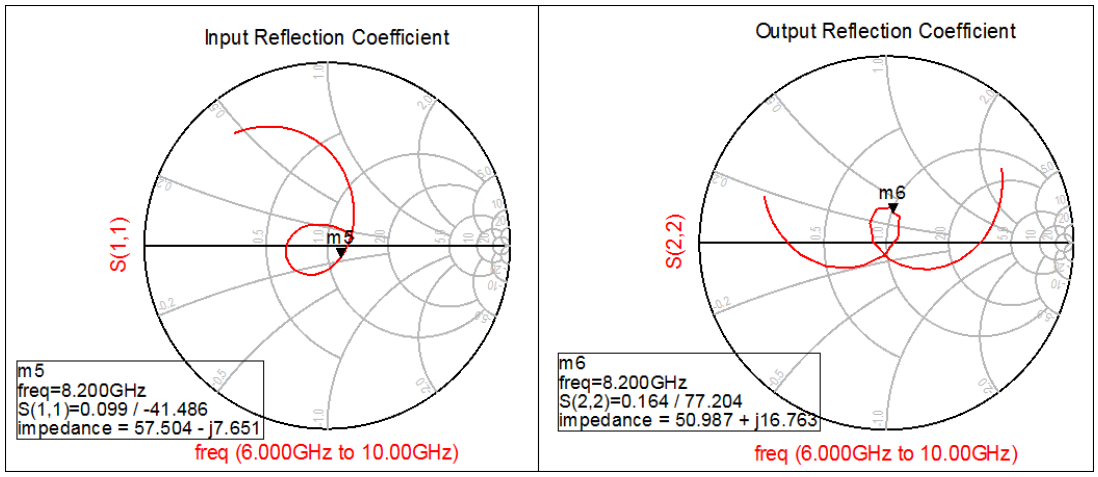

Figure 3.28: Input and output reflection coefficients of the PA (designed with CPW structures)

Gain results and reflections at different frequency points are seen in Figure 3.29. Approximately 11.8 dB gain was obtained in the operation band. Average gain decreases by 1.4 dB and minimum reflection point increases up to -20 dB as against the previous design step results.

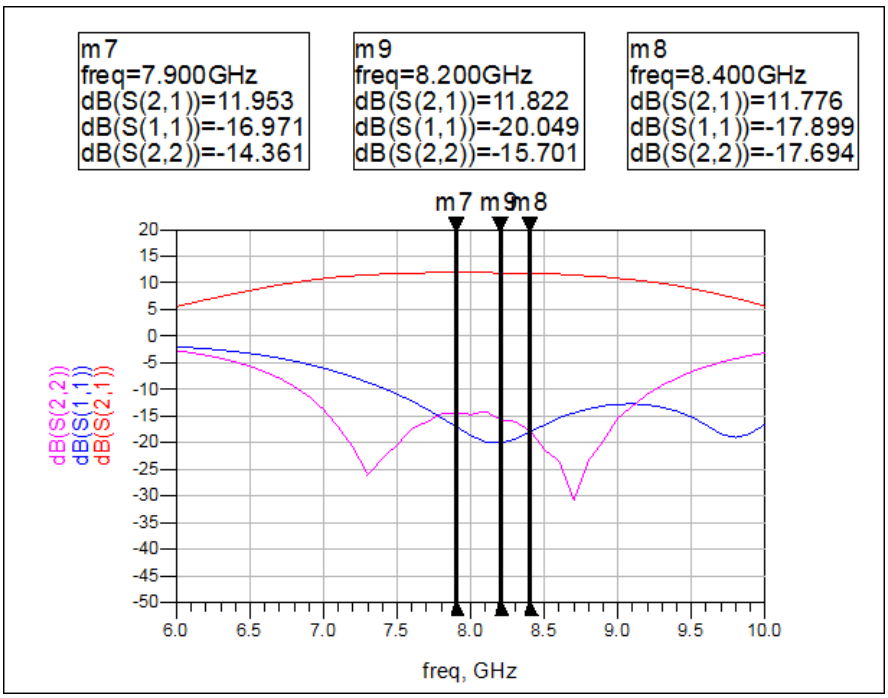

Figure 3.29: Gain and reflection changes with frequency (in dB scale) of the PA (designed with CPW structures)

Lastly, in this section, stability factor of a designed PA is analyzed. Stability factor equals to minimum 1.713 at 8.1 GHz as seen in Figure 3.30. Stability coefficient comes in good point and oscillation risks reduce with CPW technology because ideal TLINs and elements have almost zero losses but the realized ones have higher losses including conductivity and TanD loss that is the dielectric loss.

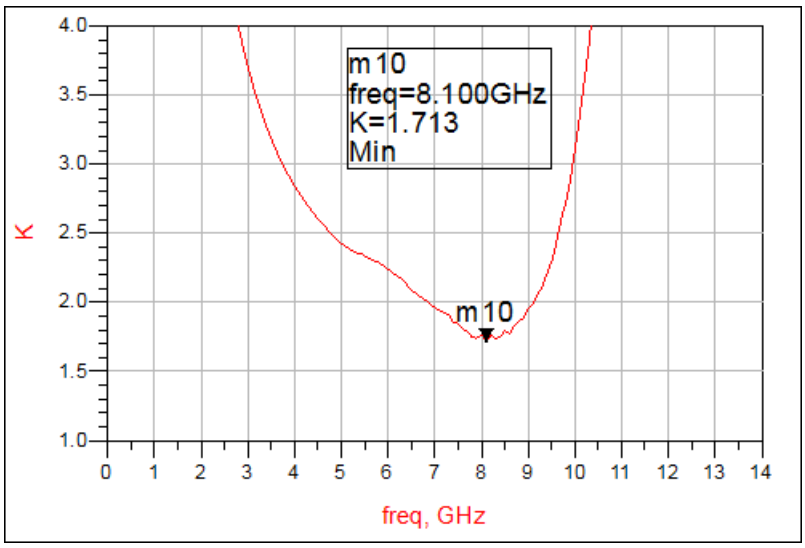

Figure 3.30: Stability of the PA (designed with CPW structures)

As a result, transformation of PA design from ideal elements to CPW technology in ADS Momentum was completed. All ideal TLINs were converted and DC bias structures were realized due to their significance. Gain and input/output reflections become worse with respect to those obtained in ideal case and the response of the designed PA was moved away from the unstable condition point.

3.4.1 ADS Substrate Properties

Defining substrate is very important for obtaining accurate simulation results. It is optimized and well-defined due to long time experiences in NANOTAM. At this point, precision of defined material properties is significant in terms of obtaining consistent fabrication results with that of simulations. Although properties of various materials including resistive, dielectric and conductive materials, are specified by the suppliers, their responses during fabrication process can be differed from data-sheet due to clean room conditions, temperature effects and so on. Therefore, as a result of conducting lots of measurements, simulations and comparing their results, substrate parameters are verified accordingly. Finally, optimum values and fabrication conditions are found.

Based on past experiences, gold purity is a very effective factor for metal coating and it changes electromagnetic response of all RF components. Moreover, real value of resistor used in fabrication directly affects available gain of RF PAs and stability factor. Angular variations in coating device are another negative effects that result in altering the material values during fabrication process. Therefore, angular variations are not desired.

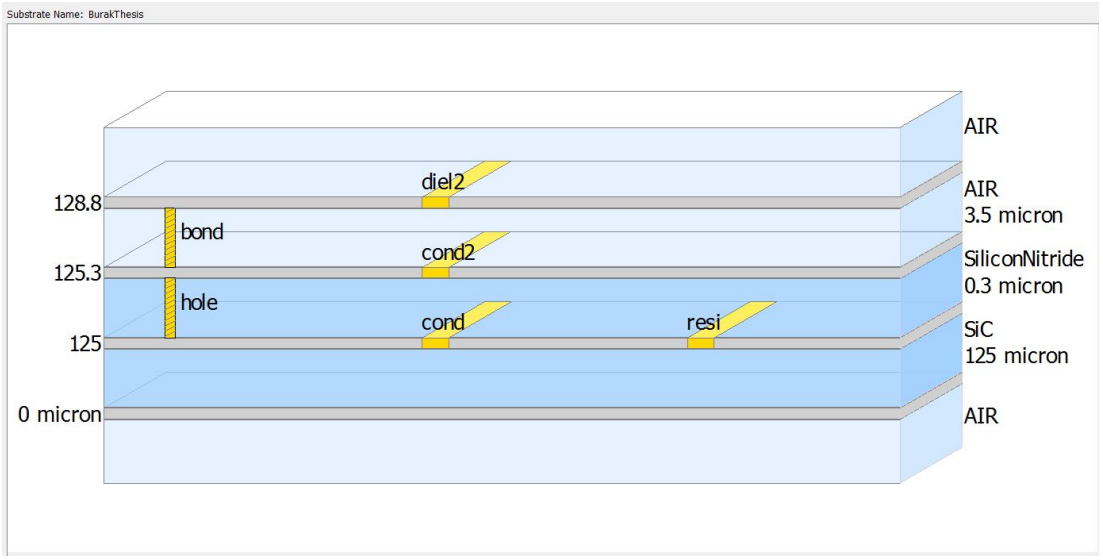

Figure 3.31: A cross-sectional view of substrate used in simulations

A cross-sectional view of substrate used in simulations is presented in Figure 3.31. The definitions of layers have been done according to ADS [9] algorithms and requirements. The main layers, which are called as diel2, cond2, cond and resi correspond to air-bridge, first (bottom) metal, second metal and resistor in realization of the design, respectively. Bond and hole components are used for connecting the layers each other. In addition, little differences can be observed during process of MMIC production. However, it is expected that substrate properties and material thicknesses are constant.

The defined substrate has been used in simulations. The smallest air-bridge hight is 3.5 μm and approximate dielectric thickness is 300 nm. Furthermore, layers have been defined in sheet as shown in Figure 3.31. Diel2, cond2 and cond layers are specified as gold with 2.2 μm thickness and resi layer is defined as 85 nm resistive material. In addition, bond and hole connections are defined as PEC

(Perfect Conductor).

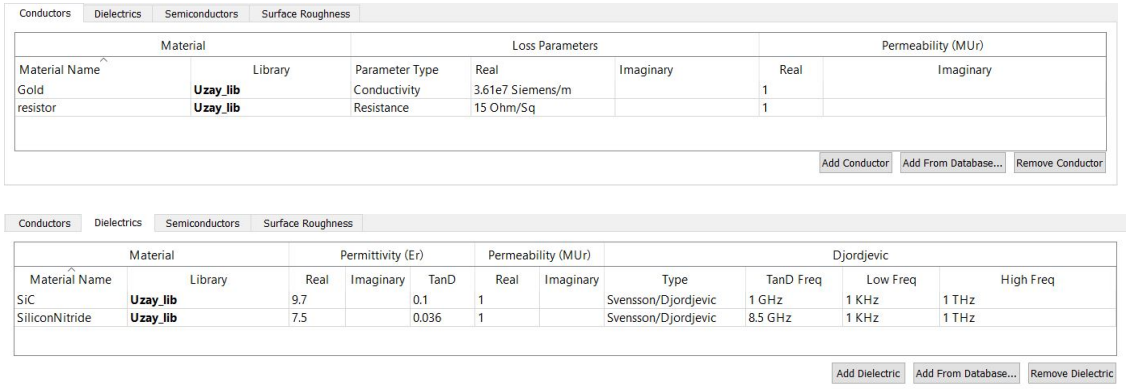

Figure 3.32: Material properties of substrate used in simulations

All of numerical values are entered the program to obtain accurate results. Material properties, which are used in simulations, is shown in Figure 3.32. Conductivity of gold and value of resistor equal to 3.61e7 Siemens/m and 15 Ohm/Sq, respectively. SiC and SiliconNitride permittivities are 9.7 and 7.5, respectively. Their permeabilities are directly defined as 1. Moreover, SiC and SiliconNitride TanD values are 0.1 and 0.036, respectively. SiliconNitride TanD value was assigned based on frequency range because it is the main dielectric material for capacitor elements in the design. In addition, TanD (Dielectric Loss) is resulted from voltage and current differences and it goes up, when the operating frequency increases [14]. If dielectric constant (permittivity) scales up, capacitive effect of element increases, which is derived from Eq. (3.10) [19].

3.5 Power Amplifier Layout Design in ADS Momentum

PA layout design is the other important step. Therefore, real material properties, expected variations during fabrication and previous experiences are taken into consideration to obtain very similar simulation results with that of measurements of manufactured PA. From this point of view, all lumped element layouts and CPW structures are designed in ADS Momentum based on defined substrate properties, which are explained in Subsection 3.4.1. Finally, general design steps and tracks based on related simulation results and explanations are presented in this section.

Realized gate and drain bias parts have been already analyzed in Section 3.4. Transistors' s-parameter data are defined the program via using data items. Therefore, appropriate spaces are considered in the layout design to active device placements. Furthermore, intended PA is comprised by two electrically connected parallel transistors to obtain high power. Therefore, connection of transistors are perfectly combined via symmetrical transmission lines. This means that additional inductors and T-shape CPW structures are inserted.

Initial input and output stages of PA layout are shown in Figure 3.33 and important structures are circled. Their layouts are directly drawn based on width, gap and length values of CPWs whose schematic was given in Section 3.4. Layout design of these stages has high priority. Therefore, the rest of matching circuits are tuned based on their characteristics.

White circles indicate isolation circuitries. Approximately 150 Ω resistor is used at the input stage and two big capacitances are connected to 75 Ω resistor serially at the output stage. By this way, adequate isolation between two active devices are provided. In addition, these stages can be supposed as a two-way divider (combiner) network, which are consisted of two branches and one resistive element.

On the other hand, a parallel RC circuitry, which is circled in yellow, is shown in Figure 3.33. It provides to design a stable PA. This structure is required high capacitive value to reduce capacitor RF inference. However, layout design of needed capacitor is meaningless due to determined realization limits. Therefore, two capacitors are connected in parallel to reach necessary value.

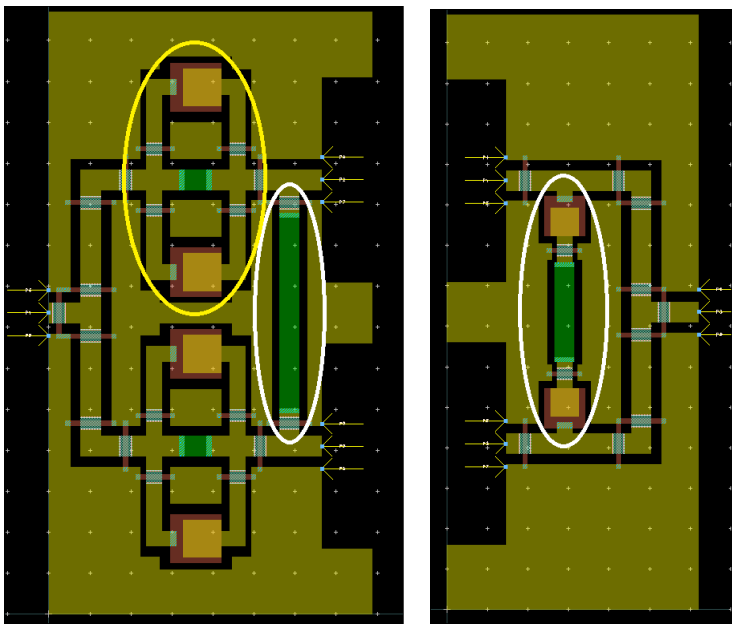

Figure 3.33: Initial input (left) and output (right) stages of the PA layout

Additional inductors and T-shape CPW structures are exhibited in Figure 3.33. These are used for connecting elements to each others and integrating resistors to circuit, respectively. Moreover, ground planes between capacitors and resistor in stability part are placed to get exact CPW response from inductors, which are placed on stability circuitries. Minimum dimensions of ground planes equal to $50 \times 50\ \mu m^2$.

Connection of ground planes is significant to get good RF responses from CPW structures. Air-bridges, which are seen in Figure 3.33, are used for connecting them to each others. Two consecutive air-bridges are elementarily placed with λ /10 intervals. However, interval values can be reduced to obtain better ground connection. If number of air-bridges increases, extra losses become exist.

After addition of input and output stages, PA schematic is seen as in Figures 3.34 and 3.35. The rest of CPW structures and lumped elements are properly tuned and optimized.

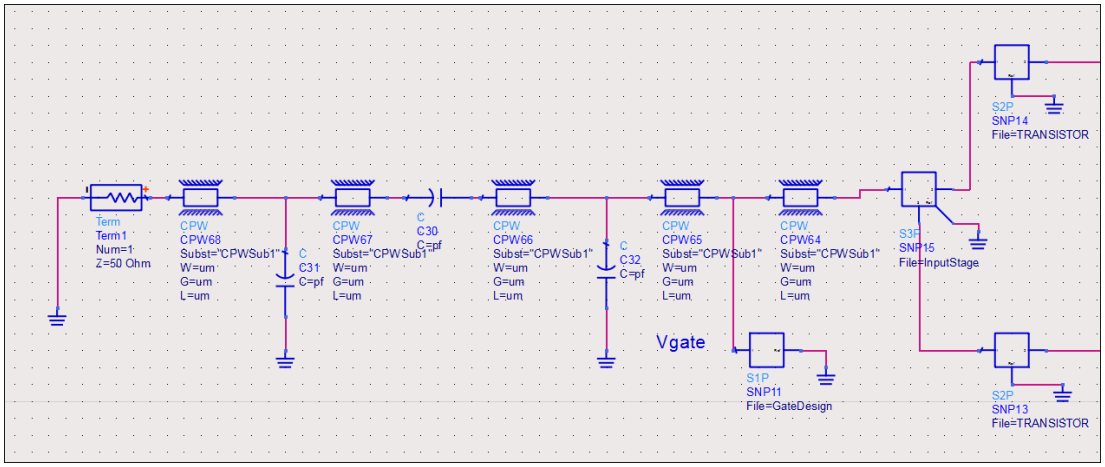

Figure 3.34: Input matching circuit

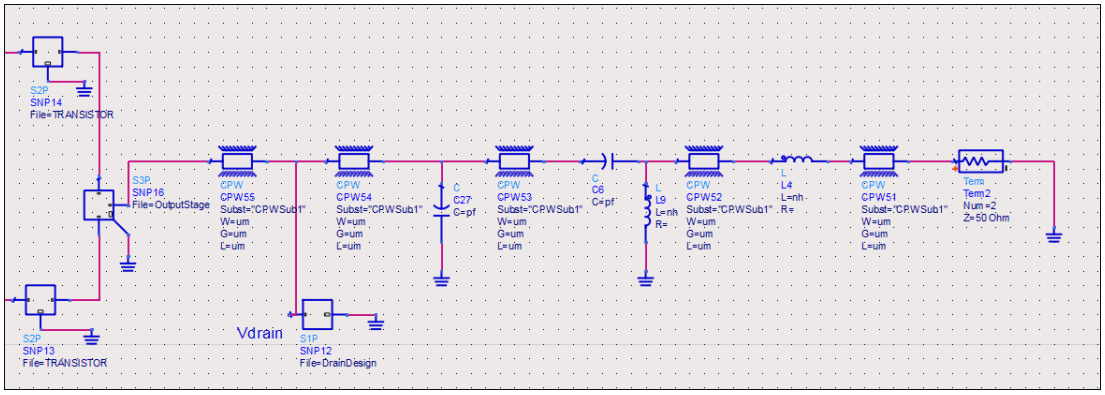

Figure 3.35: Output matching circuit

After tuning and optimization of remained elements, it is clearly seen in Figure 3.36 that gain reduces and return losses get worse.

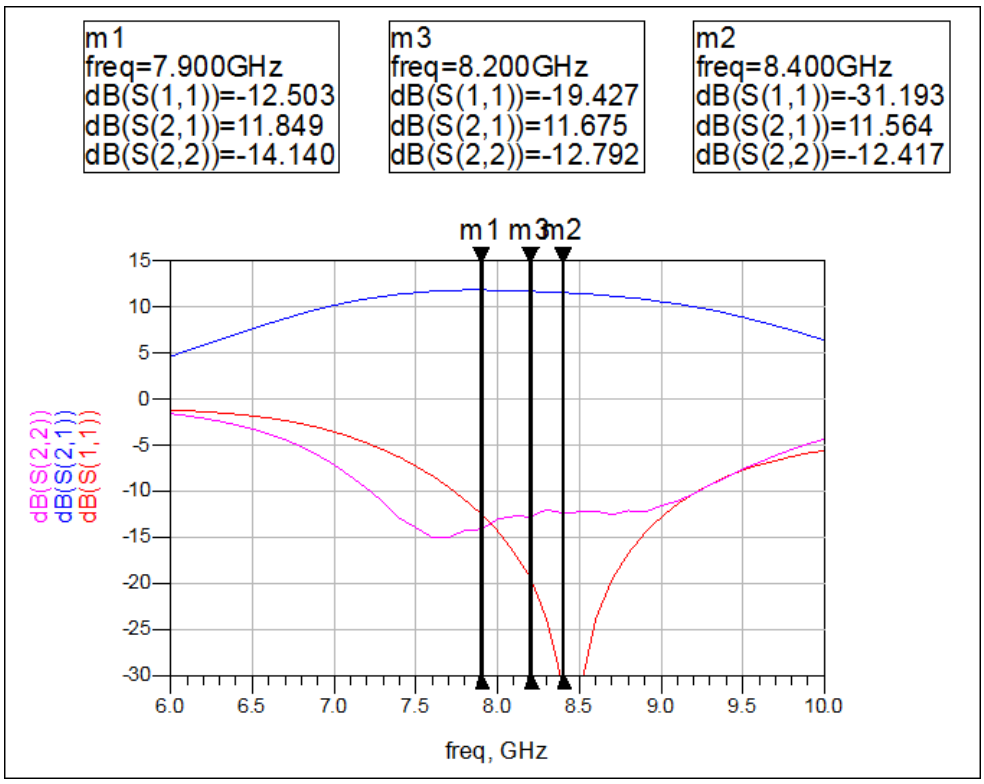

Figure 3.36: Gain and reflection changes with frequency (in dB scale) of the PA (before realization)

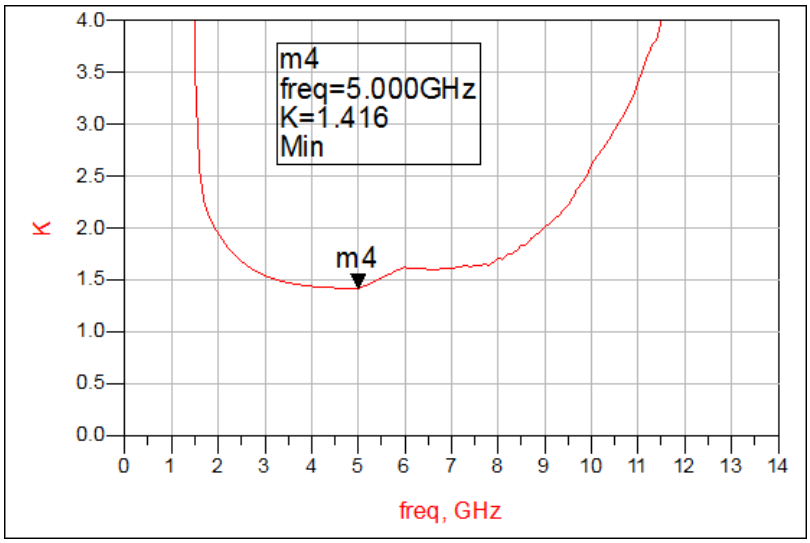

Figure 3.37: Stability of the PA (before realization)

Stability factor is marked as 1.416 at 5 GHz as seen in Figure 3.37. Although

increasing stability factor is expected by diminishing gain level, available gain decreases because of reverting return loss performance of designed PA.

On the other hand, it is well known that load of active devices are matched to an impedance based on load-pull measurements to obtain high output power and input matching circuit is constructed to achieve gain requirements. Therefore, first, lumped elements and CPW structures are realized and inserted to design in order to fix load impedance because the rest of the circuit is optimized according to desired gain.

Designing input and output matching circuits are completed by drawing lumped element layouts. At that point, drawn elements are properly simulated based on defined equations and techniques that are presented in Section 3.9. Finally, PA layout design is suitably finished in the light of specifications, fabrication restrictions and mask size limitations. The final layout is shown in Figure 3.38.

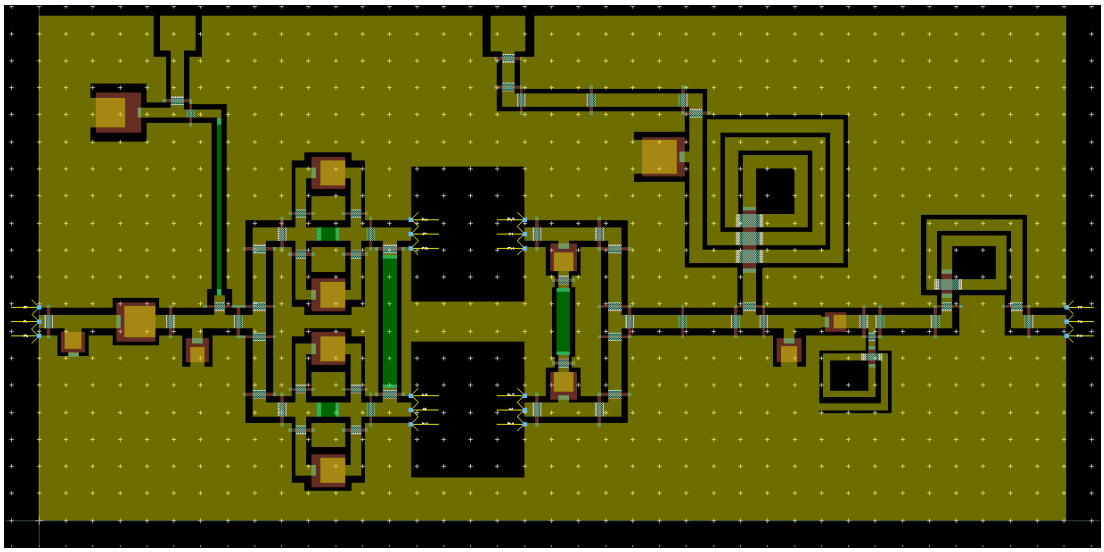

Figure 3.38: Layout of PA design

Drain and gate bias structures, input and output stages are integrated into source and load matching circuits. In addition, information about DC block capacitances were given beforehand. Large capacitance is placed for blocking DC current on input side and it does not affect RF characteristic of power amplifier.

However, at the output side it gets involved in device impedance matching.

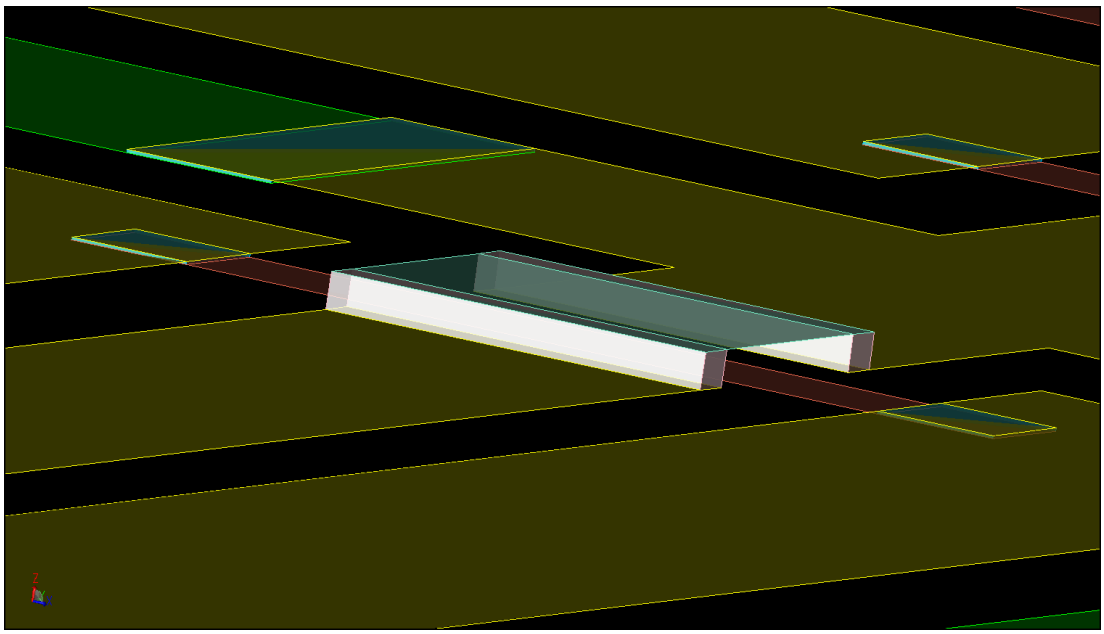

Figure 3.39: A perspective 3D view of Air-Bridge structures

After final layout simulation, a perspective 3D view of device is generated and zoomed in an air-bridge structure as shown in Figure 3.39. Air-bridges provide RF signal continuity to TLINs and connection chance to ground planes.

Final simulation results of PA design is presented in Figure 3.40. S(1,1) result is a little bit low but it is still matched with projected specifications. S(2,2) result still seems very good. Based on desired goals, they must be smaller than -10 dB and gain must be higher than 9 dB. However, approximately 10.1 dB gain is attained. This difference is kept for additional losses, which can be resulted from fabrication conditions. Moreover, 0.48 dB variation is seen from 7.9 GHz to 8.4 GHz in Figure 3.40. However, it is still acceptable.

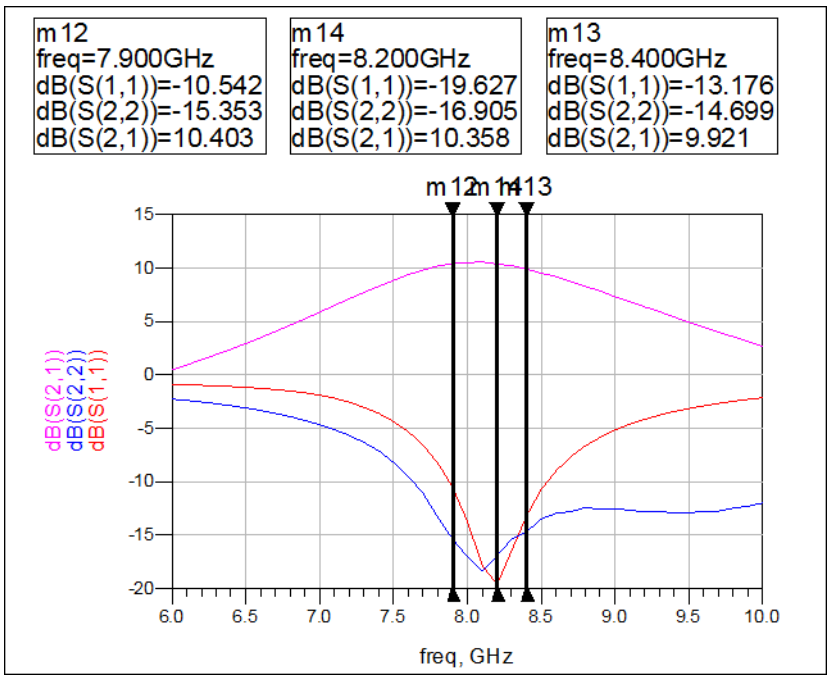

Figure 3.40: Gain and reflection changes with frequency (in dB scale) of the PA (after realization)

Stability factor equals to 3, which is shown in Figure 3.41. It can be said that manufactured PA will not be oscillated because stability factor is bigger than 1. Simulation results of device layout show that gain reduces and stability performance gets better in comparison with simulations that were performed before realization of designed PA.

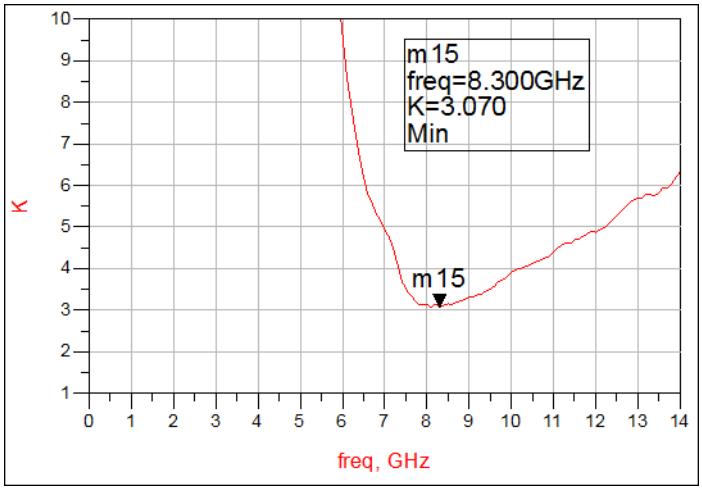

Figure 3.41: Stability of the PA (after realization)

Finally, the last design step is presented in this section. Layout of the PA is prepared to design mask in next section. In addition, it is specified that transistor data had been used from beginning to end of design as a model. Additionally, this data belongs to transistor that shows average RF characteristics from among all of measured devices. Therefore, there can be the small differences in measurement results. Frequency band may shift lower or higher frequencies depends on fabrication variations. PA gain can either increase or decrease depending on gate types. In addition, capacitance values and transistor impedances can be changed and some dissimilarities can be observed in measurement results.

3.6 Mask Design of Power Amplifier

Mask preparation of designed PA is the last step before fabrication and it is basically illuminated in this section. According to device layout sizes, more than one design can be placed on the mask. In addition, photo-mask design of layout is prepared before positioning device. Photo-mask of the PA layout is presented in Figure 3.42.

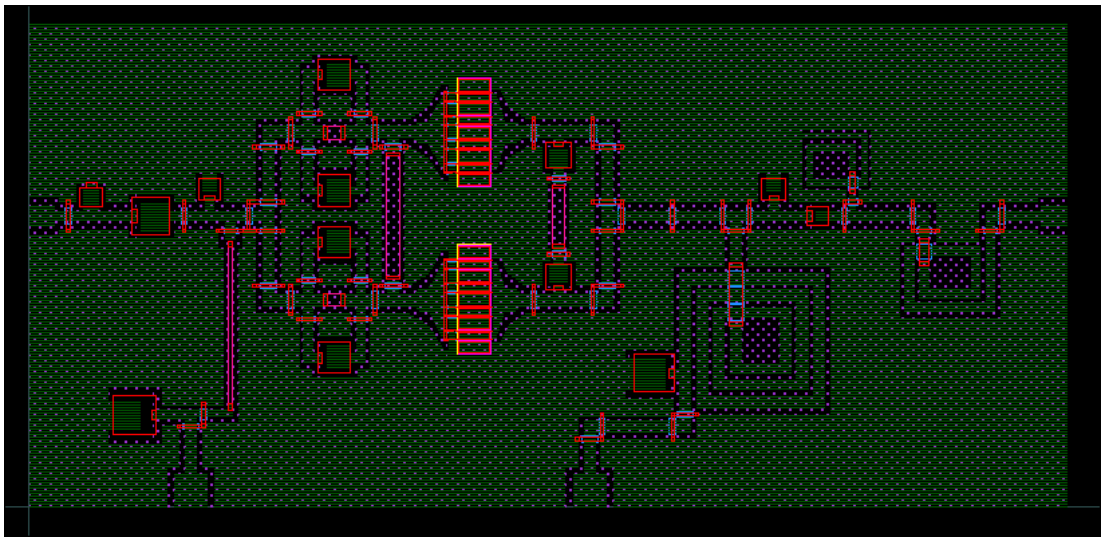

Figure 3.42: A top view of Photo-Mask design of PA layout

There are lots of layers that are very significant for fabrication. Locations and size limitations are defined with referenced to priority of fabrication steps based on production engineers' experiences. Additionally, missed layers result in unexpected effects on device performance. For instance, lack of one air-bridge causes short circuit between signal line and ground. As a result, designed device does not work properly. Therefore, designers should pay close attention to photo-mask design.

Air bridges are used to connect ground planes of CPW structure. An air bridge structure is shown in Figure 3.43. Its photo is taken by SEM. Ground connection metal is seen underneath of structure and its height was measured as 2.7 um.

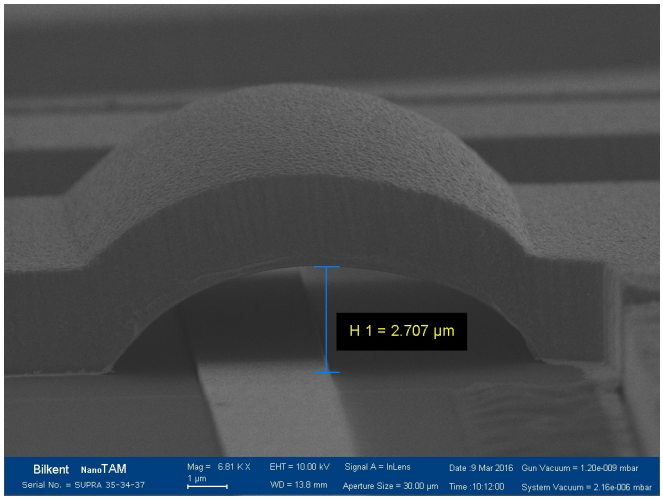

Figure 3.43: SEM image of an Air Bridge structure

Resolution limits of process is defined according to designed device. Contrast between fabrication and masks is directly distinguished by verification markers. Additionally, reference markers are inserted to mask to properly adjust layer places and they provide size information about structures.

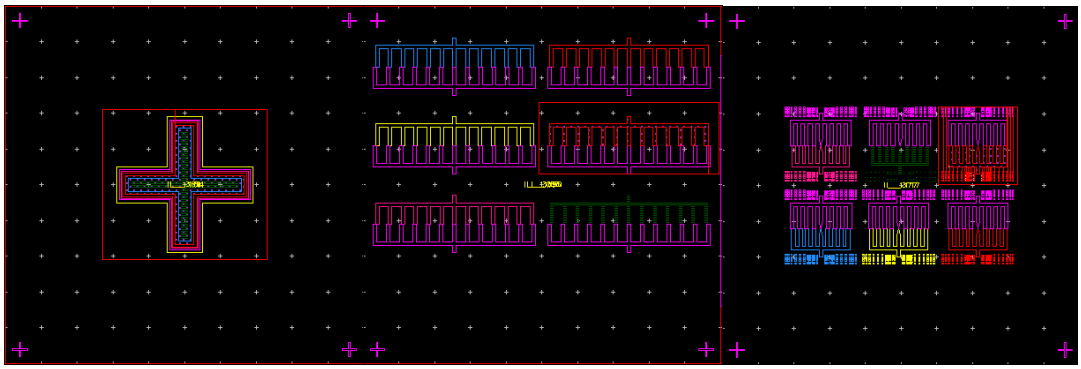

Figure 3.44: A top view of verification markers of the Mask

Different verification markers are presented in Figure 3.44. The left one is used for aligning mask position and other markers provide to determine deviation of layers between mask and fabrication. Colors in the markers indicate different layers. Therefore, layer positions can be easily checked during fabrication process.

Another essential issue is gate drawing. Different gate types are designed and used for MMICs such as single line, gamma and T-shaped gates. SEM image of

gamma gate structure is shown in Figure 3.45. They are drawn after deciding gate length and width and distances between drain and source planes. These parameters directly affect transistor's available gain, maximum output power and source/load impedances.

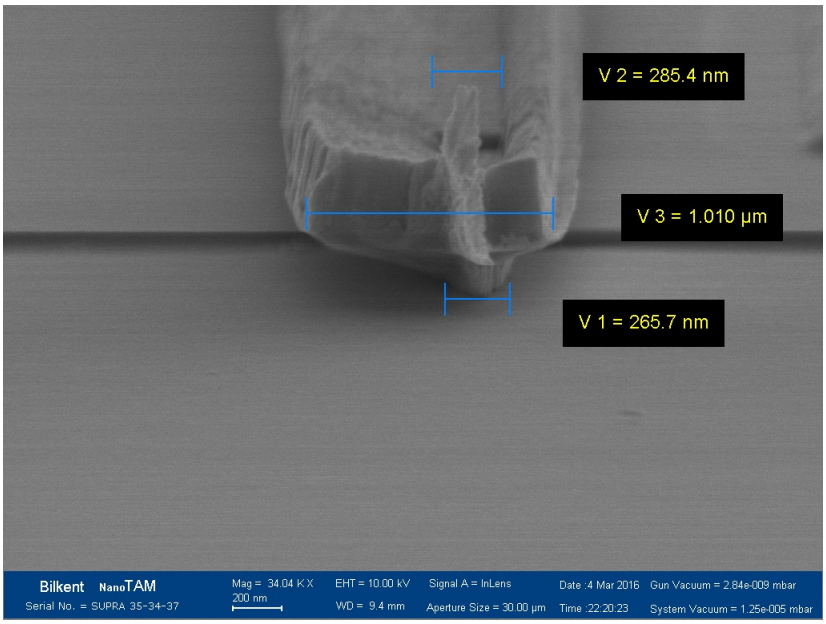

Figure 3.45: SEM image of the Gamma Gate structure

A top view of transistor with gate structure is shown in Figure 3.46. Four e-line markers are placed on corners of transistor location as seen in the figure. These referenced markers guide to electron beam device to construct gates. On the other hand, zoomed view of two gate fingers is presented in the same figure.

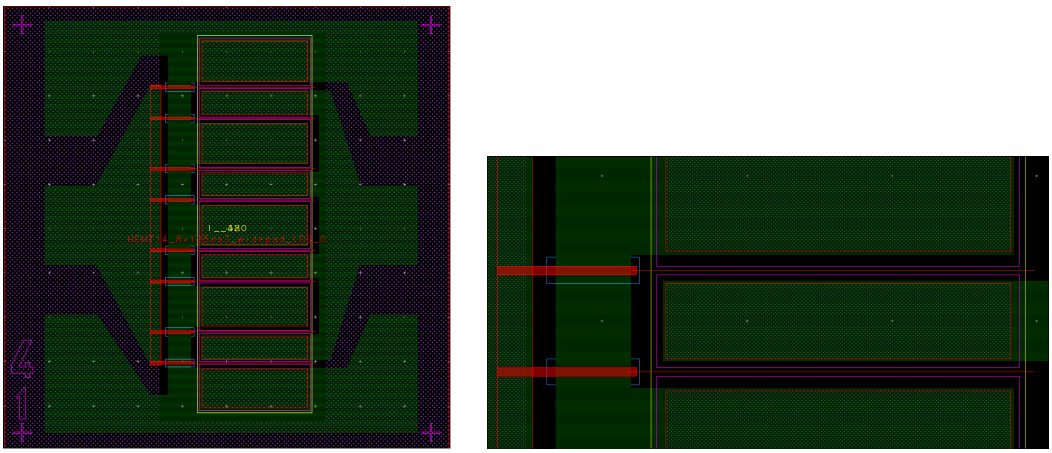

Figure 3.46: A top view of transistor with Single Line Gate

Moreover, transmission line measurement (TLM) patterns are inserted to mask to verify fabrication. An example pattern can be seen in Figure 3.47.

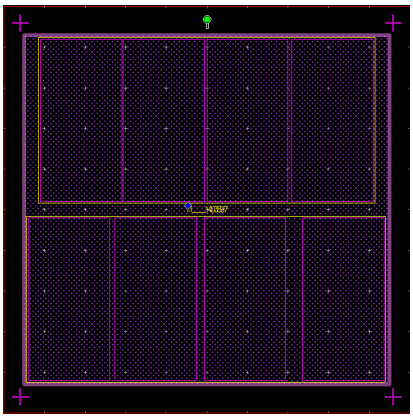

Figure 3.47: A figure of TLM pattern

Finally, mentioned verification structures and device designs such as power amplifiers, transistors and passive elements are placed on the mask. Therefore, designed MMIC PA fabrication is made based on mask design and it becomes ready for gain and power measurements after verifying fabrication by measuring TLM patterns, transistors and passive elements.

3.7 Gain Measurements and Comparison of Simulated and Measured Gain Results of Power Amplifier

The main focuses are gain measurement setup, manufactured device measurement results and fabrication verification after this point.

Measurements are more important than simulation results for designers because fabrication variations, failures and simulation accuracy are determined with measurements. An image of a manufactured and measured PA is presented in Figure 3.48.

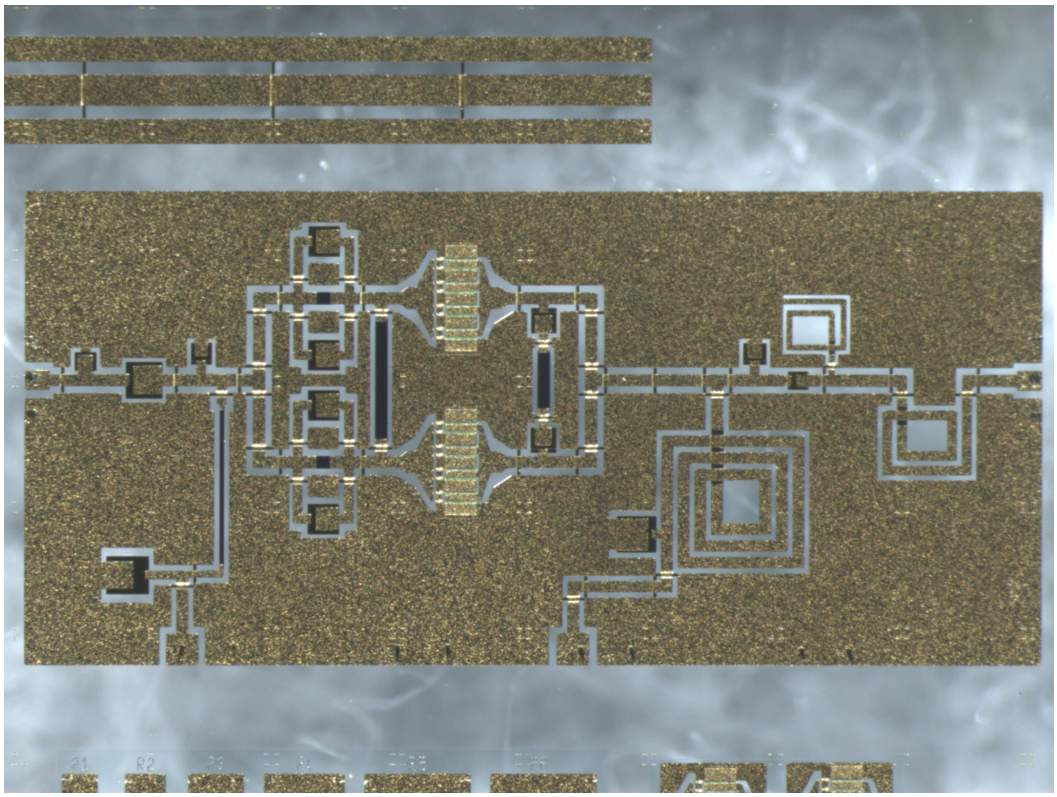

Figure 3.48: A top view of manufactured PA

Gain measurements will be presented after definition of setup. Measuring fabricated PA is performed with Network Analyzer (NA). Calibration of NA has

been done in a frequency range that includes operating frequency band of the device. After calibration, manufactured PA is probed via using DC and RF probes. Finally, gain measurement data are recorded.

Gain measurement setup is shown in Figure 3.49.

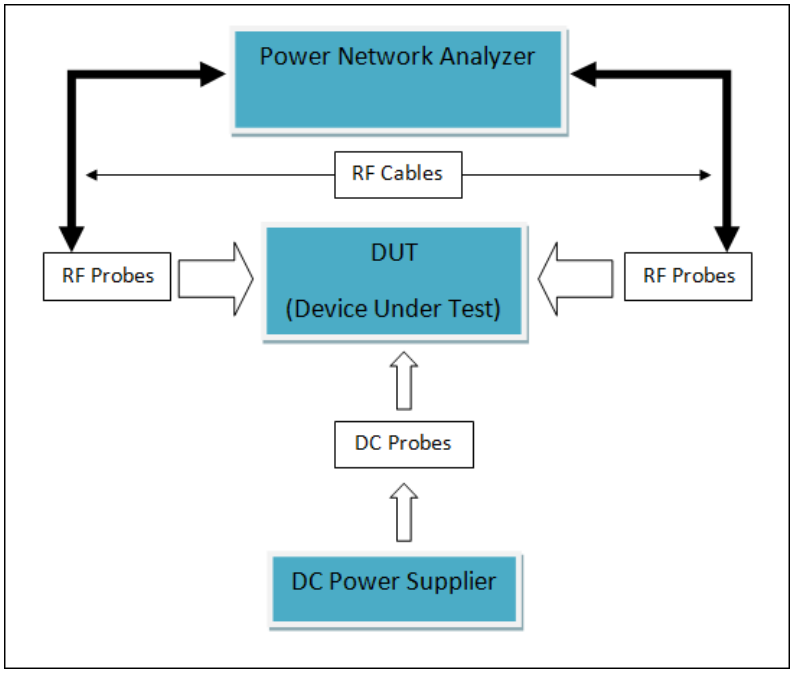

Figure 3.49: A view of setup for gain measurements

After analyzing measurement data, they are compared with simulation results as seen in Figures 3.50 and 3.51. It was indicated that transistor model is called 8x125 in Section 3.2. Two different transistor data were specified for comparison. These transistors are exactly the same. The photo-mask has separate transistors to check the performance. These data were recorded from different manufactured MMIC wafer, which were fabricated in the same manner. First transistor data had been also used during the design of the PA and second transistor data was newly measured from manufacturing PA wafer for verifying fabrication accuracies. In addition, it is safe to do comparison between simulation and measurement results of manufactured PA by this way again.

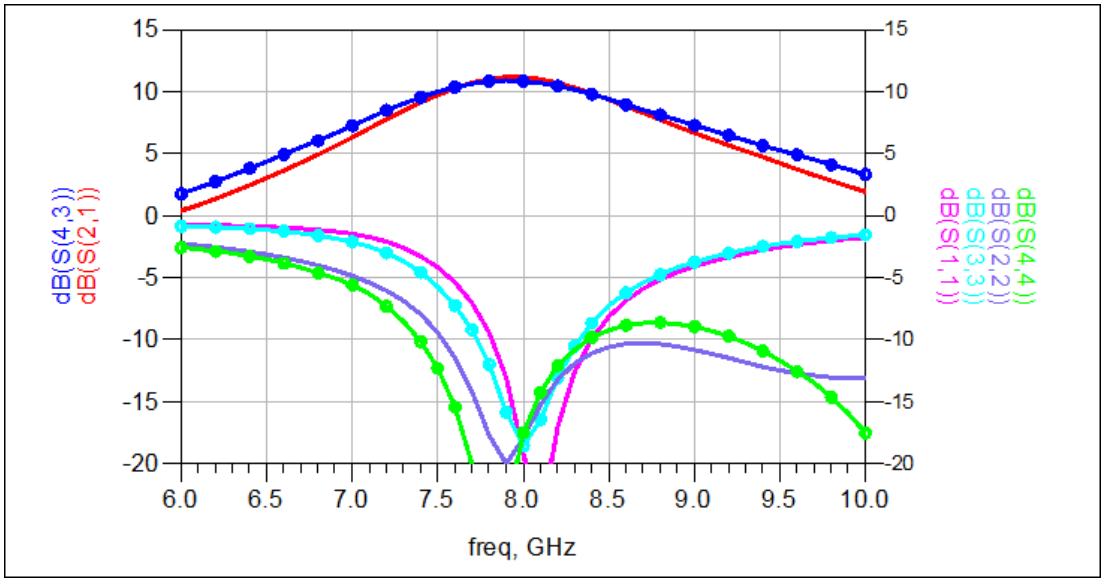

Figure 3.50: Comparison of simulation and measurement (circled lines) results; gain and reflection changes with frequency (in dB scale) of manufactured PA with second (new) transistor data

Figure 3.50 shows comparison of measurement and simulation results with second transistor data. Circled lines belong to measurements of realized PA in the figure. Results are clearly presented in Table 3.1. Measured gain varies between 9.8 dB and 10.9 dB. It can be said that frequency band shifted downward approximately 0.3 GHz. In addition, reflection performances are adequate at operating frequency except 8.4 GHz. This circumstance again results from shifted operating frequency.

On the other hand, manufactured PA does not show any oscillation characteristic during measurements. Therefore, it can be said that resistive characteristic of fabrication is very similar with predictions and consistent with simulation parameters.

Table 3.1: Measurement and simulation results of manufactured PA with second (new) transistor data

	S11(dB)	S22(dB)	S21(dB)
@7.9 GHz (Measurement)	-15.8	-24	10.9
@7.9 GHz (Simulation)	-13	-20	11.2
@8.2 GHz (Measurement)	-13	-12	10.5
@8.2 GHz (Simulation)	-17	-13.2	10.7
@8.4 GHz (Measurement)	-8.7	-9.8	9.8
@8.4 GHz (Simulation)	-9.9	-11	9.9

Gain and return losses are plotted again with using transistor data that had been used in simulations, as seen in Figure 3.51. Downward shift is explicitly seen. Midpoint of band is at 7.9 GHz instead of 8.2 GHz according to measurement results of fabricated device. However, RF characteristics consistent with simulations, which were performed by first transistor data.

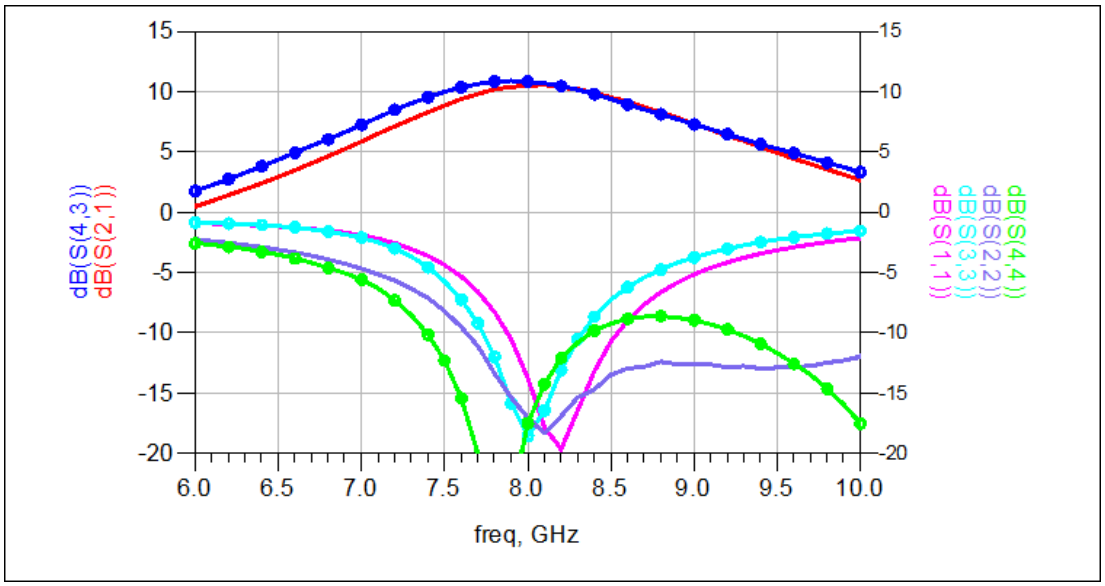

Figure 3.51: Comparison of simulation and measurement (circled lines) results; gain and reflection changes with frequency (in dB scale) of manufactured PA with first (old) transistor data

Table 3.2 obviously presents comparison between simulation results and measurements. Simulations were repeated with first transistor data to verify design with fabrication. Gain is the same along frequency band except 7.9 GHz and measured reflection performances become worse than simulation results.

Table 3.2: Measurement and simulation results of manufactured PA with first (old) transistor data

	S11(dB)	S22(dB)	S21(dB)
@7.9 GHz (Measurement)	-15.8	-24	10.9
@7.9 GHz (Simulation)	-10.5	-15.4	10.4
@8.2 GHz (Measurement)	-13	-12	10.5
@8.2 GHz (Simulation)	-19.6	-16.9	10.4
@8.4 GHz (Measurement)	-8.7	-9.8	9.8
@8.4 GHz (Simulation)	-13.2	-14.7	9.9

Finally, it is clear that fabricated PA properly works in terms of gain and stability. Measurements and simulation results are so close to each other. Additionally, fabrication was verified by a set of simulations. Furthermore, it is obvious that transistor impedances are affected by the gate formation. There is not dielectric thickness variation for this fabrication but if there was, it would affect internal capacitances of transistor.

As a result, a stable PA was manufactured and it has approximately 10.5 dB gain.

3.8 Power Measurement Results of Power Amplifier

Output power level of an amplifier is another important feature. At very beginning of the design gain and output power goals were defined. Gain results are presented in Section 3.7 and P_{out} is shown in this section based on desired output power level.

Figure 3.52 presents a view of power measurement setup. Setup is calibrated at 8 and 8.4 GHz. After calibration, manufactured PA is probed via DC and RF probes. Finally, output power level is measured by power meter at defined frequencies with activating PA by signal generator.

If the power measurement system is deeply analyzed, it is noticed that during calibration approximately 31.5 dB loss is observed in output side. Measured losses result from cable (1 dB), attenuator (30 dB) and RF probe (0.5 dB). Therefore, measured total losses added to power value that read on power meter. These losses show approximately 0.5 dB alteration from 8 GHz to 8.4 GHz.

In consideration of setup analysis, power measurements were performed at 8 GHz and 8.4 GHz till the 2.8 dB and 2.1 dB compression points, respectively. Linear operation specifications lead to limit compression point up to maximum 2 dB. Therefore, manufactured PA is measured up to 2.8 dB compression point.

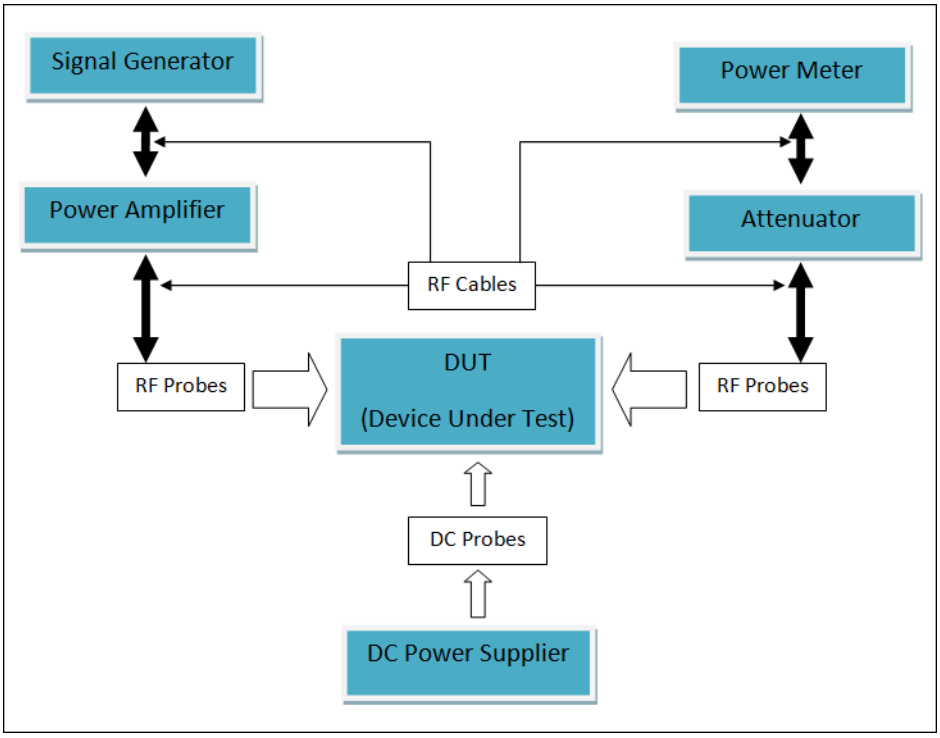

Figure 3.52: A view of setup for output power measurements

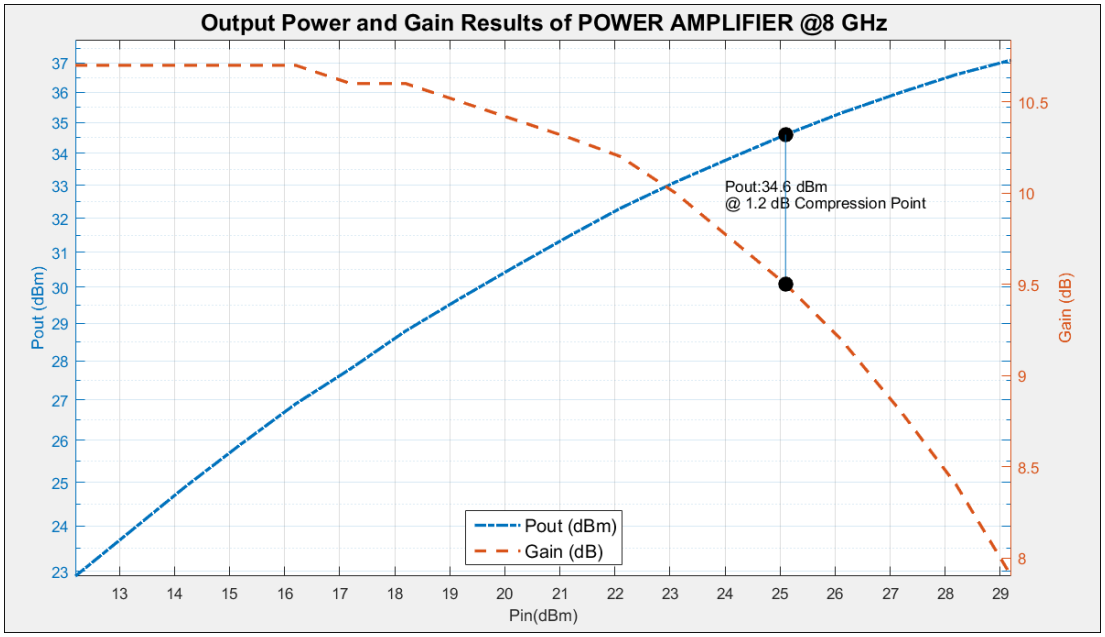

Figure 3.53: The output power measurement result at 8 GHz

Figures 3.53 and 3.54 present measured output power level of the PA. P_{out}

equals to 34.6 dBm at 8 GHz and 36.6 dBm at 8.4 GHz about 1.2 and 1.3 dB compression points, respectively. When input power increases, output power and compression level of the PA also increases. Therefore, output power reaches 37.1 dBm at 8 GHz and 37.8 dBm at 8.4 GHz about 2.8 and 2.1 dB compression points, respectively by increasing input power.

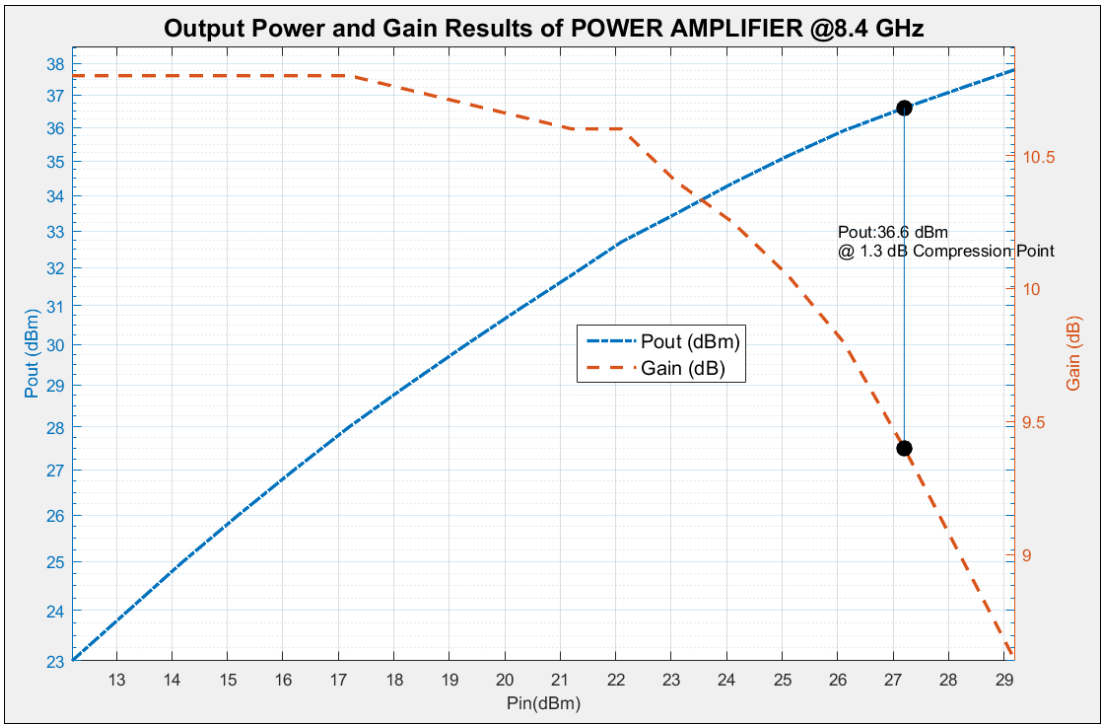

Figure 3.54: The output power measurement result at 8.4 GHz

Furthermore, it should be indicated that the small measurement differences are sometimes observed in available gain level of fabricated PA because of measurement setups. Gain measurements are performed by NA, which is calibrated via proper cal kit. However, output power measurement setup is calibrated by low loss TLIN element. In addition to, internal amplifier, signal generator and cables are checked in this way. However, exact loss difference between 8 and 8.4 GHz (400 MHz range) of setup is not directly distinguished. These differences can be called as measurement errors. Internal amplifier that adjusts input power level of testing device, is used in input side of output power measurement setup. This amplifier begins to start working properly after a required input signal level.

Finally, maximum output power of manufactured PA equals to 5.1 W and 6 W at 8 GHz and 8.4 GHz, respectively. Although higher output powers were attained from other fabrications, which are processed in the same way, this level is adequate to achieve desired goals. Additionally, efficiency calculation is performed for compression case at 8.4 GHz and it is resulted that fabricated PA design works with 40 % efficiency as seen in Eq. (3.5). It should be noticed that two transistors totally draw 600 mA current under 2.1 dB compression, when drain side is biased with 25 V.

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{6\ Watts}{25\ V \times 600\ mA} = 40\ \% \tag{3.5}$$

3.9 Design of Passive Elements and Verifying Fabrication

Designing passive elements plays significant role in matching PA's source and load impedances to desired value. In this respect, each passive element has been designed and simulated before constructing matching networks. Additionally, passive element simulations are compared with measurement results to validate MMIC fabrication. Substrate properties have been defined based on known material features and previous experiences. In the light of these information passive element designs and validation steps are presented in this section.

Capacitor, inductor and resistor values have been calculated from ABCD and Y parameters, respectively during designing matching networks. These parameters have been derived from S-parameters, which are the main output of ADS momentum. Mathematical equations of passive elements are shown in Eqs. (3.6), (3.7), (3.8) and (3.9). These conventional relations are derived by transformation of S-parameters to Y parameters and ABCD-parameters [20]. They are also checked with ADS momentum equations [9] for affirmation.

$$R = -real(\frac{1}{Y(1,2)}) \tag{3.6}$$

$$L = \frac{-imag(\frac{1}{Y(1,2)})}{2 * \pi * f} \tag{3.7}$$

$$C = \frac{\frac{1}{-imag(ABCD(1,2)}}{2 * \pi * f} \tag{3.8}$$

$$C_{Shunt} = \frac{imag(ABCD(2,1))}{2 * \pi * f} \tag{3.9}$$

Two different series capacitors were added to mask design apart from transistor and PA designs. After manufacture, capacitor measurements are compared with simulation results. It is the most critical analogy due to importance of dielectric material thickness. In addition, inductor and resistor simulations are matched against fabrication results.

Designed resistor has been used for biasing gate voltage. Simulations based on indicated substrate properties in Subsection 3.4.1 are performed. Sheet resistance of the material equals to 15 $\Omega/\square$. After performing resistor simulation, S-parameters have been extracted from recorded data. In addition, resistor value is also calculated using Eq. (3.6).

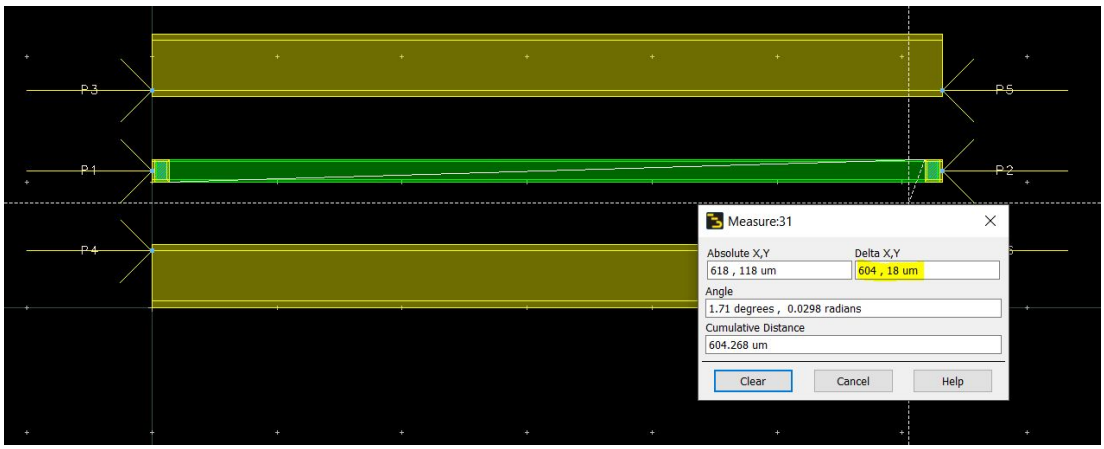

Figure 3.55: Designed resistor layout

Figure 3.55 shows layout of designed resistor, which equals to 500 Ω. Resistor dimension equal to $604x18$ μm^2. Below calculation shows desired resistor value.

$$\frac{604\mu m}{18\mu m} = 33.5 \text{ Squares} \Longrightarrow \text{R} = 15\ \Omega/\square\ *\ 33.5\ \square = 502.5\ \Omega$$

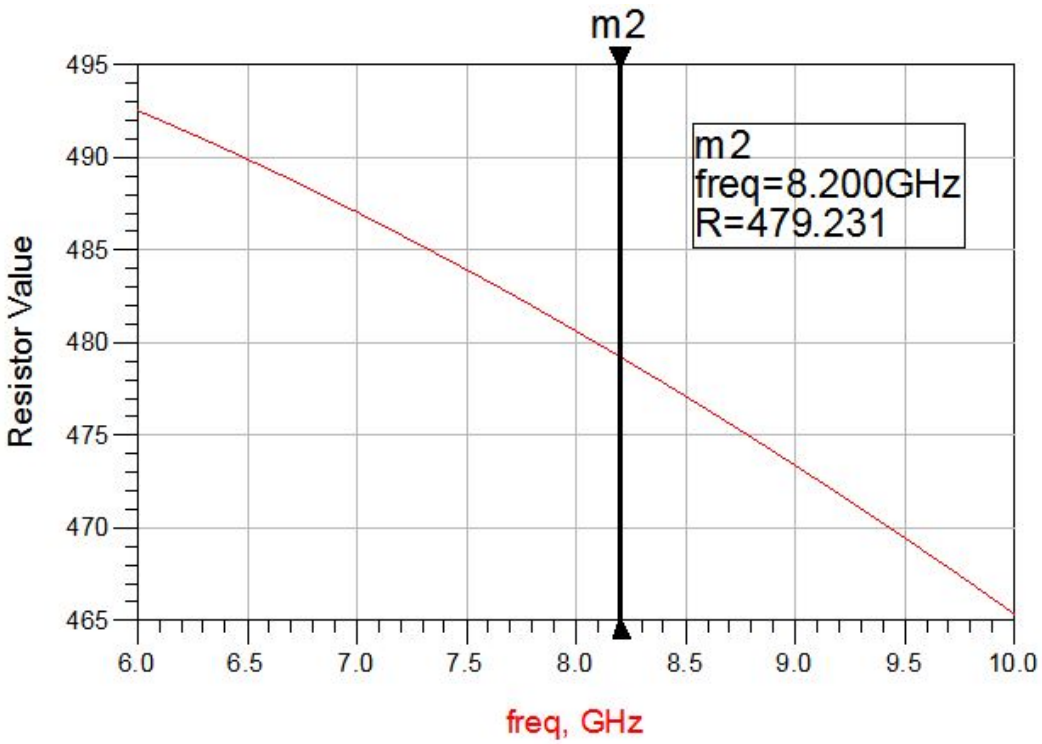

Figure 3.56: Simulation result of designed resistor

Simulated resistor value is shown in Figure 3.56. It approximately equals 479 Ω at 8.2 GHz. Thus, it can be said that hand calculation and simulation results are so close to each other. Approximately 20 Ω difference is originated from additional TLINs, which are placed on starting and end points of resistor layout. Furthermore, this small difference is compensated with tuning other components, which have resistive effects.

On the other hand, inductor values are not directly determined. However, inductor layouts are designed by taking into consideration fabrication restrictions. Gap, which is center vacancy of each inductor, has chosen at least $70\mu m$. Calculating inductive values of TLINs is done by ADS line calculation tool. Additionally, matching networks may be in need of longer TLINs. In such cases if this type of bended inductors are used instead of TLINs, required area is reduced.

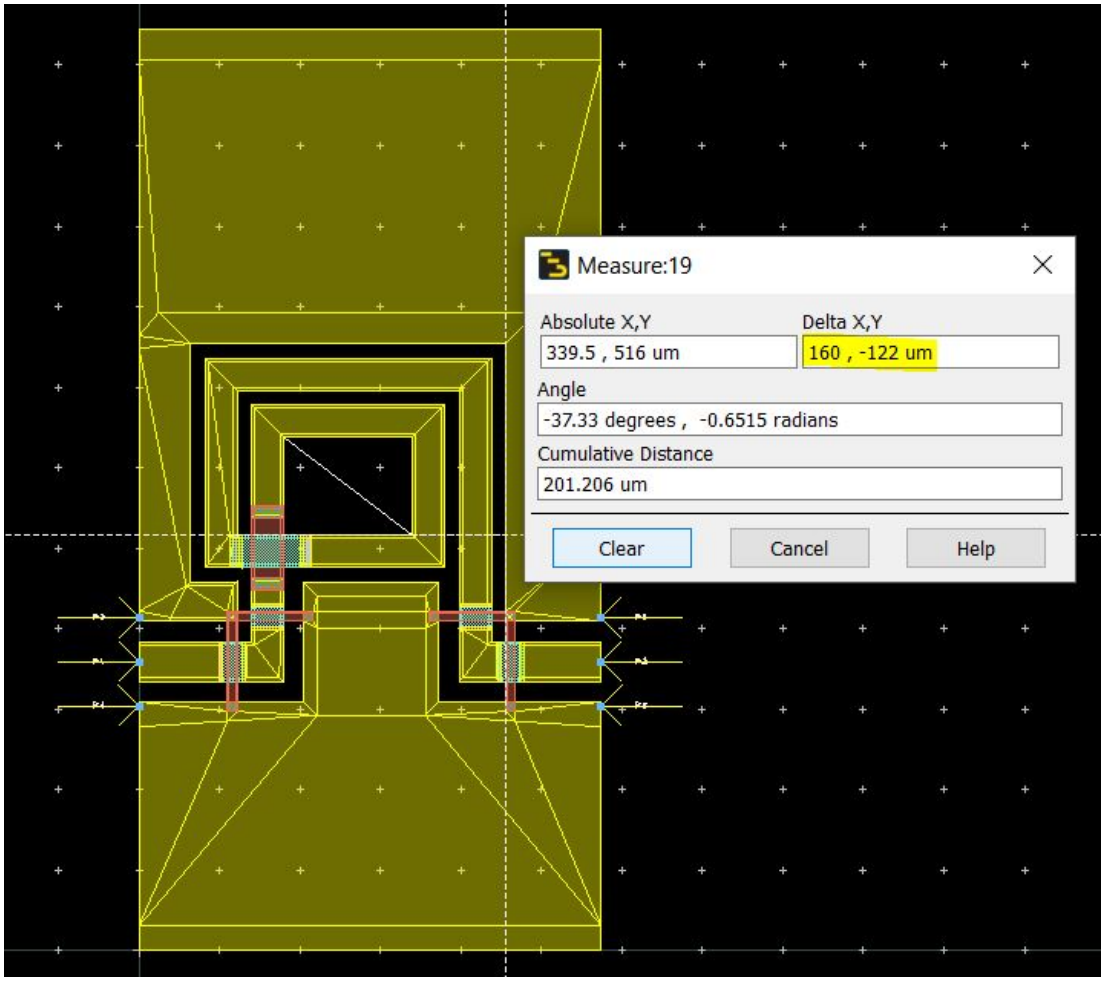

Figure 3.57: Designed inductor layout

Designed inductor layout is presented in Figure 3.57. It has been used at the output stage of the designed PA. 1 nH inductor is required at 8.2 GHz. Gap area of 1 nH inductor equals to $160x122$ μm^2 to match against fabrication restrictions.

As a result, designed inductor value was simulated using Eq. (3.7) and result is shown in Figure 3.58. Inductor value equals to 1 nH and it does not change too much in operating frequency.

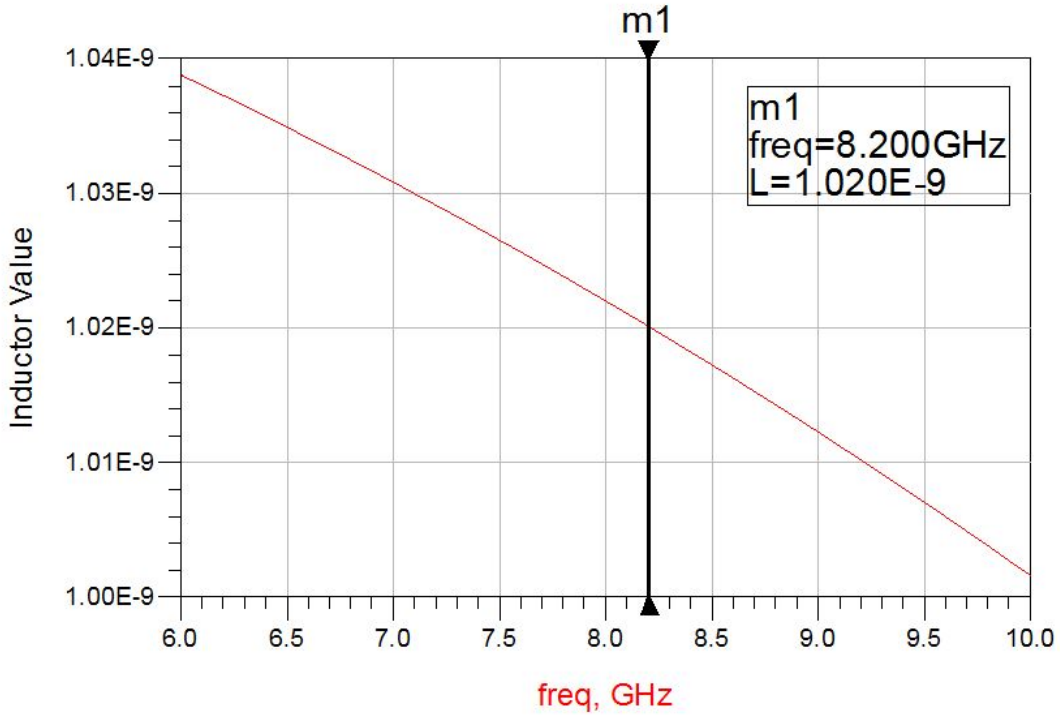

Figure 3.58: Simulation result of designed inductor

Finally, simulations based on defined formulas and measurement results of two different capacitors have been presented in this section. Calculations have been done using conventional formula of capacitance, Eq. (3.10), which is confirmed by Bahl analyses [19]. κ equals to 7.5 as dielectric constant of defined material. Vacuum permittivity equals to $8.8562x10^{-12}$ F/m. "A" is the capacitor area and "d" is the dielectric thickness, which equals to 300 nm. In addition, substrate properties are explained in Section 3.4.1 in detail.

$$C = \frac{\kappa \varepsilon_0 A}{d} \tag{3.10}$$

Capacitors, whose layouts are shown in Figure 3.59, are designed to verify the substrate. Dimensions of the capacitors equal to $89x80$ μm^2 and $79x60$ μm^2, respectively. Their values equal to 1.576 pF and 1.049 pF, which are calculated using Eq. (3.10).

$$C_1 = \frac{7.5 \star 8.8562 \times 10^{-12} \star 89 \times 80 \times 10^{-12}}{300 \times 10^{-9}} \text{ F} = 1.576 \text{ pF}.$$

$$C_2 = \frac{7.5 \star 8.8562 \times 10^{-12} \star 79 \times 60 \times 10^{-12}}{300 \times 10^{-9}} \text{ F} = 1.049 \text{ pF}.$$

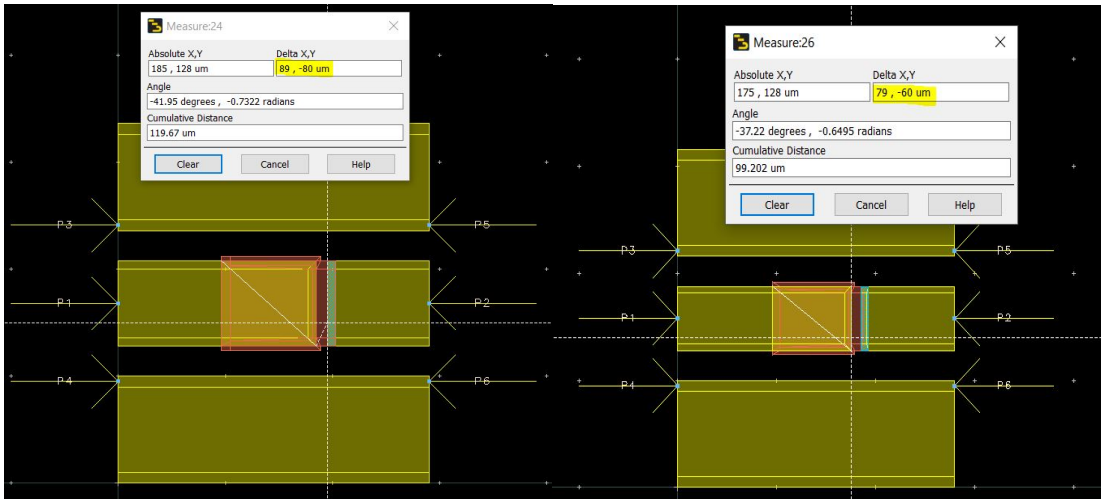

Figure 3.59: Layout design of capacitances (C_1 on left and C_2 on right)

Simulations and measurements of C_1 are presented in Figure 3.60. Desired capacitance value approximately equals to 2.8 pF. Therefore, it is noticed that simulations are in good agreement with fabrication results. Approximately 1.3 pF difference between hand calculations and simulations are originated from additional TLINs, which are added to the design to perform measurements. However, coherence of simulation and measurement results are more important. In this case, measurement and simulation results are very close to each other as shown in Figure 3.60.

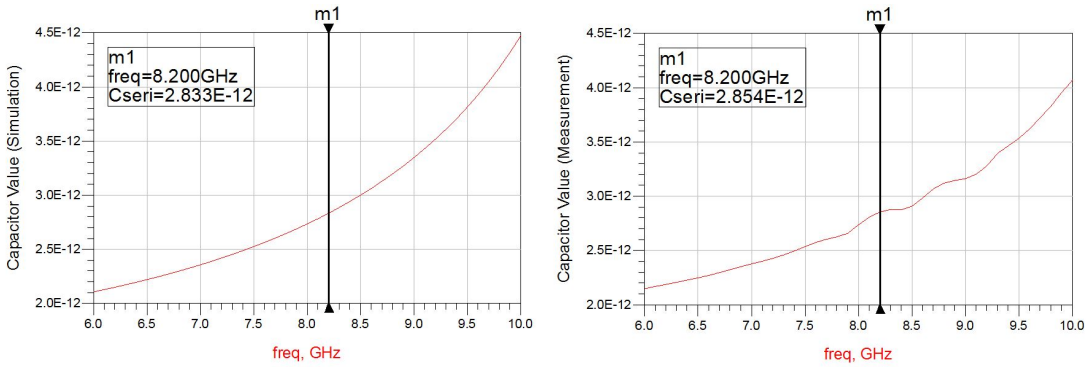

Figure 3.60: Simulation (left) and measurement (right) results for C_1

Simulation and measurement results of C_2 is presented in Figure 3.61. They are almost the same. When the results are compared with hand calculations, it is obvious that difference is roughly 0.5 pF. Calculated C_2 is 1.049 pF and according to results, it approximately equals to 1.5 pF. As a result, when desired value of capacitance decreases, differences between hand calculation and measurements and simulation results vanish.

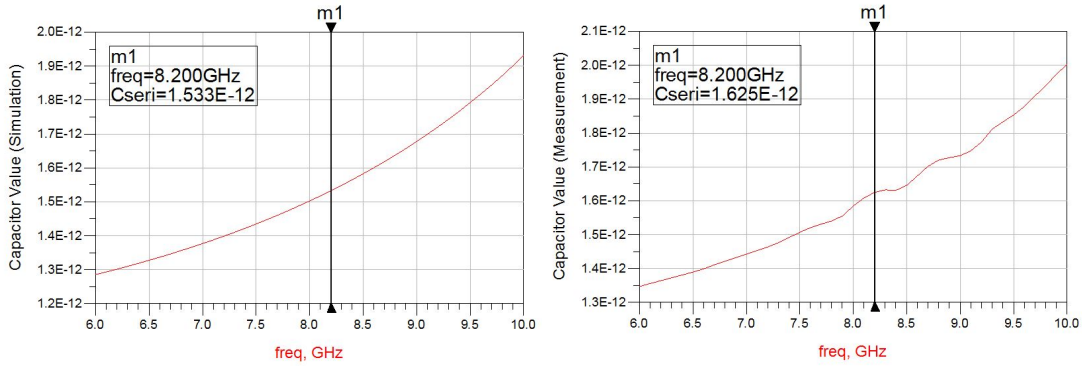

Figure 3.61: Simulation (left) and measurement (right) results for C_2

Finally, the design steps of passive elements are clearly explained and verification of process is demonstrated by comparison of simulation and measurement results of capacitors. It is noticed that there can be 0.3 pF difference between simulation and measurement results. The difference is resulted from dielectric material thickness, which is rarely changed in some fabrications.

Chapter 4

Wilkinson Power Divider

4.1 Basic Properties of Wilkinson Power Dividers

Splitting the available power is essential for many RF applications. WPDs are used for obtaining a MMIC PA together with relatively high output power by connecting three PAs in parallel. From this point of view, basic properties of WPDs are presented in this section by definition of theoretical information. In addition, only divider properties are analyzed because dividers and combiners reciprocally show the same RF characteristic.

Decreasing total IL of designed WPD is the main desired goal. IL, which is determinant of transfered power level of an N-way WPD. Calculations of IL are done using Eq. (4.1). In the equation, n takes a value from 2,3,...,N and input power is equally divided by N times. IL theoretically equals to 4.77 dB as shown in Eq. (4.2) for a three-way, equal split WPD.

$$S_{1n} = -10\log_{10}\frac{1}{N} \tag{4.1}$$

$$S_{1n} = -10\log_{10}\frac{1}{3} = 4.77 \text{ dB} \tag{4.2}$$

The main purpose of WPDs is to divide the acquired power without phase differences between each branches. In addition, high isolation should be provided among three output ports to reduce coupling effects. Characteristic impedance of each branch equals to $Z_0\sqrt{3}$ and isolation resistor equals to Z_0 with respect to common node of all output ports to design proper WPD [21]. Where Z_0 equals to 50 Ω in this work. Additionally, length of each branch equals to $\lambda/4$ independent from number of branches [13].

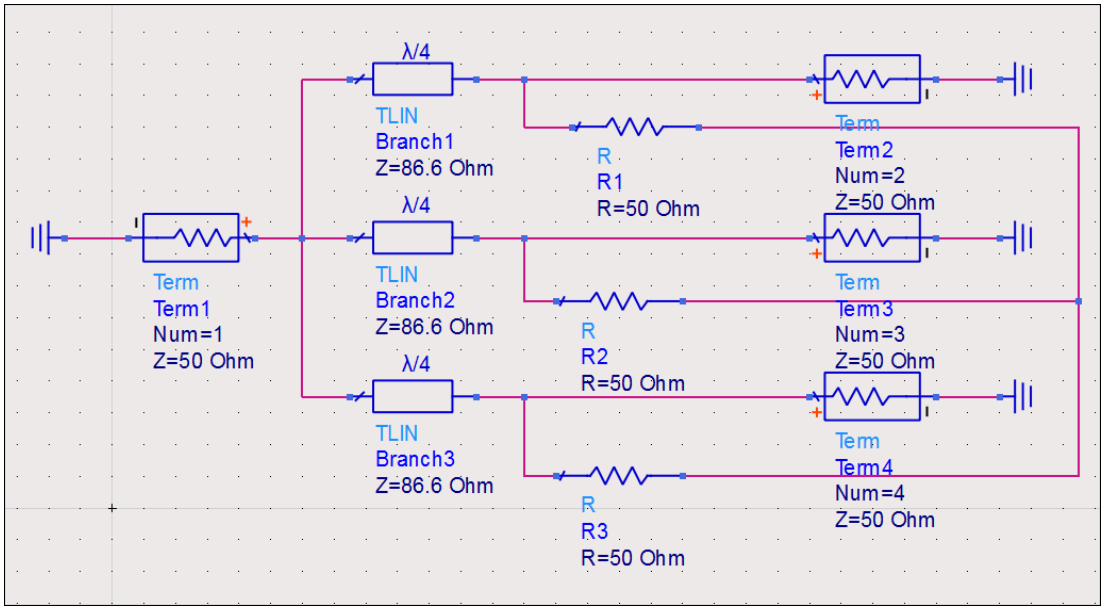

Figure 4.1: A schematic view of equal, three-way WPD circuit

A schematic view of equal, three-way WPD circuit diagram is shown in Figure 4.1 [13]. Isolation resistor values are defined according to common node in the figure but in MMIC technology the values change because of process. Air-bridge structures are used to construct desired topology. Isolation resistor between side branches is connected using air-bridges. In addition, bond wire structures are also used instead of air-bridges as shown in Figure 4.2 [21]. However, bond wire structures are relatively lossier than air-bridges.

On the other hand, there are different types of equal, N-way WPDs such as radial, fork and so on. They are constructed using number of needed two-way unequal WPDs [21].

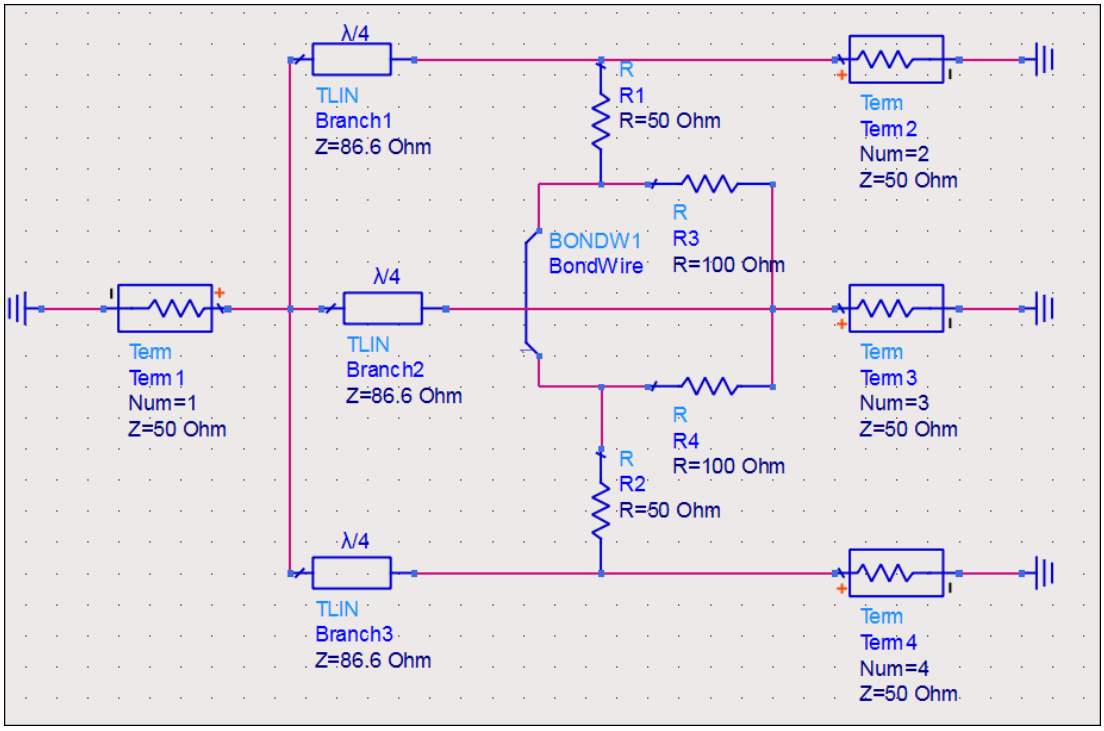

Figure 4.2: A schematic view of equal, three-way WPD circuit with different topology

Finally, designing a small size MMIC becomes compulsory for many projects because technological improvements need the small systems. At this stage, different matching topologies and TLIN shapes are usually used in to reduce total size of the design and obtain compact MMIC PA chips. The circuit model of TLIN gives designers chance to match a WPD by using additional capacitors and inductors. One of the popular technique is adding an extra capacitor to branches [11]. Secondly, WPDs' IL level and isolation between output ports are tuned to desired dB levels by inductive loading techniques and using stubs [22]. Additionally, coupled line structures are used in reducing WPDs sizes [23]. These techniques are theoretically suitable for N-way WPDs.

4.2 Wilkinson Power Divider Design in ADS Momentum

Designing a WPD is a part of this thesis. The output power of design increases by paralleling three PAs in a MMIC. To combine them, a WPD is designed at desired operating frequency, which is presented in this section. However, layout and mask design steps are not expressed in detail because they have been already analyzed in the previous chapters.

According to Figure 4.2 in Section 4.1, initial design is performed in ADS Momentum [9]. After tuning initial design parameters, required physical dimensions of WPD are defined. The distance between each adjacent output ports approximately equals to 750 μm, if coupling effects and physical distance requirements of PAs are taken into consideration. Therefore, lengths of isolation resistors are increased. In addition, reflection performances are hardly improved because of fabrication restrictions.

On the other hand, it is expected that fabricated WPD will work with lower loss than simulation and because of decreased conductivity.

Layout of designed WPD is presented in Figure 4.3. Isolation resistor values between side branches and middle to side branch approximately equal to 130 Ω and 150 Ω , respectively. The resistive effects of TLIN piece and air-bridge that are used in connecting resistors, circled in white in the figure.

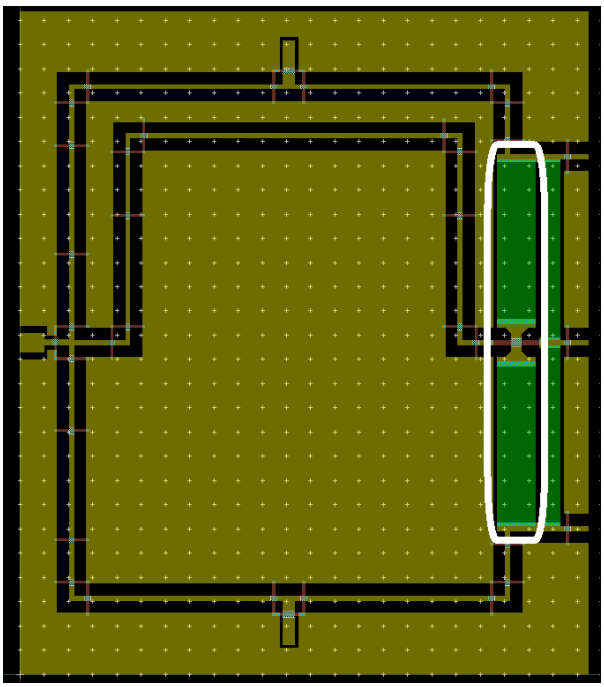

Figure 4.3: Layout of designed WPD

Lengths of side branches and middle branch equal to approximately 3000 μm and 3300 μm, respectively instead of 9146 μm that corresponds to $\lambda/4$ at 8.2 GHz. It is clear that the dimension of WPD was dramatically reduced. In addition, line impedances were tuned and open stubs were added to middle of side branches as presented in Figure 4.3 to reduce the branch lengths. Other mission of the stubs is to diminish the asymmetry effects of middle branch.

As a result, design of WPD gives chance to reduce total dimension of designed MMIC PA, if the branches are meandered using available ground space. Therefore, designed WPD dimension can be scaled based on required MMIC effective area.

After finishing the design, WPD photo-mask was prepared. It is shown in Figure 4.4 and two WPDs were connected back-to-back in order to perform measurements via two-port network analyzer. Finally, IL was measured after manufacturing the design.

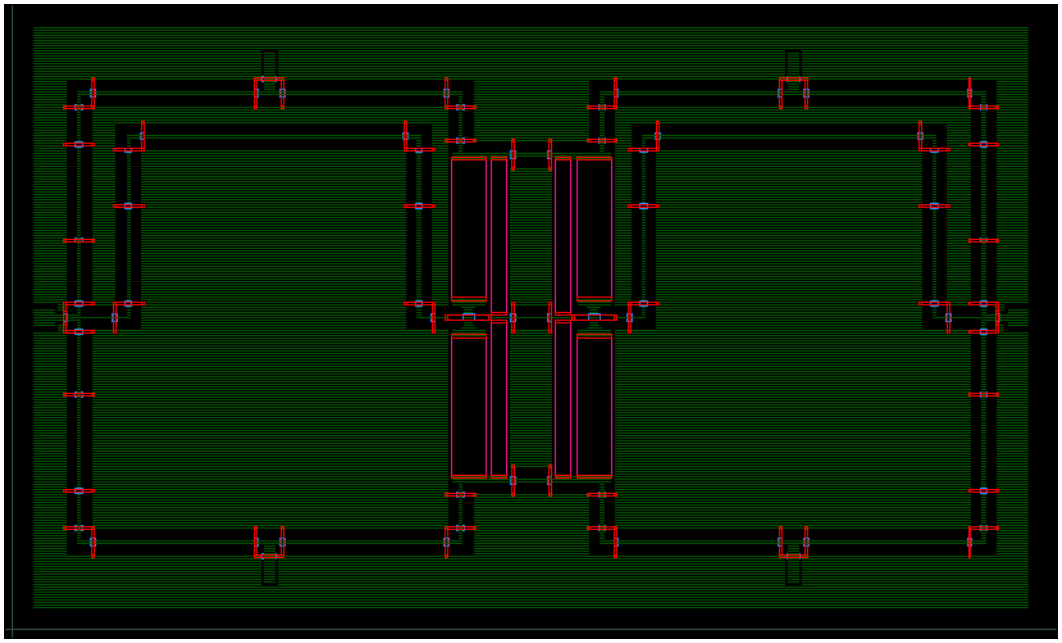

Figure 4.4: A figure of WPD Photo-Mask

4.3 Comparison of Simulation and Measurement Results of Manufactured Wilkinson Power Divider

After finishing fabrication, measurements have been performed via NA. Detailed information about NA and measurements are described in Section 3.7.

Simulation results are shown on top of the measurement results in Figure 4.5. As it is expected, decreased conductivity and low IL directly affect RF characteristic of designed WPD.

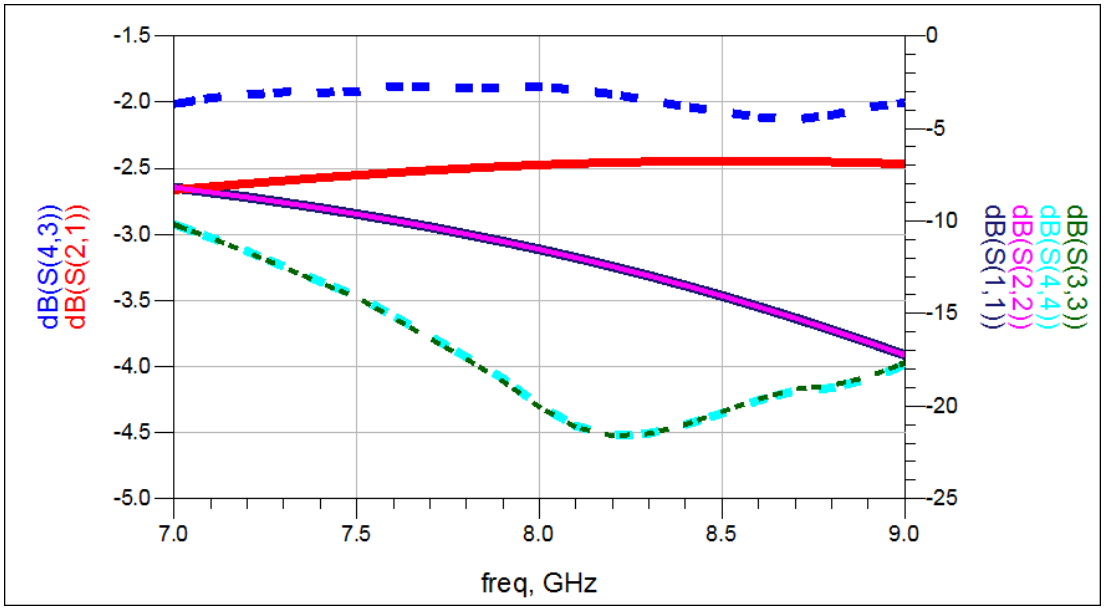

Figure 4.5: Comparison of measurements (dotted lines) and simulation results of designed WPD

According to measurements, IL of designed WPD equals to approximately 0.9 dB (dotted line) through frequency band instead of 1.25 dB (solid line, simulated WPD). Furthermore, return losses are smaller than -10 dB at operating frequency in simulations. Conductivity decreases because of fabrication conditions including temperature effects, metal thickness variations and so on. Therefore, fabricated WPD RL is improved to -17 dB or lower levels. The values are enough to combine

three PAs and to increase output power of fabricated MMIC PA.

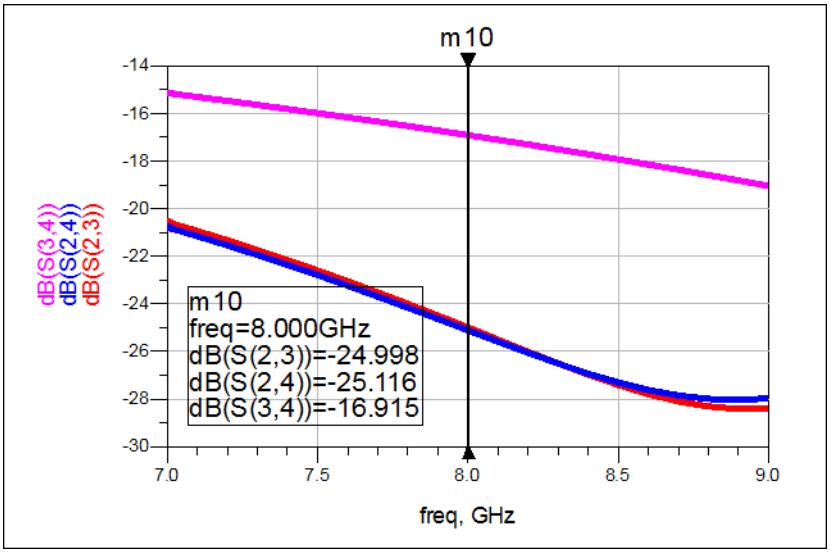

Figure 4.6: Isolation between output ports of simulated WPD design

Additionally, isolation between output ports has been analyzed according to only simulation results because of measurement restrictions. Figure 4.6 shows that output ports are perfectly isolated from each other. S(3,4) parameter indicates isolation between side branches and other parameters indicate isolation between side branches and middle branch. S(3,4) has relatively bad performance due to asymmetrical topology of designed WPD but it is in good agreement with desired goals.

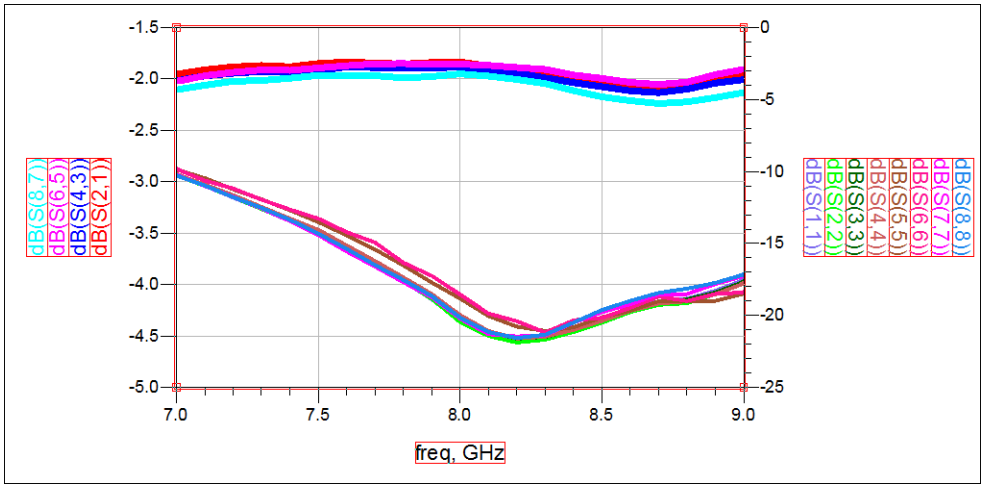

Figure 4.7: Measurement results of the same WPDs from different fabricated wafers

Lots of different measurement results are presented in the same graph to verify fabrications. Additionally, initial predictions about conductivity are proven by measurements in Figure 4.7.

Finally, Figure 4.7 shows that designed WPD can be conveniently used. Manufactured WPD adds approximately 0.9 dB loss and it is suitable for input or output matchings of designed PA. Additionally, it should be noticed that if WPD output ports are directly matched source impedance of PA, designed MMIC dimensions can be decreased. Therefore, total losses can be reduced.

Chapter 5

Conclusion and Future Work

In conclusion, after brief introduction of this study, PAs and their classes were basically mentioned in Chapter 2. According to design requirements and desired goals, X-Band Class AB PA design steps were presented in Chapter 3. Finally, an equal, three-way WPD design was reported in Chapter 4.

The design foresights, possible encountered problems and MMIC technology of HPAs had been taken into consideration in Chapter 2. Afterwards, DC bias conditions were defined in Chapter 3 to obtain class AB PA, whose main objective was to stay in near linear region with little distorted output signal waveform. From this point of view, selection of transistor was examined temper to gain, output power and operating frequency. Used transistors in MMIC structures, fabrication techniques, design steps and process limitations were also presented in Chapter 3. After analyzing all required information, the design had been done in ADS momentum. In addition, photo-mask design methods and mask placement conditions were mentioned. According to illuminated process steps, fabrication had been completed. Measurements of manufactured devices were performed and compared with simulation results. Finally, fabrication was verified by comparing of passive device simulation results and measurements in Chapter 3.

On the other hand, an equal, three-way WPD was designed and mentioned in

Chapter 4. Three PAs will be combined by WPD to obtain relatively high output power. At this point, desired goals for WPD design were defined and design steps were shown in Chapter 4. In addition, it was aimed acquiring miniaturized WPD with low IL. Then, simulation results were contrasted with measurements. Finally, it was shown that fabricated WPD gives chance to scale total dimension of MMIC device.

Eventually, manufactured PA works with 40 % efficiency and provides on the average 10.2 dB gain. Maximum output power equals to 36.6 and 37.8 dBm at 1.3 dB and 2.1 dB compression points, respectively at 8.4 GHz. On the other hand, designed WPD works in wide band range with approximately 1 dB IL.

As a future work, designed PA will be connected in parallel using presented WPD design. One driver amplifier will be added in front of paralleled PAs. Therefore, approximately 40 dBm output power and 18 dB gain will be obtained from one MMIC device. In addition, temperature influences on fabricated PAs will be researched, required precautions will be defined and output power performance will be increased.

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