High Performance n-MOSFETs with Novel Source/Drain on Selectively Grown Ge on Si for Monolithic Integration

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Abstracts

We demonstrate high performance Ge n-MOSFETs with novel raised source/drain fabricated on high quality single crystal Ge selectively grown heteroepitaxially on Si using Multiple Hydrogen Anealing for Heteroepitaxy(MHAH) technique. Until now low source/drain series resistance in Ge n-MOSFETs has been a highly challenging problem. Source and drain are formed by implant-free, *in-situ* doping process for the purpose of very low series resistance and abrupt and shallow n^+/p junctions. The novel n-MOSFETs show among the highest electron mobility reported on (100) Ge to-date. Furthermore, these devices provide an excellent I_{on}/I_{off} ratio(4×10^3) with very high I_{on} of 3.23μA/μm. These results show promise towards monolithic integration of Ge MOSFETs with Si CMOS VLSI platform.

Introduction

As Si bulk CMOS devices approach their fundamental scaling limit, diverse research is being done to introduce novel structures and high mobility channel materials to circumvent this limit. The lower effective mass in Ge that leads to higher mobility of carriers compared to Si has prompted renewed interest in Ge-based devices. Moreover, monolithic integration of Ge with Si devices could provide an alternative solution for continued scaling of devices for future nanoelectronics applications. Very promising results for bulk Ge p-MOSFETs have been demonstrated, with up to 4× hole mobility enhancement. However, Ge n-channel MOSFETs have exhibited very poor performance that obstructs CMOS device realization in Ge. The poor passivation of Ge interface is one of the critical challenges. Also, relatively low n-type dopant solubility [1,2] and fast n-type dopant diffusion [3] during dopant activation in Ge make it difficult to fabricate source and drain (S/D) in n-channel Ge MOSFETs. This paper provides a promising approach for high performance Ge MOSFET processing techniques, in particular Ge growth with *in-situ* doping for raised source/drain and monolithic integration of Ge with Si CMOS VLSI platform.

Selective Ge heteroepitaxial growth

The initially deposited rough Ge surface due to the lattice mismatch with Si, characterized by islanding is considerably smoothened by a high temperature hydrogen annealing [4]. On this smooth layer, second epitaxial growth is performed, followed by another hydrogen annealing until desired epi layer thickness is reached. This MHAH procedure is performed on selectively grown Ge on Si through a SiO_2 window for monolithic integration (Fig 1). Under low deposition temperature (600°C) and partial pressure (8Pa), excellent selectivity is obtained, with Ge deposited only on the exposed Si surface and not on the oxide region. However, when either the temperature or pressure is increased, Ge can nucleate more easily on SiO_2 surface, and selectivity tends to be degraded. The reduction in the Ge nucleation density comes at the expense of lower Ge growth rate, thus a compromise may be needed when choosing the growth condition for selective Ge growth. After 4 cycles of deposition and hydrogen annealing on the selective area(50μm × 50μm), the root mean square (RMS) roughness of the resulting film was determined to be 0.65 nm by atomic force microsco microscopy (AFM) scans on 10 μm ×10 μm area (Fig. 2, 3). Due to the multi-step Ge growth, H_2 annealing, and dislocation trapping by SiO_2 sidewall on the selective area, high quality Ge film with minimal dislocation density ($<10^7 cm^{-2}$) can be achieved at the smaller window size (Fig. 4). The undoped epitaxial Ge layer shows a slightly p-type ($5\times10^{14} cm^{-3}$) characteristic.

Ge n^+/p junction diode characteristics

For an abrupt and box shape n^+/p junction in Ge, in-situ doping with phosphorus (P) using PH_3 is applied during the epitaxial growth. A four-point probe method was used to measure the sheet resistance of n-type in-situ doped Ge layers. The resistivity of this P-doped Ge layer decreases monotonously with increase in $F(PH_3)/F(GeH_4)$ mass-flow ratio until it reaches a minimum value and eventually increases due to the formation of poly-crystalline Ge (Fig. 6). The growth rate is relatively independent of the mass-flow ratio, and mainly depends

on the growth temperature. Measured growth rates are 65, 53.5, and 43nm/min at the growth temperature of 600, 500, and 400^oC, respectively. At 600^oC growth temperature, the resulting n^+/p junction has a junction depth of 97nm and a peak electrically activated concentration of 2×10^{19} cm^{-3} (Fig. 7(a)). Larger junction depth (122nm) was obtained in the ion implanted sample annealed at 600^oC for 1min. Table 1 compares the results of both techniques. The *in-situ* doped profile also exhibits an abrupt edge near n^+/p junction indicated by spreading resistance probe (SRP) data yielding a decay slope of the P concentration of 13 nm/decade, while 24 nm/decade was measured from the ion implanted sample (Fig 7 (a), (d)). The n^+/p junction formed by *in-situ* doping at 600^oC shows better diode characteristics with 1.1×10^4 on/off ratio and high forward current density (120A/cm^2 at 1V) than conventional ion-implanted junction which has 1.37×10^3 on/off ratio and 15 A/cm^2 forward current density at 1V (Fig. 8). This is despite the fact that the *in-situ* doped sample has slightly lower peak electrically active dopant density (2×10^{19} cm^{-3}) than the ion implanted sample (5×10^{19} cm^{-3}). This result can be attributed to the fact that the *in-situ* doped diode sample does not suffer from defect formation and transient enhanced diffusion and thus has more uniform box shape profile.

Ge n-MOSFETs

Device fabrication

A 500-nm-thick SiO_2 film was thermally grown on a lightly doped p-type (100) Si substrate at 1100 ^oC. The SiO_2 film was then patterned by dry-etching followed by wet-etching to define desired locations for Ge growth. The wafer was cleaned according to the standard Si wafer cleaning process and immediately loaded into an Applied Materials Centura RP-CVD epitaxial reactor. Selective MHAH technique was used to grow high quality single crystal Ge on Si for Ge n-MOSFET fabrication (Fig. 9). This technique naturally provides a device isolation structure. Based on the n^+/p junction technique mentioned above, optimized S/D engineering techniques were implemented to fabricate raised S/D Ge n-MOSFETs. The interface engineering technique including GeO_2 passivation was implemented by plasma radical oxidation after a thin Si layer growth (1-1.5nm) on epi-Ge. By oxidizing Si and then Ge, a SiO_2 (3nm) and GeO_2 (1nm) layer were formed as the gate stack [5].

Device Characterization

Because suppressing off current and maximizing I_{on}/I_{off} ratio are challenging issues concerning Ge nMOSFETs, I_{on}/I_{off} measurement was performed. The Ge n-MOSFETs with W/L_G ratio of 130μm/100μm provide one of the highest I_{on}/I_{off} ratio of 4×10^3 at 1.2V drain voltage and show the off current density of 6×10^{-4} μA/μm. In addition, it exhibits high I_{on} per width (3.23μA/μm) (Fig.10). Effective mobility versus E-field is extracted from Ge nMOSFET by split-CV measurement. For comparison, the Si universal electron mobility is also shown. The data measured from the device show among the highest electron mobility (μ_n) reported on (100) Ge to-date with peak μ_n being around 540 cm^2/V-s (Fig. 12) [6].

Conclusion

We have successfully achieved high performance Ge n-MOSFETs by using novel raised S/D technology on the selectively grown Ge on Si. Excellent diode and transistor on/off ratios are obtained in Ge n-MOSFET. It also shows the highest electron mobility on (100) Ge to-date. This Ge MOSFET fabrication technique shows a promising step toward integrating high performance Ge devices with Si CMOS VLSI platform.

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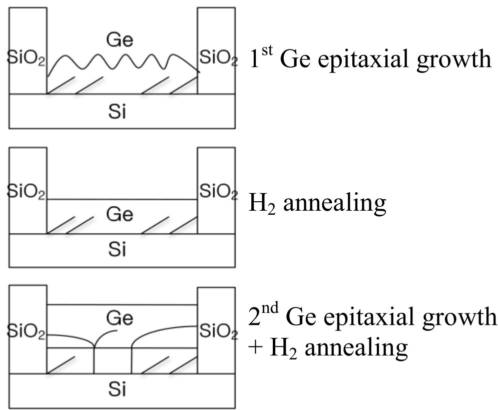


Fig. 1 Process flow schematic of the selective MHAH method to grow high quality Ge layer on Si for the monolithic integration. Here, hydrogen annealing effectively reduces the surface roughness.

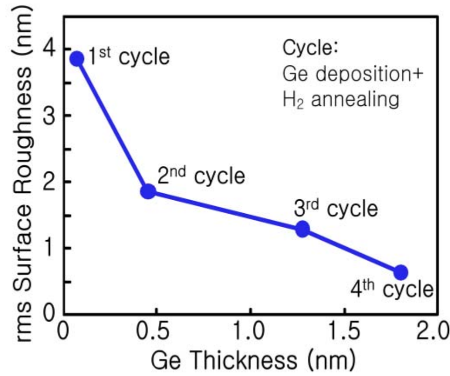


Fig. 2 RMS surface roughness as a function of the thickness of selectively grown Ge on Si. (50μmx50μm SiO_2 window size for Ge growth)

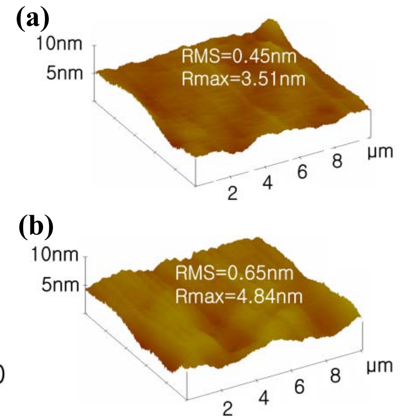


Fig. 3 Tapping mode AFM images of 1.8 μm thick (a) bulk Ge growth and (b) selective Ge growth after MHAH. The RMS surface roughness of (a) and (b) is 0.41 and 0.61 nm respectively.

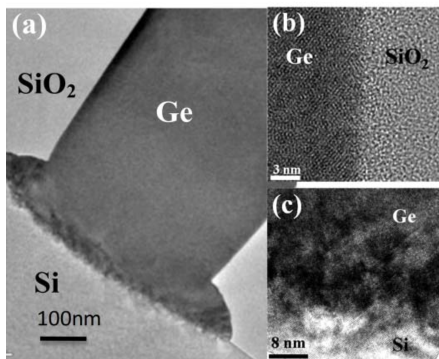
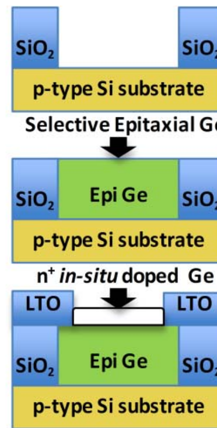


Fig. 4 (a) Cross-sectional TEM image of epi-Ge layer selectively grown on patterned SiO_2/Si with 500nm SiO_2 window width. (b) High resolution image at the interface between Ge layer and SiO_2 side wall. (c) High resolution image at the interface between Ge layer and Si substrate.



- **Open SiO_2 window for Ge growth**
- **Selectively epitaxial Ge growth on patterned SiO_2 window**
- **Isolation using LTO**
- **Etch LTO for n^+ Ge layer**
- **Selectively n^+ *in-situ* doped Ge growth**
- **Electrode deposition (Ti/Al)**
- **Measurement**

Fig. 5 Schematic images and process flow for n^+/p junction formation on selectively grown Ge (undoped epitaxial growth Ge; p-type substrate : 5x10^{14} cm^{-3}) using *in-situ* doped growth method.

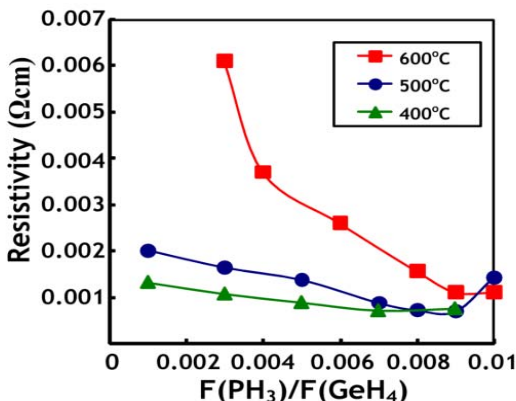


Fig. 6 Resistivity of phosphorus-doped Ge layers as a function of the $F(PH_3)/F(GeH_4)$ mass-flow ratio after *in-situ* doped layer growth.

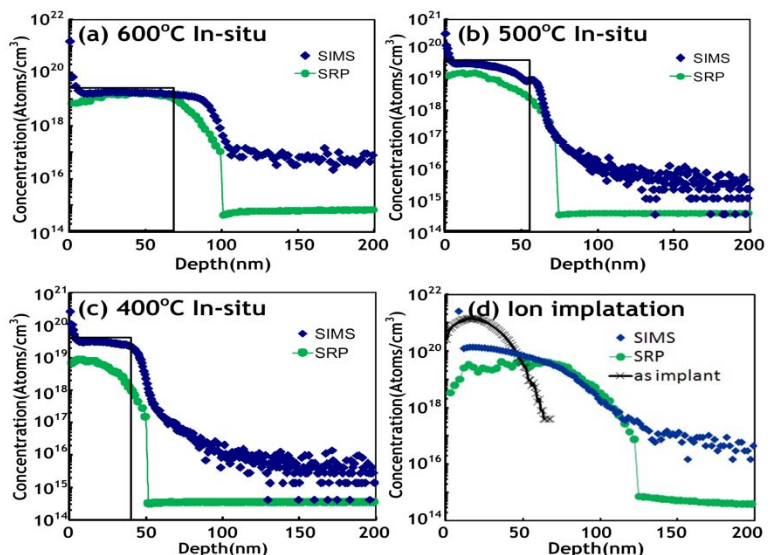


Fig. 7 SIMS and SRP profiles (carrier concentration (cm^{-3}) as functions of depth (nm)) in n^+/p junction using (a) 600°C, (b) 500°C, and (c) 400°C *in-situ* doped Ge layer growth for 1min, and (d) ion implanted Ge annealed at 600°Cfor 1min.
P_{31}+:4x10^{15}cm^{-2} and 18keV

	Abruptness (nm/decade)	Junction depth(nm)	Activation (%)
600°C *in-situ*	13	100	100
500°C *in-situ*	8	75	65
400°C *in-situ*	7	64	30
Ion Implantation	24	122	50

Table. 1 Comparison of Ge n^+/p junctions for different *in-situ* doped Ge conditions and ion implantation with 600°C/1min annealing.

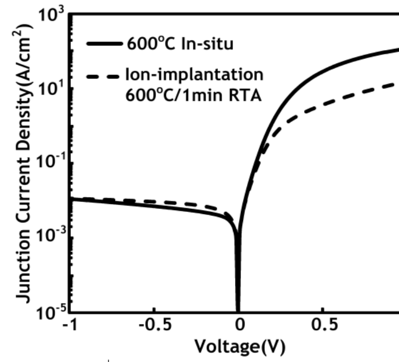


Fig. 8 n^+/p junction current density (A/cm^2) of 600°C *in-situ* doped and ion implantation samples.

- **Thermal oxidation, etch oxide window**
- **Selectively epitaxial Ge growth on patterned SiO_2 window**
- **LTO deposition, etch LTO for S/D**
- **Selectively n^+ *in-situ* doped Ge growth on S/D (a)**
- **Etch LTO on Gate**
- **Si epitaxial growth and plasma radical oxidation(SiO_2/GeO_2) (b,c)**
- **Al deposition and pattern Gate stack(Al/SiO_2/GeO_2)**
- **Forming gas annealing@350°C (d)**

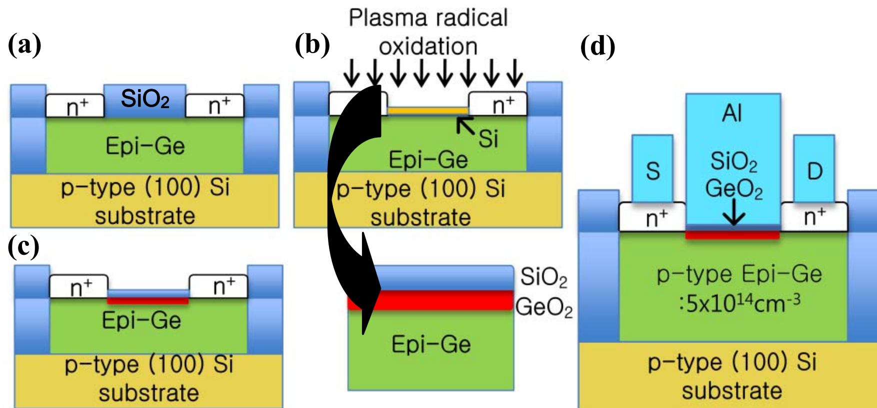


Fig. 9 Ge n-MOSFETs process flow. Selectively grown epitaxial Ge (p-type: $5x10^{14}cm^{-3}$) is used for n-MOSFETs. (a) Based on the selectivity, the n^+ *in-situ* doped Ge (600°C, 1min) is formed at S/D, defined by SiO_2 window. (b) After a thin layer Si growth on epi-Ge, Si and Ge are oxidized by plasma radical oxidation step, forming SiO_2(3nm) and GeO_2(1nm) as gate stack.

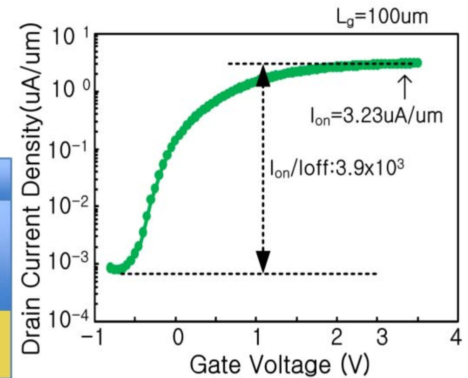


Fig. 10 I_D (μA/μm)-V_G (V) characteristics for Ge n-MOSFET fabricated on undoped epi-Ge. I_{on}/I_{off} is $3.9x10^3$ when V_D is 1.2V. I_{on} is 3.23μA/μm.

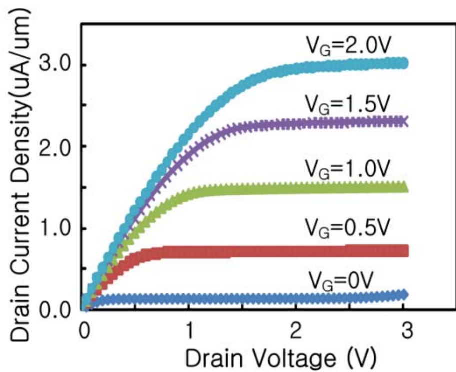


Fig. 11 I_D (μA/μm)-V_D (V) characteristics for Ge n-MOSFET (L_G=100μm) fabricated on selective undoped epi-Ge on Si (p-type: $5x10^{14}cm^{-3}$).

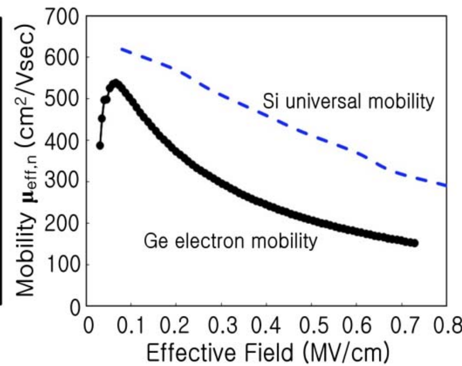


Fig. 12 Electron mobility (cm^2/V·sec) as a function of effective field (MV/cm) in Ge n-MOSFET on selectively grown epitaxial Ge (p-type: $5x10^{14}cm^{-3}$).

	Diode on/off	Transistor on/off	Peak μ_n (cm^2/Vs)
This work	10^4	$4x10^3$	540
Ref. [6]	10^3	$10^{1.5}$	420
Ref. [7]	10^4	$1x10^3$	410
Ref. [8]	10^3	-	270

Table. 2 Comparison of Ge n-MOSFETs performance in this work and previously reported data.