2012 12th IEEE International Conference on Nanotechnology (IEEE-NANO)
The International Conference Centre Birmingham
20-23 August 20112, Birmingham, United Kingdom

ZnO Based Charge Trapping Memory with Embedded Nanoparticles

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***Abstract* — A thin film ZnO charge trapping memory cell with embedded nanoparticles is demonstrated by Physics Based TCAD simulation. The results show 3V increase in the V_t shift due to the nanoparticles for the same operating voltage. In addition a ~6V reduction in the programming voltage is obtained due the nanoparticles. In addition, the effect of the trapping layer and tunnel oxide scaling on the 10 year retention time is studied.**

Index Terms* - *ZnO, Memory, Nanoparticles, Charge Trapping, Nano

I. INTRODUCTION

With the current trend of super handheld computing devices like the iPad, low power memory devices are necessary. Research has commenced to determine if nanotechnology can be utilized to achieve this goal. This includes the use of nanowires or nanoparticles to enhance the performance of memory devices [1-4].

Recently, ZnO metal-oxide semiconductors have been extensively investigated as channel materials for thin film transistors (TFTs). As a result, memory devices based on ZnO is of interest [5-8]. In this work we demonstrate by TCAD a nonvolatile memory device with a ZnO film as the charge-trapping layer in addition to ZnO channel material with embedded nanoparticles that reduces the operating voltage.

II. TCAD STRUCTURE AND MODEL

Figure 1 shows the basic structure of the memory cell simulated using the Synopsys™ TCAD tools. A Physics Based TCAD approach is used with key parameters modified to account for the new materials highlighted in table 1 [9-15]. The structure is stack of ZnO (channel) followed by a 5 nm Al_2O_3 (tunnel oxide), 2 nm ZnO (trapping layer) and 15 nm of Al_2O_3 as the blocking oxide.

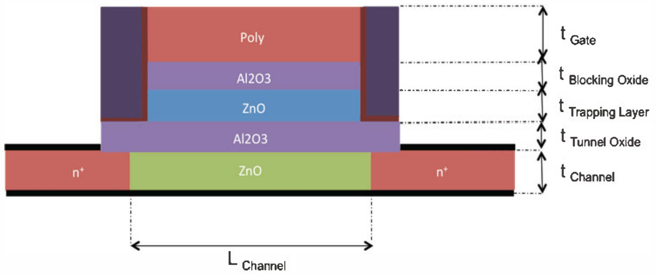

Figure1: Cross-section of the simulated memory cell

	Al_2O_3	SiO_2	ZnO	Si_3N_4
Relative Permittivity	9.5 (6 to 9)	3.9	8.75	7.5
Band Gap	6.65 eV	9 eV	3.37 eV	5 eV
Electron Affinity	2.58 eV	0.9 eV	4.5 eV	1.9 eV
Electron Tunnel Mass	$0.43m_0$	$0.44m_0$	$0.24m_0$	$0.36m_0$
Hole Tunnel Mass	$0.5m_0$	$1m_0$	$0.59m_0$	$0.38m_0$

Table 1: Physics Based TCAD material parameters

Figure 2 is the band diagram of the structure with zero applied voltage. The diagram shows a quantum well between blocking and tunnel oxides in the trapping layer due to the band offsets. Electrons can tunnel from the ZnO substrate to this potential well within the trapping layer. By adding nanopartciles embedded in the trapping layer additional energy levels will be availble for the electrons to tunnel into thus increasing the memroy effect.

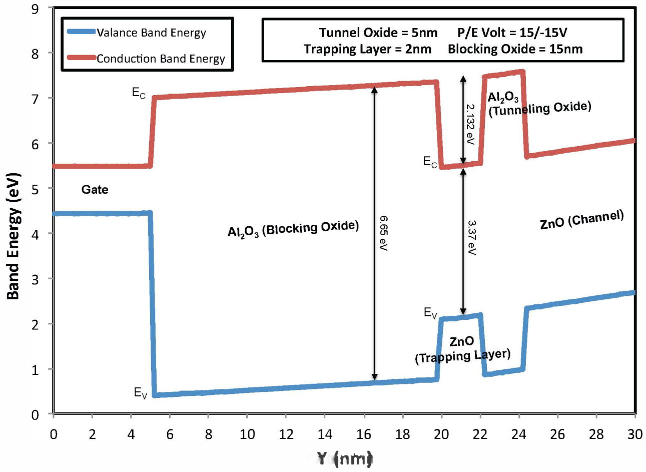

Figure 2: Conduction and valance band energy across the device (V=0)

Manuscript received July 4, 2012. This work was supported by the Masdar Institute of Science and Technology

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II. MEMORY EFFECT

In order to test the functionality of the memory cell the threshold voltage is measured after programing and erasing. The program and erase states of the device are simulated for several cycles to achieve a stead-state charge density and then the I_d-V_g curves are simulated to extract the corresponding threshold voltages. During each cycle, both the drain and source are set to zero voltage then a 2.5 ms wide positive pulse (15 V) is applied to the gate during the programming cycle followed by a 5ms wide negative pulse (-15 V) during the erase cycle. Each pulse is separated by 2.5ms. Throughout the program and erase cycles, the electrons and holes can tunnel between from the ZnO channel to the trapping layer channel. The charge distribution established in the program state is mainly due to electrons tunneling into the ZnO trapping layer from the channel. During the erase cycle when the negative bias is applied to the gate, electrons will tunnel out of the ZnO trapping layer and into the channel, but the majority of the tunneling comes from holes that tunnel into the ZnO trapping layer from the channel. When inside the trapping layer they then recombine with stored electrons.

Figure 3 plots the I_d-V_g curve of both the programed and erase states using 15 V/-15 V respectively for a memory cell with parameters in figure 2. In this case the V_t shift is only around 0.346 V. This is due to the fact that the electrons that tunnel across the Al_2O_3 tunnel oxide can only be trapped in a quantum well of around 2eV due to the conduction band offsets between ZnO and Al_2O_3. Additional available quantum states in the ZnO layer are needed to allow for more electron trapping and hence a larger V_t shift.

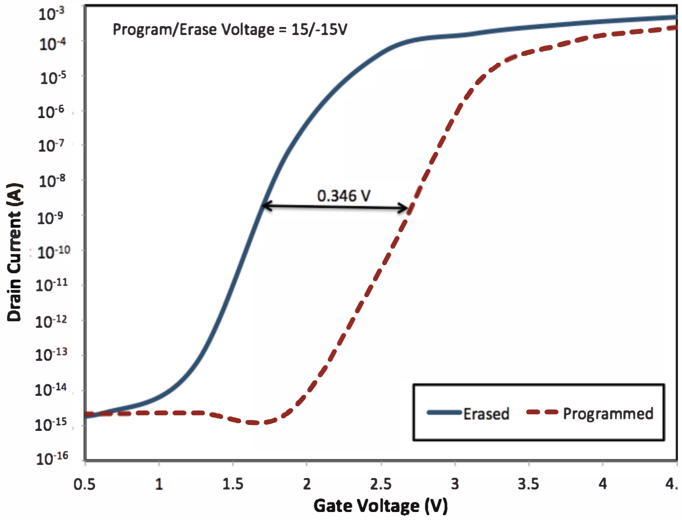

Figure 3: I_d-Vg with and without nanoparticles

III. EFFECT OF NANOPARTICLES

a. *VT SHIFT*

In order to study the effect to adding nanoparticles in the ZnO trapping layer additional states are added at different energy levels. Figure 4 shows the band diagram of the ZnO layer with added quantum states located at E_c - E_{trap} = 1 eV (donor state) and E_c-E_{trap} = 2.5 eV (acceptor) with density of 10^{20} cm^{-3}. The values were taken from previously studied Si_3N_4 SONOS memory [16-17].

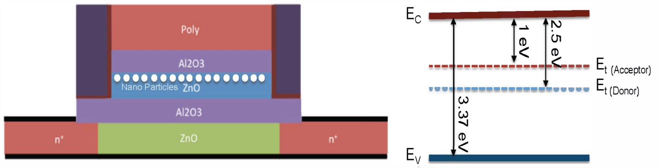

Figure: 4 **Left:** Device structure with the nanoparticle within the trapping layer. **Right**: The band diagram of the ZnO layer with added quantum states

In addition the density of nanoparticles is also studied. The simulation includes a density of $1x10^{10}/cm^3$ and $1x10^{20}/cm^3$. Figure 5 plots the I_d-V_g curve of both the programed and erase states using 15V/-15 V respectively for a memory cell with parameters in figure 2 with and without nanoparticles. The V_t shift increases from 0.346 V to 2.1V and 3.4 V for $1x10^{10}/cm^3$ and $1x10^{20}/cm^3$ density of nanoparticles respectively for the same programing voltage applied. The nanoparticles increase the amount of tunneling for the same voltage applied and thus the V_t shift increases.

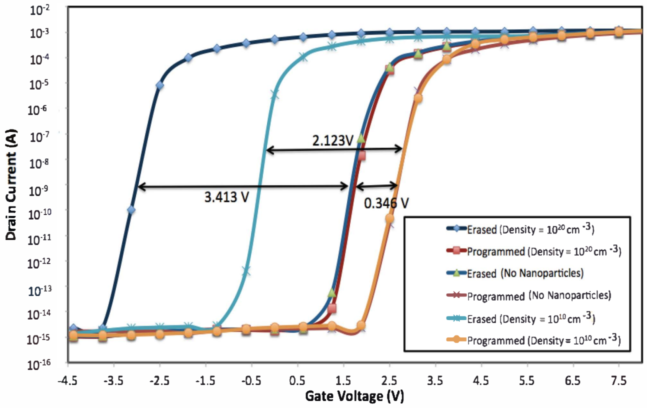

Figure: 5 I_d-Vg with and without nanoparticles.

b. *PROGRAMMING VOLTAGE*

In addition to affecting the amount of V_t shift, the nanoparticles also affect the programming voltage needed. Figure 6 shows the threshold voltage shift vs. programing voltage with and without the nanoparticles showing the reduction in programing voltage. For a 3V V_t shift the programming voltage reduces from 18V to 12.5V. It should be noted, the nanoparticles can be spin coated between separate ZnO Atomic Layer Deposition (ALD) growth steps.

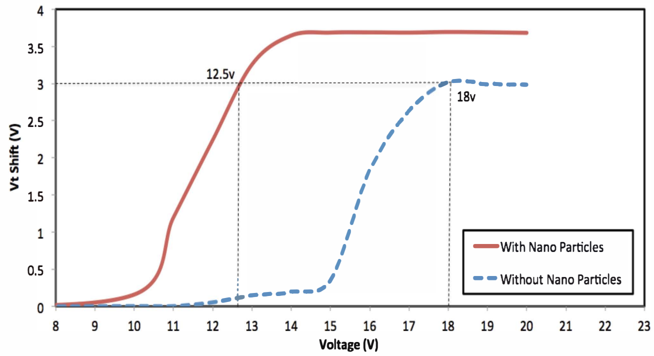

Figure 6: V_t shift vs. programming voltage (with and without nanoparticles)

IV. EFFECT TUNNEL OXIDE AND TRAPPING LAYER

a. V_t shift

In charge trapping memory cells, the tunnel oxide and trapping layer thickness are key design pararatmers. The nanoparticles will allow for furthur scaling of the tunnel oxide do to the programming voltage reduction. Figure 7 plots the effect of tunnel oxide thickness on the threshold voltage shift for different program/erase voltages with trapping layer thickness of 2 nm. The plot shows for tunnel oxide thickness larger than 15nm no memory effect is observed since no tunneling occurs. As the tunnel oxide is scalled below 15nm the V_t shift increases due to the onset of tunneling. The larger the progamming voltage the larger the electric field and the more tunneling occurs from the ZnO channel to the trapping layer. Figure 8 plots the effect of trapping layer thickness on the threshold voltage shift. The thicker the trapping layer, the more charge can be trapped and the threshold voltage shift is larger.

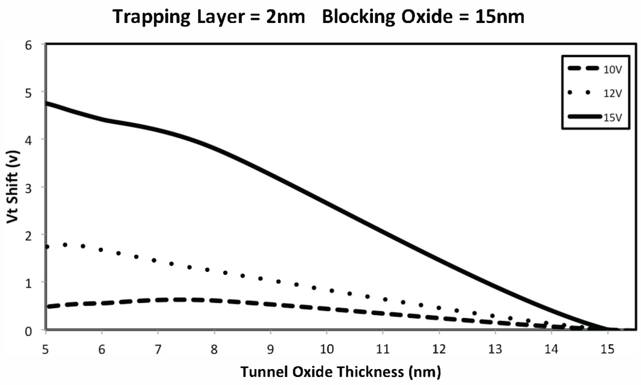

Figure 7: V_t shift vs. tunnel oxide thickness for different programming voltages

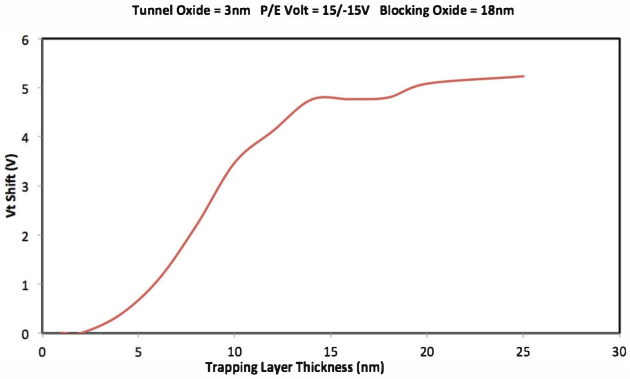

Figure 8: V_t shift vs. trapping layer thickness

b. Retention

A 10-year transient simulation is used to model the retention of ZnO nanoparticle memory. The electron density stored in the traping layer as a function of time, is shown in figure 9 for different tunnel oxide thickness with programming and erasing voltage = 15/-15V and trapping layer thickness of 2 nm. The thicker the tunnel oxide the better retention since less electrons can tunnel out and less holes can tunnel into the trapping layer. The nanoparticles allow for furthur scaling of the tunnel oxide without sacraficing on retention

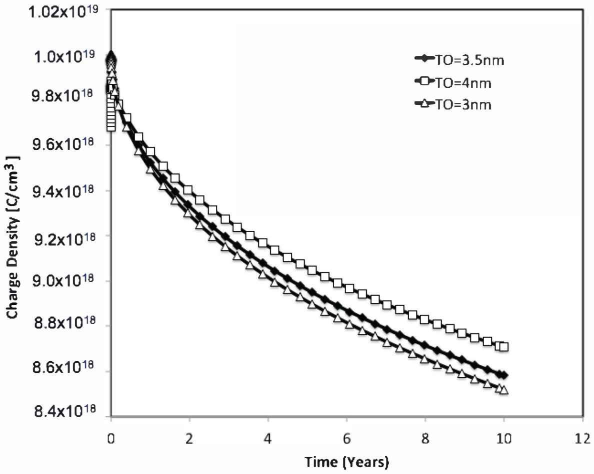

Figure 9: Electron and hole charge densities as a function of time for different tunnel oxide thickness

V. SUMMARY

A nanoparticle enhanced thin film ZnO charge trapping memory cell is demonstrated. The nanoparticles increase the V_t shift for the same programming voltage. In addition, the nanoparticles reduce the programming voltage required. Finally these results show that nanoparticles can be used to improve current memory technologies and offer an exciting path for future nano-memories

ACKNOWLEDGMENT

We gratefully acknowledge financial support for this work provided by the Masdar Institute of Science and Technology.

REFERENCES

[1] R. Ohba, N. Sugiyama, K. Uchida, J. Koga, and A. Toriumi, "Non- volatile Si quantum memory with self-aligned doubly-stacked dots," *IEEE Trans. Electron Devices,* vol. 49, no. 8, pp. 1392–1398, Aug. 2002.

[2] M. Takata, S. Kondoh, T. Sakaguchi, H. Choi, J.-C. Shim, H. Kurino, and M. Koyanagi, "New nonvolatile memory with extremely high density metal nano-dots," in *IEDM Tech. Dig.,* 2003, pp. 553–557.

[3] J. De Blauwe, "Nanocrystal Nonvolatile Memory Devices," *IEEE Transactions On Nanotechnology, vol. 1, no. 1, March* 2002

[4] C. gyu Hwang, "Nanotechnology enables a new memory growth model," Proceedings Of The IEEE, vol. 91, no. 11, November 2003

[5] D. Gupta, M. Anand, S.W. Ryu, Y.K. Choi, and S. Yoo, "Nonvolatile memory based on sol-gel ZnO thin-film transistors with Ag nanoparticles embedded in the ZnO/gate insulator interface", Appl. Phys. Lett., vol. 93, no. 22, 2008.

[6] H. Yin, S. Kim, C. J. Kim, I. Song, J. Park, S. Kim, and Y. Park, "Fully transparent nonvolatile memory employing amorphous oxides as charge trap and transistor's channel layer,"Appl. Phys. Lett., vol. 93, no. 17, October 2008.

[7] S. Kang, Y. Kim, H. S. Seo,S. W. Son, E. A. Yoon, S. Joo and C. W. Ahn, "High-performance and room-temperature-processed nanofloating gate memory devices based on top-gate transparent thin-film transistors," Appl. Phys. Lett., vol. 98, no. 21, May 2011.

[8] E. Kim, Y. Kim, D. H. Kim, K. Lee, G.N. Parsons, and K. Park, "SiNx charge-trap nonvolatile memory based on ZnO thin-film transistors," Appl. Phys. Lett., vol. 99, 2011.

[9] Y. T. Shih, M. K. Wu, M. J. Chen, Y. C. Cheng, J. R. Yang, And M. Shiojiri, "ZnO-based heterojunction light-emitting diodes on p-SiC(4H) grown by atomic layer deposition," Applied Physics B - Lasers and Optics, vol. 98, 2010

[10] M. L. Huang, Y. C. Chang, C. H. Chang, T. D. Lin, J. Kwo, T. B. Wu, And M. Hong, "Energy-band parameters of atomic-layer-depositionAl_2O_3/InGaAs heterostructure," Appl. Phys. Letter, vol. 89, 2006.

[11] S. J. Pearton, D. P. Norton, K. Ip,Y.W. Heo, T. Steiner, "Recent progress in processing and properties of ZnO," Prog. Mater. Sci., vol. 50, no. 3, pp. 293-340, 2005.

[12] M. Specht, M. Städele, S. Jakschik, and U. Schröder, "Transport mechanisms in atomic-layer-deposited Al_2O_3 dielectrics," Appl. Phys. Lett., vol. 84, no. 16, 2001.

[13] P. Vitanov, A. Harizanova, T. Ivanova, T. Dimitrova, "Study of $ZrO_2/Al_2O_3/ZrO_2$ and $Al_2O_3/ZrO_2/Al_2O_3$ Stack Structures Deposited by Sol-Gel Method on Si," IOP Conf. Ser.: Mater. Sci. Eng. 8, 2010.

[14] Yee-Chia Yeo,Tsu-Jae King and Chenming Hu, "Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology," Journal of Applied Physics, vol. 92, no. 12, 2002.

[15] V. Rose and R. Franchy, "The band gap of ultrathin amorphous and well-ordered Al_2O_3 films on CoAl(100) measured by scanning tunneling spectroscopy," Journal of Applied Physics, vol. 105, no. 7 2009.

[16] J. Bu and M.H. White, "Design considerations in scaled SONOS nonvolatile memory devices," Solid-State Electronics, vol. 45, no. 1, pp. 113–120, 2001.

[17] P. Chakraborty, S. S. Mahato, T. K. Maiti, S. Saha and C K Maiti, "Nanocrystal Non-Volatile Flash Memory Devices: A Simulation Study," NateHCA, IETE Mumbai Centre, 2007.