

# A Performance Enhanced Power Divider Structure

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**Abstract**—We analyze the bandwidth capability of a divider with a series RLC circuit at the isolation arm. Analytical expressions for optimal component values are given. Bandwidth limiting effect of the pad capacitances of the chip resistors is analyzed. These parasitic capacitors are compensated by the proposed structure. Broadband characteristic of the new divider is verified by experimental results.

**Index Terms**—wideband power divider, isolation resistor parasitics, pad capacitance.

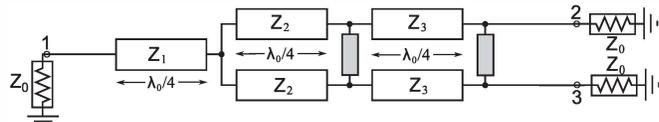


Fig. 1. A symmetrical 2-way power combiner/divider network. White boxes are quarter-wave transmission lines. Gray boxes represent the lossy isolation arms. Possible contents of a gray box: Symmetrical lossless components with isolation resistors in the middle.

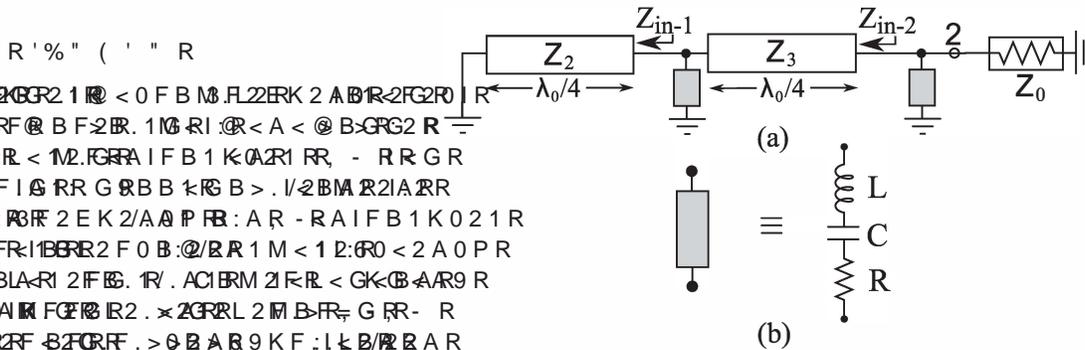


Fig. 2. a) Odd mode equivalent circuit of the divider in Fig. 1. b) Possible content of a gray box for wideband operation: Series RLC network.

## ANALYSIS AND DESIGN OF THE DIVIDER

$$2Z_1Z_2 = 2Z_0^2 \quad R$$

$$\frac{Z_2^2 Z_0}{4Z_1^2} = Z_0 \frac{1 + \Gamma_e}{1 - \Gamma_e} \quad R$$

$$\frac{Z_1}{Z_2} = \sqrt{\frac{1 - \delta}{2(1 + \delta)}} \approx \frac{1}{\sqrt{2}} \left( \frac{1 - \delta/2}{1 + \delta/2} \right) \quad R$$

(G < A 9 R R A 1 R Z R . A 1 Z R . F Z R > 0 K > . C 2 R R

$$\frac{Z_1}{Z_0} = 2^{-1/4}(1 - \delta/2)$$

$$\frac{Z_2}{Z_0} = 2^{1/4}(1 + \delta/2)$$

' : 2 R B 1 1 0 B 1 2 B K < L . 0 2 F D R K G R B M A R R 9 R 0 R 2

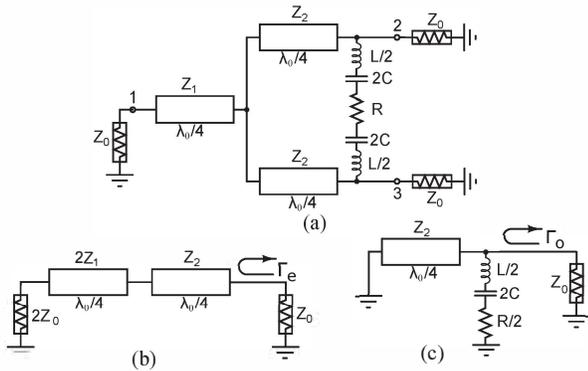


Fig. 3. a) Broadband 2-way divider. b) Even-mode equivalent circuit. c) Odd-mode equivalent circuit.

. A 1 R R F 2 G B A I R 2 Z R A 1 0 R 2 A 1 2 F R

$$\frac{1}{\sqrt{LC}} = 2\pi f_0$$

I R\_0, M 2 R @ C B I G | 2 R \delta. & B R R 0 . A I R = 2 R I B L R > K Z G = R  
 2 Z\_0(1 \pm \delta)/(1 - \delta). ' : 2 R G @ . > B 2 F E G K < A I M R 1 2 F A R I R  
 G < A D : 2 R 2 G < G I B @ Z R A 2 A G I R < < A M A I R 2 G C I 2 B R R  
 I : 2 R : B F I E 1 R G @ < < G C A Z B R R R A 1 R

$$\frac{R}{Z_0} = 2 \frac{1 - \delta}{1 + \delta} \approx 2(1 - 2\delta)$$

' B R 0 . > 0 K > . I 2 R I R R . A . > P I < 0 M 2 R B > R B M I R C F B . 0 : R

< A R - R 2 R 1 2 6 A I 2 B R A 1 M < 1 0 B R A 1 < I B 3 F A R < \delta . G R

f\_0(1 - k) < f < f\_0(1 + k). & < A \delta 2 R A 1 Z R . F Z R > 0 K > . I 2 - 1 R

F 2 R B k R R 2 C < 0 I K F 2 R R C . 1 0 R C . 0 < I . A D I 2 R G K < A I B R

K G < A 9 R A 1 R k R < G R A B M A R . @ 2 I 2 F R N < @ I K 0 2 R

C . I 1 B I R 2 R F B K M 1 - R 0 I : 2 R F . 1 2 Z R A 1 M < C I 2 R 3 B F @ . A 0 2 R

B 3 R 2 R < L < 1 2 E F R 2 B I R A 1 C D R : B K / 2 F R A B I K R B H R < G R

C K F C B M 2 R F B C B : C G F F K 0 k A R 2 R M : 2 F 2 R R G R A 2

B K K G < A R B R F I I 2 F A G < < G C A Z B R R 2 R A 1 K 0 I B F R

R < G @ C > 2 @ D I A I I 2 R R 9 < R @ C 2 1 . I F 0 A R @ < < G C A Z B R R

I : . I R G B R @ C 2 A G : 2 R G F R G < B 3 R 2 R C . 0 < I B R : 2 R

A 2 M R B A 6 9 K F B 3 I B 2 R G B > . I F @ A R 2 0 I G R I B R R L 2 A R

R @ B 1 2 R F 0 K 2 R R A G 2 F I B B A G I R I R 2 R 2 G < G G B R 1 2 1 R

/ P R > . 0 < A B R 2 @ < C B < A 2 < A 2 R 2 0 I < B 3 R 2 R L 2 A R

R @ B 1 2 : 2 R 2 I M B - A - F R G B > . I R @ A R R I < @ k B F A 1 R A 0 2 R

< 9 R G : B M I G R R A 1 M < 1 0 2 F 3 B F @ B 3 R 2 R < L < 1 2 F 2 R A 1 M < B 3 R 2 R A C K 2 R K F A C G N R 2 > . G R 2 R K I C K I R

2 I M 2 2 A B R F 2 E K 2 A 0 < A G R R I : 2 R . F . @ 2 I 2 F I G R F 2 I K F A C A 1 R G B > . I < B G R R I 2 R F B 2 3 F 2 2 1 B @ B M G R

|S\_{22}|, |S\_{32}| G I . F 2 R B I M 2 R F 2 G 0 R < C 2 F R @ 2 2 2 R 9 R R I : 2 R A C K I R A G @ < < G C A Z B R R R 2 > < @ < A A 2 4 P R B 3 G R

< G R C > B I R R 2 R 2 E K < F 2 @ F C B A 2 A K 2 B R 0 : < 2 U 2 R R I : 2 G 2 R G K M k G 2 R R F 2 G 2 A I 2 A R N I 2 A 1 2 1 R I B 3 F G G B A R

/ . A 1 M < F I : A R 2 3 R F 2 G S 2 9 R R C . C 2 F R

' : 2 R @ C > 2 @ 2 A B 3 I R < B A R F 0 K G R R 5 0 K > k B B R 2 R

C . F . G < B 3 R 2 R K @ C 2 B @ C B A 2 A 2 G I R 2 B @ . E > R R

0 . C . 0 < I B B R F B K B 3 I R 2 B 2 F \theta B @ C B A G A B G A R 6 0 . A I > P R < L < G 2 I F K 0 k A F 2 B 1 K A 2 9 R M . G @ C > 2 @ 2 A I 2 1 R

. 4 2 0 I : 2 R 2 F 3 B F @ < A 0 R G R B . N R G 9 3 F 2 E K 2 @ B P R 3 R B A . R R G K / G I M k 2 R R : < 0 = A B G B @ @ - F 9 R

. R 0 : < E R G < G B B R 2 R L 2 @ B 1 2 : 2 R B @ C B A 2 A I G R R I R G : B M G R : B I B 3 R 2 R < L < 1 2 F M R 0 G < 9 I B 2 R I : R 2 B 2 B F R

R  
R

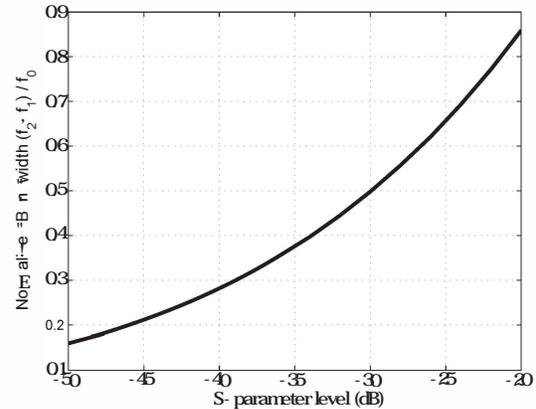


Fig. 4. Achievable bandwidth versus the desired S-parameter level for the divider in Fig. 3. The bandwidth is normalized with the center frequency.

R

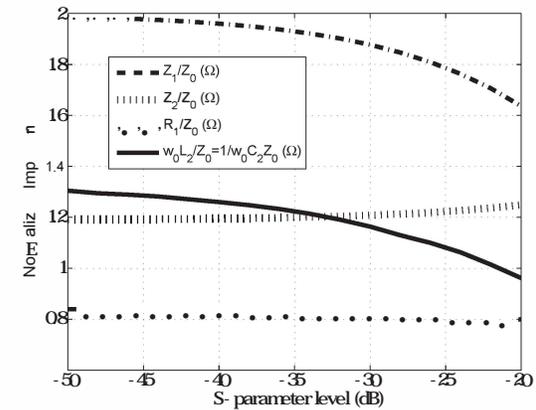


Fig. 5. The component values to achieve the bandwidth ranges expressed in Fig. 4.

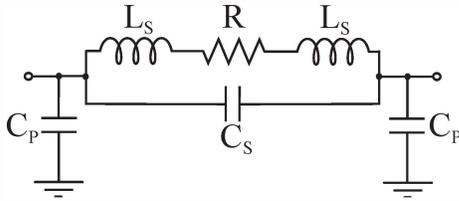


Fig. 6. Equivalent circuit of a chip resistor.

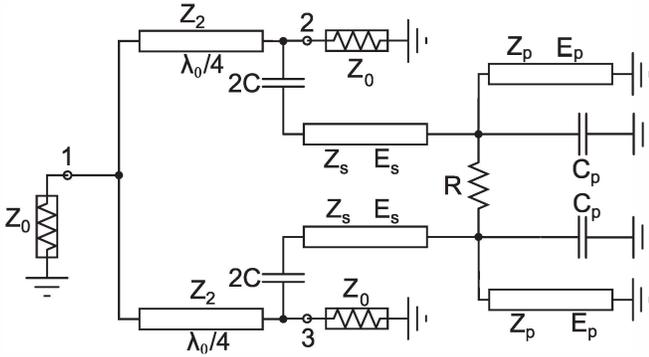


Fig. 7. Schematic diagram of a 2-way divider with symmetric transmission lines in the isolation arm to enhance the band and to compensate the parasitics of the resistor.

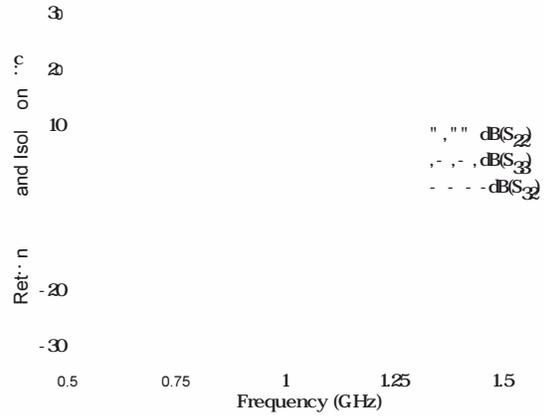


Fig. 9. Measured return loss and isolation characteristic of the divider in Fig. 8.

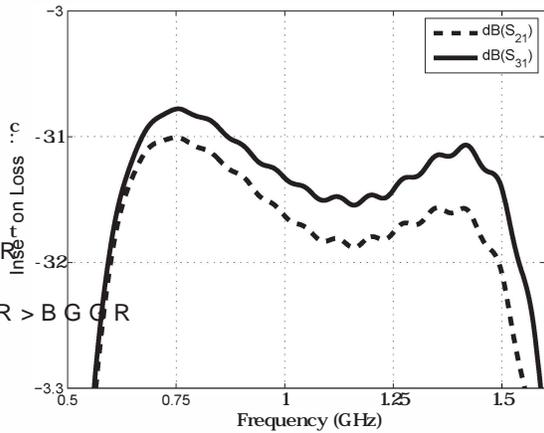


Fig. 10. Measured insertion loss characteristic of the divider in Fig. 8.

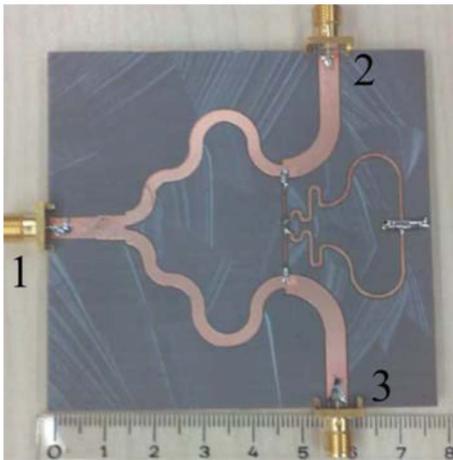


Fig. 8. Implemented 2-way power divider (Fig. 7).

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