FABRICATION, CHARACTERIZATION, AND PARAMETER EXTRACTION OF GaAs MESFETS

A THESIS

SUBMITTED TO THE DEPARTMENT OF PHYSICS

AND THE INSTITUTE OF ENGINEERING AND SCIENCES

OF BILKENT UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

MASTER OF SCIENCE

By

Erhan Pelelken Ata

28 January 1994

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I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Master of Science.

Assoc. Prof. Recai Ellialtıoğlu (Supervisor)

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Master of Science.

Prof. Atilla Aydınlı

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Master of Science.

Assist. Prof. Erkan Tekman

Approved for the Institute of Engineering and Science:

Prof. Mehmet Baray
Director of Institute of Engineering and Science

Abstract

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Erhan Polatkan Ata
M. S. in Physics
Supervisor: Assoc. Prof. Recai Ellialtıoğlu
28 January 1994

Metal Semiconductor Field Effect Transistor (MESFET) is the most widely used active element of today's microwave industry. After development of the MESFET technology, the microwave industry gained a high acceleration, especially in the telecommunication field.

In this study, GaAs MESFETs with various dimesions and geometries were fabricated. Characterization and parameter extraction of these devices were performed, by means of low and high frequency measurements. The low cut-off frequency of the MESFETs produced were attributed to the non-optimized gate recess etch.

Keywords: MESFET, GaAs, Schottky Contact, Ohmic Contact, active channel, analytical model, small-signal model.

Özet

GaAs MESFET ÜRETİMİ, KARAKTERİZASYONU VE PARAMETRELERİNİN ELDESİ

Erhan Polatkan Ata
Fizik Yüksek Lisans
Tez Yöneticisi: Doç. Dr. Recai Ellialtıoğlu
28 Ocak 1994

Metal Yarıiletken Alan Etkili Transistör (MESFET), günümüz mikrodalga endüstrisinin en yaygın kullanılan elemanıdır. MESFET teknolojisinin gelişmesinden sonra mikrodalga endüstrisi, özellikle iletişim alanında, önemli ivme kazanmıştır.

Bu çalışmada, değişik boyut ve geometrilerde GaAs MESFETler üretilmiştir. Bu cihazların karakterizasyonu ve parametrelerinin eldesi alçak ve yüksek frekans bölgelerinde yapılan ölçümlerle gerçekleştirilmiştir. Üretilen MESFETlerin düşük kesim frekansları, optimize edilmemiş kapı (gate) oyuğu aşındırmasına bağlanmıştır.

Anahtar Sözcükler: MESFET, GaAs, Schottky eklemi, ohmik eklem, aktif tabaka, analitik model, küçük sinyal modeli.

Acknowledgement

I am grateful to Assoc. Prof. Dr. Recai Ellialtıoğlu for his guidance, motivation, and invaluable supervision during my graduate study.

I wish to express my sincere gratitude to Dr. Nacer Debbar who introduced me to the semiconductor technology.

Special thanks are due to Ahmet Oral, İsmet Kaya, and Erkan Tekman for their invaluable supports, helps, and friendship.

I wish to thank to members of the Advanced Research Laboratories and physics department, without whom this study would be impossible.

I am in debt to family and friends for their supports and patience.

This project was performed under the auspices of the Ministry of Defense, Undersecretariat for Defense Industries, Grant No: SSM-90-AG-033.50.

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Chapter 1

Introduction

1.1 Introduction

In a well known article published in 1952, W. Shockley[1] introduced the concept of a *Field Effect Transistor* (FET), and proposed the term "unipolar" to distinguish it from the bipolar transistor. However, the introduction of the *Metal Semiconductor Field Effect Transistor* (MESFET), which should not be confused with silicon FETs (MOSFET, J-FET), is as late as, 1966 by C.A. Mead. Even though in the early 1970s, according to the journals dealing with microwave components, the GaAs MESFET "had potential," but would not easily replace its existing competitors. In the field of MESFET applications, main competitors were:

1. The traveling wave tube (TWT) for low and medium power amplification;
2. diodes, especially Gunn and IMPATT, used as microwave sources;
3. the silicon bipolar transistor, used as low noise or power amplifier, or as a microwave source for frequencies up to 7 or 8 GHz.

At that time bipolar transistors were making great progress, especially in power amplification area. BJTs with power outputs in the order of a few watts at 2-5 GHz range were promising for the silicon industry. Thus in 1970, MESFET

was "unwanted stranger" in the industry, compared with its well-established competitors, even though its frequency and noise performances were far better. Figure 1.1 shows gain and noise figure performance for a MESFET in 1973.[2] For a comparison it also shows the best noise performances of bipolar transistors and TWTs. Although, the MESFET figures were obtained in the laboratory, they

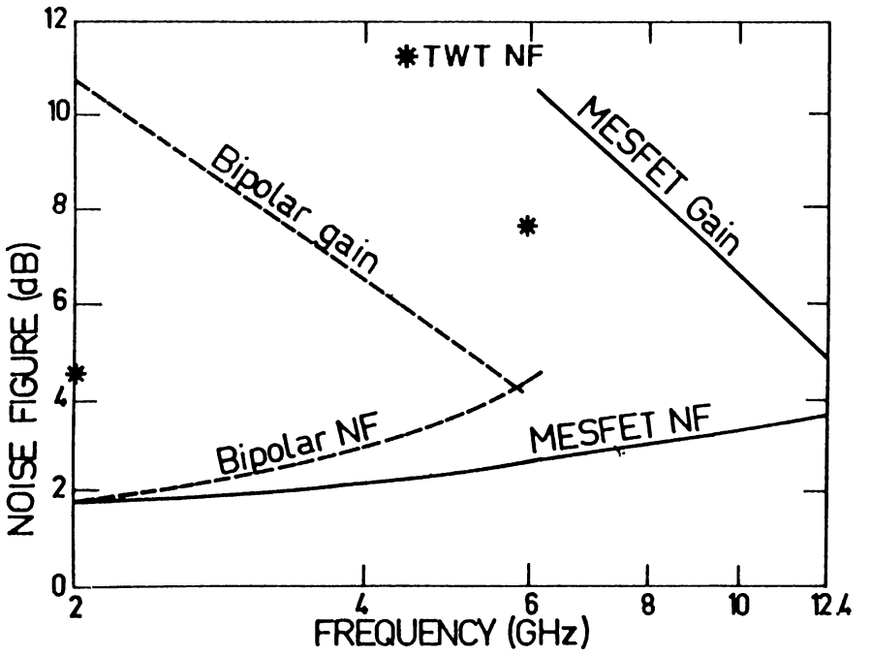

Figure 1.1: Performance comparison of TWT, BJT, and MESFET
1973 state-of-the-art performance comparison between bipolar junction transistor, MESFETs, and traveling wave tubes

clearly show the devices superiority. At the time, very few laboratories attempted to build MESFETs, which were very difficult to produce. The adaptation to the new technology was not so simple. First of all the material, GaAs, was quite unfamiliar and difficult to process. The most experienced people in the area were those who were working on Gunn diodes. However the conditions are entirely different: the MESFET has a planar structure; requiring an active layer and an insulating layer, therefore has two interfaces. It also requires a Schottky contact. Second, the factories attempted to start by manufacturing devices with one micron gate length, which was smaller than that normally found

in semiconductor industry at the time.

From a few GHz to several tens of GHz frequency range, though leaving its place to *High Electron Mobility Transistor* (HEMT) and the *Heterojunction Bipolar Transistor* (HBT), MESFET is the most widely used active component. The success of MESFET is due to the semiconductor material, namely GaAs. Electron mobility in this material, for example 8500 $cm^2/V \cdot sec$ versus 1500 for n-type silicon, for the same concentration of carrier densities. Additionally, the maximum saturation velocity for GaAs ($\sim 10^7 cm/sec$) occurs at a lower threshold field (3500 V/cm versus 10000 for Si). Also, GaAs has a better insulating substrate than silicon, which allows low parasitics and true monolithic circuit realization. Finally, GaAs is more radiation tolerant than silicon, which enables its use in space with very low protection against radiation.

Although all of these advantages were known, GaAs was primarily used only in the production of bulk effect diodes, utilizing other specific electrical properties (e.g. electrons moving from one valley to another).

However, even today further efforts are necessary to improve reliability. Optimization of the processes, for efficient and competitive production, is still a major problem. Considerable work has been carried out in these directions, but there are still problems to be solved, such as passivation, reliable ohmic contacts *etc.*, at least by some manufacturers. Short and medium term drifts still cause degradation of devices, and differences in behavior and/or performance can still arise between transistors from different batches.

1.2 The Material:GaAs

Over thirty years, GaAs has been the subject of intensive scientific study and a very large literature on the subject formed. There are several reasons for such intensive interest.[3]

First, GaAs is a compound semiconductor combining group III and group V elements from the same row in the periodic table as the group IV semiconductor, germanium. The charge exchange existent in the bonding of the lattice adds an

ionic component to the mainly covalent bond of Ge and the band gap is expected to increase. This increase in band gap offers a wider range of electrical resistivity and the protection of extrinsic semiconductor behavior to high temperatures as well as some other useful properties. These properties are very valuable for the device physicist and engineer.

Second, as substitutional impurity atoms from groups II, IV, and VI will act as donors and acceptors in the GaAs lattice, extra degrees of freedom are available when compared to Ge or Si.

Third, when the whole family of III-V is investigated, from InSb to AlP including inter-periodic compounds such as InP, AlSb, and alloys such as GaAsP (the first commercially significant III-V semiconductor) or GaAlAs (which allows the band gap to be varied without significantly changing the inter-atomic distance), the potential advantages over the group IV elements Sn, Ge, Si, C (diamond) are even more obvious. The study of GaAs as a prototype is clearly justified in both academic and applied sense.

1.2.1 Properties of GaAs

Crystal Structure

GaAs at room temperature has a density of $5.317g \cdot cm^{-3}$ and crystallizes into zinc blende structure, which consists of two equivalent, inter penetrating face-centered cubic lattices, one containing Ga atoms and the other As atoms. The lattice is broadly equivalent to that of Si, which has a diamond structure, but due to presence of dissimilar atoms, there exist some significant differences in the crystal properties. A shift of valance charge from gallium to arsenic atoms results in a mixed (ionic/covalent) bond compared to the covalent bond in germanium and silicon. This has very significant effects on the electronic band structure and increases the bond strength (the melting point of GaAs is higher than that of Ge).

Another result of the existence of dissimilar atoms is the difference in the chemical activities of opposite (111) crystal faces in GaAs. If (111) planes of

GaAs crystal are considered, it can be seen that all Ga atoms lie on a plane parallel to As atoms, which also lie on another plane 0.8 Å apart, whereas the next nearest Ga plane is 2.4 Å apart from As plane. This structure results in observations of different etch rates, depending on the plane (Ga or As) on surface, reacting with etchant. The etch rate difference for different planes causes different etch profiles in different directions, which sometimes may cause problems related to process of GaAs.

Electrical Properties of GaAs

Band Structure In the sense of device physics, the electronic band structure of a semiconductor is its most significant property. The band structure determines the main electrical and optical properties that generate the device functions. Since experimental data give accurate but limited information at particular points in Brillouin zone , a complete and accurate band structure information is difficult to obtain. Theoretical calculations, due to some approximations, can predict the band gap structure only with some uncertainty. However, there exist "working" band structure models. In 1.2 partial band structures of GaAs and Si at 300 K, obtained by the pseudo potential calculations, are seen.[3]

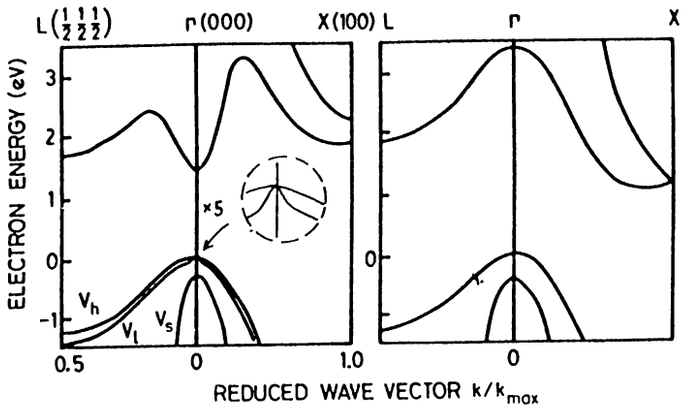

Figure 1.2: The partial band structures of GaAs and Si at 300 K
Showing the uppermost valance bands and the lower conduction bands along two of principal directions in the crystals. The magnified (×5) insert shows the detail at Γ of the light and heavy hole bands in GaAs (V_l and V_h)

In GaAs and Si, the valance band maxima occur at zero wave vector point (Γ) and the nature of the bands at this point determines hole conduction properties. The minimum allowed energy for conduction band states also occur at Γ in GaAs but is located near the X point in Si, so the electron wave vector has a finite magnitude and direction [100] for conduction electrons in Si, which affects some electrical and optical properties.

The band gap of GaAs (1.412 eV at 300 K) is larger than that of Si (1.08 eV at 300 K), which in turn results in a lower steady state density of thermally generated carriers in GaAs ($10^6 cm^3$) compared to Si ($10^{10} cm^3$). Thus GaAs has the advantage for better isolation (higher resistivity) than Si, which is an important property for lowering device parasitics.

Since the curvature of conduction band minimum of GaAs is higher than that of Si at the conduction band minimum, the electron effective mass in GaAs ($0.063 m_o$ at Γ) is much lower than that of Si ($0.3 m_o$ near X), which, in conjunction with the fact that scattering rates are of similar magnitude, explains the higher mobility of electrons in GaAs. Higher mobility means higher operating frequency, and faster devices.

Semi-Insulating GaAs In practice isolation regions in GaAs is achieved either by mesa etching or by means of forming deep electronic states near the center of the band gap, which lock the position of the Fermi level close to its intrinsic position. Defects can produce electronic states at any position in the band structure and many produce states near the middle of the band gap (deep states). If these deep states are dense enough, they can effectively control the electron occupancy of the crystal, resulting in the pinning of the Fermi level close to the defect state energy. For example, substitutional chromium atoms on the gallium sites, produce deep state close to the center of the gap and are used to control the resistivity. Lattice damage caused by irradiation with fast particles (electrons, protons, ions) also produces deep states, whereas proton is the preferred one due to its better depth and spreading characteristics.[3]

Since present semiconductor technology is mainly based on planar devices,

whose active layer thicknesses are very small, the surface phenomena can be critical for some applications. The termination of the crystal at the crystal surface causes some electronic state formation. When a metal comes in intimate contact with semiconductor, depletion barriers can be generated (this is the case for GaAs). If this barrier height is very small or if some extra work is done to obtain a locally high carrier concentration in the semiconductor to form a thin barrier allowing high electron tunneling rate, ohmic contacts are formed. If these conditions are not satisfied the barrier results in a rectifying Schottky contact. The barrier height formed with GaAs is almost independent of the metal work function, which is not the case for Si.

As mentioned earlier, the high mobility and high drift velocity of the GaAs are, its main advantages for the microwave devices. The electron drift velocity versus electric field curves for GaAs and Si is depicted in figure 1.3. When an electron in the semiconductor is subject to an electric field, it rapidly (about 10^{-12} seconds) achieves a velocity that is a function of electric field strength. As it is seen in figure 1.3, this relationship is linear with the proportionality constant *mobility*, μ, for low values of field.

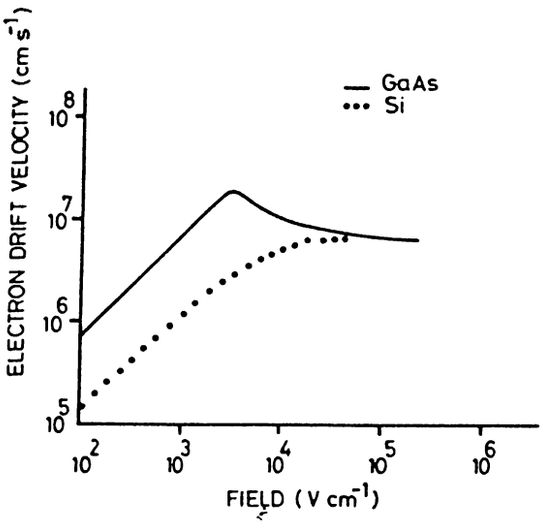

Figure 1.3: The velocity-field characteristics of GaAs and Si conduction electrons

1.2.2 Growth of GaAs

The MESFET requires bulk material for substrates and epitaxial material for the high quality active region. Both must be doped to the correct carrier type and impurity level. The management of these processes is extremely critical because it is the most important determining factor in the final device performance, especially for the microwave devices where the operation depends so much in purity and characteristic of the epitaxial material.

The substrate is necessary as a mechanical support for the very thin epitaxial layer, and acts as a basement during growth of epitaxial layer. Commercially available substrates' thicknesses vary in the 100-500 μm range. For planar devices, such as MESFETs and logic elements, substrate resistivities must be in the $10^4 - 10^8 \Omega cm$ range.

Bulk Growth

Bulk material is usually grown in the form of large ingots of single crystal; the major problem to be overcome during growth of the compound semiconductor arises due to the high vapor pressures resulting at growth temperature. These volatile components must be contained either by growth in a completely sealed system or by suppression of the volatilization by encapsulation of the melt in an inert liquid .[4]

Bulk ingots are usually produced using the *Liquid-Encapsulated Czochralski* (LEC) technique,[5] in which the crystal is slowly rotated and pulled out from a melt through a molten boric oxide encapsulant, at the melting temperature of GaAs (1513 K). While this is a lower temperature than that of Si, the equilibrium overpressure and stoichiometry control problems are the drawbacks compared to Si.

Another method, widely used for production of large quantities of em n-GaAs substrate material is the *Horizontal Bridgeman* (HB) technique.[5] The main advantage of this method is that, it is readily automated. A boat containing the semiconductor compound and crystal seed is sealed inside a quartz tube, the

other end of which contains a small arsenic excess. The furnace consists of at least two zones, one held at $612°C$ in which the arsenic end of the tube sits. The ingot is melted at $1270°C$ and moved slowly out of the hot area into the cooler one, resulting in a crystallization. The completed crystal usually has a shape defined by the shape of the boat, somewhat circular up to the level of the melt. This "D" shaped crystal is sawn perpendicular to (100) axis and made round.

Even though, by using variations of above two methods, the grown GaAs crystal has many dislocations. These dislocations not only introduce trapping states, alter the etching properties of the wafer, but most importantly can affect the electrical performance of the devices. Exactly how this occurs is not known, up to our knowledge, but it is proposed that dislocations affect the activation energy of ion-implants. Studies have shown that source-drain current and threshold voltage of logic FETs are strongly correlated with dislocation density.[6] In general LEC material exhibits a greater dislocation density than that of HB material. This is mainly due to the higher temperature gradient in the LEC method. The problems due to these dislocations can be solved by epitaxial growth of a GaAs buffer layer which will be virtually dislocation free and will heal dislocation propagation to the active part of the material.

After a useful substrate is obtained by growth and processes such as sawing, grinding, polishing, *etc.*, an active region for devices must be formed on the substrate. This is done either by epitaxial growth or ion implantation.

Epitaxial Growth

Material of highest electrical quality is produced by epitaxial growth, *i.e.* production of controlled thin film, techniques at temperatures between 900 and 1100 K. The growth of such layers are essential to all state of the art devices. The active region of the component can be defined in thickness, carrier type, and impurity level and profile to optimize performance. The low growth temperatures enable both impurity and stoichiometric defects to be controlled at concentrations below $10^{15}cm^{-3}$, which cannot be obtained in ingots. Epitaxial layers are generally of higher crystal quality than the substrate they are grown.

Although crystal defects tend to propagate in the immediate epitaxial layers, as the layers gets thicker some healing takes place. If an active (doped) layer is directly grown on the substrate, the impurities and defects in the substrate will degrade the crystalline properties and therefore the electrical properties of the material. Thus, buffer layers of un-doped GaAs are usually epitaxially grown on the substrate before active layers are grown.

There are, basically, three types of epitaxy used for GaAs, namely *Liquid Phase Epitaxy* (LPE), *Vapor Phase Epitaxy* (VPE), and *Molecular Beam Epitaxy* (MBE).

LPE is the oldest technique used to grow epitaxial layers on GaAs crystals. It is an inexpensive method and is capable of growing many material compositions including GaAlAs, but unfortunately not suitable for microwave devices. In this technique, a GaAs substrate is placed on a slider that can be moved across surfaces of molten materials contained in boats. These melts are gallium saturated with the desired materials, such as As (to form un-doped GaAs) or dopants. The temperature gradients are such that the melts are just at the solidification temperatures, so that they solidify onto the crystal substrate. The major problem of LPE is the difficulty of growing uniform layers over large surface areas. However, this technique gives successful results for LEDs and such structures, which, in contrast to microwave devices, do not need thin, uniform high quality epitaxial layers.

VPE is one of the most frequently used methods for epitaxial growth. In this method, the Ga, As, and the dopant atoms are brought to the wafer in gaseous phase. Under appropriate physical conditions, reactions take place on the surface of substrate that result in deposition of the atoms on the surface such that they replicate the crystal structure. There are mainly two variations of VPE. In the VPE technique with trichloride transport, the substrate is placed in a quartz slice holder in a reactor tube. At a temperature close to 800 ^{o}C, growth is obtained by the reaction of $AsCl_3$ with Ga in the presence of H_2 to produce GaCl, As_4 and HCl. Although wide usage of this method, its limitations in terms of uniformity and profile control have led to the development of an alternative

VPE system using an organometallic compound for gallium transport, namely *Metal-Organic Chemical Vapor Deposition* (MOCVD). In this method, generally trimethylgallium ($Ga(CH_3)_3$) is used as the Ga source and arsine (AsH_3) is used as the arsenic source. The main advantage of the method are the ability to produce complex heterostructures and the good control of both layer thickness and doping. Major problems of this system is its high cost and safety requirements related to arsine.

MBE is another major method of growing epitaxial layers. In this technique substrate is placed in an ultra high vacuum (generally 10^{-10} to 10^{-11} torr) and required materials are evaporated from ovens (effusion cells) and stick on the heated substrate to form an epitaxial layer. With proper control of the sources (Ga, As, Al, Si, *etc.*) almost any material composition and doping can be obtained. Even single atomic layer growth is possible. MBE's advantages are that it can produce almost any epitaxial layer composition, layer thickness, and doping, and can do so with high accuracy and uniformity across a wafer. Disadvantages include high vacuum requirements, complex and costly equipment, and slow growth rate. Ultra high vacuum, that is required in the growth chamber, is extremely difficult to maintain, especially in the presence of heated substrates and heated effusion cells. Growth rate is typically a few microns per hour, which is very low compared to other techniques which have approximately a few microns per minute growth rates.

Ion Implantation

Ion implantation remains as the most economical method to form active layers for GaAs MESFET devices. In this procedure, dopant atoms are introduced into the substrate surface by ion implantation, with typical energies and doses of 30 keV to 400 keV and 10^{12} to $10^{14} atoms/cm^2$. Such implantation greatly damages the crystal lattice. This damage is healed by the method known as "activation of implant", in which a high temperature annealing step (~850 °C) is performed to anneal out the lattice damage and allow the implanted atoms to move onto lattice sites. Activation is generally in the order of 75% to 95%, and depends on the

implanting and annealing conditions. Main advantages of implantation are , its well establishment due to silicon industry, high uniformity over a wafer, economy, and capacity. Beyond these there is another major advantage, doping can be performed locally by selectively masking the wafer, no other technology offers such a flexibility (at least without major complications). The main disadvantage of the ion implantation is that the doping profile transition cannot be as abrupt as the epitaxial methods, since the implanted donors nearly follow a Gaussian distribution.

Chapter 2

MESFET Principles and Design

2.1 GaAs MESFET

2.1.1 Basic Structure and I/V Characteristics

MESFET in its geometrical structure, is very similar to *Field Effect Transistor* (FET) introduced by W. Shockley in the early 1950s.[1] Cross section and planar views of general structure of a MESFET is depicted in figures 2.1 and 2.2. Three metal electrodes, namely gate, drain, and source are in contact with a thin semiconductor (n-GaAs in this work) active layer. Contacts to both source and drain are accomplished by means of ohmic metallization, whereas, the gate is a Schottky barrier contact. Current through the active layer, the channel, can be controlled by the depletion region formed by the Schottky gate. As the reverse bias on the gate increases, the depletion layer penetrates deeper into the active region, and vice versa. When there is no potential difference between source and drain, the depletion region is symmetrical, however in normal operating conditions, drain is biased to a higher potential than source, thus gate-drain junction is more reverse biased than gate-source junction resulting in a deeper depletion region on the drain side.

Most microwave MESFETs, and those produced in our laboratory, are depletion mode devices. In this kind of devices, when there is no bias applied on

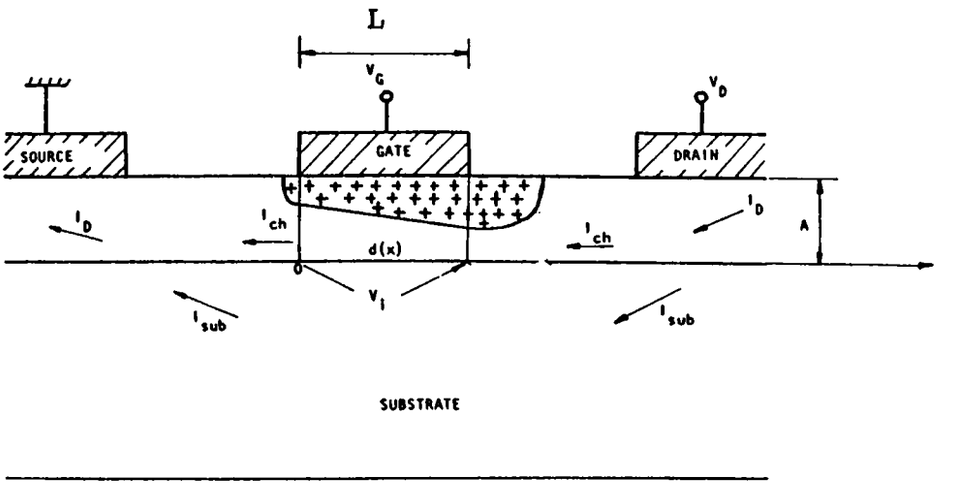

Figure 2.1: Cross section of a MESFET

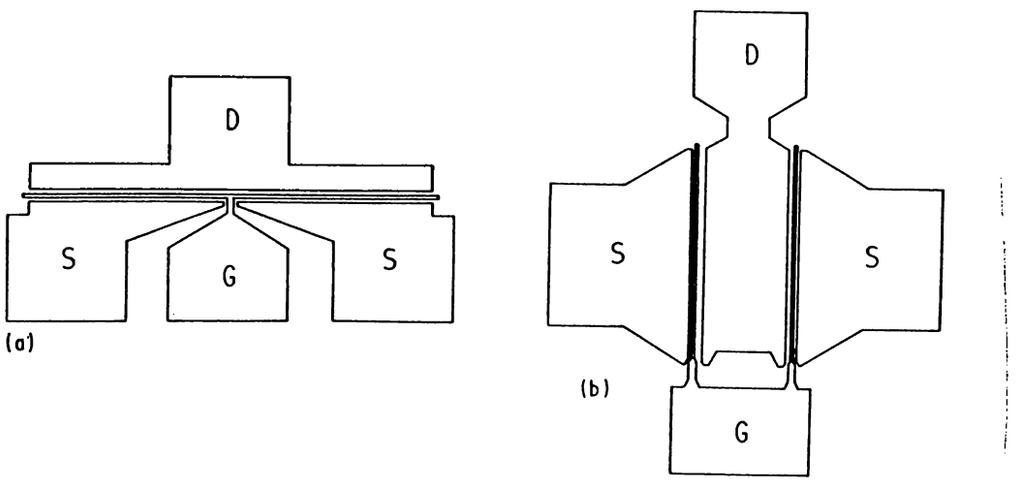

Figure 2.2: Plan views of MESFETs
(a) MESFET with "T" type gate, (b) MESFET with "Π" type gate

the gate, the depletion layer does not penetrate all through the active region, thus there exists a low resistance path for current through the drain-source terminals, namely the drain-source current, I_{ds}. Enhancement mode devices do not conduct current through drain-source contacts, unless a forward gate bias is applied. In this work enhancement MESFETs are disregarded. Hereafter, the term MESFET stands for n-GaAs depletion type device. For a depletion type MESFET, when

enough reverse bias is applied, the depletion region will extend across the entire active channel and will result in, although not infinity due to leakage currents, a high drain to source resistance. The potential required to deplete the channel is the "threshold voltage", V_T, and the corresponding phenomenon is known as "pinch-off" condition. For reasonably low biases, the current through the source-drain contacts is linearly proportional to the applied bias. Thus for small biases the region in between the source-drain terminals behave like an almost linear resistor. For larger biases, however, the semiconductor material (GaAs) itself limits the maximum carrier velocity, causing current saturation to occur. Figure 2.3 shows the current-voltage relationship expected from an ideal MESFET, as just described.

Actual MESFET I-V characteristics are similar to the ideal characteristics, with the important exception that the slope of the curves remains slightly positive even after saturation velocity is reached, which is due to the finite output conductance of the device. Charge domain formation, charge injection into the non-ideal semi-insulating substrate, surface effects and channel-substrate interface states are the main reasons of the finite conductivity. The magnitude of the current for a given drain-source bias will be directly proportional to the gate width, Z, of the device. On the other hand gate length, L, mainly determines device's gain and frequency characteristics. Gain and cut-off frequency, f_T, increases with decreasing gate length.

It is important to note that, for an optimal device performance, a decrease in gate length must be compensated with corresponding decrease in other device dimensions as well as an increase in channel doping densities.

2.1.2 Output Conductance and Transconductance

For analog applications, the I-V curves are not as useful as their derivatives. The derivative of drain-source current with respect to drain-source voltage, while gate-source voltage is kept constant, is defined as the output conductance of the MESFET, g_{ds},

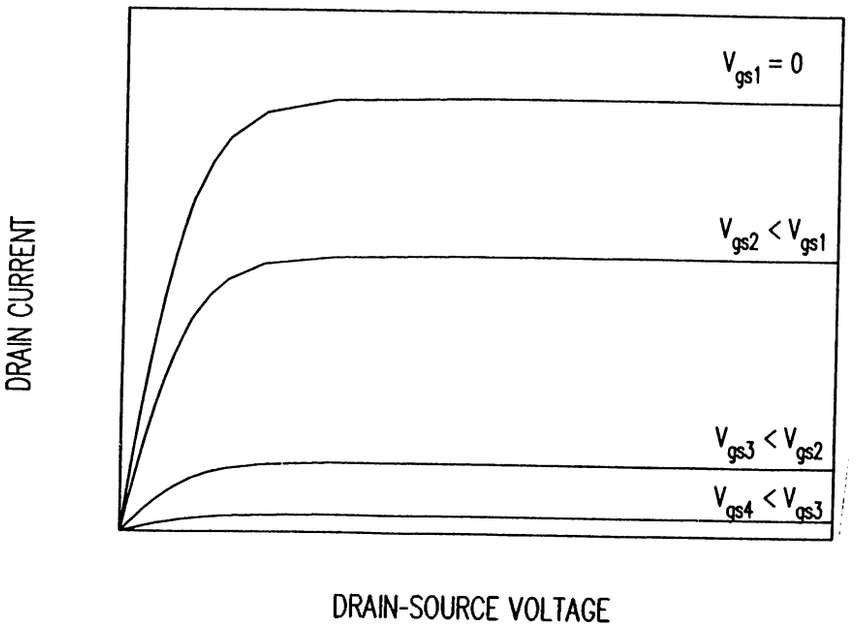

Figure 2.3: Ideal MESFET I-V characteristics.
Ideal drain-source current as a function of drain-source voltages for several gate-source voltages.

$$g_{ds} = \frac{1}{r_{ds}} = \left(\frac{dI_{ds}}{dV_{ds}}\right)_{V_{gs}} \tag{2.1}$$

where r_{ds} is output resistance sometimes used instead of output conductance.

The output conductance of the device is an important characteristic in analog applications, due to the fact that it plays a significant role in determining the maximum voltage gain available from the device and optimum output matching properties. Generally low output conductance, equivalently high output resistance, is required, which means flat $I_{ds} - V_{ds}$ curves. Output conductance is directly proportional to device gate width and inversely proportional to channel doping concentration, N_d, and active layer thickness , a.

Since deep levels play an important role in determining the output resistance of GaAs MESFETs, these characteristics are strongly frequency dependent at relatively low frequencies (DC to approximately 1 MHz).

The device transconductance, g_m, is defined as the slope of the $I_{ds} - V_{gs}$ characteristics with the drain-source bias kept constant,

$$g_m = \left(\frac{dI_{ds}}{dV_{gs}}\right)_{V_{ds}} \tag{2.2}$$

The transconductance of the MESFET is one of its most important indicator of device quality for microwave and millimeter wave applications. When all other characteristics are equal, a device with high transconductance will provide higher gains and better high frequency performance. Transconductance of MESFET is directly proportional to gate width and is inversely proportional to gate length. Deep levels cause a decrease in the transconductance, by the increasing frequency. Measured microwave transconductances are typically mentioned to be 5 to 25 % lower than measured DC values.[7]

2.1.3 Capacitance-Voltage Characteristics

Gate-source capacitance of a MESFET is defined as,

$$C_{gs} = \left(\frac{dQ_g}{dV_{gs}}\right)_{V_{gd}} \tag{2.3}$$

where Q_g is the depletion region charge beneath the gate. similarly gate-drain capacitance can be defined as,

$$C_{gd} = \left(\frac{dQ_g}{dV_{gd}}\right)_{V_{gs}} \tag{2.4}$$

Since source terminal is grounded under typical operating conditions, gate-source and drain-source bias voltages are those directly controlled. Thus, gate-source capacitance is often defined as,

$$C_{gs} = \left(\frac{dQ_g}{dV_{gs}}\right)_{V_{ds}} \tag{2.5}$$

Equations 2.3 and 2.5 are not equivalent, but describe slightly different quantities. This difference is usually small but can be significant if calculations are based on physically based models. Nevertheless, these capacitance definitions are not used in theoretical or experimental studies, instead, use of equivalent circuit capacitances is preferred.

The gate-source capacitance is one of the main parameters that determine the input impedance and frequency performance. To first order, the input impedance of a MESFET in a standard common source configuration, with typical bias levels applied, is simply the impedance of the gate-source capacitance in series with a few ohms of resistance. Thus, gate-source capacitance must be reduced to improve the high frequency performance. The gate-source capacitance increases with increasing gate length, gate width, channel doping density, and gate-source voltage. The dependence on geometry is not linear due to fringing charge effects.

It is clear that the gate-drain capacitance of MESFET is closely related to gate-source capacitance. In the normal mode of operation for amplifiers and oscillators, primary characteristic affected by the gate-drain capacitance is the reverse isolation of the device. Gate-drain capacitance increases with increasing gate length, gate width, channel doping density, and gate-drain voltage, similar to gate-source capacitance as expected because of symmetry.

2.1.4 Second Order Effects

The basic operating principles discussed up to this point do not explain some deviations from ideal characteristics under certain operating conditions. However, for some applications an understanding of such deviations from first order theory can be critical. Especially, the low frequency dispersion of device characteristics, and the behavior of the device near pinch-off often cause deviations from the first order predictions. Device characteristics which have been observed to

shift at low frequencies include output resistance, transconductance, and device capacitances.[8] For small signal applications these effects can be ignored since the frequency of interest is well above these frequencies, but for large signal applications these effects must also be taken into account.

Output Resistance as a Function of Frequency

Many of the electrical characteristics of GaAs MESFETs shift dramatically at low frequencies[9] (below about 1 MHz). As frequency is increased above DC, device output resistance can drop by as much as an order of magnitude. The frequency range of the transition can vary from below 10 Hz to more than 1 MHz. Although these frequency dispersion effects take place well below the frequency bands of typical operating frequencies, they still affect the large signal performance. The low frequency dispersion effects also causes complications in the parameter extraction techniques.

Transconductance as a Function of Frequency

Low frequency shifts in transconductance values are also observed for MESFETs, whereas the shifts are typically, on the order of 5 to 25 % as mentioned earlier. However, even these small drops in the transconductance can cause unpredictable errors in device modeling applications, especially for large-signal circuitry.

Sub-threshold Effects

When MESFET is biased near pinch-off, the physical phenomena that dominate the device performance are different than those under normal operating conditions. As a result the pinch-off occurs more gradually than predicted by most models, which can be extremely important for digital applications and for certain mixer topologies. In the theoretical definition of threshold it is assumed that depletion region is completely free of mobile carriers and the substrate is a perfect insulator. In an actual device, the boundary between the edge of the depletion region and the un-depleted channel is gradual and occurs over

a distance of several Debye lengths. A graded transition also occurs between the active channel and the substrate, and as the device is pinched-off, these two graded regions are forced closer to each other. When these two transition regions meet each other the free carrier density in the channel never reaches the background donor density level, also high electric field values at the channel-substrate interface can cause carrier injection into the substrate. These effects cause a more gradual decrease of current as the device is biased towards pinch-off.

2.2 Analytical Models for MESFETs

2.2.1 Introduction

Although basic concepts of MESFETs are well understood, device modeling is still a challenging problem. The modeling is important for computer aided design and simulation of circuits. There are several approaches for analytical modeling of low frequency characteristics of MESFETs. In following sections two main approaches, namely "square law" and "complete velocity saturation" models, preceded by an outline of "long-channel" model, are discussed. Square law model provides an accurate model for low voltage pinch-off MESFETs and an approximate description for higher pinch-off voltage MESFETs. The complete velocity saturation model accurately describes high pinch-off voltage devices but overestimates the drain-source current in low pinch-off voltage devices. However, both models take into account the source and drain series resistances and the output conductance, providing simple analytical expressions for current voltage characteristics, which are in good agreement with experimental data.

2.2.2 The Long-Channel (Shockley) Model

The analysis of MESFET is usually carried out in parallel to that of JFETs, since their structures are very similar. The first analysis was carried out by Shockley,[1] with the assumption of two gates, on the two opposite sides of active channel, depleting through the channel. The analysis of MESFET is similar but carried

out with a single Schottky gate. In this model a uniform effective channel donor density equal to electron density in the un-depleted active region and a constant mobility is assumed. Thus threshold voltage, V_T is given by

$$V_T = -V_p + V_{bi} \tag{2.6}$$

where, V_p is the pinch-off voltage, defined across the channel and given by

$$V_p = \frac{qN_d a^2}{2\epsilon_s}. \tag{2.7}$$

Shockley also used an approximation so called "gradual channel", which is based on the assumption that the bias of the gate junction is a slowly varying function of position.

The fundamental equation of the field effect transistor is obtained by integrating incremental potential change from the source side to the drain side of the gate with respect to distance along channel, that is

$$I_{ch} = g_0 \left(V_i - \frac{2}{3} \frac{(V_i + V_{bi} - V_G)^{\frac{3}{2}} - (V_{bi} - V_G)^{\frac{3}{2}}}{V_p^{\frac{1}{2}}} \right) \tag{2.8}$$

where I_{ch} is the channel current, V_i is the voltage drop in the channel across the region under the gate, and

$$g_0 = \frac{q\mu N_d Z a}{L} \tag{2.9}$$

is the conductance of the metallurgical channel. If series resistances of drain to gate and gate to source regions are neglected, then $V_i = V_{ds}$. Fundamental FET equation is only applicable up to the pinch-off. When $W(L) = a$ (pinch-off condition) current saturation occurs, and the Shockley saturation voltage is

$$V_{i,sat}^S = V_p - V_{bi} + V_G \tag{2.10}$$

where S stands for Shockley. Thus, the saturation current is

$$I_{ch,sat}^S = g_0 \left(\frac{1}{3} V_p + \frac{2}{3} \frac{(V_{bi} - V_G)^{\frac{3}{2}}}{V_p^{\frac{1}{2}}} - V_{bi} + V_G \right). \tag{2.11}$$

The transconductance in the linear region can be derived from fundamental equation as

$$g_m = g_0 \frac{\sqrt{V_i + V_{bi} - V_G} - \sqrt{V_{bi} - V_G}}{\sqrt{V_p}}, \tag{2.12}$$

and the transconductance in the saturation region is

$$g_m^S = g_0 \left(1 - \sqrt{\frac{V_{bi} - V_G}{V_p}}\right). \tag{2.13}$$

For small drain-source voltages, $V_i \ll V_{bi} - V_G$, channel current and transconductance can be approximated by

$$I_{ch} \simeq g_0 \left(1 - \sqrt{\frac{V_{bi} - V_G}{V_p}}\right) V_i \tag{2.14}$$

$$g_m \simeq \frac{g_0}{2} \frac{V_i}{\sqrt{V_p(V_{bi} - V_G)}}. \tag{2.15}$$

Gate-source and gate-drain capacitances are defined as

$$C_{gs} = -\frac{\partial Q}{\partial V_g} \Big|_{V_i - V_G = constant} \tag{2.16}$$

$$C_{gd} = \frac{\partial Q}{\partial V_i} \Big|_{V_G = constant} \tag{2.17}$$

Q is the total charge in the depletion region given by

$$Q = qN_d Z \int_0^L W(x)\, dx \tag{2.18}$$

Except in the region close to the pinch-off, where the Shockley model is not applicable because the extension of depleted region beyond the gate should be taken into account, solutions for capacitances can be approximated by[10]

$$C_{gs} = \frac{C_{gs0}}{\sqrt{1 - V_{gs}/V_{bi}}} \tag{2.19}$$

$$C_{gd} = \frac{C_{gs0}}{\sqrt{1 - V_{dg}/V_{bi}}} \tag{2.20}$$

where

$$C_{gs0} = C_{dg0} = \frac{ZL}{2}\sqrt{\frac{\epsilon_s q N_d}{2V_{bi}}}. \tag{2.21}$$

When there is no bias applied to the MESFET, total gate capacitance is equal to that of the depletion region due to built in potential, which is equally divided between source and drain because of symmetry. For non zero biases, C_{gs} and C_{dg} behave as capacitances of equivalent Schottky diodes connected between the gate and the source, and gate and the drain, respectively.

2.2.3 Velocity Saturation-The Square Law Model

Shockley's model assumes a non saturating electron velocity, which is a very crude approximation. Pucel *et al.*[11] proposed a simple approximation for the field dependence of the electron velocity assuming that the velocity is proportional to the electric field until the value of saturation velocity v_s is reached at $\mathcal{E} = \mathcal{E}_s$ and then becomes constant

$$v = \begin{cases} \mu\mathcal{E}, & \mathcal{E} < \mathcal{E}_s \\ v_s, & \mathcal{E} \geq \mathcal{E}_s \end{cases} \tag{2.22}$$

The velocity saturation is first reached at the drain side of the gate where the electric field is highest according to the Shockley model, *i.e.* when $\mathcal{E}(L) = \mathcal{E}_s$ which is equivalent to

$$\left(\frac{du}{dX}\right)_{X=1} = \alpha \tag{2.23}$$

where

$$\alpha = \frac{\mathcal{E}_s L}{V_p}, \tag{2.24}$$

$u = V(x)/V_p$ and X=x/L, and origin of x is defined to be on the source side end of the gate. For large α, $\alpha \gg 1$, solution approaches

$$V_{i,sat} + V_{bi} - V_G = V_p \tag{2.25}$$

which is identical to corresponding equation 2.10 of Shockley model. The opposite limiting case, $\alpha \ll 1$ and $\alpha \ll 2(1-\sqrt{\frac{V_{bi}-V_G}{V_p}})\sqrt{\frac{V_{bi}-V_G}{V_p}}$, corresponds to the velocity saturation model

$$V_{i,sat} = \alpha V_p \tag{2.26}$$

The saturation current is given by

$$I_{dss} = qN_d v_s Z(a - W(L)) \tag{2.27}$$

where the depletion region width $W(L)$ at the drain side of the gate is given by

$$W(L) = a\sqrt{\frac{V_{bi} - V_G + V_{i,sat}}{V_p}} \tag{2.28}$$

In dimensionless units i_s ($\equiv I_{dss}/g_0 V_p$) is

$$i_s = \alpha(1 - \sqrt{u_s + u_G}) \tag{2.29}$$

where $u_s = \frac{V_{i,sat}}{V_p}$ and $u_G = \frac{V_{bi}-V_G}{V_p}$ are dimensionless saturation and gate voltages. In the limiting case, $\alpha \to \infty$ (long gate device with a small pinch-off voltage) equation 2.29 reduces to the corresponding equation 2.10 of the Shockley model. In the opposite case, $\alpha \ll 1$, (short gate and/or large pinch-off voltage)

$$i_s = \alpha(1 - \sqrt{u_G}) \tag{2.30}$$

which corresponds to the simple analytical model proposed by Shur,[12] and can be approximated by the interpolation formula,

$$i_s = \frac{\alpha}{1 + 3\alpha}(1 - u_G)^2 \tag{2.31}$$

which coincides with the equation used for JFET saturation current in the SPICE model[13]

$$I_{dss} = \beta(V_G - V_T)^2 \tag{2.32}$$

where

$$V_T = V_{bi} - V_p \tag{2.33}$$

and transconductance parameter β chosen as

$$\beta = \frac{2\epsilon_s \mu v_s Z}{a(\mu V_p + 3v_s L)} \tag{2.34}$$

This may be an explanation for success of SPICE JFET model used in some cases for MESFETs. The transconductance at the onset of saturation is

$$g_m = 2\beta(V_G - V_T) \tag{2.35}$$

Equation 2.34 is dependent on V_p which is a function of two main parameters doping concentration and channel thickness. In figure 2.4, the variation of β vs. V_p characteristics with varying doping and active channel thickness is shown.

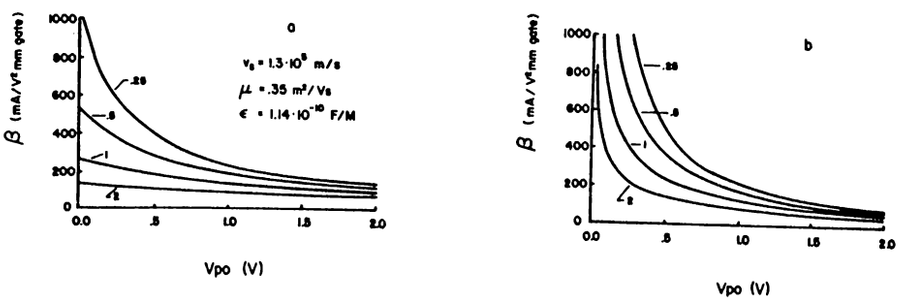

Figure 2.4: β at the onset of the saturation vs. V_p.
(a) V_p varies due to the variation in doping (a=0.1 μm); (b) V_p varies due to the variation in the thickness of the active layer ($N_d = 1.2 \times 10^{17} cm^{-3}$). Numbers near the curves correspond to the gate lengths in micrometers.

Transconductance at low pinch-off voltages increases for devices with sub-micron gates. The values of β (hence, transconductance for the same voltage swing) increase with the decrease of the device thickness and with the increase in doping. However increase in β is followed by increase in device capacitances, C_{gs} and C_{dg} (see equations 2.19- 2.21), while the parasitic capacitances do not increase, therefore thin and highly doped layers increase the operation speed. High doping

also has the advantage of decreased active layer thickness for a given value of the pinch-off voltage, which makes it possible to minimize short channel effects which are observed for $L/a < 3$.[14]

The analyses given above are valid only for the case when electron velocity saturates at the drain side of the gate. At higher drain-to-source voltages the electric field in the channel increases, resulting in velocity saturation in larger portion of the channel (gate length modulation). This effect was noted by Pucel, Haus, and Statz,[11] so that the models that include gate length modulation are sometimes referred to as the PHS (Pucel-Haus-Statz) model, although two region model is a more commonly used name. Works of Shockley[1] and Shur[15] results in a rather complicated expression for the saturated portion of gate length, L_s. Further work of Curtice[16] and Chen *et al.*[17] resulted in the rather simple equation for drain-source current,

$$I_{ds} = I_{sat}(1 + \lambda V_i)\tanh(\eta V_i) \tag{2.36}$$

where η is chosen in such a way that for $V_{DS} \to 0$ equation 2.34 transforms into a corresponding equation of the Shockley model.

$$\eta = G_{ch}/I_{sat} \tag{2.37}$$

where

$$G_{ch} = g_0(1 - \sqrt{u_G}) \tag{2.38}$$

is the channel conductance at low drain-source voltages predicted by the Shockley model,

$$g_0 = qN_d\mu Za/L \tag{2.39}$$

is the full channel conductance. This model is referred to as square law model. Experimental[18] and theoretical[19] works increase the evidence that square law model is approximately valid for low pinch-off voltage devices. The source and

drain series resistances R_s and R_d can be included in the model as follows. The gate voltage is

$$V_{gs} = V_G + I_{sat}R_s. \tag{2.40}$$

Constant λ in equation 2.36 is empirically determined and accounts for the additional output conductance beyond the output conductance due to gate length modulation. The drain-source voltage is

$$V_{DS} = V_i + I_{sat}(R_s + R_d) \tag{2.41}$$

which completes the set of equations of analytical square law model. Last thing to note is that, this model has the slight difference from Curtice model,[16] used for parameter extraction in our laboratory, that it includes the gate length modulation effect and source and drain series resistances.

2.2.4 Complete Velocity Saturation Model

The value of β approaches to the value which corresponds to complete velocity saturation everywhere in the channel when

$$V_p \gg 3\mathcal{E}_s L. \tag{2.42}$$

For $1\mu m$ gate MESFETs $\mathcal{E}_s L$ is close to 0.3-0.4 V so that above condition is satisfied by pinch-off voltages higher than 3 V. At such pinch-off voltages the assumption of complete velocity saturation in the channel becomes valid,[12] which means that at large drain-source voltages, voltage drop, V_{si}, across the region where electron velocity is not saturated, can be neglected compared with $V_{bi} - V_G$

$$V_{si} \ll V_{bi} - V_G. \tag{2.43}$$

The expression for drain-source saturation current for this case is[12]

$$I_{sat} = qN_d v_s Za(1 - \sqrt{u_G}). \tag{2.44}$$

According to equation 2.42 this equation may not be satisfactory close to the threshold when voltage drop V_{si} may lead to a considerable relative change in the width of the un-depleted region and hence in the drain-source saturation current. However, even in this region equation 2.44 can still be used as a satisfying interpolation formula.

The source series resistance does not change V_{gs} (compared to V_G) at low values of V_i because the values of the channel current and hence of the voltage drop across R_s are small, which enables the use of the same interpolation formula (equation 2.36) for drain-source current as for the square law model.

$$I_{ds} = I_{sat}(1 + \lambda V_i)\tanh(\eta V_i) \tag{2.45}$$

where η is chosen in such a way that, as $V_{DS} \rightarrow 0$ above equation transforms into a corresponding equation of the Shockley model

$$\eta = \frac{G_{ch}}{I_{sat}} \tag{2.46}$$

where G_{ch} is given by equation 2.38, constant λ is the same empirical constant which is used in the square law model to account for the output conductance. The drain-source voltage

$$V_{DS} = V_i + I_{sat}(R_s + R_d) \tag{2.47}$$

completes the set of equations for analytical complete velocity saturation model.

2.3 Small-Signal Model

Small-signal MESFET model is very important for a circuit designer since it provides lumped element approximation for the device, which can be used in circuit simulators. A well chosen model, with properly extracted elements will work for frequencies higher than those at which model parameters are extracted. Another property of this model is that it enables device scaling, which enables performance prediction of unmeasured devices which can be scaled to a modeled

one. In this work the most widely used small-signal model in figure 2.5 is considered. This model has the advantage that its elements can be uniquely determined from S-parameter data and provides an excellent match with S-

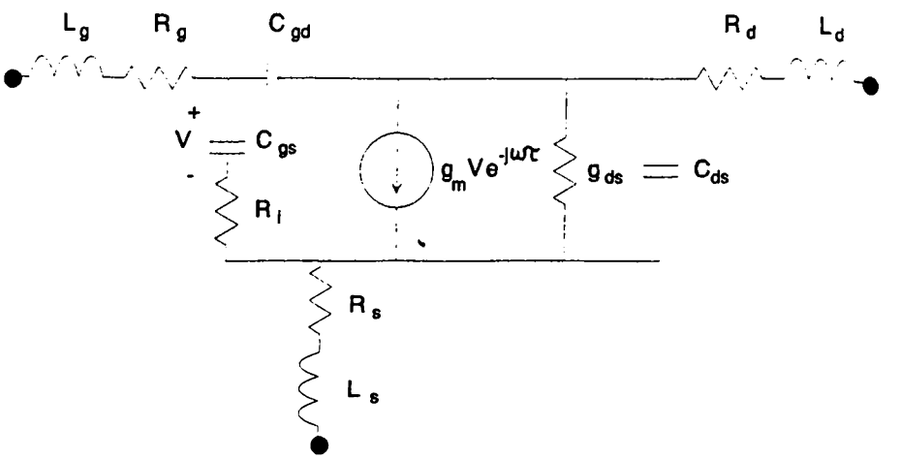

Figure 2.5: MESFET small-signal model.

parameters up to 26 GHz.[7]

Equivalent Circuit Elements

In figure 2.6 the small-signal model is drawn on cross section of MESFET, in order to clarify physical origins of model elements. Each of these elements are explained below. The elements other than parasitic ones, namely L_g, L_d, L_s, R_g, R_d, and R_s, make the intrinsic MESFET.

Parasitic Inductances The parasitic inductances are mainly due to the metal pads of the device, therefore they are highly geometry dependent and analytical modeling is extremely hard. In general, gate inductance is higher than drain and source ones, especially for short gate length devices. Typical values given in literature[7] are on the order of 1-10 pH. If the device is packaged, these inductances will increase depending on package and bonding, and the dominating inductances will be those of the bonding wires and package.

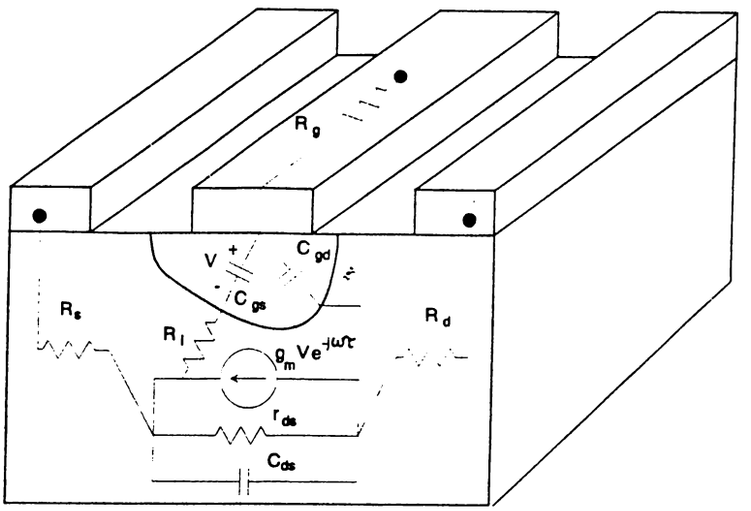

Figure 2.6: MESFET small-signal model showing physical origins of elements.

Parasitic Resistances The resistances R_s and R_d correspond to the resistances due to ohmic contacts and bulk semiconductor up to the channel, the gate resistance R_g corresponds to the resistance of the Schottky contact. For the devices with dimensions close to those fabricated in our laboratory, all of these resistances are on the order of a few ohms. Although these resistances show slight bias dependence, they are usually assumed to be equal to their $I_{dss}/2$ values for device modeling.

Capacitances The capacitances C_{gs} and C_{gd} correspond to depletion charge variations in response to gate-source and gate-drain voltages respectively. The drain-source capacitance C_{gd} corresponds to the geometrical capacitance between drain and source metals. Other geometric capacitances, especially when the back surface of wafer (as for the MESFETs produced in our laboratory) is not coated with a conductor, can be neglected due to large distances compared to that of drain-source distance. Under normal bias conditions, depletion region close to drain is thicker than the part close to source as shown in figure 2.6, so that C_{gd} is larger than C_{gs}. C_{gs} and C_{gd} are bias dependent, however C_{ds} is not considered

to be so. Typical values of C_{gs} is on the order of 1 pF/mm gate width. Other two capacitances are usually a fraction of C_{gs}. Symmetry implies that $C_{gs} = C_{gd}$ for $V_{ds} = 0$.

Transconductance The transconductance g_m models the current modulation effect of the depletion region beneath the gate. Transconductance is inversely proportional to gate length L, and directly proportional to gate width.

Output Conductance Output conductance g_{ds} models the variation of drain to source current in response to drain-gate voltage variation. It is inversely proportional to gate length and is frequency dependent. RF output conductance can be significantly higher than DC output conductance due to deep level states.

Transconductance Delay The depletion region width does not change instantaneously in response to a change in gate voltage, the delay of this response is modeled by the transconductance delay τ. Propagation delay of the applied electrical signal also contributes to τ.[20] Typical values of τ are on the order of 1 ps.

Charging Resistance Main function of the charging resistance R_i is to improve S_{11} matching. However, in literature[7] it is noted that the presence of R_g is usually sufficient to match the real part of S_{11} and also that extraction of R_i is a difficult task, therefore if possible can be neglected. The physical meaning of this resistance is not clear as well.

2.4 Design of MESFETs

Masks, for the MESFETs fabricated in our laboratory, were designed by the layout editor ARTIST, of CADENCE software. Since the material (GaAs wafer with MESFET structure on it) to be processed were not present and even its characteristics were not determined by the time of design, the MESFET design

was carried out for a very general structure. There had been reports on rules for scales of MESFETs, relating channel dopant concentration to gate length.[21,22] These reports give simple formulas for channel doping, for a first order estimate of optimal device performance. All of the given formula can be approximated by the following formula[23]

$$N_d = \frac{1.6 \times 10^{17}}{L} \tag{2.48}$$

for $L \sim 1\,\mu m$. According to this formula, in case of a moderately doped ($\sim 10^{16}\,cm^{-3}$) channel, longer gate length will result in a more optimized device. Thus inclusion of various gate length devices helps process optimization. In our design, for higher transconductance and cut-off frequency demands, 1 μm gate length MESFETs were included. Also 2 and 3 μm gate length devices were included. For each MESFET gate length, two different geometry for gate fingers were designed. One type was with "T" shaped and the other was with "Π" shaped gate finger geometry. Also, for possibility of having problem due undercut profile of GaAs, each type of device was oriented in two perpendicular directions.

All of $1\,\mu m$ devices has gate width of $50\,\mu m$, however For 2 and 3 μm devices gate widths of 50, 100, and 200 (for only Π shaped gate) μm exist.

The distances between gate-drain and gate-source contacts were also varied from device to device. All of the 2 and 3 μm device gates were symmetrically placed in the channel, that is, the spacings between gate-source and gate-drain contacts were equal. These spacings were designed to be 1 and 2 μm. Spacings were 2 μm for 200 μm gate widths, 1 μm for 50 μm gate widths. Both value of spacings were used for 100 μm gate width devices. Thus there are 7 different types of 2 and 3 μm MESFETs.

For 1 μm gate length devices, gate-source spacing was 2 μm and gate-drain spacing was 1 μm. Thus there are two different types of 1 μm MESFETs.

However, during mask alignment it came out that we cannot control the exact place of gate in between source and drain, therefore in the actual devices these spacings are not controllable.

For metallization, extension of metals over the mesas were planned such that, a metallization (except for gate metal) covers mesas in the corners, so that if

in one direction undercut profile of mesa causes problem, in the other direction no problem arises due to undercut. For RF probing short coplanar waveguides, whose grounds are terminated at sources of MESFETs, were also included in the final metal mask.

For material characterization, FATFETs of 50 μm gate lengths and 100 μm gate widths were designed, with 2 μm gate-source and gate-drain spacings.

For ohmic-contact characterization, TLM structures of 20 μm width with 2, 4, 8, 10, 15, 20, and 25 μm contact spacings were designed.

Alignment marks were designed such that, in each mask level alignment with the previous mask and/or the first mask was possible. Some simple MMIC circuits, MIM detectors, Hall structures, and some resistor structures were also included in the mask, which are beyond the scope of this thesis work.

Chapter 3

Fabrication Processes

3.1 General Outline of a MESFET Process

Fabrication process of MESFET is largely dependent on the wafer to be processed, however basic process steps do not differ much. Since there had been no experience in GaAs process until March 93, the basic process steps, such as lithography, were studied on Si samples. After the device quality wafer and masks arrived the actual process begun. Most critical process steps in fabrication are lithography, alignment of masks (especially gate mask), lift-off, and alloying. Process starts with mesa etching for isolation of devices from each other. Mesa etch is done such that the active channels of each mesa are isolated. Depth of mesa is dependent on wafer doping profile. Following the mesa etch ohmic metalization is done by the lift-off method. To obtain ohmic contacts, this metal must be alloyed. Composition and alloying temperature of ohmic contacts are observed to be the most critical processes. After lift-off and alloying the Schottky metal is applied by means of lift-off. Then if the processes are successful, one obtains working MESFETs, however, in order to be able to probe the devices, a last metal deposition must be performed, since the geometry of devices are not appropriate for RF probing and also thickness of Schottky plus ohmic metalization thickness is not sufficient for good probing. If one tries to increase these thicknesses, lift-off process will be very risky due to small dimensions in ohmic and gate masks.

3.2 Sample Cleaning

The cleanliness of the sample (a piece of wafer),the materials used (metals, chemicals, etc.), environment, and the masks are extremely critical in the success of the fabrication. A dirt in an early process step results in larger dirts or defect as the forthcoming processes are performed. The formula for yield of a process, with the assumption that the defects are uniformly distributed, is[24]

$$Y = \exp(-DA_c) \tag{3.1}$$

where D is the defect density and A_c is the critical or active area of the sample in process. The critical area is the area of the devices that when a defect exists in this area, device will not work appropriately. Thus the cleanliness is important for a high yield.

The environment cleanliness for our process was very good. All the processes were carried out in a class 100 (a cubic foot of air contains less than 100 particles that are $0.5\,\mu m$ or greater in diameter) room, however routine checks had shown that the environment was much cleaner than this value since this room was planned for a larger working group. Human is the main source of airborne dirt and dust in the environment, so that cover-alls, hoods, and booties are worn in this environment. Also during processes gloves (against dirt from hands and/or protection from chemicals) and masks (against any possible particle from face) are used. Temperature of the environment is kept constant at $21 \pm 1\,^{\circ}C$.

3.2.1 Cleaning Techniques

Cleaning of materials and samples before each process is a must. For wafer cleaning the common method used is TCE (trichloroethylene), acetone, and iso-propanol (iso-propyl alcohol) hot baths. Each of these chemicals are semiconductor grade (SC), that is, they are extremely pure and filtered in sub-microns. These chemicals are heated in beakers up to their boiling points and sample is kept for a few minutes in each one sequentially. The preferred technique is to use the vapor of these chemicals, since it contains less contaminants, however

in this technique contaminants on tweezers may also move onto samples therefore care must be taken with cleanliness of holders also. The contaminants removed by these chemicals are oils, grease, and residual photoresist. Dust like dirts are removed by nitrogen blow prior to wet cleaning. After these three baths sample is either cleaned with flowing DI (de-ionized) water or directly dried with nitrogen blow. Cleaning before metalization also includes a HCl (hydrochloric acid) bath for removal of oxide layer. The metals evaporated are also cleaned by the conventional TCE and acetone bath prior to being loaded in the evaporation boats. Masks are cleaned before and after each process by means of rinsing in acetone followed by an iso-propanol rinse. For stubborn resists AZ100 commercial resist remover is also used, but mask cleaning by this solvent is avoided for the possibility that it may attack the metalizations of masks although we had not observed any such effect. Sometimes for non-critical steps cleaning on the spinner is also performed, for example for the final metalization this method is sometimes used. Cleaning is the most frequently performed process in manufacturing of devices.

3.3 Photolithography

Photolithography follows cleaning in frequency. Almost before any major process a photolithography step is performed. Photoresist are energy sensitive chemicals that change their chemical properties under exposure to light. Photoresist coating is done by means of spinner. Thickness of resist coating depends on the spinning speed and resist viscosity. There exist two kind of photoresists, positive and negative. Positive resist is the one that exposed parts are developed (removed) by a special solvent called developer, for negative resist reverse is true, that is un-exposed parts are developed. In MESFET processes carried out in our laboratory commercial positive resists AZ5214 and AZ4210 are used. Spinning speed for both of these resists were 6000 RPM for 30 seconds throughout all of the processes, resulting in $1.2\,\mu m$ and $1.8\,\mu m$ film thicknesses for AZ5214 and AZ4210, respectively. After the resist is spun it must be prebaked for a good

adhesion to the GaAs surface. If this prebake is done on a hot-plate, the time required is a few minutes, however, in the oven, the required time rises by a factor of 10 or so. By trial and error, resist prebake temperature in the oven is chosen to be $95\,^{\circ}C$ for half an hour, on the other hand, for hot-plate $100\,^{\circ}C$ prebake for 1 minute gave good results. Nevertheless, since accurate control of hot plate was very difficult, oven is used for baking throughout the fabrication. After the prebake the resist is cooled down to room temperature. The spun resist thickness is not uniform over the sample, at the edges thickness of the resist increases by a factor of two or so, therefore especially for critical steps (ohmic and gate metalization masking steps), the edges must be removed for a good contact of the mask and resist surface. By using appropriate shaped Si or GaAs wafer pieces these edges are exposed and developed prior to exposure through the photo mask. After several trial and errors, the exposure time was decided to be 1 minute at 12 mW optical power at E-line (320 nm) of the mercury exposure lamp for masks other than gate mask. For the gate mask the conditions are the same except for a 20 second exposure time. The reason for different exposure times is that, gate mask is made on a quartz substrate which has about 90 % transmittance at the exposure wavelength which is two times higher compared to others which are made on alumino silicate substrates with about 40 % transmittance at the wavelength of interest. Also difference in resists and their thicknesses are effective for determining the exposure conditions. After exposure if the forthcoming process contains lift-off, the sample is dipped in chlorobenzol for 15 minutes, the reason of which will be explained in lift-off section. Development is done in a 1:4 developer (AZ400 K): DI water solvent. This rate is advised in the data sheets of the developer and gives good edge shape and moderate development time (1 to 4 minutes, depending on process, resist, and exposure). Determining whether the resist is developed or not is very critical especially for lift-off. This profession is gained by experience since development times for the same processes have been observed to be different from time to time, some uncontrollable parameters such as slight variations in concentration, heat or prebake may be affecting this time duration. When developing the resist since

the patterns are on the order of a few ten of microns for most of the masks, the thing to observe is the slight color variations on the sample, and when shining a light on the sample. After this experience is gained, development is usually successful. This success is very important since in our work it is observed that, especially for small patterns, most of the contaminants come into scene after the developments. The reasons for this may be: some kind of contaminant that may be present in the developer bottle, which is very unlikely if someone had not made a really big mistake; some kind of contaminant coming from beakers used which is also unlikely since always same beaker was used for development and the problem has not been observed so frequently; partially developed resist forming residual contaminant, if not taken off the surface appropriately, which is the most probable reason. As the development is completed, the sample is rinsed in flowing DI water for more than 1 minute, then the sample is blown dry by nitrogen, and observed under an optical microscope. If sample is over-developed it can be cleaned by acetone and TCE, then it is processed again. In case of under-development the sample is immersed in developer once more, however, this second development is sometimes observed not to be very successful, since it introduces contaminants. However, by luck, one can get rid of these contaminants with a good rinse in DI water. If the forthcoming process is etching, prior to that a postbake is performed at $95\,^{\circ}C$ for 15 minutes for a better sticking of resist on GaAs. If this postbake is not done, wet etchant attacks through GaAs-resist interface and the etch geometry does not follow the resist geometry resulting in wiggly patterns. If for any reason unwanted resist remains on the sample even after the acetone rinse, then the AZ100 remover is used.

3.4 Wet Etching and Oxide Removal

For isolation of independent MESFETs, mesas are etched on the GaAs sample with a thickness such that the buffer layer is exposed to air. The high resistance of the buffer layer provides a good isolation between discrete devices. The etch depth must not be too high since in this case the metalization can be problematic

due to the fact that the metalization for ohmic contacts is usually on the order of $0.2\,\mu m$, about one to two tenth of a typical mesa height. Another possible problem can be anisotropic etching which is exhibited by most of the wet etchants. The etch profile of these etchants depends on the orientation, that is, for example, they etch different in $\langle 011 \rangle$ cleavage planes. Mesa walls in [110] direction make angles less than 90° with substrate while mesa walls in perpendicular direction, $[1\bar{1}0]$, make angles greater than 90°. The edges that have undercut etch may cause metalization discontinuities, thus this problem must be handled while designing masks, and depositing the metal. Metal thickness must not be small in order to cover such steps. The etchant used for mesa formation is a mixture of H_3PO_4 : H_2O_2 : H_2O (5:1:10 in volume) which is an anisotropic etchant. This etchant is also used for gate recess etch which enables Schottky metal to contact with active layer by removing highly doped cap layer. Initial etch rate of this solution is about $0.4\,\mu m/min$, but this rate changes with time. Therefore before each recess, small GaAs samples are used for determining the etch rate. After the etching, the surface of GaAs is oxidized which can cause problematic ohmic and Schottky contacts. In our processes only Schottky contacts coincide with etched GaAs, thus oxide removal is only needed after the gate recess. For oxide removal $HCl : H_2O$ (about 1:1 in volume) mixture is used for a few minutes. It must be noted that before using the etchants the resists must be post-baked as explained before and surface must be extremely clean in order to obtain a uniform etching. Non-uniform etching is especially observed close to mesas. This may be due to a very thin resist layer that cannot be developed easily because high surrounding resists which are not developed on purpose, may be affecting developer flow.

3.5 Lift-off

Unlike Si, metalizations for GaAs are not done by etching unwanted metal regions. The reason is mainly that many metal etchants also etch GaAs and the most widely used metal, gold, requires strong etchants that the etching of GaAs can not be avoided. Furthermore, the etching of composite metalizations, such as

AuGe/Ni/Au used for ohmic contacts, is a very difficult process. Due to all of these problems the lift-off technique is preferred in GaAs metalizations. In this technique the required pattern is obtained by exposure and development, such that the parts of GaAs that will be coated by metal are exposed to air. Then sample is coated with required metal composition. If the edge shape of developed resist is appropriate and the resist is at least two or three times thicker than the overall metal thickness then resist can be removed, in acetone for example, with a lift-off of unwanted metalization. This technique is critical in the sense that if it is not satisfactory there is no return. Lift-off is done in hot acetone and by experience one can decide in a few minutes time whether it will be successful or not. In our process, we helped the lift-off by flushing the acetone using a syringe and in some cases ultrasonic cleaner was also used. However, ultrasonic cleaner must be the last try since it causes the tearing-off of the required metalizations and it may also brake the sample since GaAs is very fragile. For an easy lift-off the edge shape of resist must be undercut. This edge shape is realized by putting the sample in chlorobenzol for 15 minutes before development. Chlorobenzene increases the resistance of the resist against developer at the surface, thus surface development of the resist becomes slower than other parts which results in the required edge shape. This technique works well with both of the resists used in MESFET processes.

3.6 Metalizations

Metalizations are the vital part of the processes, especially ohmic metalization to GaAs is a very complicated and yet not fully understood problem. Choice of metalization system depends on the contact type and facilities of evaporation. In our laboratory we do not have an e-beam evaporation system yet operational, thus it is not possible to use Pt in Schottky metalization, which prevents the diffusion of Au into GaAs.

3.6.1 Ohmic Contacts

In literature, various metalization systems are proposed for ohmic contacts on n-type GaAs. Most commonly used metal composition is the eutectic AuGe (12 % Ge in weight) which has an approximate melting point of $360\,^{o}C$ with a Ni overlay. The lack of the reproducible and reliable ohmic contacts to moderately doped n-GaAs has been a problem from the beginning in GaAs technology.[25] The AuGe/Ni system also suffers from unreliability and un-reproducibility problems, however, it is noted that best alloyed ohmic contacts to n-GaAs are obtained with AuGe/Ni system,[26] therefore this system was chosen for ohmic contacts of the MESFET fabricated in our laboratory. Another criteria for choosing this system was the existence of an extensive literature compared to other systems.

Mechanisms of ohmic contact alloying has not been fully understood. However, it is commonly believed that Ge dopes the GaAs during alloying.[27] This phenomenon is explained as follows; above the melting point of eutectic alloy the metal melts and GaAs is dissolved in this melt. When cooling begins GaAs regrows epitaxially at the interface while keeping a high concentration of Ge as an n-type dopant with a concentration of about $2 \times 10^{19} cm^{-3}$. Au helps this process by gathering Ga. During this process, protrusions, which are believed to be able to dope Ge into GaAs and therefore to be the major paths of current flow, are formed and cause a rough interface.[28] A thin layer of Ni is believed to act as a wetting agent which prevents balling-up of the AuGe and to play a role of catalyst for the reaction between GaAs and Au and also to provide a driving force for Ge diffusion. The concentration of Ni should not exceed 2.67 % of AuGe in weight, otherwise GaAs solubility will increase resulting in nonhomogeneous island type growth of GaAs.[26] In literature, it is almost impossible to find a commonly used ratio of AuGe and Ni but taking data from several sources[24,26,28,25] resulted in that about $250\,\mathring{A}$ Ni for $1000\,\mathring{A}$ AuGe would work. For a period of time, we were out of W evaporation boats for Ni, thus we tried AuGe contacts without Ni and could not have satisfactory results. The exact total thickness of AuGe/Ni is not critical but proposed values are distributed in the $800 - 2500\,\mathring{A}$ range, however, contact resistance will increase as thickness gets smaller. It is also advised[24] to use

a final gold over layer in order to decrease sheet resistance and improve probing. This extra Au layer is believed not to degrade the contact due to the existence of Ni barrier. Thickness of this final Au layer is limited by lift-off process. It is chosen to be 2500 $\AA$.

The eutectic ratio of AuGe is satisfied either by using premade material, or evaporation of each metal in appropriate ratios. In our laboratory, the second method was used with 350 $\AA$ Ge and 600 $\AA$ Au deposition thickness which were monitored by means of a quartz crystal thin film deposition controller with an accuracy better than 10 %.

In MESFET life tests, gradual degradation of the source and drain AuGe ohmic contacts have been reported.[29] Also it is known that contact resistance of this system increases with increasing temperature, time, and bias.[30] It may degrade even near room temperature.[31] For the MESFETs produced in the first batch, the donor concentration was $2 \times 10^{17} cm^{-3}$ and the ohmic contacts were observed to die off within a few weeks time. The cause of this is most probably that, the increase in sample temperature during processes for final metalization enhanced the activation of the degradation mechanism and resulted in a fast kill of ohmic contacts. However, since during this time period no DC measurements were performed, so the cause and the time it takes to the loss of ohmic contact behavior were not determined uniquely.

3.6.2 Schottky Contacts

Almost any metal in contact with GaAs results in a Schottky barrier, however, good adhesion and thermal stability must be satisfied by a good Schottky metal. The last two criteria eliminate most of the metals, since GaAs diffuses rapidly in many metals causing degradation of Schottky contact. The common choices for Schottky contact to GaAs are Al, Cr, Mo, and Ti. However, these metals are not good conductors. In order to increase conductivity usually a gold overlay is deposited on top of the Schottky metal. On the other hand, gold has the drawback of diffusion through metals such as Cr and Ti. In order to prevent

this, a barrier layer such as Pt or Mo must be used in between. Thickness of the Schottky and the overlay metals are not critical, and are limited by the lift-off process.

3.7 Actual Processes

3.7.1 Mesa Isolation

Mesa isolation is the first major step in MESFET fabrication. This process started with a rectangular shaped (about 1.2×1.6 cm) GaAs sample cleaved in [110] and [1$\bar{1}$0] directions. Cleaning was done in standard hot TCE, acetone, and iso-propanol. Then a drop of photoresist AZ4210 was spun at 6000 RPM. After prebake in the oven for 30 minutes, sample was cooled down and edges are removed in 1:4 ratio of developer(AZ400 K):DI water solution. Mesa1 mask was aligned for optimum number of MESFETs, and resist was exposed for 1 minute. After the development, a postbake was done due to forthcoming etching process. The etch rate of the etchant H_3PO_4 : H_2O_2 : H_2O (5:1:10) is determined by testing on small GaAs pieces and observing the etch profile by means of DEKTAK 3030 depth profiler. The GaAs MESFET structure at hand has a 0.6 μm capping layer which is $2 \times 10^{18} cm^{-3}$ n-doped for a good ohmic metalization and has a 0.4 μm active layer n-doped to $4 \times 10^{16} cm^{-3}$ (see figure 3.1). Therefore, mesa etch was about 1.4μm deep in order to be far away from the tail of active layer doping. Before the mesa etch the resist thickness was measured by DEKTAK 3030. Etching was performed in a few steps such that the etch depth was measured following each step assuming that the resist is not etched much compared to GaAs (this fact was observed in previous etchings, that the resist is etched about 1:20 of GaAs). After the mesa etch is completed, resist leftovers are cleaned by acetone.

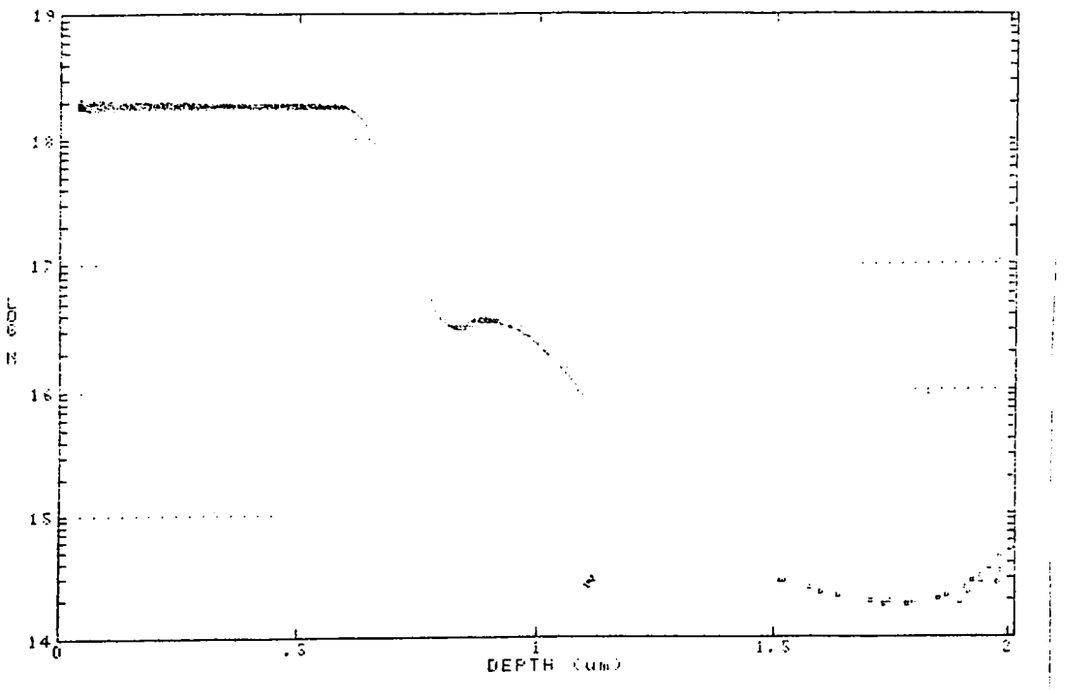

Figure 3.1: Carrier concentration profile of epi-wafer used for fabrication of MESFETs.

3.7.2 Ohmic Metalization

The sample was cleaned in a standard manner once more. It was coated with resist AZ4210 and was spun and prebaked. Ohmic metalization mask was aligned to mesa level pattern, already defined on the sample, by means of alignment marks and the sample was exposed to UV light for 1 minute. Before the development, the sample was kept in chlorobenzol for 15 minutes in order to harden the surface of the photoresist against the developer. The development was performed in a standard (1:4) developer solution and observed under an optical microscope. The GaAs surface was cleaned by HCl:DI water (approximately 1:1) solution

and the sample was loaded in Leybold L-560 box-coater. Evaporation of Au/Ge ($600\,\mathring{A}/350\,\mathring{A}$) was carried out in a vacuum of about $10^{-6} mtorr$. Since we can evaporate two different metals in one session, in the box coater, Ge boat is unloaded and Ni boat is loaded in the box-coater for an evaporation of Ni/Au ($250\,\mathring{A}/1500\,\mathring{A}$). After the evaporation the sample is unloaded and put in hot acetone for a few minutes. In order to promote the lift-off pressurized acetone is flush on the surface of the sample by means of a syringe. Then the sample was observed under an optical microscope while it was in acetone. If the lift-off metal dries on sample it is impossible to take it off. After being sure that all of the metal was lifted-off, the sample was taken out of acetone beaker while it is continually washed by pressurized fresh acetone to make sure that none of the metal pieces in the acetone beaker stick on the sample. In almost every lift-off process, a few of devices were shorted by means of partially thorn metals which are held on GaAs on one end thus can not be washed away easily. After lift-off is completed the metal thickness was measured to be around the value programmed into the deposition system. The error in total thickness was less than 10%, however the error in the ratios of the metals evaporated is expected to be much less than this value.

3.7.3 Alloying

Alloying is a very critical process for obtaining good ohmic contacts. In the literature, alloying temperatures for AuGe vary mainly between $400\,^{\circ}C$ and $460\,^{\circ}C$, thus, four different alloying temperatures, namely $400, 420, 440, 460^{\circ}C$, were tried with a sample cleaved into smaller pieces after mesa etch and ohmic metal deposition were completed. Alloying was carried out in RTP (rapid thermal processor) in a N_2 atmosphere. Samples to be alloyed were kept in $150 - 200\,^{\circ}C$ for a few minutes in order to heat the GaAs, then temperature was raised to the alloying value in 15-20 seconds and was kept constant for 1 minute. After the alloying, samples were left for cooling in the RTP. Then the electrical properties of the contacts were measured. Relative comparison of the alloyed contacts were

done by measuring the conductivity of Hall bars which were placed on the same chip. Comparisons of the four different samples showed that the best alloying temperature is $400\,^{\circ}C$. Considering the surface morphology and the fact that the observed resistances for Hall bars were comparable with $400\,^{\circ}C$ alloyed sample even with worse probing due to lack of Au on the surface, it is decided to use $420\,^{\circ}C$ for alloying. Actual MESFET sample was alloyed at $420^{\circ}C$ as noted before.

3.7.4 Gate Metalization

After alloying, the sample was cleaned by standard procedure. The MESFET structure at hand had a very thick, $0.6\,\mu m$ highly doped cap layer which could not be recessed, with gate resist pattern, successfully due to the small dimensions (1, 2, and 3 μm gate lengths) of openings on it. Therefore, the Au layer on top of the ohmic contacts were used as an etch stop for approximately 0.3 μm recess. Then oxide layer is removed by the HCl:DI (1:1) water mixture and the sample is cleaned again. Resist AZ5214 was spun at 6000 RPM and prebaked in oven as in previous processes. Then the resists at the edges were developed and gate mask was aligned to ohmic level. Since gates of 1 μm lengths exist on the mask this alignment step (especially angle alignment) is very difficult with the present optics and requires experience and tedious trials. After the alignment, the sample was kept in chlorobenzol for 15 minutes, then developed and observed under optical microscope. The sample was then post-baked in oven for the following gate recess process. GaAs is recessed through the patterned gate resist for removal of the highly doped cap layer thus enabling Schottky contact to the active layer. The etch of GaAs is defined by the gate slot on the resist pattern, however undercutting effect of etchant provides a larger recess width than the gate length. This effect in combination with the undercut profile of the resist results in a gate narrower than the recessed slot, thus surface depletion of gate is minimized resulting in smaller parasitic capacitances. For gate recess etchant's etch rate was determined as in the mesa etching and recess etch is done about 0.4 μm

deep. This etching was observed to be not uniform, however since the yield was not that important, fabrication process is carried on. Following the gate recess, oxide removal process was performed by HCl solution. As the gate metal, Ti/Au (200 $\AA$/2000 $\AA$) composition was evaporated in the box-coater. Lift-off process for the gate metal is a bit more difficult than that for ohmic or final metal since the thickness of resist layer, AZ5214, is less than that of AZ4210. However, this process is also well developed and usually no problem exists if the procedures explained in ohmic metalization section are followed.

3.7.5 Final Metalization

Although MESFETs are operational after gate metalizations, they are not suitable for probing, especially for RF probing. For good low frequency probing the metalization must be as thick as possible and the metal must make a good contact with the probe tip. For RF probing, in addition to these, the geometry of the metalization is also important. RF probing is performed with Tektronix TMP 9610 microwave probes which provide transmission from tapered coplanar waveguide, (CPW) with 100 micron pitch distance and 50 micron transmission-line width at the probe tip, to K-type microwave female connectors usable mode free to 40 GHz. Thus the final metalization for MESFETs provide two CPWs to drain and gate, whereas the source is connected to common outer strips of CPWs which provide ground path during probing. The final metal layer is also used for increasing the thickness of probe pads defined in earlier masks. The most suitable metal for this aim is Au. However, in earlier steps, Al was sometimes preferred since it is easily removed by developer AZ400 K. The reason for preference of removability of final level is explained in dielectric encapsulation section below. Final metal process was the same as the ohmic metalization step except for the mask and the evaporated metal (Au of 2500 $\AA$).

3.7.6 Dielectric Encapsulation

Dielectrics in GaAs technology are used for protective encapsulation, for capacitors, and for crossover insulations. For the MESFETs fabricated in our laboratory encapsulation is needed only for protecting the devices from environmental contamination and mechanical damage. However, during the first MESFET processes when the fabricated devices were tried to be encapsulated by SiO_2 prior to the final metalization, they were damaged. Process begun with deposition of dielectric material all over the sample by PECVD (plasma enhanced chemical vapor deposition). Then resist AZ4210 was spun, prebaked, and exposed with the opening mask which defines windows on dielectric for electrical contact of the final metal with the device pads. After the development, the sample was postbaked and then immersed in buffered HF, which etches SiO_2 but does not attack Au. Electrical measurements after this process showed that the resistances were very high, at first the etching process was blamed for this failure. Thus, we developed an original process, that is by making use of the image reversal property of AZ5214. It behaves as a negative resist with a nice undercut profile suitable for lift-off, if baked on hot plate at $105\,^{o}C$ for 1 minute, exposed through mask, baked once more as in previous bake, flood exposed, and developed. We used lift-off technique for SiO_2 coating of the sample except for the openings, and we succeeded this process in which no etchant was used. However, devices were dead once more. As a final chance we tried to leave hard baked photoresist on the active regions of devices by using mesa mask, this method did not work either. We decided to probe the devices at first and postpone the encapsulation to a later time. Thus Al was a suitable metal for this purpose since it can be easily removed by the developer, AZ400 K. However, although MESFETs produced after this decision were very good in DC performance ($\approx 270mS/mm$ transconductances were observed for a number of 1 μm gate length devices), their ohmic contacts were observed to be insulators after Al metalization. The reason of this phenomenon is not clear yet, but as mentioned in ohmic contact section, in the literature it is noted that ohmic contacts to GaAs are not stable even at room temperature, however our processes vary between 95 and $140\,^{o}C$, the temperature

at which photoresist begins to crack. It is possible that these processes promoted the degradation mechanisms which were already active, resulting in death of the contacts. The fabricated MESFETs have totally different ohmic contact properties due to high surface donor concentration and thus comparison of them is not possible with the previously produced (and dead) MESFETs.

Chapter 4

Measurement Techniques

4.1 Low Frequency Measurements

4.1.1 Transmission Line Model-TLM

For the evaluation of the quality of ohmic contacts the *Transmission Line Model* (TLM) method offers a practical solution. The TLM structure, used for planar contact resistance measurements, is formed by a series of identical rectangular ohmic contact structures which are spaced by varying intervals as shown in figure 4.1. If a voltage is applied between any two adjacent contacts, with

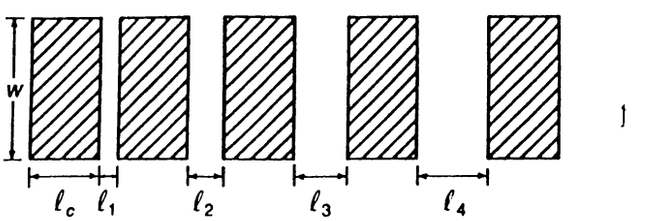

Figure 4.1: A TLM structure
With ohmic contacts of length l_c, width w, and contact spacings of l_i.

separation l_i, then the resistance is

$$R = 2R_c + r_s\frac{l_i}{w} \tag{4.1}$$

where R_c is the resistance of a single rectangular contact and r_s is the sheet resistance of the semiconductor between the contacts. Repeating this measurement between other adjacent contacts gives a plot of resistance versus contact separation. The slope of this graph gives r_s/w, and its intercept with resistance axis gives $2R_c$ and thus the normalized contact resistance $r_c = R_c/w$. However, none of these data gives enough information about the actual metal-semiconductor barrier resistance, since the portion of the contact conducting the current is not known. Two different possibilities of ohmic metal diffusion is shown in figure 4.2. If the metal diffuses all through the active channel, then the current flow out of the contact area wd is uniform, and specific contact resistivity is $\rho_c = R_c wd$. In practice, however, only a partial diffusion of some elements of

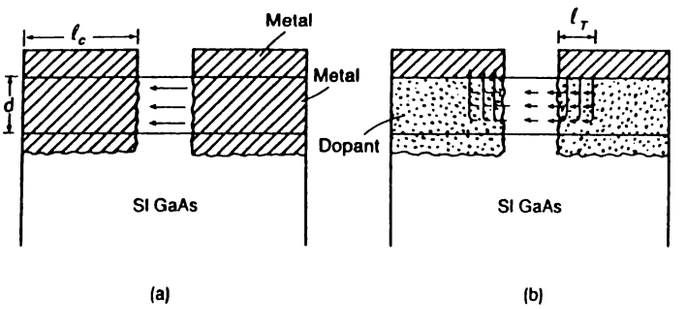

Figure 4.2: Two possible diffusion processes for ohmic metallization
(a) The metal diffuses all through the active layer; (b) one or more elements of the metal diffuse partially through the active layer. The arrows correspond to expected current flow for each case

ohmic alloy, such as Ge diffusion in the case of AuGe contact on GaAs, into the active layer is observed. Due to small conductivity of this diffused part, there will be a current crowding towards the inner edges of contacts, causing a nonuniform current flow. This problem is solved by Berger[32,33] by introducing transmission line model.

Figure 4.3 shows a transmission line model for a partially diffused ohmic contact. Current $I(0)$ entering the left contact region at $x = 0$, flows horizontally while being lost through the infinitesimal vertical resistors, $(\rho_c/w)dx$, until it vanishes. Since the channel thickness a is small, the current density can be

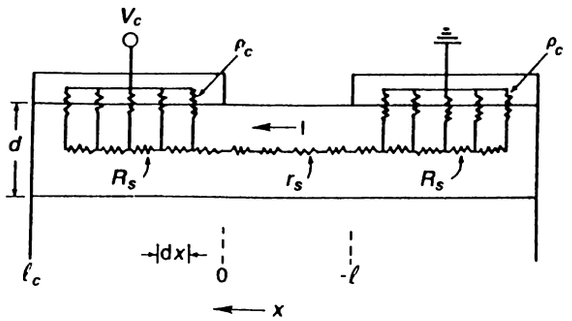

Figure 4.3: A TLM equivalent circuit for current flow in a thin-layer semiconductor device

assumed to be uniform over the cross section wa. Then for the region $0 \leq x \leq l_c$, following transmission line equations can be written

$$dV(x) = -\frac{R_s}{w} I(x) dx \tag{4.2}$$

$$dI(x) = \frac{w}{\rho_c} [V_c - V(x)] dx \tag{4.3}$$

where R_s is the sheet resistivity of the material under the contact, which in general, is different than the sheet resistance r_s of the channel between the contacts. Solution for the voltage is

$$V(x) = V_c + [V(0) - V_c] \cosh(kx) + \frac{1}{k} \frac{V(x)}{dx} \mid_{x=0} \sinh(kx), \tag{4.4}$$

where $k^2 \equiv R_s/\rho_c$. Using $I(l_c) = 0$ and $\frac{dV}{dx} \mid_{x=0} = -R_s I(0)/w$ in the above equation, the contact resistance can be found as

$$R_c = \frac{V(0) - V_c}{I} = \frac{\sqrt{R_s \rho_c}}{w} \coth(k l_c) \tag{4.5}$$

The condition $kl_c \geq 2$ corresponds to electrically long contacts, which is usually true for typical TLM structures, for which $R_c \simeq \sqrt{R_s \rho_c}/w$. Therefore,

$$\rho_c \simeq \frac{w^2 R_c^2}{R_s} \tag{4.6}$$

Transfer length, that corresponds to effective length for current conduction, is given by

$$l_T = wR_c/R_s = \sqrt{\rho_c/R_s} \tag{4.7}$$

Thus, the effective contact area is approximately wl_T.

END-RESISTANCE TECHNIQUE

The standard TLM method does not give enough information about the sheet resistance R_s of the active channel between the contacts. In that, technique to obtain ρ_c, R_s is assumed to be equal to the sheet resistance of the channel under the contacts, r_s, which generally results in large errors. Reeves and Harrison[34] proposed an additional measurement to overcome this problem. If a third contact is added to the left of $x = l_c$ in figure 4.3 which carries no current, then its potential with respect to V_c will be $V(l_c) - V_c$. Then the end resistance R_e is

$$R_e \equiv \frac{V(l_c) - V_c}{I(0)} = \frac{R_c}{\cosh(l_c\sqrt{R_s/\rho_c})}. \tag{4.8}$$

For electrically long contacts $\sqrt{R_s\rho_c}$ is obtained from measurement of R_c, and $\sqrt{R_s/\rho_c}$ is obtained from measurement of R_e/R_c, therefore both R_s and ρ_c can be determined. While designing TLM structure, care must be taken for not to have $kl_c > 10$ in which case R_e/R_c becomes less than 10^{-4} which in turn means a difficult R_e measurement.

Averages of several measurements on good TLM structures, resulted in the following values; $R_c = 64\,\Omega$, $r_s = 730\,\Omega/\square$, $R_s = 180\,\Omega/\square$, and $\rho_c = 9 \times 10^{-5}\,\Omega - cm^2$. These results mean that, the ohmic contacts obtained still needs further optimization since a very good ρ_c should be lower than the obtained value, by

an order of magnitude. Also, it must be noted that if end-resistance technique were not used, then $\rho_c = 150 \times 10^{-5}\,\Omega cm^2$ would have been obtained, which has a significant difference with the actual value.

4.1.2 DC Characterization of MESFETs

First thing to be done when characterizing, almost, any electrical device is to obtain its DC characteristics. For the estimation of the device characteristics such as output conductance g_{ds} and transconductance g_m, data relevant to drain-source current versus drain-source voltage and drain-source current versus gate-source voltage respectively will be enough. For this purpose, a modular DC source/monitor unit (HP4142A), with four medium power units and a high power unit, which is automated by the control of a computer is used. Although,the output conductance, the DC currents, and transconductance depend on the operating frequency of the MESFET, DC data are useful for first order estimates of RF performance. In figure 4.4, I_{ds} versus V_{ds} characteristics of a 1 μm gate length MESFET is presented. The output conductance, g_{ds}, can be determined from the slope of the curves. For example, at $V_{ds} = 2\,V$ and $V_{gs} = 0\,V$, output resistance is about 2 $K\Omega$. The finite resistance is mainly due to deep level impurities at the substrate-active layer interface. It must be noted that for lower gate voltages, breakdown occurs at lower drain-source voltages. This breakdown is due to increase of reverse bias voltage over gate-drain contacts. From the starting points of breakdown, breakdown voltage of gate Schottky contact can be estimated to be around 5 V. Such a low breakdown may be due to Au diffusion through Ti, resulting in a degraded Schottky contact, as well as the surface depletion.[35] Also it shows that gate-drain spacing is very small, which is due to uncontrollability of precise gate alignment with optical lithography. Drain-source current saturation starts around 1 V, which is a typical value for the 1 μm gate-length MESFET. Another thing to be noted is that, the device pinch-off is not complete, that is there is a finite drain-source voltage even for high reverse bias of the gate-source. This is most probably due to reaching of depletion region, either

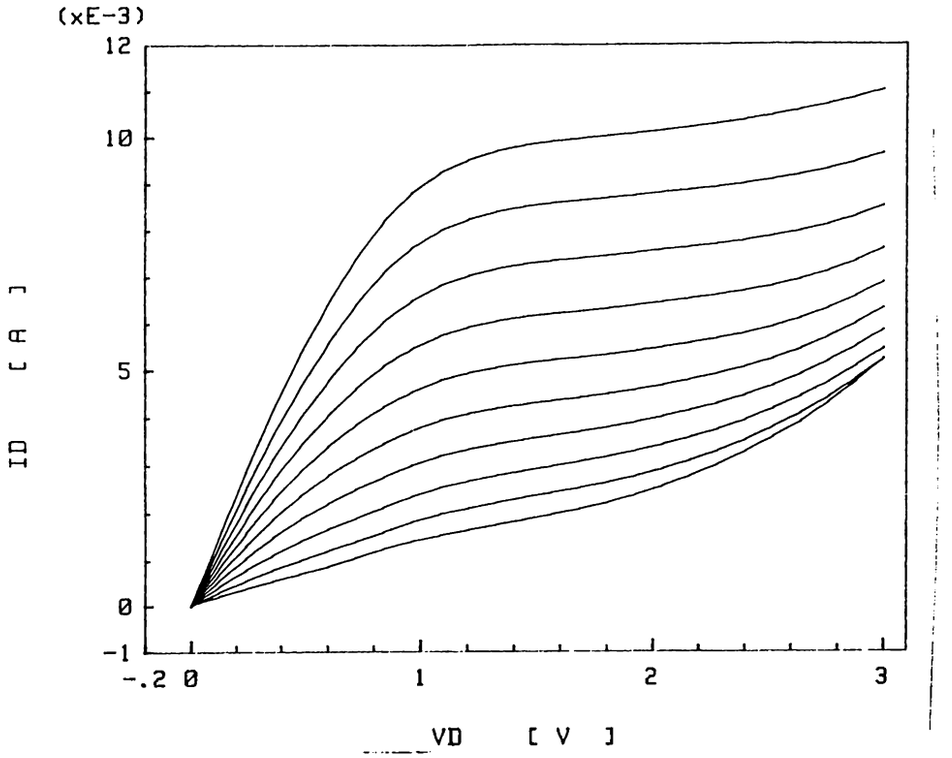

Figure 4.4: $I_{ds} - V_{ds}$ characteristics of a 1 μm gate length MESFET. V_{gs} starts from 0.3 V, and decreases to $-2.4V$ in -0.3 V steps.

surface or bulk, under the drain contact region where the carrier concentration is very high compared to the active channel.

In figure 4.5 drain-source current, I_{ds}, and extrinsic transconductance, g_m, versus gate-source voltage, V_{gs}, is presented. The square-law dependence of drain-source current on gate-source voltage is clear. The derivative of the curve, transconductance, is almost linear in V_{gs}. These both show that, the carrier concentration in the active channel of the MESFET is almost uniform. If the effect of source-resistance is included, the intrinsic transconductance will be,

$$g_{mi} = \frac{g_m}{1 - g_m R_{gs}} \tag{4.9}$$

which is higher than extrinsic transconductance, g_m. Figure 4.6 shows intrinsic and extrinsic transconductances of another 1 μm gate length MESFET with

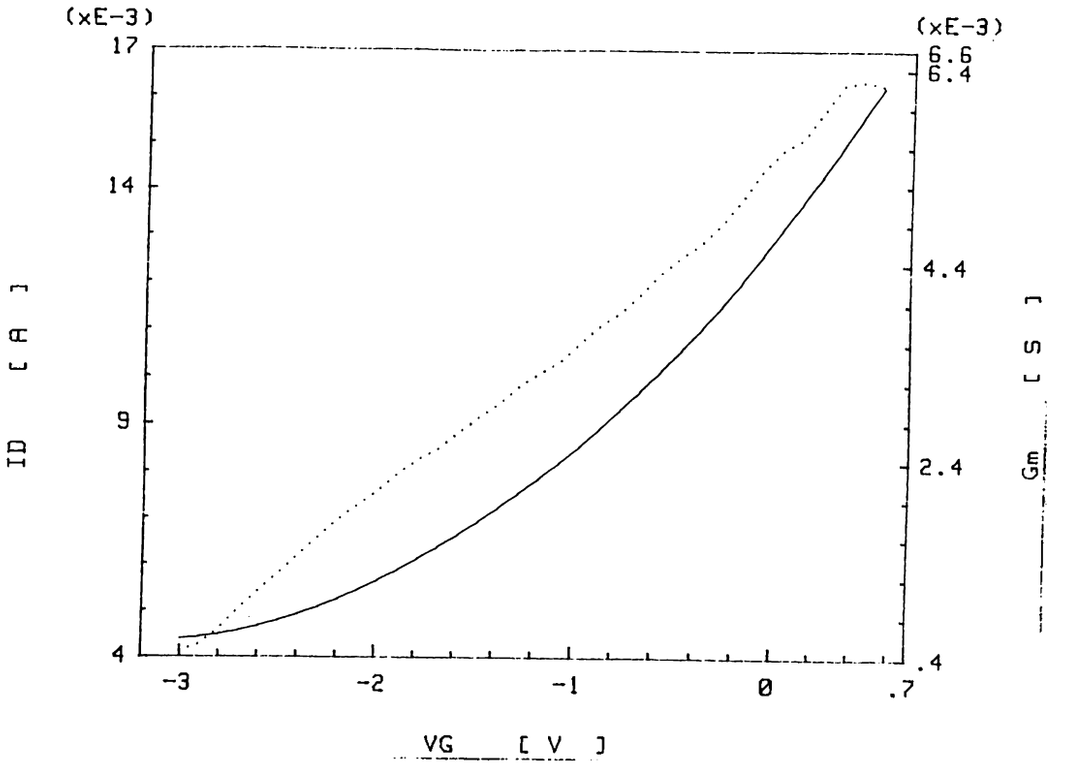

Figure 4.5: I_{ds} and g_m versus V_{gs} curves for 1 μm gate length MESFET. Solid line corresponds to I_{ds}, dotted line corresponds to g_m.

$R_{gs} = 17\,\Omega$.

Determination of Parasitic Resistances

For the determination of the parasitic resistances, the most widely used method is that proposed by Fukui,[36] which offers three DC current-voltage measurements. The principle is the making use of the ideal diode equation, which is highly accurate for low voltages. The gate current can be written as

$$I_g = I_{gs}\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \tag{4.10}$$

then the voltage drop is,

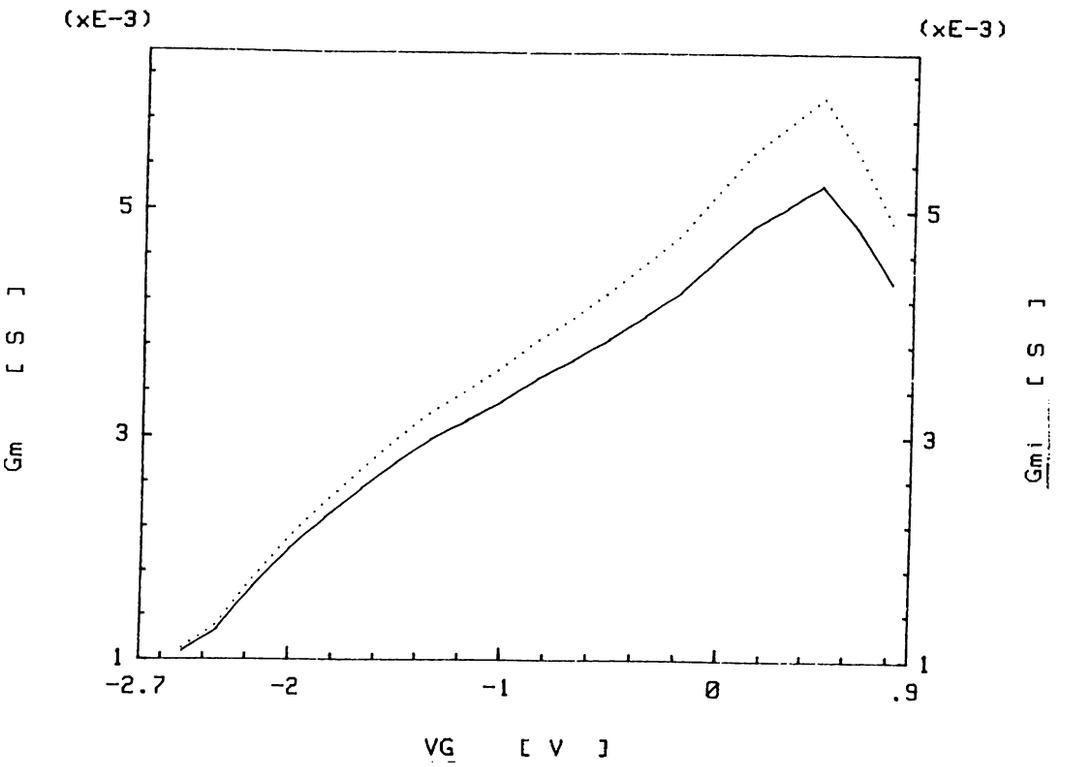

Figure 4.6: Comparison of intrinsic and extrinsic transconductances
Solid line represents extrinsic transconductance, g_m, whereas dotted line represents intrinsic transconductance, g_{mi}.

$$V = \frac{nkT}{q} \ln\left(\frac{I_g}{I_{gs}} + 1\right) \tag{4.11}$$

where I_{gs} is the reverse saturation current, and V is the voltage drop on the ideal diode. For an ideal diode, the $I_g - V_g$ relation has a constant slope on a semi-log plot. This is also valid for a good practical Schottky diode, however as the current increases the voltage drop across the parasitic resistance of the device becomes important. The potential drop across a practical gate junction, including effect of any parasitic resistance R_{ser} in series with it, is

$$V_g = V + I_g R_{ser}. \tag{4.12}$$

The series resistance can be found by using the difference between ideal and

practical diode voltages at the same current value. In mathematical form,

$$R_{ser} = \frac{V_{g0} - V_{i0}}{I_g} \tag{4.13}$$

where V_{g0} is the measured gate voltage at current I_{g0} and V_{i0} is the voltage drop across the ideal gate diode at current I_{g0} and is obtained by extrapolating the linear portion of the measured data to the desired current.

This technique is modified for determining parasitic resistances of MESFET. For this purpose three separate measurements are performed. First measurement is performed on gate-source path while drain is open. Second is performed through gate-drain while source is open. Third and last measurement is performed with both drain and source grounded together. The corresponding series parasitic resistances are denoted by R_a, R_b, and R_c, respectively. The relations between these resistances and MESFET parasitic resistances are

$$R_a = R_g + R_s \tag{4.14}$$

$$R_b = R_g + R_d \tag{4.15}$$

$$R_c = R_g + \frac{R_d R_s}{R_d + R_s}. \tag{4.16}$$

Solutions for MESFET parasitics are then

$$R_g = R_c - \sqrt{R_c^2 - R_c(R_a + R_b) + R_a R_b} \tag{4.17}$$

$$R_d = R_b - R_g \tag{4.18}$$

$$R_s = R_a - R_g \tag{4.19}$$

There may be a bias dependence of resistances obtained by means of this method. At low forward voltages, for example, the measurement accuracy is reduced because the differences between the measured and ideal currents are small. The bias dependence of gate resistance is much higher, since it is a Schottky junction. Microwave models, however, do not include this bias dependence of parasitic resistances. It is a common experience, to use 10 to 50 % higher gate resistance

in microwave models.[7] Another problem with this method is, that the data are taken for forward biased gate, while normally MESFET is operated with reverse biased gate. However, in literature the resistance values obtained by this method, especially R_s and R_d, are mentioned to be well accurate.[37] There exist other methods for extraction of parasitic resistances as well,[38,39] however, these techniques require optimization of a large amount of S-parameter data, and they also do not give more reliable results[40] due to the optimization techniques' sensitivity to the start up value choices.

In figure 4.7 a sample curve used for parasitic resistance extraction is presented. This curve corresponds to gate current while both the drain and the source are grounded, that is, R_c measurement. The y-axis position of cross

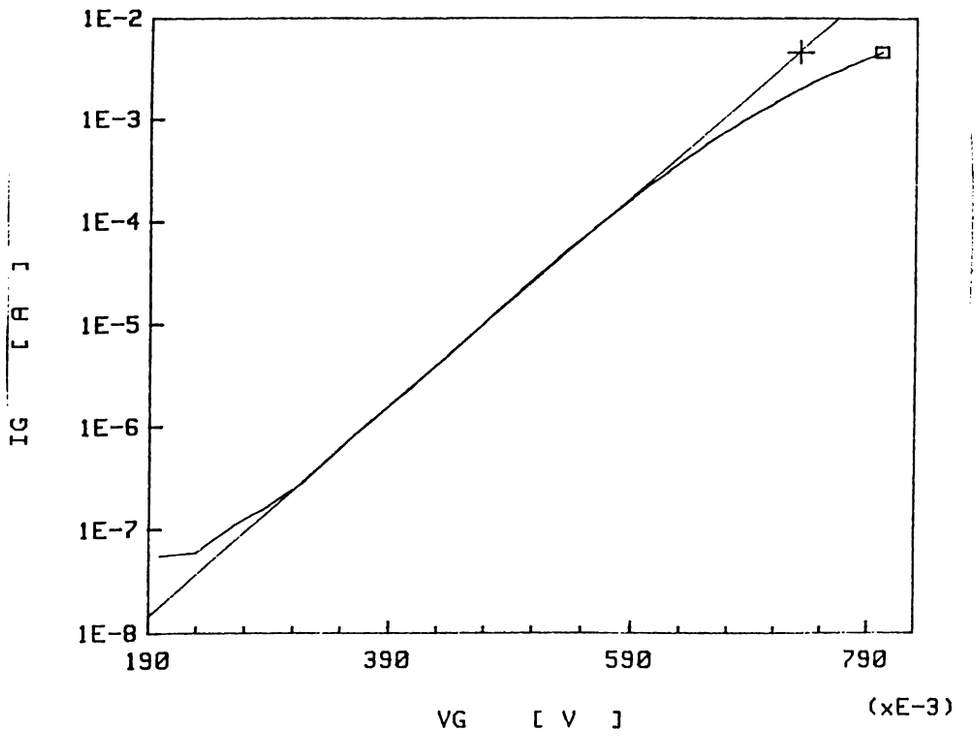

Figure 4.7: Determination of R_c
Voltage difference between cross and square is 70 mV, whereas they are located at $I_g = 4.63\,mA$, thus $R_c = 15\,\Omega$

and square is $I_g = 4.63\,mA$, and their x-axis position difference is $\Delta V_g = 70\,mV$, which gives $R_c = 15\,\Omega$. Similar determination of $R_a = 25\,\Omega$ and $R_b = 29\,\Omega$ gives parasitic resistances as $R_g = 4\,\Omega$, $R_s = 21\,\Omega$, and $R_d = 25\,\Omega$, for the same MESFET.

Determination of Some Large Signal Model Parameters

Tuyl and Liechti[41] proposed a large-signal MESFET model to be used in simulators in 1974, which was later simplified by Curtice,[16] and became a basis for most of nonlinear models in use today. Curtice model mainly consists of voltage controlled current source I_{ds}, gate-source capacitance C_{gs}, gate-drain capacitance C_{gd}, drain-source capacitance C_{ds}, and the clamping diode D_{gs}. Nonlinear terms are only I_{ds} and C_{gs}. I_{ds} is a function of the intrinsic drain-source and gate-source voltages and electron transit time τ. C_{gs} is assumed to be only a function of the intrinsic gate-source voltage. Curtice model describes drain-source current, for $V_{gs} > V_T$, as

$$I_{ds}(V_{gs}, V_{ds}) = \beta(V_{gs} - V_T)^2(1 + \lambda V_{ds})\tanh(\alpha V_{ds}) \tag{4.20}$$

where V_{gs} and V_{ds} are the intrinsic terminal voltages and β, V_T, λ, and α are the model parameters to be determined. Parameters β and V_T can be determined from simple DC measurements, however, determination of other parameters require optimization of s-parameters measured at various bias points and requires a tedious number of measurements (usually more than 20 different set of s-parameters are used). On the other hand, DC curve fits give a first order approximation for λ and α. Thus a curve fit to FATFET $I_{ds} - V_{ds}$ characteristics is performed resulting in $\lambda = 0.017$ and $\alpha = 1.444$, since these parameters are material dependent (except for scaling factors) they can be used for a first order guess for other MESFETs.

For determining V_T and β the method used is to apply a very small drain-source bias just to ensure that drain-source current is positive and λV_{ds} is almost zero. In this case,

$$I_{ds} \approx \beta(V_{gs} - V_T)^2 \tag{4.21}$$

which means that the slope of $\sqrt{I_{ds}}$ vs. V_{gs} curve gives β and its intersection with V_{gs} axis gives V_T.

In figure 4.8 $\sqrt{I_{ds}}$ versus V_{gs} curve of a FATFET is presented with a linear

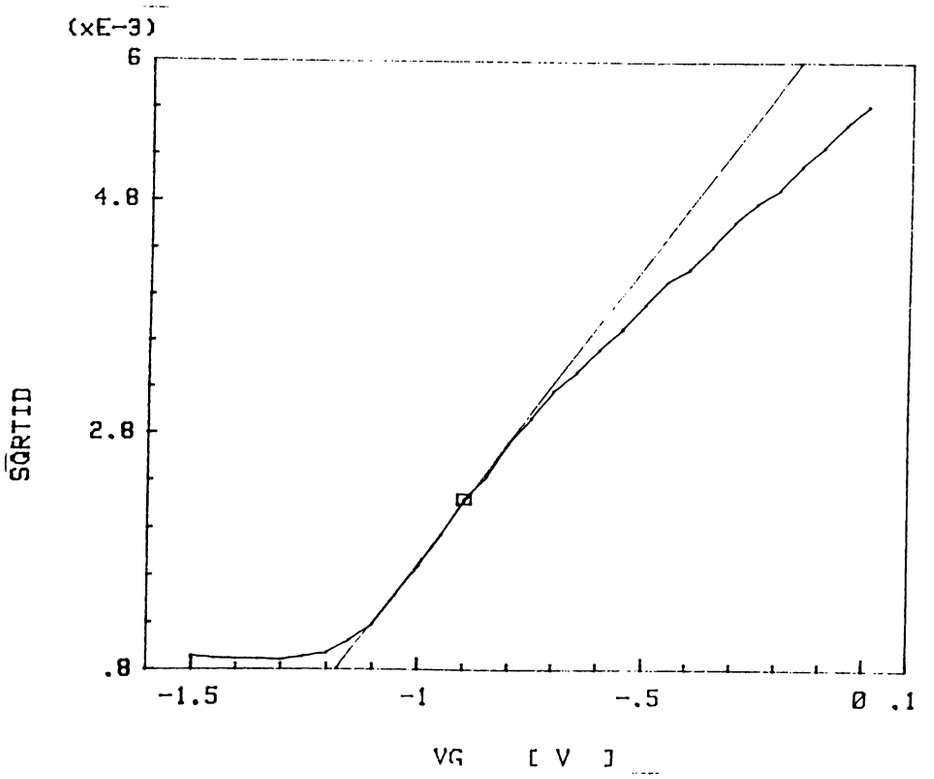

Figure 4.8: $(I_{ds})^{1/2}$ versus V_{gs} curve of FATFET
The straight line is a linear least squares fit to curve around the square, where series resistance effects seems to be minimum

regression line around the point located by a square. The threshold voltage is determined by the x-axis intersection of the linear regression line as $V_T = -1.35\,V$ and the slope gives $\beta = 5.07 \times 10^{-3}$.

Determination of Basic Parameters

The gate current, for $V_{gs} > 3kT/q$ is given by the relation

$$I_g = I_{gs} \exp\left(\frac{qV_{gs}}{nkT}\right) \tag{4.22}$$

where

$$I_{gs} = A^* T^2 \exp\left(-\frac{qV_{bi}}{kT}\right) \tag{4.23}$$

in which, A^* is the effective Richardson constant ($8.7\,A/cm^2/K^2$), n is the diode ideality factor, and V_{bi} is the Schottky barrier built-in potential. The ideality factor n can be determined from the slope of the I_g vs. V_{gs} curve plotted in logarithmic scale for forward gate biases. I_{gs} is found by extrapolating the linear part of the curve, to I_g axis.

In figure 4.9 I_g versus V_{gs} curve is presented in semi-log scale. The slope of the linear fit line is 15 which gives $n = 1.11$. The intersection with I_g axis is at $I_{gs} = 47\,pA$.

Once these parameters are obtained, the basic device parameters V_{bi}, N_d, N_d^+, and a can be determined as explained below.

The built-in potential can be determined from the relation

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{A^* T^2 LZ}{I_{gs}}\right) \tag{4.24}$$

where L and Z are the gate length and width respectively. In fact, since depletion region under the gate metal is wider than the Schottky metal forming it, effective gate length can not be determined geometrically. To overcome this problem, FATFET is a suitable structure, which has a large gate length. The FATFET structure produced in our laboratory has 50 μm gate length, which is very large compared to possible surface depletion width (around 0.5 μm at most). Thus using the above formula with $L = 50\,\mu m$ and $Z = 100\,\mu m$, at room temperature $V_{bi} = 0.72\,V$.

The ionized donor concentration N_d^+ can be determined by[36]

$$N_d^+ = \frac{1}{V_T + V_{bi}} \left(\frac{12 I_{dss}\,|_{V_{gs}=0}}{Z}\right)^2 \times 10^{16}\ cm^{-3} \tag{4.25}$$

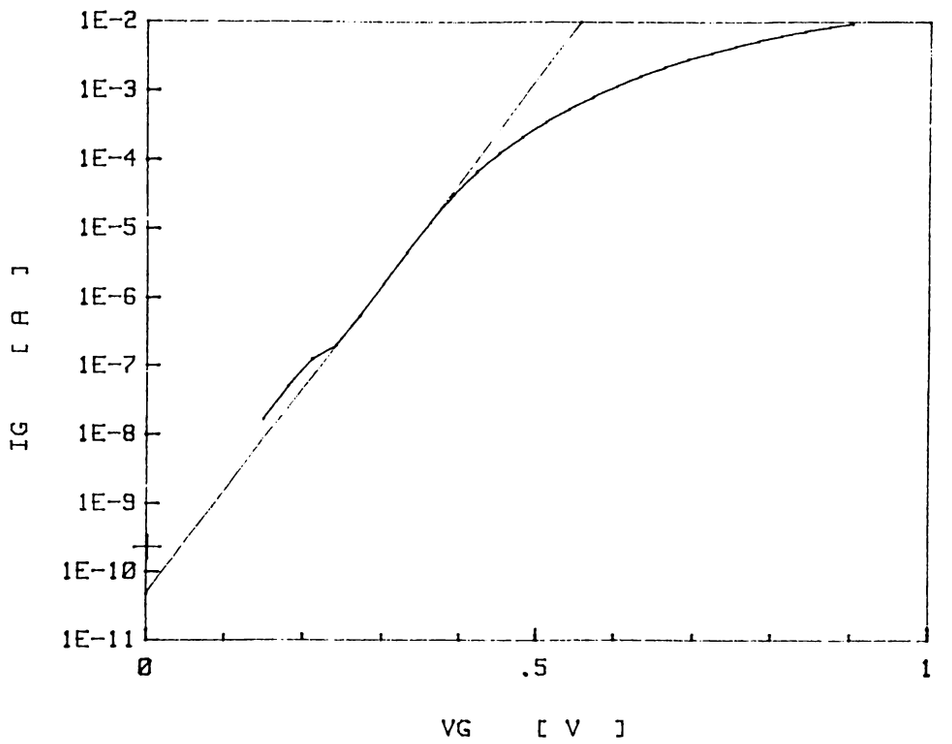

Figure 4.9: Semi-log plot of I_g versus V_{gs}
Slope of straight line is 15, and its intersection with I_g axis is at $47\,pA$.

Substitution of relevant data ($I_{dss}\ |_{V_{gs}=0}= 11\,mA$, $Z = 100\,\mu m$), gives $N_d^+ = 0.9 \times 10^{16} cm^{-3}$. The ionized donor concentration (which is very close to the donor concentration, at room temperatures) is given by the equation

$$N_d = N_d^+ \times \exp\left(-q\frac{V_{bi} - \Phi_F}{kT}\right) \tag{4.26}$$

where $\Phi_F = 0.706\,V$ is the Fermi potential for intrinsic GaAs at room temperature. Substitution of V_{bi} results in $N_d = 1.5 \times 10^{16} cm^{-3}$. By using the depletion approximation, the effective active channel thickness, a, can be found from the relation

$$a = \sqrt{\frac{2\epsilon_o\epsilon_s(\mid V_T \mid + V_{bi})}{qN_d}} \tag{4.27}$$

where ϵ_o is the dielectric permeability of vacuum ($8.85 \times 10^{-14} F/cm$) and ϵ_s is the dielectric constant of GaAs (12.5). The active channel thickness for the sample is found to be $0.4\,\mu m$.

For the determination of low field electron mobility, μ_o, the open channel resistance, R_o, given by

$$R_o = \frac{L}{q\mu_o N_d a Z} \tag{4.28}$$

can be used. For the determination of R_o the depletion approximation is used. According to this approximation depletion depth is proportional to $\sqrt{V_{bi} - V_{gs}}$. Thus, for low drain voltage in the non-saturation region of the MESFET, drain current is

$$I_{ds} \approx \frac{1}{R_o} X \cdot V_{ds} \tag{4.29}$$

where

$$X \equiv \left(1 - \sqrt{\frac{V_{bi} - V_{gs}}{V_{bi} - V_T}}\right)^{-1} \tag{4.30}$$

Then,

$$R_o = \frac{V_{ds}}{I_{ds} X} \tag{4.31}$$

which enables the determination of R_o from the slope of the Ro vs. X curve, where $Ro \equiv V_{ds}/I_{ds}$. Once R_o is determined low field mobility can be calculated by using equation 4.28.

In figure 4.10 Ro versus X curve is presented. The slope of this curve at low values of X (that is at low reverse gate bias) gives $R_o = 890$ which yields $\mu = 4930\, cm^2/V \cdot sec$.

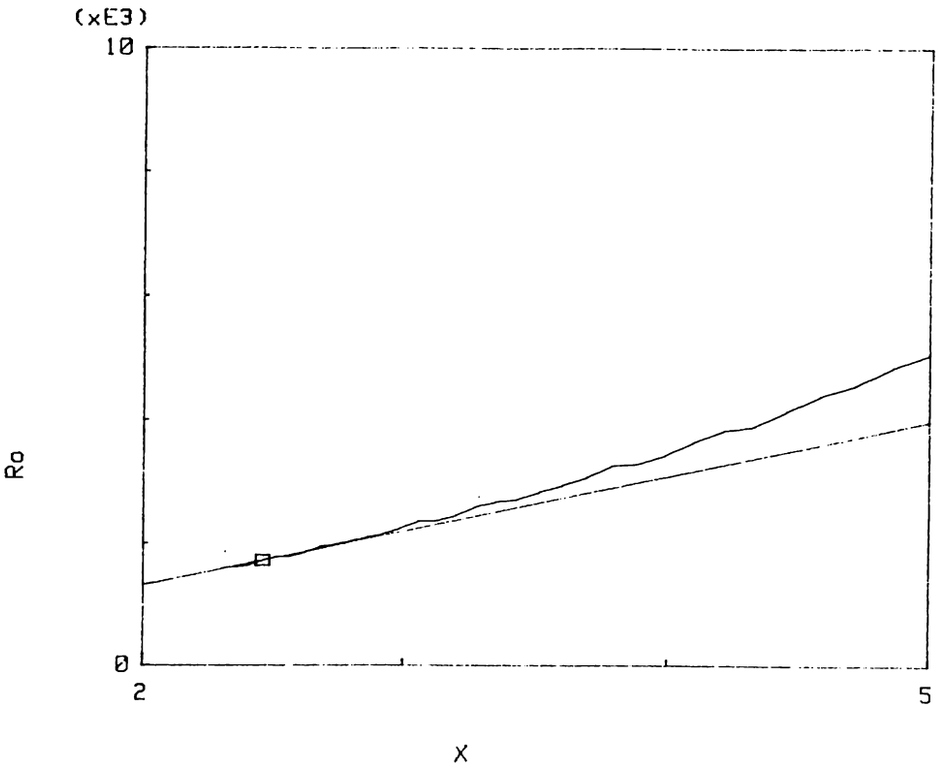

Figure 4.10: *Ro* versus X graph
Slope of the regression line is 820 Ω

4.2 High Frequency Characterization

4.2.1 RF Characterization of MESFETs

In order to be able to use the fabricated MESFET in circuitry, one needs its small-signal and/or large-signal equivalent models' parameters. Usually for small-signal models, the output conductance $g_{ds}(V_{ds}, V_{gs})$, transconductance $g_m(V_{ds}, V_{gs})$, gate-drain capacitance $C_{gd}(V_{ds}, V_{gs})$, and gate-source capacitance $C_{gd}(V_{ds}, V_{gs})$ are assumed to be bias dependent, while drain-source capacitance C_{ds}, charging resistance R_i, and transconductance delay τ are assumed to be almost bias independent and are extracted at $I_{dss}/2$. At higher frequencies parasitic inductances are also included.

Extraction of Intrinsic Elements

The parameter extraction of a MESFET starts with microwave S-parameter measurements for different biases of device, in the frequency range of interest. Such a technique was first described by Minasian,[42] and since then variations of this method[43,44] is commonly used to extract parameters. In this work the small-signal model in figure 4.11 is used for parameter extraction which was offered by Minasian, and is the most widely used model since its parameters can be uniquely determined without any use of optimization techniques the way commercially available softwares such as Super Compact, HP MDS, LIBRA, or Touchstone extract parameters. At lower microwave frequencies (5-10 GHz depending on the geometry) parasitic inductances are neglected as a common experience.

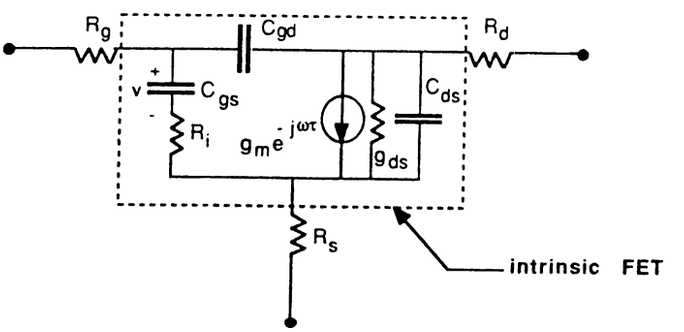

Figure 4.11: MESFET small-signal model without parasitic inductances

The parasitic resistance values are determined by the Fukui method. Measured S-parameters are converted to z-parameters by use of the following equations,

$$Z'_{11meas} = \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{\Delta} \tag{4.32}$$

$$Z'_{12meas} = \frac{2S_{12}}{\Delta} \tag{4.33}$$

$$Z'_{21meas} = \frac{2S_{21}}{\Delta} \tag{4.34}$$

$$Z'_{22meas} = \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{\Delta} \tag{4.35}$$

where prime stands for normalized z-parameters (to $Z_0 = 50\Omega$, characteristic impedance of the transmission line to MESFET) and

$$\Delta = (1 - S_{11})(1 - S_{22}) - S_{12}S_{21} \tag{4.36}$$

Intrinsic z-parameters can be written, in terms of de-normalized intrinsic z-parameters, as follows

$$z_{11meas} = Z_{11meas} - (R_g + R_s) \tag{4.37}$$
$$z_{12meas} = Z_{12meas} - R_s \tag{4.38}$$
$$z_{21meas} = Z_{21meas} - R_s \tag{4.39}$$
$$z_{22meas} = Z_{22meas} - (R_d + R_s) \tag{4.40}$$

which are converted to y-parameters by means of,

$$y_{11meas} = \frac{z_{22meas}}{\mid z \mid Z_0} \tag{4.41}$$
$$y_{12meas} = \frac{z_{12meas}}{\mid z \mid Z_0} \tag{4.42}$$
$$y_{21meas} = \frac{z_{21meas}}{\mid z \mid Z_0} \tag{4.43}$$
$$y_{22meas} = \frac{z_{11meas}}{\mid z \mid Z_0} \tag{4.44}$$

where $\mid z \mid = z_{11meas}z_{22meas} - z_{12meas}z_{21meas}$. The y-parameters of the intrinsic MESFET can be expressed as,[42]

$$y_{11} = \frac{R_i C_{gs}^2 \omega^2}{D} + i\omega(\frac{C_{gs}}{D} + C_{gd}) \tag{4.45}$$
$$y_{12} = -i\omega C_{gd} \tag{4.46}$$
$$y_{21} = \frac{g_m \exp(-i\omega\tau)}{1 + i\omega R_i C_{gs}} - i\omega C_{gd} \tag{4.47}$$
$$y_{22} = g_{ds} + i\omega(C_{ds} + C_{gd}) \tag{4.48}$$

where $D = 1 + \omega^2 C_{gs}^2 R_i^2$. These four equations are used to extract model parameters.

Extraction of capacitances Determination of gate-drain capacitance is straightforward. Optimum value is found by a least-squares fit for the slope of $Im[y_{12meas}]$ versus ω curve, *i.e.*

$$C_{gd} = -m_{y_{12}} \tag{4.49}$$

where $m_{y_{ij}}$ is the slope of the corresponding regression line. Similarly, $C_{ds} + C_{gd}$ can be extracted from y_{22meas} data, yielding drain-source capacitance as,

$$C_{ds} = m_{y_{22}} - C_{gd} \tag{4.50}$$

For the extraction of gate-source capacitance, low frequency assumption is used, that is $(\omega C_{gs} R_i^2) \ll 1$. Then $Im[y_{11}] \approx i\omega(C_{gs} + C_{gd})$, and

$$C_{gs} = m_{y_{11}} - C_{gd} \tag{4.51}$$

where $m_{y_{11}}$ is the slope of the regression line to $Im[y_{11meas}]$ data at low frequencies. Usually, imaginary parts of y_{11meas}, y_{22meas}, and y_{12meas} are linear for low frequencies, which simplify the capacitance expressions as,

$$C_{gd} = -\frac{Im[y_{12meas}]}{\omega} \tag{4.52}$$

$$C_{ds} = \frac{Im[y_{22meas}]}{\omega} - C_{gd} \tag{4.53}$$

$$C_{gs} = \frac{Im[y_{11meas}]}{\omega} - C_{gd} \tag{4.54}$$

which mean that capacitances can be extracted at single or over a small number of frequencies.

Extraction of g_{ds} and g_m Output conductance y_{22} is, at low frequencies

$$g_{ds} = Re[y_{22meas}]. \tag{4.55}$$

At higher frequencies $Re[y_{22meas}]$ falls of, but the low frequency data results in a reliable output conductance over a large frequency range.[7] Flatness of low

frequency data also enables the use of a single or a few averaged data point for extraction.

Transconductance can be written as

$$g_m \exp(-i\omega\tau) = g_{mr} + j g_{mi} \tag{4.56}$$

where

$$g_{mr} = Re[y_{21}] - Im[y_{21}]R_i C_{gs}\omega - \omega^2 C_{gd} C_{gs} R_i \tag{4.57}$$

and

$$g_{mi} = Re[y_{21}]R_i C_{gs}\omega + Im[y_{21}] + \omega C_{gd}. \tag{4.58}$$

However, for a typical MESFET usually

$$g_m \approx Re[y_{21}] \tag{4.59}$$

which is valid up to around 2 GHz, thus g_m can be computed from a single or a few averaged y_{21} data.

Extraction of τ and R_i It is clear that for extraction of R_i one should use $Re[y_{11}]$, since the use of $Im[y_{21}]$ requires knowledge of τ. However, determination of R_i is a harder job due to the noisy data especially at low frequencies. Thus it is better to use higher frequency data for extraction, assuming the small-signal model is still valid. Solution of the quadratic equation for R_i gives

$$R_i = \frac{1 - \sqrt{1 - \frac{4(Re[y_{11}])^2}{\omega^2 C_{gs}^2}}}{2Re[y_{11}]} \tag{4.60}$$

Another method offered in the literature is the optimization of R_i to fit S_{11} data,[45] however, it is noted that this method does not promise much better performance since R_i's effect to S_{11} is second order at worst. Another criticism comes from the fact that R_i does not provide a unique model performance and its physical meaning is still not clear. The primary function of R_i is to contribute to the real part of the device model input impedance and the time required for the channel

current to respond to gate voltage variation. However, both of these effects are also included by means of R_g and τ, respectively.

The parameter τ is significant at higher frequencies, however it can be determined at lower frequencies easily, with the approximations that $\omega\tau \ll 1$ and $D = 1$, as

$$\tau = \frac{Im[y_{21}]/\omega - g_m R_i C_{gs} - C_{gd}}{g_m} \tag{4.61}$$

However, if very high frequency limit is considered it is advisable to use

$$\tau = -\frac{1}{\omega}\tan^{-1}\left(\frac{g_{mi}}{g_{mr}}\right) \tag{4.62}$$

which is valid for all frequencies at which the model can be used.

Summary of Equations Used for Parameter Extraction The parameter extraction is performed in two groups, one at lower frequencies, the other at higher. At lower frequencies $(\omega C_{gs} R_i)^2 \ll 1$ approximation gives,

$$C_{gd} = -Im[y_{12}]/\omega \tag{4.63}$$

$$C_{ds} = Im[y_{22}]/\omega - C_{gd} \tag{4.64}$$

$$C_{gs} = Im[y_{11}]/\omega - C_{gd} \tag{4.65}$$

$$g_{ds} = Re[y_{22}] \tag{4.66}$$

$$g_m = Re[y_{21}] \tag{4.67}$$

and at higher frequencies,

$$R_i = \frac{1 - \sqrt{1 - \frac{4(Re[y_{11}])^2}{\omega^2 C_{gs}^2}}}{2Re[y_{11}]} \tag{4.68}$$

$$\tau = -\frac{1}{\omega}\tan^{-1}\left(\frac{g_{mi}}{g_{mr}}\right) \tag{4.69}$$

where

$$g_{mr} = Re[y_{21}] - Im[y_{21}]R_i C_{gs}\omega - \omega^2 C_{gd} C_{gs} R_i \tag{4.70}$$

$$g_{mi} = Re[y_{21}]R_i C_{gs}\omega + Im[y_{21}] + \omega C_{gd} \tag{4.71}$$

Extraction of Parasitic Inductances

A method of extraction of parasitic inductances is the cold chip technique, proposed by Diamond and Laviron,[46] which makes use of S-parameter data at zero drain-source bias. However, this technique is mainly useful for packaged devices, since the inductances are dependent on substrate and therefore on biasing conditions, for example gate strip inductance given by Ladbrooke[20] as

$$L_g = \frac{\mu_0 W Z}{m^2 L} \tag{4.72}$$

where m is the number of gate fingers and μ_0 is the permeability of free space. On the other hand, the method described below is valid for both packaged and non-packaged devices. The extrinsic device z-parameters can be written as

$$Z_{11} = z_{11} + (R_g + R_s) + i\omega(L_g + L_s) \tag{4.73}$$

$$Z_{12} = z_{12} + R_s + i\omega L_s \tag{4.74}$$

$$Z_{21} = z_{21} + R_s + i\omega L_s \tag{4.75}$$

$$Z_{22} = z_{22} + (R_d + R_s) + i\omega(L_d + L_s) \tag{4.76}$$

The extrinsic inductance extraction method is based on the fact that the effects of the series inductances can be neglected at lower frequencies, and the extracted intrinsic elements at higher frequencies, namely τ and R_i, are valid.[7] Therefore, the inductances are extracted by the following formulae,

$$Im[Z_{11meas}] - Im[z_{11model}] = \Delta Z_{11} = \omega(L_g + L_s) \tag{4.77}$$

$$Im[Z_{12meas}] - Im[z_{12model}] = \Delta Z_{12} = \omega L_s \tag{4.78}$$

$$Im[Z_{21meas}] - Im[z_{21model}] = \Delta Z_{21} = \omega L_s \tag{4.79}$$

$$Im[Z_{22meas}] - Im[z_{22model}] = \Delta Z_{22} = \omega(L_d + L_s) \tag{4.80}$$

from which inductance values can be extracted.

4.2.2 RF Measurements

For s-parameter measurements, we have used two Tektronix TMP 9610 microwave probes, connected to HP 8510C automatic network analyzer (ANA). The calibration of network analyzer was done as follows. For open correction, the probes were held close to each other in air, to determine cross talk of probes when they are probing MESFETs. Short correction was performed by simply probing large metal pads. Match correction was the most problematic one, since we did not have any 50 Ω matched load suitable for probing. This problem was solved by using a matched through line, and assuming the paths to ANA ports acts as a match load. After, performing these corrections, the errors for short and open were observed to be very small (better than -70 dB cross coupling, better than 0.1 dB reflection mismatches), thus in our opinion, although this method is non-standard, it resulted in satisfactory calibration of ANA.

V_{ds}	V_{gs}	C_{gd} (fF)	C_{gs} (fF)	C_{ds} (fF)	$R_{ds}\,(K\Omega)$	$R_i\,(\Omega)$	$g_m\,(mS)$	$\tau\,(10^{-11}\,sec)$
2 V	0.0 V	27	813	640	1.48	22.5	4.3	7.6
2 V	-0.5 V	26	780	645	1.66	9.2	3.8	6.4
2 V	-1.0 V	31	757	633	1.57	15.6	2.8	7.1
1 V	0.0 V	44	778	625	0.31	8.8	3.4	5.8
1 V	-0.5 V	40	757	575	0.39	8.6	3.3	6.1
1 V	-1.0 V	36	750	595	0.54	8.6	3.0	6.2

After calibration, RF data, for various bias conditions, were taken and samples of s-parameters (6 to 12) were taken for manipulations resulting in the intrinsic small-signal model parameters given in table above. Extraction of parasitic resistances was explained in the related section (for the specific MESFET mentioned here, $R_g = 4\,\Omega$, $R_s = 21\,\Omega$, and $R_d = 25\,\Omega$). Calculations done for extraction of parasitic inductances has shown that, these elements' values are strongly dependent on the frequency range of data taken, therefore an average of these values over several frequency ranges are taken to give $L_s \approx 290\,pH$, $L_g \approx 480\,pH$, and $L_d \approx 400\,pH$. After obtaining the small-signal model elements, the corresponding s-parameters, S_{ij}^{mod}, of model were calculated for corresponding

frequencies. The average error terms defined as,

$$E_{ij} = \frac{1}{n} \sum_{k=1}^{n} \frac{\mid S_{ij}^{k} - S_{ij}^{mod,k} \mid}{\mid S_{ij}^{k} \mid} \tag{4.81}$$

were calculated to be $E_{11} = 2.5\%$, $E_{12} = 19.2\%$, $E_{21} = 9.4\%$, and $E_{22} = 2.8\%$. The cut-off frequency,

$$f_T = \frac{g_m}{2\pi C_{gs}} \tag{4.82}$$

is seen to vary between 0.65 GHz and 0.85 GHz. This frequency limits are very low for an ordinary MESFET. The reasons for such low operation frequencies can be partially explained by the low transconductance, which is mainly due to moderate doping level of the active channel. Another reason may be the deep recess sidewalls, which increase the geometrical capacitance effects. The distance between high conductive mesa walls and gate metal may be as low as 0.1 μm. This explanation is also consistent with the explanation of low break-down voltages of the devices.

Chapter 5

Conclusion

The importance of GaAs MESFETs is due to their widespread use in microwave electronics, which is the backbone of today's satellite communication, military electronics, and avionics. Since their first appearance in 1966, they had been the subject of an enormous work. It took more than ten years, to solve their optimization and reliability problems. However, after their problems are solved and they begun come out to market from the laboratories, they became the most preferred device of high-frequency electronics.

In this study, we succeeded the fabrication of GaAs MESFETs. These MESFETs were designed, aiming for small-signal operations. The most critical part of the fabrication was the ohmic-contact formation. The epi-structure of the wafer, used for the first successful batch of MESFETs produced, had an active layer of dopant concentration $2 \times 10^{17}\, cm^{-3}$. We succeeded, seemingly, to produce very good ohmic contacts (with $\rho_c \sim 10^{-6}\, \Omega \cdot cm^2$), which were made directly on the $2 \times 10^{17}\, cm^{-3}$ doped active channel. The DC data taken were very good, one of the most important parameters, namely transconductance, was observed to exceed $270\, mS/mm$ for $1\, \mu m$ gate-length MESFETs, with a maximum drain to source saturation current higher than $0.8\, A/mm$. These values can be well compared to the state-of-the-art MESFETs produced in the fore coming laboratories in the world. However, during dielectric encapsulation processes we observed that the devices were destroyed. At first we thought that,

encapsulation process was responsible for the killing of devices. Therefore, we postponed this process to a later time and produced a new batch of devices up to the final level metallization. However, devices were killed once again, either during final metallization process (which was not performed before, since normally it follows dielectric encapsulation) or after the completion of the devices.

Then, we started the fabrication once more with a wafer which had a completely different epi-structure. This structure had a $2 \times 10^{18} cm^{-3}$ doped cap layer and a $5 \times 10^{16} cm^{-3}$ doped active layer. The highly doped cap layer brought the advantage of easier ohmic-contact formation, however it added an extra etch process for making good Schottky contacts to the active channel. This extra etching process brought out the problems of process uniformity and repeatability. Even the geometries, a few microns apart, came out to be etched in different natures. For example, ohmic contacts of TLM patterns, which are only a few microns apart, had shown very non uniform ohmic contact properties. The extra etch step included, also resulted in a degradation in the over-all ohmic-contact quality. Since the etching was, and hence the device performances were, non-uniform, neither comparison of devices with each other nor a statistical data base formation was possible. Therefore, data relevant to only some of the devices were taken and manipulated. These manipulations are not meant to be complete, but they form the basis of a complete process and material test and development procedure.

The results obtained are consistent with basic MESFET theory. The DC characteristics are good, even though parasitic resistances are little high. One of the important drawbacks of the MESFETs is their low breakdown voltages. However, as far as small-signal operation is concerned, this low breakdown is not important.

The material data, extracted from device characteristics, are also realistic and consistent with theory and the data given in the literature. However, due to non-uniform characteristics some of the devices resulted in inconsistent results, thus they were disregarded. The extraction of small-signal equivalent circuit parameters were also satisfactory.

Although the MESFET fabrication proved to be successful, there still remains problems to be solved. The etching process must be optimized to obtain higher uniformity and yield. Ohmic-contact process still needs further optimization and reliability tests. The protective dielectric encapsulation must also be performed. Since there is no barrier layer to prevent diffusion of the Au overlay through Ti, Schottky contact degradation in time is expected. Solution of this problem is as simple as deposition of a barrier metal, such as Pt, in between Au and Ti, which will be performed later when the e-beam evaporator is in operation.

Further work is planned on the fabrication of some simple MMIC circuitry which are mainly based on the same types of MESFETs fabricated. Also, with the experience obtained by MESFET fabrication, it is a rather simpler task to switch to HEMT fabrication. HEMTs are very similar to MESFETs in their characteristics, with superior performance. Thus, main part of their characterization and parameter extraction needs either a slight or no modification to those of MESFETs.

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