Analysis of HfO_2 and ZrO_2 as High-K Dielectric for CMOS Nano Devices

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***Abstract*— An analysis has been made on high-K dielectrics (HfO_2 and ZrO_2) for the CMOS process up to 14 nm FAB technology node. The aim is to study the reduction in gate leakage current for Nano-scale devices. High-K Dielectric having $K \geq 20$ is beneficial for CMOS Nano-devices, reducing the gate leakage current when $EOT \leq 0.5$ nm. MOS structure with high-K, i.e., HfO_2 and ZrO_2, has been simulated in SILVACO T-CAD to consider as gate stack: metal/oxide/p-Si for the different FAB nodes; 45, 32, 22 & 14 nm. SiO_2 is considered a reference to optimize the MOS structure with high-K dielectric. As a result, 7-8 times the higher physical gate oxide layer is achieved compared to SiO_2, which has a significant impact on minimizing the gate leakage current.**

Keywords—CMOS, high-K dielectric, E.O.T, ITRS, FAB node, TCAD

I. INTRODUCTION

Silicon (Si) is still a backbone of the CMOS industry, and its scaling has been followed Moore's law successfully for the last three decades [1]. The FAB technology node reaches 14 nm or below, almost a monoatomic layer [2]. Therefore, miniaturization of the gate oxide thickness is crucial to bear the device scaling to control the gate capacitance and threshold voltage, etc. [3]. Though the scaling of CMOS devices reaches the structural limitation, further scaling is becoming a significant challenge due to quantum effects, etc. Therefore, there is a need to address the gate direct tunneling, sub-threshold leakage current, GIDL degradation, DIBL, and ultra-shallow S/D junction depth issues adequately [4].

Below the 65 nm FAB node, the space charge regions near the source and drain of MOSFET are overlapped, known as short channel effects [5]. Therefore, the leakage current increases, which affects the device's performance and reliability. To continue the further journey predicted by Moore's law, the dielectric constant (K) > 3.9 is preferred as high-K. High-K material is used first for the 45 nm FAB technology node. Equivalent Oxide Thickness (EOT) is a reference to measure the thickness of High-K equivalent to SiO_2. Low EOT provides a reasonable physical layer thickness w.r.t technology node [6].

In this work, we are focused on high-K material to address CMOS process issues having $EOT \leq 0.5$ nm for Nano-device fabrication and study MOS structure with high-K to analyze the capacitive behavior during accumulation and inversion phenomena. The purpose is to adjust the optimum physical layer of high-K. Section-II describes a brief detail about High-K dielectric while Section-III elucidates MOS structure for different FAB nodes. The comparative analysis of high-K, i.e., HfO_2 and ZrO_2, will be discussed in section-IV. Finally, the conclusion has been made in section-V.

II. ABOUT HIGH-K DIELECTRICS

The thickness of gate oxide has a vital role in controlling the bias; minimum thickness will increase the electric field between the gate and channel of the MOSFET. Therefore, the reduction in the gate oxide layer has an impact on the channel potential influenced by the gate bias compared to drain [7]. Low EOT with a higher electric field can handle the leakage current. $EOT \leq 0.5$ nm with K > 3.9 is preferred to reduce the several orders gate leakage current compared to SiO_2.

By lowering the FAB technology node, *IC* speed will be increased ~ 30%. Fig. 1 represents the predicted trends of EOT for past, present, and future. The 'Planner' trend starts from 2008 when the high-K is used *for the* first time for the 45 nm FAB node. The upper and lower limit of this trend shows that the EOT value varies from 1 to 0.5 nm, not exactly followed in the semiconductor industry. In 2013, a 22 nm FAB node was introduced known as "UTB FD," where EOT predicted ~ 0.7 to 0.4 nm for 22 nm to ≤ 14 nm FAB node, respectively. At last, MG trend describes EOT future further by ITRS-2015 plan. For nano CMOS devices, it predicts EOT from 0.8 to 0.4 nm for FAB technology nodes of 14 nm to 7 nm, respectively [8].

High-K attributes the following parameters for the CMOS process; high permittivity, high barrier height, reduced leakage current, low power consumption, low direct tunneling, stability, and compatibility with gate metal and FAB process. Several high-K dielectrics can be considered as a potential candidate for current and future CMOS devices; Fig. 2 shows a high-K dielectric w.r.t band gap (E_g). The large fringing field may affect the source and drain terminals of MOSFET; high-k allows the

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fast switching of the transistors as required for the processor and storage device applications. Therefore, K ≥ 20 has a reasonable thickness to provide a sufficient barrier against the gate leakage current [9].

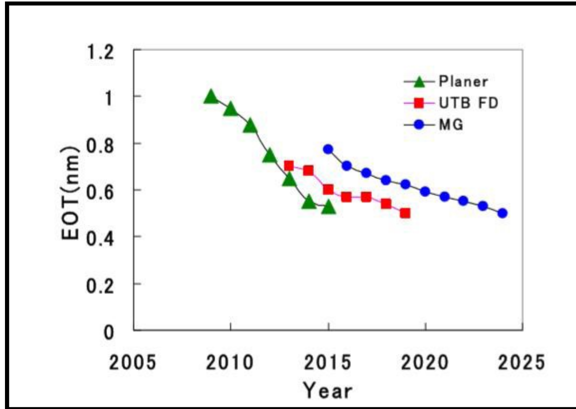

Fig. 1. Predicted EOT w.r.t ITRS roadmap [8]

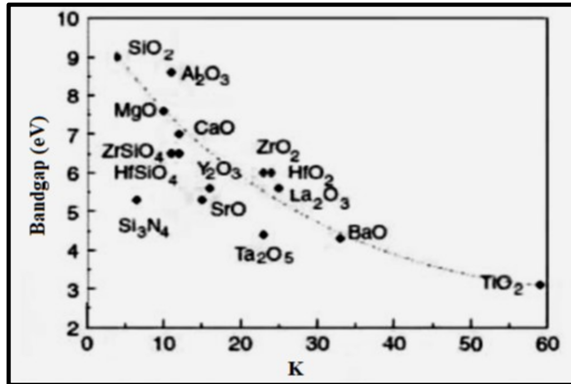

Fig. 2. Dielectric constant (K) vs band gap (E_g) [9]

Different high-K dielectric materials are analyzed w.r.t EOT and capacitance (C) as shown in Fig. 3. Most high-K materials have a similar response except Si_3N_4, MgO, and Y_2O_3. The relation between physical layer thickness w.r.t EOT is shown in Fig. 4. From the result, TiO_2 shows the highest physical thickness, which is almost three times higher than the others, but E_g is < 3eV. Therefore, it is not feasible for fabrication due to die size constraints and future prediction of chips. Similarly, MgO and Y_2O_3 materials have limitations due to K < 20, limiting the EOT constraints [9]. ZrO_2 and HfO_2 have K ~ 22 and 25, respectively, and can easily grow on Si substrate. The properties of HfO_2 and ZrO_2 are almost the same, including their mismatch with Si <100> substrate as tabulated in Table I.

In this work, we focused on HfO_2 and ZrO_2 to investigate further according to FAB technology node from 45 to 14 nm. We compared the physical layer thickness w.r.t. EOT and effective gate length of FAB nodes as tabulated in Table II. From the comparison, HfO_2 and ZrO_2 provide better isolation (~ 8-10 times higher than the SiO_2 physical layer) to reduce the gate leakage current and increase the device's reliability. Regardless of the FAB process advantage, we evaluated that both dielectrics are suitable to act as gate oxide thickness for 14 nm FAB nodes. Even ZrO_2 may perform better due to the least dielectric, low density, and higher bandgap compared to HfO_2 [10].

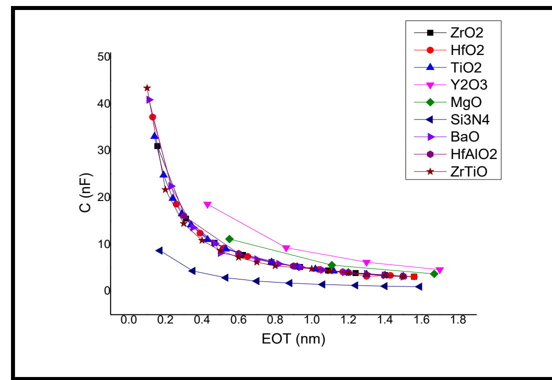

Fig. 3. Capacitance vs EOT of different high-K

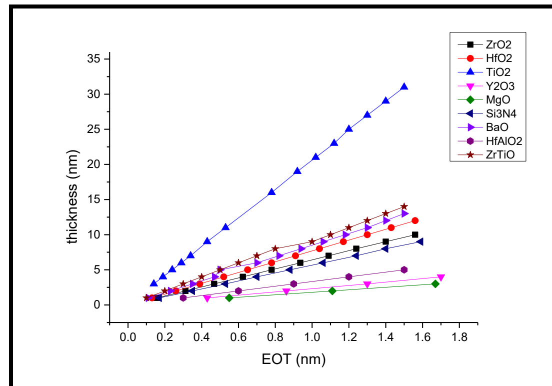

Fig. 4. Physical thickness vs EOT of different high-K

TABLE I. PHYSICAL PROPERTIES OF HfO_2, ZrO_2, AND SiO_2

Material Properties	**HfO_2**	**ZrO_2**	**SiO_2**
Dielectric Constant	30	25	3.9
Bandgap	5.7 eV	5.8 E_v	9.0 E_v
Refractive Index	2.2	2.05	1.46
Density	9.68 g/cm^3	5.74 g/cm^3	2.27 g/cm^3
Lattice mismatch with Si<100>	5.7 %	6 %	—
Coefficient of Thermal Expansion	—	1.2 x 10^{-5} K^{-1}	5.0 x 10^{-7} K^{-1}
Melting Point	2800^0 C	2700^0 C	1600^0 C
Etchability	HF solution	HF solution	HF solution
Lattice Parameter	5.116 Å	5.1 Å	5.43 Å

TABLE II. PHYSICAL GATE OXIDE THICKNESS W.R.T CMOS FAB TECHNOLOGY NODE

CMOS Node (nm)	**Effective Gate Length (nm)**	**EOT (nm)**	**Physical Oxide Layer Thickness**	
			HfO_2 (nm)	***ZrO_2 (nm)***
45	30	1.1–1.5	9–12	7–10
32	25	0.9–1.2	7–9	6–8
22	18	~ 0.5	4.0	3.0
14 or below	11–12	~ 0.4	3.0	2-3

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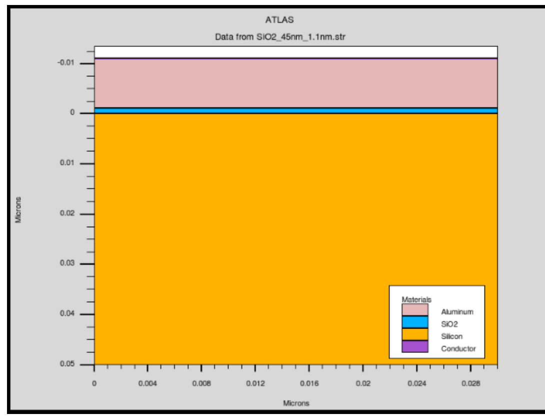

Fig. 5: MOS structure with EOT ~ 1.1 nm for 45 nm FAB

III. High-K Analysis with MOS Structure in T-CAD

To analyze high-K dielectric, MOS structure was developed in SILVACO T-CAD having gate stack: metal/oxide layer/p-Si (substrate). Al is used as metal both at the top (as a gate) and bottom (back contact) of the MOS structure. Similarly, the physical layer of SiO_2/high-K (HfO_2 and ZrO_2) is used to act as gate oxide w.r.t FAB technology node. A P-type substrate is used with a doping concentration ~ 1E17cm^{-3}. The width of the MOS structure was adjusted according to effective gate length w.r.t FAB node while z-direction was adjusted having area ~ 1.0 cm^2 with Si substrate having thickness ~ 50 nm. Al ~ 10 nm is used as gate metal. From T-CAD simulations, C-V analysis is performed with the frequency ~ 1 MHz, and gate sweep voltage varies from -3 to +2V.

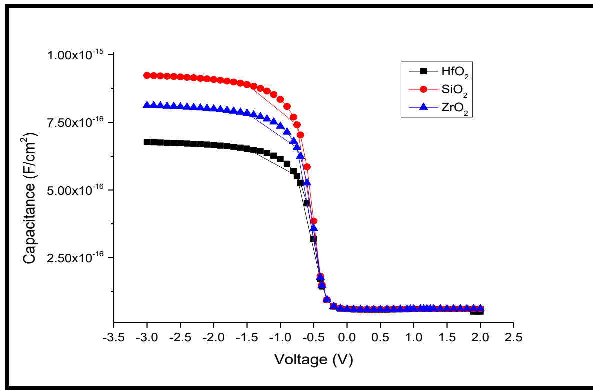

Fig. 6: C-V analysis of 45 nm FAB node with MOS structure having different gate oxide layers

A. MOS Performance for 45 nm FAB Node

45 nm FAB node has EOT ~ 1.1-1.5 nm. Initially, the MOS structure is designed with SiO_2 (as a reference) with a physical layer thickness of ~ 1.1 nm. The effective gate length is selected ~30 nm, while Al and Si substrate have thicknesses ~10 nm and 50 nm, respectively. The 2D cross-sectional view is shown in Fig. 5. After MOS structure, C-V analysis is performed by T-CAD simulation. Fig. 6 shows the C-V analysis of different MOS structures with gate oxide layers of SiO_2, HfO_2, and ZrO_2. The capacitance of SiO_2 at V= -3 V is ~ 0.9 fF/cm^2, while the capacitance is reduced in the threshold voltage (V_{th}) region to ~ 6x10^{-17} F/cm^2 due to the inversion phenomena (as a general principle of the MOS).

After that, the structure is further modified by replacing the SiO_2 gate oxide layer with high-K dielectric, i.e., HfO_2 and ZrO_2 with thicknesses ~ 9.0 and 7.0 nm, respectively (equivalent to EOT ~ 1.1 nm). HfO_2 and ZrO_2 based MOS structures have similar responses during the inversion phenomena, which reflects that the electrical characteristics of high-K are the same while the physical gate thickness is 7-8 times higher than SiO_2. However, in the non-inversion (accumulation) region (at -3V), the capacitances of MOS structure having HfO_2 and ZrO_2 layer is 0.67 and 0.812 fF/cm^2, respectively.

B. MOS Structure Performance for 32 nm FAB Node

For 32 nm FAB, MOS structure parameters were adjusted as mentioned in Table II. After 2D structures, C-V analysis is performed by T-CAD simulation. MOS structure having SiO_2 layer provides a capacitance ~ 0.95 fF/cm^2 in accumulation region (when V_g is -3V). In contrast, the MOS structure with HfO_2 and ZrO_2 layer has the capacitance of 0.69 and 0.82 fF/cm^2, respectively. All MOS structures have the same behavior in the inversion region with the same value of V_{th}. From the C-V analysis of 45 and 32 nm FAB nodes, the capacitance is almost the same due to the very close value of EOT, i.e., 0.9 - 1.1 nm.

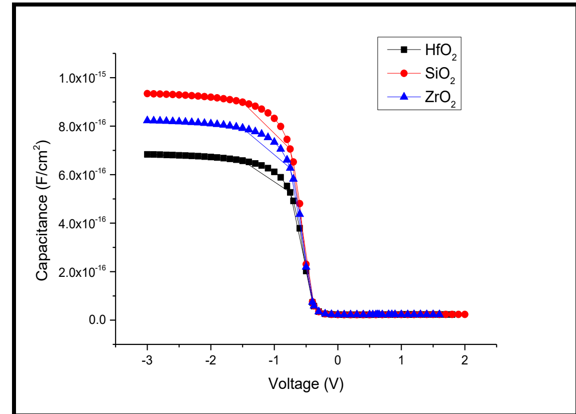

Fig. 7. C-V analysis of 14 nm FAB node with MOS structure having different gate oxide layers

C. MOS Structure Performance for 22 nm FAB Node

For the 22 nm FAB node, EOT ~ 0.5 nm is considered with MOS structure having a physical oxide layer thickness of ZrO_2 and HfO_2 is 3 and 4 nm, respectively. The effective gate length ~18 nm is also adjusted according to the 22 nm FAB node while other physical layers parameters are kept constant. After C-V analysis by AC simulations in T-CAD, the capacitances of MOS structure having HfO_2, ZrO_2, and SiO_2 layers are 0.90, 1.04, and 1.2 fF/cm^2, respectively, while the capacitance in inversion phenomena is the same from Vg ~ -0.5V to +2V for all MOS structures.

D. MOS Structure Performance for 14 nm FAB Node

For the 14 nm FAB node, MOS structures are developed having EOT ~ 0.4 nm. The effective gate length is reduced to ~11.5 nm while the other parameters are kept constant. Fig. 7 shows C-V analysis of MOS structures for 14 nm FAB node. From the results, the capacitance of HfO_2, ZrO_2, and SiO_2 is 0.70, 0.81, and 0.93 fF/cm^2, respectively (in the accumulation region when V_g is ~ -3 V).

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Hence, as an advantage of high-K dielectrics, the accumulation region's capacitive behavior is better than the conventional gate oxide layer of SiO_2. The physical gate thickness is ~ 6-7 times higher, which has a significant effect on the reduction of gate leakage current, where at least 2-3 monoatomic layers are required [11].

IV. Comparison of HfO_2 and ZrO_2 as High-K

HfO_2 and ZrO_2 are the most promising materials to act as gate oxides for Nano CMOS devices due to their excellent physical properties. Therefore, the following comparative analysis has been made.

TABLE III. Performance Analysis of HfO2 and ZrO2 w.r.t FAB Technology Node

FAB Node (nm)	EOT (nm)	Effective gate length (nm)	Physical gate oxide layer thickness of High-K		Capacitance in Accumulation Region (V_g =-3 V)		
					Ref.	High-K	
			ZrO_2 (nm)	HfO_2 (nm)	SiO_2 (fF/cm^2)	ZrO_2 (fF/cm^2)	HfO_2 (fF/cm^2)
45	1.0	30	7	9	0.92	0.81	0.67
32	0.9	25	6	7	0.95	0.82	0.69
22	0.5	18	3	4	1.2	1.0	0.9
14	0.4	11.5	2	3	0.93	0.81	0.7

A. Physical and Electrical Properties Analysis

The capacitance in the accumulation region of MOS operation is studied (in SiO_2, HfO_2, and ZrO_2). The results are tabulated in Table III. From the comparison, we observed that high-K dielectric provides at least 2-3 atomic layers for EOT = 0.4 nm for nanoscale CMOS devices, which has a significant effect on the reduction of gate leakage current. As per square area, the capacitance in the accumulation region is reduced up to 15 – 22% compared to SiO_2, while the effective gate length size is reduced to 11.5 nm (61% size reduction) for the same transconductance. Hence the yield density is increased by reducing the FAB node.

B. High-K Fabrication for CMOS Process

The fabrication process of ZrO_2 and HfO_2 (as high-K) deposited on Si substrate is illustrated in Table IV. MOSCAP process flow for ZrO_2 deposition; Buffered oxide etch (BOE) is used to form the active area ~ 5×10^{-5} cm^2. High-density plasma (HDP) system is also used for the etching of ZrO_2 with HBr/CF_4 gases, where the maximum etch rate is ~ 70.8 nm/min by a mixture of gases. Zr is deposited by sputtering, having pressure ~ 5×10^{-7} Torr with a deposition rate of ~ 12 nm/min. Pt is deposited as a metal gate using sputtering at 300°C with 2×10^{-2} Torr.

MOSCAP process flow for HfO_2 deposition; Hafnium silicate ($HfSiO_4$) will be deposited by Physical Vapor Deposition (PVD) with 'Ar' as an ambient gas. After that, the wafer is then thermally annealed with NH_3, and TaN is deposited at last with Reactive Ion Etching (RIE).

TABLE IV. Fabrication Process Comparisons of ZrO_2 & HfO_2

S.no	MOSCAP steps	ZrO_2 [13]	HfO_2 [14]
1	Wafer cleaning	Piranha	
2	Oxide growth	Field oxidation; 350 - 400 nm at 950° C for 2 hours (Typical pattern area ~ 5 x 10-5 cm^2)	
3	Oxide Etching	HBr/CF_4 is used with high density plasma (HDP) system. Max. etch rate ~ 70.8 nm/min for ZrO_2 at HBr (75%)/ CF_4 (25%) gas mixing ratio.	Precise etch depth for ultra-thin HfO_2 (3.5 nm) films by using ALET with Ar beam and BCl_3 gas. ALET-etched HfO_2 by supplying BCl_3 gas and Ar beam at the higher level pressure.
4	Dielectric deposition	Zr deposition ~ 2-4 nm: DC magnetron sputtering	Co-sputtering of Hf and Si RPA (500-700^0 C, NH_3, 5-60 sec)
5	Annealing process	RTP (300 -900^{0}C)	PDA
6	Gate deposition	Pt deposition ~ 150 nm: DC magnetron sputtering (300^0 C, 200 W, Ar pressure at 20 mTorr)	TaN deposition by reactive sputtering Gate patterning and Reactive Ion Etching (RIE) for TaN HF dip and contact Al deposition
7	Contact electrode deposition	Pt electrode patterning (aqua regia)	Contact patterning and Al etch
8	Post annealing	Post-Pt anneal	anneal (450^0 C, 20min)
9	Backside contact	Al deposition	

Zr-silicates with the incorporation of 'N' into the ZrO_2 stack are useful to improve thermal stability, reduction in B penetration, and leakage current. Similarly, $HfSi_xO_y$ film is also a good alternative as gate dielectric due to its drastic physical properties over HfO_2, e.g., crystallization temperature, interface properties, and thermal stability. The interface roughness can be improved by Hydrogen Plasma Treatment (HPT) and HCl solution etching to grow atomic layer having thickness up to 3 nm [12].

V. Conclusion

To meet the current and future demands, scaling down in CMOS is continued towards the nanoscale devices $\leq$ 14 nm FAB technology node, but SiO_2 has limitations due to severe direct tunneling effect. As a result, high gate leakage current may affect the device's operation and reliability.

High-K dielectric is an attractive solution to act as a thick gate oxide layer to overcome gate leakage current issues and provide EOT < 0.5 nm as desired. In this paper, high-K dielectric, HfO_2, and ZrO_2 are investigated with their physical modeling of MOS structure in T-CAD for different FAB technology nodes (45-14 nm). We studied that the physical gate oxide layer up to 30 Å is achieved with High-K, the least requirement to overcome the gate leakage current. The capacitance in the accumulation region of MOS operation is also reduced to 15 – 22% compared to SiO_2, while on the other hand, the size of the effective gate length is reduced to 11.5 nm with better control on the gate. Hence, the size of CMOS devices is

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reduced to 61%, which has an impact on increasing the package density.

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