Improved T_{MAX} Estimation in GaN HEMTs Using an Equivalent Hot Point Approximation

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Abstract—In this article, heat generation distribution and maximum device temperature of gallium-nitride (GaN) high-electron-mobility transistors (HEMTs) are investigated by using the 2-D electrothermal and finite-element method (FEM) simulations. Devices with different gate lengths and source-to-drain spacing are investigated. It is observed that the maximum device temperature (T_{MAX}) depends on the drain-to-source spacing and is almost independent of the gate length and that the assumption of a uniform heat generation region, under the gate, is not accurate; this is contrary to conventional calculation methods. Moreover, based on the results, a new approximation is proposed to use in the FEM simulations that can estimate T_{MAX} more accurately. This method does not require physics-based technology computer-aided design (TCAD) simulations and can work with a low mesh density. The performance is compared with prior methods.

Index Terms—2-D device simulations, AlGaN, channel temperature, finite-element analysis, gallium nitride (GaN), high-electron-mobility transistors (HEMTs), hot point, self-heating, technology computer-aided design (TCAD), thermal analysis, thermal resistance.

I. INTRODUCTION

GALLIUM-NITRIDE (GaN)-based high-electron-mobility transistors (HEMTs) are high-performance devices that show superior performance in high-power amplifiers and switching applications [1]–[3]. The high bandgap leads to an elevated breakdown voltage [4]. The 2-D electron gas (2DEG) provides excellent electron mobility

and saturated electron velocity, which are crucial for high-frequency devices [5]. These properties make GaN HEMTs an advantageous option for 5G applications [6].

Although GaN has many advantages, some of its drawbacks prevent real device implementations from achieving the optimal theoretical performances. Self-heating is one of the main limitations that should be considered during the design [7], [8]. The physical parameters, such as mobility and electron velocity, depend on temperature. Hence, the device performance is directly affected by its temperature [9], [10]. Moreover, breakdown mechanisms are adversely affected by elevated temperatures. Thus, reducing temperature is important for maintaining reliability and lifetime [11]. Finally, the behavior and energy level of traps are strongly linked to the temperature. Therefore, it is important to have an accurate channel temperature during trap characterization [12]–[14].

Consequently, the measurement and simulation of device temperature accurately are critical for most applications. This led researchers to work on several measurement and simulation methods to derive the channel temperature of the device. For example, micro-Raman measurements [15], infrared imaging [16], visible-UV spectroscopy [17], and electrical measurements [18] are commonly used methods in the literature. All of these methods have different advantages and limitations. In order to overcome these limitations and understand the internal dynamics of devices, simulations and device models are widely used. The most prevalent ones can be listed as analytical modeling [19]–[21], finite-element method (FEM) analyses [22]–[25], electrothermal simulations [11], [26], [27], and Monte Carlo simulations [28]–[30]. These methods also provide the channel temperature information in different precisions. Electrothermal simulations are very accurate in simulating device performance and temperature. However, they require solving thermal and semiconductor equations simultaneously in a large number of nodes and are, thus, computationally challenging. As such, one generally limits the simulation to the active region of the device only. However, this prevents designers from observing the coupling between the fingers in multifinger devices or the overall temperature of the amplifier. Also, in these simulations, several parameters should be calibrated beforehand in order to get correct device behavior. Accurate calibration can be a time-consuming task for each device. FEM simulations are valuable for simulating transistors as a whole. However, to achieve computational efficiency, designers need to simplify complex physical effects

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and implement them in a device structure. A commonly used approximation is to assume that all of the heat is generated from a uniform heat source under the gate along the surface [24], [25], [31], [32]. This approximation provides a convenient computational scheme for the simulation. However, it may not be a realistic representation and, hence, the accuracy is a concern. In this article, heat generation behavior in HEMT devices is investigated via technology computer-aided design (TCAD) simulations. It is observed that the maximum device temperature (T_{MAX}) depends on the drain–source spacing and is almost independent of the gate length, which is contrary to conventional calculation methods. In addition, a new straightforward realistic FEM method is proposed for finding the maximum channel temperature. In our previous work [33], a method was proposed to couple TCAD electrothermal simulations and FEM simulations. The same method is used to analyze and develop a simpler model, which reduces the required computational power in FEM simulations effectively and improves accuracy.

This article is organized as follows. In Section II, the TCAD simulation details are described. In Section III, the heat generation distribution for different sizes of the AlGaIn/GaN devices is investigated. In Section IV, the proposed FEM simulation method is explained and the results are discussed. Finally, the conclusions are drawn in Section V.

II. TCAD SIMULATIONS

A basic AlGaIn/GaN HEMT structure is used in TCAD calculations in order to make the simulations faster and make the results more general. The parameters used in the simulations and a sketch of a sample structure are shown in Fig. 1. The ATLAS module of Silvaco is used for 2-D TCAD simulations [34]. In order to calibrate epitaxial parameters, such as electron mobility and electron charge concentration, devices with T-gate and field plate structures are measured under dc biasing conditions and elevated base temperatures. The same biasing conditions are implemented in simulations, and the consistency of the measured and simulated I – V curves is achieved. The same epitaxy is used in simulations with an I-gate structure to observe the physical changes clearly and get more generic results in this article.

In order to observe the physical changes clearly and get more generic results, an I-gate is used in the simulations in this article. The piezoelectric charge is implemented as a function of AlGaIn thickness and concentration. A Monte Carlo simulation-based temperature-dependent mobility model is used in order to simulate the electron mobility and saturated electron velocity more accurately. In the simulation, the heating equations and semiconductor equations are coupled in order to derive the position-dependent temperature and heat generation by using the lattice temperature model. Room temperature (27 °C) is used as the base temperature.

Drain current (I_D) versus drain to source voltage (V_{DS}) and gate to source voltage (V_{GS}) graphs are shown in Fig. 1. As the drain-to-source distance (L_{DS}) increases, the access resistance (R_{access}) of the device increases because of the increased current path. In the linear region (when V_{DS} is small)

Fig. 1. (a) I_D – V_{DS} and (b) I_D – V_{GS} graphs of transistors with three different L_{DS} values simulated in TCAD simulations.

of the I_D – V_{DS} curves in Fig. 1, the I_D – V_{DS} slope is inversely proportional to the ON-resistance R_{ON} . One of the components of R_{ON} is the access region resistance. As such, devices with short L_{DS} dimensions exhibit a steeper slope as expected. Moreover, the knee voltage shifts to the right, with higher L_{DS} , indicating that electrons reach their saturation velocity at a higher drain voltage.

One of the important points in the electrothermal analysis is the simulated lengths of drain and source contacts. In the literature, many researchers make these dimensions as small as possible to reduce the required simulation area and node number [11], [27], [35], [36]; sometimes, they do not mention the length at all. However, because adiabatic boundary conditions are used at the edge of the simulation area, the boundaries can be considered as mirrors, that is, there are symmetrical and identical devices on the other side of the boundary. As the dissipated power increases, the thermal crosstalk between these devices becomes effective and causes an excessive increase in the device temperature, due to heat from the neighboring devices. On the other side of the tradeoff, a large contact size increases the simulation area and mesh node numbers. In order to find the minimum contact sizes that can be employed safely for the power levels used in this article, several simulations were performed to observe the impact of this parameter. In Fig. 2, the maximum device temperature with respect to the ohmic contact length is plotted for V_{DS} 10 V and V_{GS} 0 V, and this is the biasing point with the highest power dissipation. At this bias, 8 W/mm of power is dissipated in the device structure. The figure shows that as the contact length becomes less than 5 μm , the temperature increases dramatically. For example, a 0.5- μm contact length results in nearly 10 °C more than a 5- μm contact. The drain

Fig. 2. Variation of maximum device temperature and drain current with respect to simulated ohmic contact length in TCAD simulations where $V_{DS} = 10$ V and $V_{GS} = 0$ V.

current is also plotted in Fig. 2. Because of the temperature dependence of the electrical parameters, the drain current degrades as the contacts get shorter. This shows the importance of this parameter in simulating the device performance accurately.

In this article, the ohmic contact length is set to $5.5 \mu\text{m}$ to achieve the accuracy of the analysis while keeping the simulation area small. In general, for high-power electrothermal simulations, this parameter should be carefully selected to attain accurate results.

III. HEAT GENERATION IN HEMT

To understand the heating mechanism in GaN HEMT devices, the position-dependent heat generation rates are investigated with different L_{DS} and L_G values. In order to observe the heat generation that changes along the channel only, the heat is integrated along the y -direction, which is shown in Fig. 1. This method lets us express the heat generation as a function of the x -axis position only. Hence, we can plot the heat generation distribution along the channel easily and observe the shape of the curve clearly.

In Fig. 3, the heat generation rates of devices with different L_G values and different drain currents are plotted with respect to the position along the channel. In addition, a uniform heat generation profile is plotted for reference. Fig. 3 also shows that most of the heat is generated at the drain-side corner of the gate. This is consistent with earlier observations [16], [30]. The heat generation is clearly nonuniform. Instead, it has a Gaussian-like distribution. The reason for the nonuniform distribution of heat generation is the presence of a large electric field at the gate-drain corner [35]. As L_G changes, the heat generation profile follows the gate-drain edge closely without changing its shape. This behavior of heat generation results in a fairly steady maximum channel temperature as L_G changes. This point will be further investigated in Section IV. Moreover, the location at which the peak value of the heat generation occurs is not directly under the gate and exhibits a shift toward the drain side as the drain current decreases (as V_{GS} is made more negative). The reason is that as the channel current declines, the potential drop along the access region (between

Fig. 3. Heat generation near the gate for different gate lengths and drain currents, $L_{DS} = 4.5 \mu\text{m}$.

the drain and the gate) becomes smaller too. This means that more positive potential occurs at the channel near the gate. The difference between the gate and the channel becomes higher at lower gate voltages, and a larger electric field occurs. For example, consider the $V_{GS} = 0$ V and $V_{DS} = 10$ V case (blue dotted line) in Fig. 4. Between the source and the channel edge (0 – $1.5 \mu\text{m}$), the potential rises by 1.5 V. Across the channel (1.5 to $1.75 \mu\text{m}$), it rises from 1.5 to 6.5 V, and in the gate-drain access region (1.75 – $4.5 \mu\text{m}$), it rises from 6.5 to 10 V. Consequently, the electric field (dV/dx) is 1 , 20 , and 1.27 V/ μm , in the three regions, respectively. In the low drain current case ($V_{GS} = -3$ V and $V_{DS} = 10$ V), the electric field is 0.33 , 36 , and 0.18 V/ μm , in the three regions, respectively. This causes wider depletion and increases the resistance. This change in the electric field makes the peak point of the heat generation shift toward the drain side. However, because the power is related to the square of the current, at the higher drain currents, the generated heat increases and a higher peak value for heat generation results.

Fig. 4. Potential distribution along the channel for different drain and gate biases.

Fig. 5. Heat generation near the gate for different source-to-drain (L_{DS}) lengths and gate voltages, $L_G = 250$ nm.

In order to understand the role of access regions in the heat generation better, devices with different L_{DS} values are investigated, while L_G is kept fixed at 250 nm. In Fig. 5, the heat generation distributions in the gate region are plotted for different gate voltages. The heat generation in the gate region grows as the gate voltage increases positively as expected, and the drain current increases with the reduction in the depletion region. The change in L_{DS} becomes more influential when the drain current is higher. The reason is that, when the drain current is small, the heat generated in the access region also becomes small. Therefore, any change in the access region does not affect the heat generation in the gate region as much. However, as the channel current increases, the heat generation in the access regions becomes comparable

to the heat generation in the gate region. An increase in the access region length results in more resistance and higher heat dissipation for the same current. If the same power is applied, the heat generation from the gate region is reduced because of this reason. Therefore, less heat is generated in the gate region and more heat is generated in the access region as L_{DS} increases.

The width of the Gaussian-like heat generation shape is also important because it shows how wide is the heat generation area, which directly changes the heat generation density. Here, the heat distribution width will be defined by the full-width half-maximum (FWHM) of the Gaussian-like heat generation shape. As L_{DS} increases, the FWHM decreases with a higher rate as V_{GS} increases.

The location of the peak point of the heat generation also shifts. The potential difference between the gate and the channel decreases as the source-to-drain distance increases. More potential is dropped on the access region as the length of it increases; therefore, with a constant gate voltage applied, the potential difference of the gate and channel decreases. This causes a lower electric field. Similar to the behavior in gate length change, with a lower electric field, the peak point of the heat generation gets closer to the gate.

IV. EQUIVALENT HOT POINT APPROXIMATION

It is observed from Figs. 3 and 5 that especially when the drain current is high, the heat generated from the access region becomes comparable to that generated at the gate region. This leads to an interesting conclusion. Specifically, in the conventional approach, where it is assumed that the heat is primarily generated in the gate region, the maximum temperature is overestimated. To be able to model the heat generation better, we need to develop a new method. Our knowledge of measurable quantities, such as R_{ON} and I_D , can be used to eliminate the need for complicated simulations and to enable a fast estimation of the channel temperature.

In FEM simulations, the heating module of the COMSOL software was used [37]. The same structures were implemented in this software for TCAD simulations. To couple them and be sure that the simulations correlate, the method proposed in [33] was used. In this method, the 2-D heat generation data are derived from TCAD simulations by using the “PROBE” statements. These data are used to produce a 2-D heat generation map that FEM simulations can use via MATLAB. The heat map is implemented in FEM simulations as a position-dependent heat source. The results show that these two simulations show a perfect match with a maximum error of 3 °C. The error is caused by different material parameters and the limited precision of the probing of the heat generation.

The performance of a commonly used approximation in the literature is investigated in FEM simulations, and the accuracy is evaluated via the mentioned method. The total generated heat is implemented as a uniform heat source along the gate–semiconductor interface. This method can work with rougher meshes and is, therefore, beneficial from the computational power aspect [24], [25].

In this method, the heat generation area is defined along L_G and dissipated power is applied to this area uniformly. Any change in gate dimension, therefore, affects the power density and the resultant T_{MAX} directly. However, as observed in TCAD simulations, the actual heat generation occurs in a small area near the drain-side corner of the gate (to be named the hot spot) and does not change appreciably with variations in L_G . This difference causes this method to fail in following the trend of maximum temperature when the L_G changes. As L_G decreases, the heat generation area shrinks in the conventional approximation and the temperature increases rapidly. However, the reality is that the T_{MAX} is fairly steady for all observed gate lengths. Also, in the conventional method, the position of the heat generation is not a parameter; the heat generated in the access region is considered as generated under the gate. However, the generated heat in the access region has a minor effect on the peak temperature and squeezing the total generated heat in the gate region results in higher temperatures. As L_{DS} increases, under constant power, the heat generated in the gate region and the maximum device temperature decrease. The conventional approximation does not capture, and cannot handle, this change and results in a fixed temperature profile for the simulated structures.

Although the method proposed in [33] provides the well-calibrated and realistic channel temperatures in FEM simulations, it still requires customization for every structure and to simulate it first in TCAD simulations, then to produce the heat generation map, and to implement in FEM simulations. In addition, because the heat generation still has a sharp peak at the drain-side corner of the gate, it requires a fine mesh which requires a lot of computational power. Therefore, it is desirable to find a simpler method that can compute T_{MAX} in FEM simulations that incorporates directly measured data, without the need for TCAD simulations or a heavy computational requirement. Here, we propose such a method. It is based on using a uniform heat source at the drain-side gate corner with the length of FWHM of the Gaussian heat generation shape and a uniform heat source along the channel for implementing the heat generation related to R_{access} .

A uniform heat source is used to mimic the Gaussian-like heat generation. The validity is tested in the FEM method's simulations by implementing the same powers for each heat distribution and observing the maximum temperatures. The uniform heat source with FWHM of the Gaussian shape results in close temperature predictions compared with the original distribution. Thus, we can use a uniform heat source (with the length of FWHM of the Gaussian-like heat generation shape) in lieu of the full heat distribution.

In order to calculate the heat generated in the gate region, we can subtract the heat generated in the access region from the total dissipated power. One way to calculate the heat generated in the access region is to make TCAD simulations and integrate the position-dependent heat generation value along the access region; however, this method is too complicated. Rather than this, we can assume the access region as a basic conductor, with resistance of R_{access} , and I_D is flowing on it. Using Ohm's law, we can calculate the dissipated heat in this region, multiplying resistance by the square of the

Fig. 6. R_{access} to R_{ON} ratio for different gate voltages, $V_{DS} = 10$ V.

current. However, R_{access} should be measured or calculated in this case.

We can use R_{ON} in deriving R_{access} . However, R_{access} itself is a function of channel temperature and current [31]. Therefore, especially for higher channel currents, a correction factor should be applied to R_{ON} to derive R_{access} [38], [39]. In order to derive this expression from simulations, we have observed the electric potential along the channel for different gate biases in TCAD simulations, as shown in Fig. 4. The potential drop over the access region becomes higher when the drain current is higher [40].

Hence, we can use the potential difference and the channel current to calculate R_{access} . The ratio of R_{access} of different gate bias conditions for the condition that R_{ON} calculated is shown in Fig. 6. The increase in R_{access} is caused by the temperature rise in the access region and the quasi-saturation of carriers. This value can be directly determined by measuring the source access region resistance [38] or by basic TCAD simulations as is done here.

As an example, we can calculate the power dissipations for the $V_{GS} = 0$ V and $V_{DS} = 10$ V biasing of $L_{DS} = 4.5$ μ m and $L_G = 250$ nm (blue dotted line in Fig. 4). I_D is 0.798 A/mm, and this translates to 7.98-W/mm total heat dissipation in the device. The potential in the drain-to-gate region is 3.5 V. The resistance of this region, therefore, becomes 4.38 $\Omega \cdot$ mm.

When we look at $V_{DS} = 1$ V and $V_{GS} = 0$ V bias (black solid line in Fig. 4), the potential drop in the same region is 0.6 V. I_D is 0.313 A/mm for this case, which corresponds to a resistance of 1.91 $\Omega \cdot$ mm. The ratio of drain-to-gate region resistances of these two biasing conditions is 2.28, which is accepted as R_{access} coefficient of first bias condition. I_D of $V_{DS} = 1$ V and $V_{GS} = 0$ V corresponds to $R_{ON} = 3.19 \Omega$ mm and, because the depletion region is small due to high gate voltage, can be taken as R_{access} . From this calculation, we find 4.6-W power generated in the access region and 3.4-W power generated in the gate region. These values can be implemented as a uniform heat source along the access region and a uniform heat source at the gate-drain corner with a 60-nm length (referring to Fig. 5).

To mimic the Gaussian-like heat generation profile observed in Figs. 3 and 5, a uniform heat source with FWHM of the drain-side gate corner heat generation peak is implemented

Fig. 7. Maximum channel temperatures of different gate lengths for different gate currents and methods.

in the same corner. The values of power dissipations at the access region and gate corner for each L_G and L_{DS} are calculated with the proposed method. In 2-D FEM simulations, the calculated power in the access region is implemented as a uniform heat source along AlGaIn/GaN heterojunction. The calculated power in the gate region is implemented as a uniform heat source with width of FWHM, at the drain-side corner of the gate. The maximum channel temperatures obtained from the proposed method are shown in Figs. 7 and 8. When L_G decreases, the difference between the uniform heat source approximation and the TCAD simulations increases; however, the proposed method shows a nearly constant error. This shows the ability of the proposed method to follow L_G changes.

When L_{DS} increases, the TCAD simulation captures the change in T_{MAX} , whereas the conventional method remains constant. The proposed method follows this trend by implementing R_{access} related to the heat source as a separate heat source in the channel. The temperature values follow the trend found in TCAD simulations correctly despite the uniform heat source approximation. The maximum observed error is 5 °C and 50 °C in the proposed method and the conventional approximation, respectively.

Fig. 8. Maximum channel temperatures of different source-to-drain spacings for different gate voltages and methods.

V. CONCLUSION

In this article, TCAD simulations are used to investigate the heat generation profile in a generic GaN HEMT structure. The effect of changes in L_G and L_{DS} on the heat generation profile and maximum channel temperatures is investigated. It is observed that down to 100 nm, L_G does not change the heat generation profile appreciably because the heat is generated predominantly at the drain-side gate edge. In addition, as L_{DS} increases, the heat dissipation in access regions increases and lowers the potential drop over the gate region; therefore, the heat generation at the gate region gets reduced. A new method is developed to use in FEM simulations to get more realistic channel temperatures that follow the proper trends with parameter changes using fewer computational resources. The results are compared to a commonly used conventional method, and the procedure is explained. The generality of simulations is tested with simulations for different structure parameters. In addition to HEMTs with T-gate and field plate structures, this method can also be implemented with other planar or vertical power GaN devices with taking hot spot size and power dissipation in resistive regions into account.

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