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Utilizing embedded ultra-small Pt nanoparticles as charge trapping layer in flashristor memory cells

İkram Orak[a,*], Hamit Eren[b], Necmi Bıyıklı[c], Aykutlu Dâna[d]

[a] Vocational School of Health Services, Bingol University, 12000 Bingol, Turkey
[b] National Nanotechnology Research Center (UNAM), Bilkent University, 06800 Ankara, Turkey
[c] Department of Electrical and Computer Engineering, Utah State University, Logan, UT 84322, USA
[d] E.L. Ginzton Laboratory, Stanford University, Stanford, CA 94305, USA

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ABSTRACT

In this study, a methodology for producing highly controlled and uniformly dispersed metal nanoparticles were developed by atomic layer deposition (ALD) technique. All-ALD grown thin film flash memory (TFFM) cells and their applications were demonstrated with ultra-small platinum nanoparticles (Pt-NPs) as charge trapping layer and control tunnel oxide layer. The ultra-small Pt-NPs possessed sizes ranging from 2.3 to 2.6 nm and particle densities of about 2.5×10^{13} cm^{-b}. The effect of Pt-NPs embedded on the storage layer for charging was investigated. The charging effect of ultra-small Pt-NPs the storage layer was observed using the electrical characteristics of TFFM. The Pt-NPs were observed by a high-resolution scanning electron microscopy (HR-SEM). The memory effect was manifested by hysteresis in the I_{DS}-V_{DS} and I_{DS}-V_{GS} curves. The charge storage capacity of the TFFM cells demonstrated that ALD-grown Pt-NPs in conjunction with ZnO layer can be considered as a promising candidate for memory devices. Moreover, ZnO TFFM showed a I_{ON}/I_{OFF} ratio of up to 52 orders of magnitude and its threshold voltage (V_{th}) was approximately -4.1 V using $I_{ds}{}^{-a/b} - V_{gs}$ curve. Fabricated TFFMs exhibited clear pinch-off and show n-type field effect transistor (FET) behavior. The role of atomic-scale controlled Pt-NPs for improvement of devices were also discussed and they indicated that ALD-grown Pt-NPs can be utilized in nanoscale electronic devices as alternative quantum dot structures.

1. Introduction

Repeatable and reliable techniques for the deposition of nanoparticles (NPs) in TFFM as charge storage layers are of vital importance [1–3]. Metal NPs embedded for charge trapping layers have been an attractive alternative since metallic nanostructures have some significant advantages when compared to semiconductor counterparts such as lateral isolation of each storage site and high density of states [4–6]. Especially, gold (Au) and platinum (Pt) metal nanoparticles and nanodots are very useful for storage layer materials [7–8]. Their particle size and surface density are very important for memory fabrication and characterizations [9]. There are many ways to deposite metal NPs including DC-magnetron sputtering [10], pulsed laser deposition (PLD) [11], tilted-target sputter (TTS) [1], atomic layer deposition (ALD) [2], electron-beam evaporator [12], molecular atomic layer deposition (MALD) [13], de-wetting [14] and inject-printing [15]. Among these methods, the ALD technique shows very high homogeneous deposition characteristics on substrate surfaces, highly-controlled atomic-level thickness control, ultimate conformity and large area uniformity. Due to these advantages, the ALD technique has been commonly and increasingly used in a vast number of electronic device applications. Silicon nanocrystals (NCs) and NPs can be used in the storage layer and efficient charge trapping can be achieved within large memory windows at room temperature [4,16,17]. It has been demonstrated that germanium (Ge) and silicon (Si) NCs can form a trilayer structure between silicon dioxide (SiO_2) and metal contact layer for memory applications [18,19]. Metal NP embedded devices for charge storage characteristics are commonly exploited in flash memory technology and are typically characterized by capacitance-voltage measurements [1]. On the other hand, increased performance thin-film transistors (TFTs) are commonly fabricated by using metal NPs with complementary metal-oxide-semiconductors (CMOS) and silicon-oxide-nitride-oxide-silicon(SONOS) [11,20]. To fabricate high-performance thin-film semiconductor/gate dielectric stacks such as (ZnO, TiO_2)/(Al_2O_3, HfO_2), films were directly deposited on heavily doped substrates via ALD [16–18]. Bolat et al. demonstrated the low-temperature fabrication

* Corresponding author.
E-mail address: ikramorak@gmail.com (İ. Orak).

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of GaN TFTs via hollow-cathode plasma-assisted atomic layer deposition (HCPA-ALD), which showed decent TFT characteristics, with relatively low mobility (0.025 cm^2/V-sec) and high threshold voltages (11.8 V) [22]. The performance of non-volatile memory can be further increased by Pt-NP embedded between control oxide and tunnel oxide so that the device has improved retention and endurance characteristics. Due to Pt-NPs and metal NPs, the active charge tunneling mechanisms Fowler-Nordheim (F-N) tunneling which is the dominant mechanism responsible for the current conduction through insulating layer in MOSFETs and MOS memory devices can also be explained comprehensively [23,24]. The other tunneling mechanism is Poole-Frenkel (P-F) tunneling that is effective in dielectric thin materials when they have high density of traps [25]. The standard flash memory cell industry utilizes Channel-Hot-Electron (C-H-E) injection mechanism for operations such as lateral electric field and applied drain-source voltage [26,27]. In addition to these tunnel mechanism, the band-to-band (B-T-B) tunneling FETs allow for excellent ON/OFF current ratios compared to other memory cells and MOSFETs in ultra-low voltage applications [28,29]. Pt nanorods have been grown by ALD on Al_2O_3 and have been investigated nonvolatile memory characterization. The device has been characterized as good charge retention, efficient programmable and electron trapping capacity [30]. In-Ga-Zn-O thin film nonvolatile memory has been fabricated by using ALD Pt-NCs sandwiched between aluminum oxide (Al_2O_3) layers. The IGZO memory thin film device has been proven suitable to use applications in optical touch panels [31]

In this study, a flashristor device was presented which utilizes the effect of embedded ultra-small Pt-NPs and zinc oxide (ZnO) channel memory structure when operated as a two terminal device at room temperature. ZnO thin films are commonly used on the electronic and optoelectronic devices for electrical, physical and chemical features such as wide band gap (3.4 eV), high transparency, piezoelectricity, ferromagnetism and electron mobility values. A straight forward, one-reactor and single-load, cost effective method for fabricating the flashristor device was demonstrated using ALD. The charge-trap memory of Pt-NPs on TFFMs by electron force microscopy (EFM) was also investigated. TFFM showed improved performance in terms of larger memory window and lower operation voltage. The TFFM devices demonstrated has the potential to be utilized in next-generation non-volatile memory technology. The highly-controlled Pt-NPs can also be used for electronic device applications featuring quantum dot structures.

2. Experimental details

The flash memory cells were fabricated on a doped (1–10 Ohm.cm) p-type Si(1 0 0) wafer. The experimental steps are as follows;

- The active region of the memory cells were defined on a 300 nm SiO_2 layer grown by PECVD at 250 °C. SiO_2 surface was coated photoresist 5214 E and annealed 100 °C with hot plate. The sample surface was made isolation layer by photolitography mask and etch-patterned by standard (1:6) buffered oxide etch (BOE) solution. Finally, photoresist was removed with acetone.
- The Al_2O_3 control oxide layer was deposited in a thermal-ALD reactor system (Cambridge Nanotech–Savannah 100) with a nominal thickness of 15 nm at 250 °C using trimethyl-aluminum (TMA) and H_2O as aluminum and oxygen precursors, respectively. As the carrier gas, N_2 was used with a flow rate of 20 sccm.
- Subsequently, Pt-NPs with an average size of 2.5 nm were deposited as the charge trapping layer within the ALD reactor by using trimethyl(methylcyclopentadienyl)platinum(IV) (MeCpPtMe 3) as Pt precursor and O_3 as counter reactant. The temperature of Pt precursor was held at 65 °C to obtain a proper vapor pressure. O_3 was produced from a pure O_2 flow with a Cambridge NanoTech Savannah Ozone Generator. ALD Pt deposition was carried out at 150 °C. On top of Pt NPs, 5 nm of HfO_2 layer (using tetrakisethylmethylamino hafnium, TEMAH and H_2O) was deposited by ALD as the tunnel oxide layer at 200 °C.
- Afterwards, within the same ALD reactor, a 10 nm thick ZnO channel was deposited at 180 °C and patterned with photolitagraphy by etching in dilute H_2SO_4:H_2O (2:98) solution for 2 s.
- Finally, the source and drain contacts were thermally evaporated (100 nm thick Al , %99,99 purity) and patterned by lift-off technique.

To investigate the surface morphologies of Pt-NPs structures, High Resolution Scanning Electron Microscopy (HR-SEM) was used. Electrical measurements were performed using a Keithley 4200 semiconductor characterization system. Atomic force microscopy measurements were performed on an Asylum MFP3D system using a custom sample holder. A metal coated cantilever with a resonance frequency of 71 kHz and nominal spring constant of 2.7 N/m was used in tapping mode, while a sinusoidal voltage (0.5 V amplitude) was applied to the cantilever at a frequency of 11 kHz to avoid harmonics of electrostatic forces from interfering with the topography measurement. X-rayphotoelectron spectroscopy (XPS) was used to determine the oxidation state of various Pt-NPs in the samples.

3. Results and discussion

To investigate the memory effect of ultra-small Pt-NPs, the memory features of the charge trapping layer were characterized. As can be seen Fig. 1a and b shows 2D and 3D schematic description of ZnO TFFM. All device layers were deposited by ALD including control oxide, charge trap layer, tunnel oxide and ZnO transistor channel with thickness values of about 15 nm, 2.5 nm, 5 nm, and 10 nm, respectively. Source and drain contacts were formed by thermal evaporation with a film thickness of ~100 nm. First of all, the device is a typical thin film flash memory cell. To understand the impact of the bandgap diagram of the fabricated structure, Fig. 1c shows the bandgaps and affinities of the layers as E_g = 1.12 eV and E_{EA} = 4.05 eV for Si, E_g = 8.7 eV and E_{EA} = 1.35 eV for Al_2O_3, E_g = 5.7 eV and E_{EA} = 2.65 eV for HfO_2, and E_g = 3.3 eV and E_{EA} = 4.35 eV for ZnO. The work function for Pt-NPs is 5.6 eV, which was optimized via controlling the ALD recipe parameters. Especially charge trap layer is very effective on memory characterizations. In this study, Pt-NPs was deposited the storage layer for effective charging. It was bended applied voltage. So this is a great advantage in charging. Pt-NPs were used as charge trap layer between control (Al_2O_3) and tunnel (HfO_2) oxide layers. The negative and positive charges on the storage layer were constrained between two oxide layers. Therefore memory characteristics can be improved through this condition. Pt-NPs behaves as quantum dots and a trap layer. Thanks to this material, the memory window is further expanded. SEM images of the Pt-NPs in Fig. 1d show that Pt-NPs are very small in size (2.3–2.6 nm) with high area density (2.5×10^{13} cm^{-2}). Nanoparticle size homogeneity is similar all over the 4-inch diameter substrate surface. The XPS data is given in Fig. 1d. High resolution Pt-NPs 4f state XPS spectrum of the Pt deposited through the ALD on reference Si substrate. The peak positions were at 71.1 and 74.9 eV, respectively. The XPS peak data of these samples were suitable in the literature.

The Pt-NPs are effective on storage layer due to the I_{DS}-V_{DS} and I_{DS}-V_{GS} hysteresis. The electrical characterization of the Pt-NP-based TFFM device is given in Fig. 2, where conventional thin film transistors characteristics are measured. In Fig. 2a, when we applied voltage between source and drain contacts and changed the V_{GS} from 0 V to 6 V, it

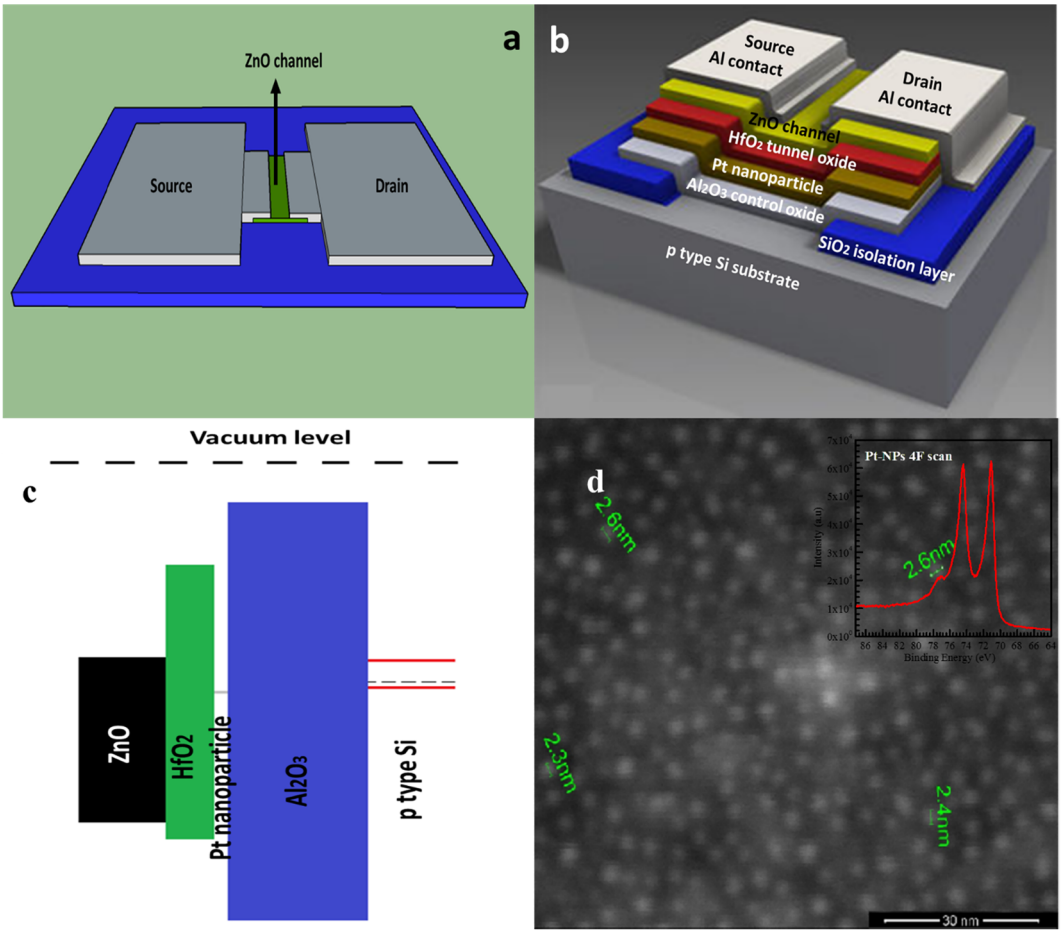

Fig. 1. (a and b) 3D schematic description of the fabricated ZnO thin film flash memory (TFFM) device (c) The bandgap structure of layers under flatband condition, (d) High-resolution SEM images of Pt-NPs.

clear was exhibited hysteresis and its characteristic behavior resembles n-type field effect transistor (FET) [32]. This shows that the device has been behaved as a classical transistor.

In the I_{DS}-V_{DS} measurements, as can be seen in Fig. 2a, there is a shift at the same point at about 5.10^{-10} A, which may have been caused by noise within the measuring system. The current curve and slope is usual behavior. So the current increases slightly with increasing V_{GS}. The V_{GS} voltage was changed at certain intervals and the measurements were taken to measure the switching effect of the transistor at the unit time. But the I_{ON}/I_{OFF} value was approximately 52 and due to the ultra-thin tunneling layer, the device did not achieve saturation [33]. Moreover, the characteristics of this TFFM device is suitable with the standard theory of FETs as shown in Fig. 2b and Eq. (1).

$$I_{DS} = \begin{cases} \mu_{eff} C_{ox} \frac{w}{L}\left[(V_{GS}-V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right](1+\lambda V_{DS}), \text{ if } V_{GS}-V_{TH} > V_{DS} > 0 \\ \frac{1}{2}\mu_{eff} C_{ox} \frac{w}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS}), \text{ if } V_{DS} > V_{GS}-V_{TH} > 0 \\ 0, \text{ if } V_{DS} > 0 > V_{GS}-V_{TH} \\ -\mu_{eff} C_{ox} \frac{w}{L}\left[(V_{GS}+|V_{DS}|-V_{TH})|V_{DS}| - \frac{1}{2}V_{DS}^2\right](1+\lambda |V_{DS}|), \text{ if } V_{GS}-V_{TH} > 0 > V_{DS} \\ -\frac{1}{2}\mu_{eff} C_{ox} \frac{w}{L}(V_{GS}+|V_{DS}|-V_{TH})^2(1+\lambda |V_{DS}|), \text{ if } 0 > V_{GS}-V_{TH} > V_{DS} \\ 0, \text{ if } 0 > V_{DS} > V_{GS}-V_{TH} \end{cases} \quad (1)$$

where V_{DS} is the source-drain voltage, V_{GS} is the gate-source voltage, μ_{eff} is the effective channel mobility, V_{TH} is the threshold voltage, C_{ox} is the areal capacitance of the gate stack, w and L are the width and length of the channel, and λ is the Early parameter. The more details about this equation were given in previous study [21].

The memory hysteresis characteristics of the device stems from Pt-NPs on the interface by stored electrons [34]. In Fig. 2(b), the device clearly exhibits positive hysteresis by I_{DS}-V_{DS} measurement. Memory window is important for non-volatile applications. It is clear that the larger the this parameter, the more suitable the device performances is for TFFM. To obtain V_{th}, we used I_{DS}-V_{GS} measurements were used. Fig. 2c shows the corresponding I_{DS}-V_{GS} and $(I_{DS})^{1/2}$-V_{GS} graphs at 0.5 V of V_{DS}. This V_{DS} V_{th} is calculated to be about −4.1 V due to the derivative and x-axis intercept of $(I_{DS})^{1/2}$–V_{GS} plot, where the square-law piecewise description of a FET can be expressed as in Eq. (1).

In order to better understand the flash memory characteristics, the I_{DS}–V_{GS} hysteresis was measured which is shown in Fig. 3a. The memory effect is shown under a gate voltage sweep from −5V to 5 V. The device has an obvious hysteresis from −5V to 5 V voltage sweep. The memory window difference between the forward and reverse V_{th} shift was found to be approximately 5.2 V. In our previous study [21], we used SiN_x on storage layer but its V_{th} shift was much narrower than the Pt-NPs based devices used in this study. It is clear that Pt-NPs

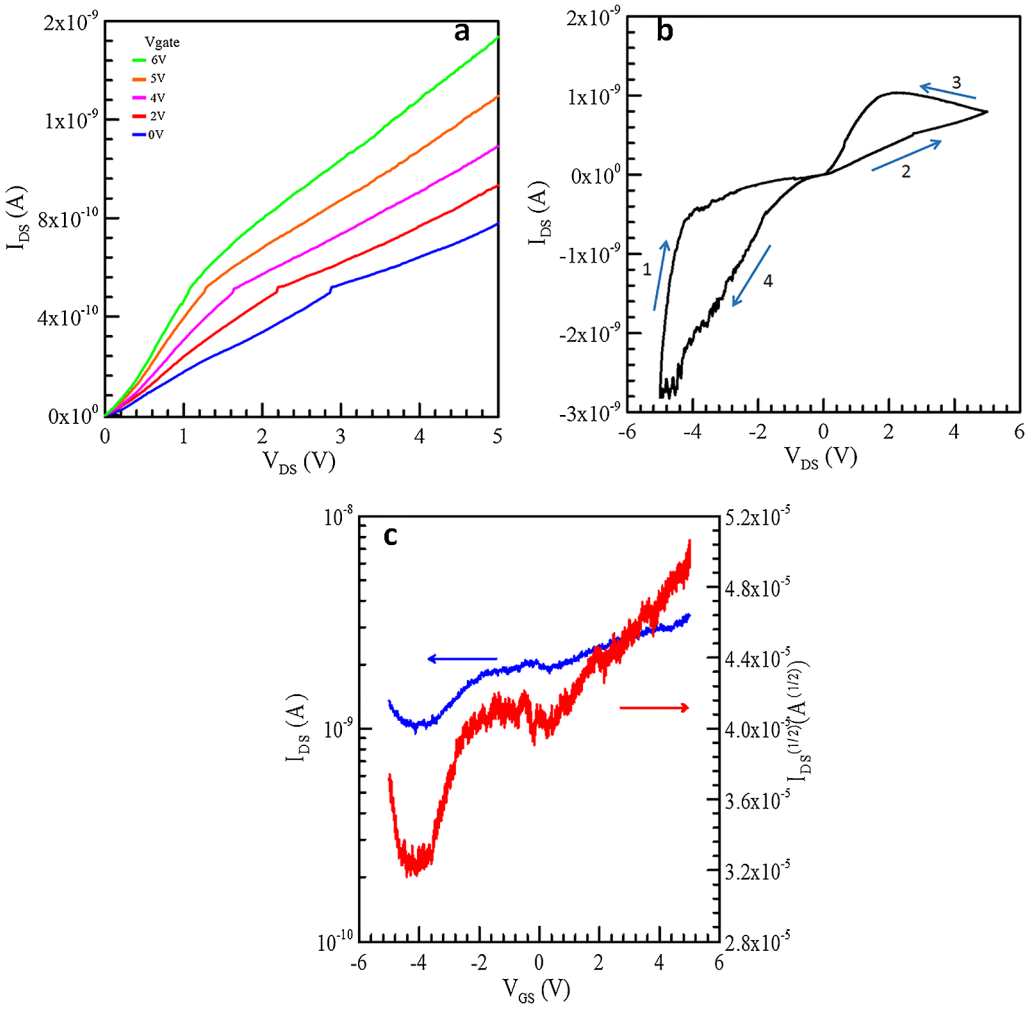

Fig. 2. (a) Classical measurement I_{DS}-V_{DS} of the TFFM sweeping V_{GS} voltage (b) Pinched hysteresis of the TFFM, (c) I_{DS}-V_{GS} measurement of the TFFM both semilog and $I_{DS}^{1/2}$-V_{GS}.

considerably attributed to the charge trapping in the oxide–channel interface [35]. Fig. 3b shows the I_{DS}–V_{GS} characterization for the exchanged V_{DS} sweep. It is shown that I_{DS} increases with V_{DS} sweep, however the memory hysteresis is merely changed around 5–5.2 V. According to these results, it can be claimed that the TFFM has very effective memory characteristics due to the highly-controlled ultra-small Pt-NPs on storage layer. Fig. 4a exhibits the transfer characteristics of the fabricated TFFM cell, sweeping the control gate voltage from −5 V to 5 V such as sinusoidal wave and afterwards in the opposite direction. When voltage difference is applied to the gate (while the source is grounded), the memory window is relatively small which is about a V_{th} shift of 0.19 V at 0.2 V, which increases with increasing gate voltage. Memory window is the maximum threshold shift during sweeping V_{GS}. The programming voltage is given in Fig. 4a with inset. The Fig. 4a is V_{GS}-time graph. As can been from Fig. 4a the applied voltage has changed with time. In this study, programming voltage was used to see the effect of the memory window at different conditions.

The large hysteresis and memory window are determined by the carriers in the Pt-NPs between the control gate and tunnel oxide layers. Finally, for the settings V_{GS} = −5V and +5 V, the memory window was found to be around 5.2 V. Moreover, the obtained V_{th} shift with Pt-NPs were measured at gate sweeping voltages at −5/+5V as can be seen in Fig. 4b. The V_{th} shift is mainly exchanged to sweeping gate voltages and charge trapping by Pt-NPs. In order to determine the charge-pulse characteristics of the device, measurements of the time-dependent behavior of the gate voltage were carried out (Fig. 4c). As can be seen from Fig. 4c, when a positive voltage pulse followed by an opposite polarity pulse was applied at V_{GS} in the range of −5/5V and under V_{DS} = 1 V, it changed with applied V_{GS} voltage. As can be seen from Fig. 4c shows that the I_{DS} values increased under applied V_{GS} voltage from −5V to 4 V. After this voltage value, the I_{DS} values show decreasing behavior. On the other hand, the I_{DS} values are mostly fixed when the applied voltage is in the saturation regime. Similarly, the I_{DS} characteristics were measured and under sweeping V_{DS} from −5 V to 5 V such as sinusoidal wave, V_{GS} = 0 V, and the obtained result is shown in Fig. 4d. Fig. 4c and d show that under bias voltage sweep, the I_{DS} values change, however they do not change under constant applied voltage. According to these results, the I_{DS} characteristics have not changed under constant voltage and this shows that the TFFM device does not allow charge passage.

In order to fully understand the device operation and Pt-NPs as a charge trapping layer, the electrostatic force microscopy (EFM) technique was utilized. In this study, Pt-NPs were deposited on a silicon surface using the ALD technique. Then, the charge states of the Pt-NPs

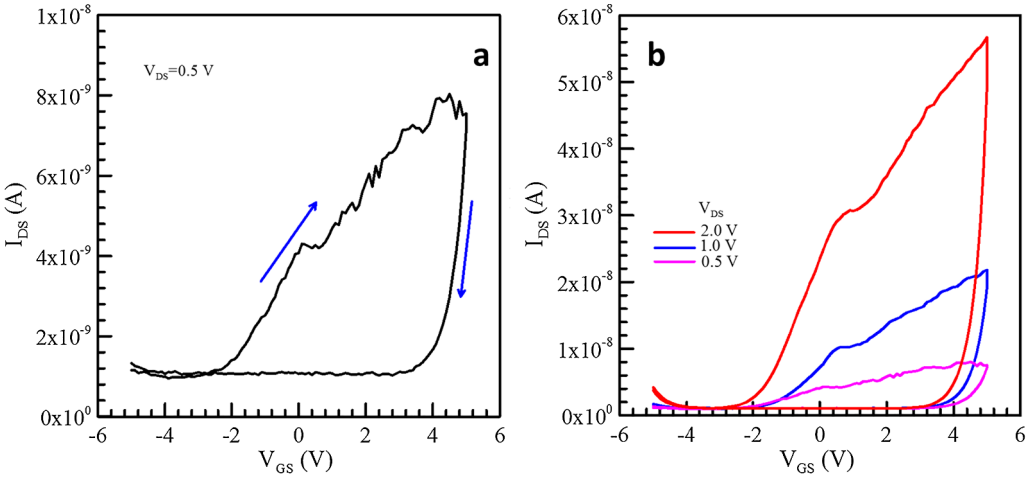

Fig. 3. (a) Measured hysteresis behavior of the I_{DS}–V_{GS} characteristics with the gate voltage sweep V_{DS} = 0, 5V, (b) I_{DS}–V_{GS} characteristics with the gate voltage sweep V_{DS} = 0, 5 V, 1.0 V, and 2.0 V.

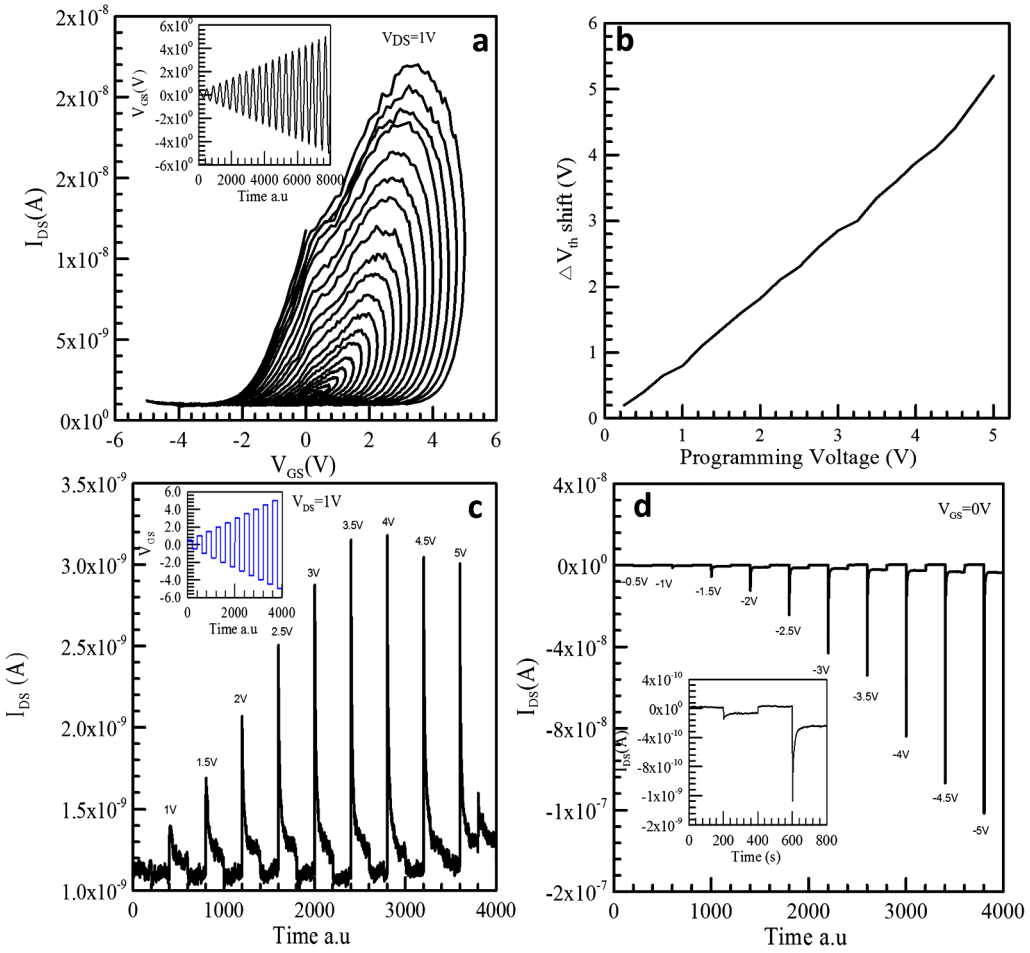

Fig. 4. (a) The characteristics of memory device I_{DS}–V_{GS} graph at V_{DS} = 1 V, (b) TFFM hysteresis versus programming voltage with Pt-NPs, (c) Charge-pulse characteristics of TFFM sweeping V_{GS} at V_{DS} = 1 V (d) Charge-pulse characteristics of TFFM sweeping V_{DS}, V_{GS} = 0 V.

surfaces were investigated using EFM tip injection. As can be seen in Fig. 5, the sample surface is charged by the EFM tip injection between −10 V and 10 V in steps of 1.25 V. Since the sample surface was scanned for surface potential mapping, the load retention time of Pt-NPs is investigated. The applied voltage and the charge injection of EFM tip are effective on the sample surface during only 1 s as shown in Fig. 5a.

After one second, the surface potential increased at some part of sample surface at room temperature. After one hour with no applied voltage, the sample surface was rescanned for potential mapping as

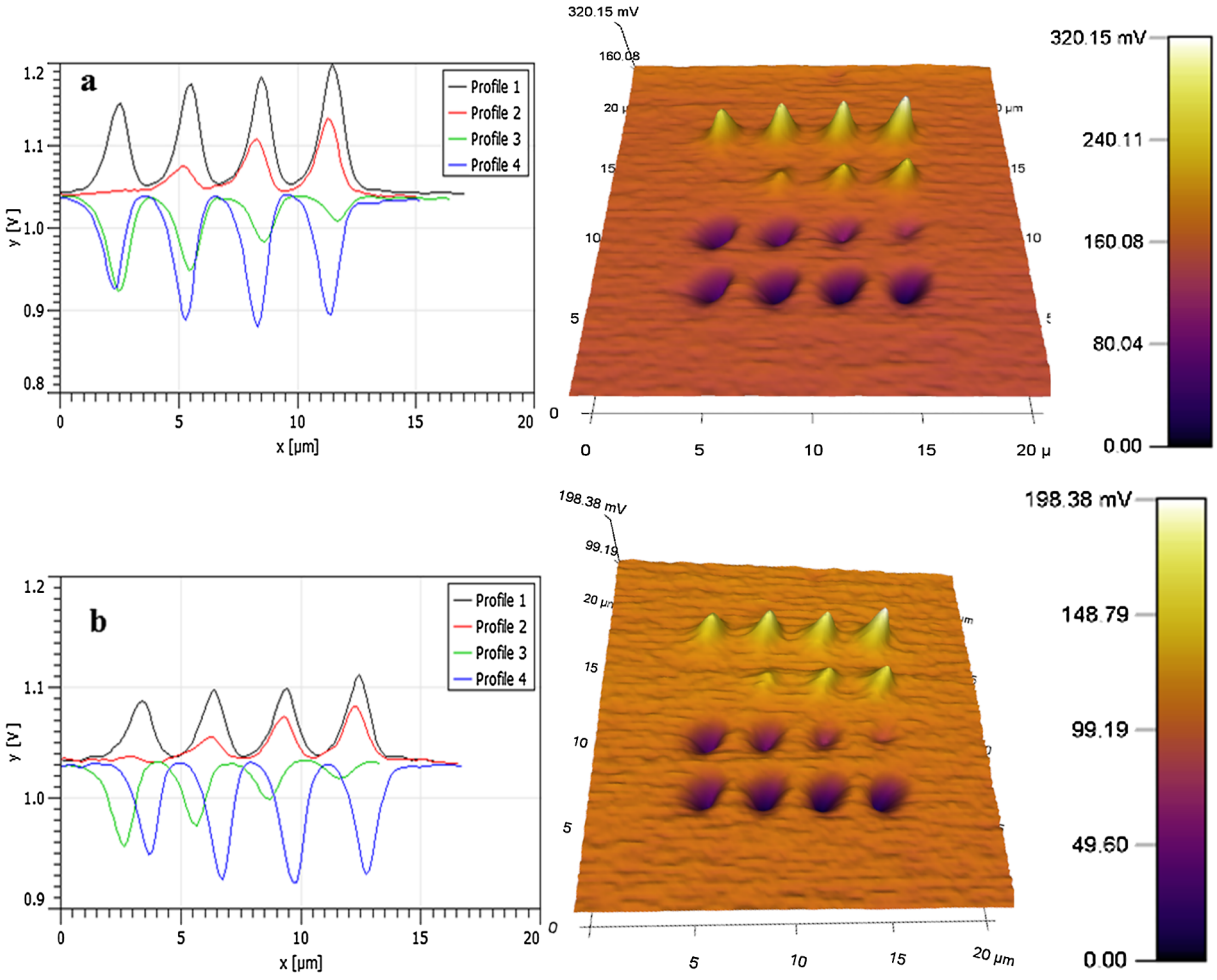

Fig. 5. (a) Applied voltage at −10 V, +10 V at 1 s in steps of 1.25 V for electron charged state (b) After 1 h waiting, surface potential measurement (c) Applied voltage at −10 V and 10 V at 0.1 s in steps of 1.25 V for electron charged state (d) Surface potential measurement after a waiting time of 1 h.

shown in Fig. 5b. Comparison of Fig. 5a and b and Fig. 6a show that the surface potential is not considerably changed. This result shows that Pt-NPs have effective charge trapping. Therefore, the Pt-NPs can be used with memory application. Then, the EFM tip charge injection is applied only for 0.1 s as shown in Fig. 5c. One hour later, the sample surface is rescanned as shown in Fig. 5d. The surface potential is different in Fig. 5c and d. However, the decrease in the rate of surface potential in Fig. 5c and d is close to each other, as can be seen Fig. 6b. As a result, a considerable charge load is observed on the sample surface. Although loaded charges on the sample surface are decreased by the time, the usage of Pt-NPs on storage layer in between control oxide and tunnel oxide layer improves memory performance according to flash memory theory. Thanks to the thin oxide layers, the charge can be trapped in between these layers for a long time since there will not be charge leakage. In addition to these layers, Pt-NPs has been improved non-volatile memory features.

4. Conclusions

Our study has demonstrated effective charge trapping by using highly dispersed and well-controlled ultra small Pt-NPs as a basis for developing high performance TFFM devices. We believe that this study is an important accomplishment which clearly shows that all device layers including the Pt-NPs can be deposited within the same ALD reactor, without any interruptions. Metallic ALD shows extreme benefits for uniformly distributed metal NPs due to very well thickness control, and large area uniformity. Memory device characterizations have been investigated such as on/off ratio, retention time, and memory window. The results show that Pt-NPs provide a larger charge trapping state due to the effective electron storage between control oxide and tunnel oxide. Importantly, Pt-NPs charge trapping are investigated with EFM tip charge injection technique. The results indicate that they are effective on storage layers due to charge trapping. The achieved impressive electrical and charge storage performance is suitable for next-generation high-performance non-volatile memory device technologies.

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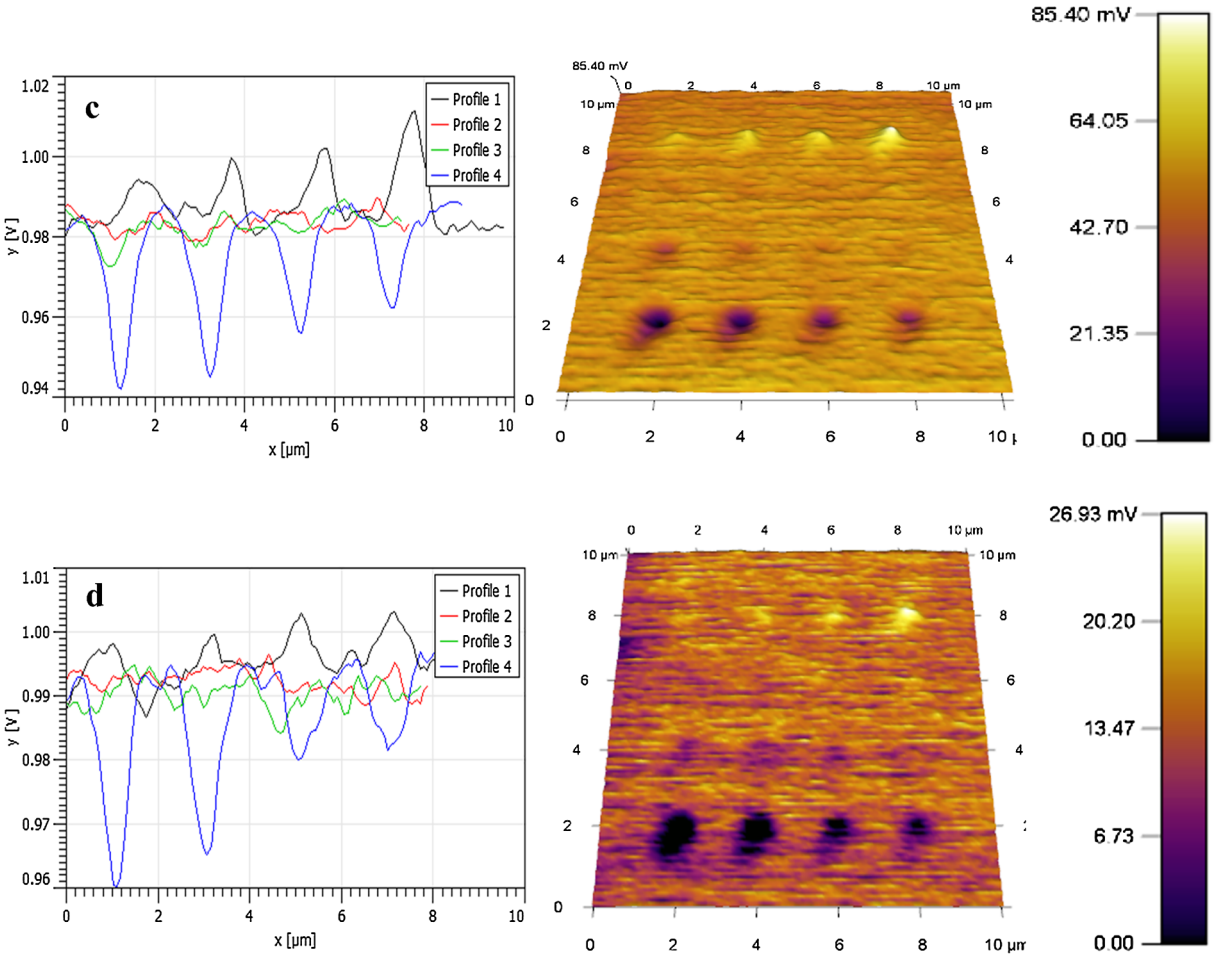

Fig. 5. (*continued*)

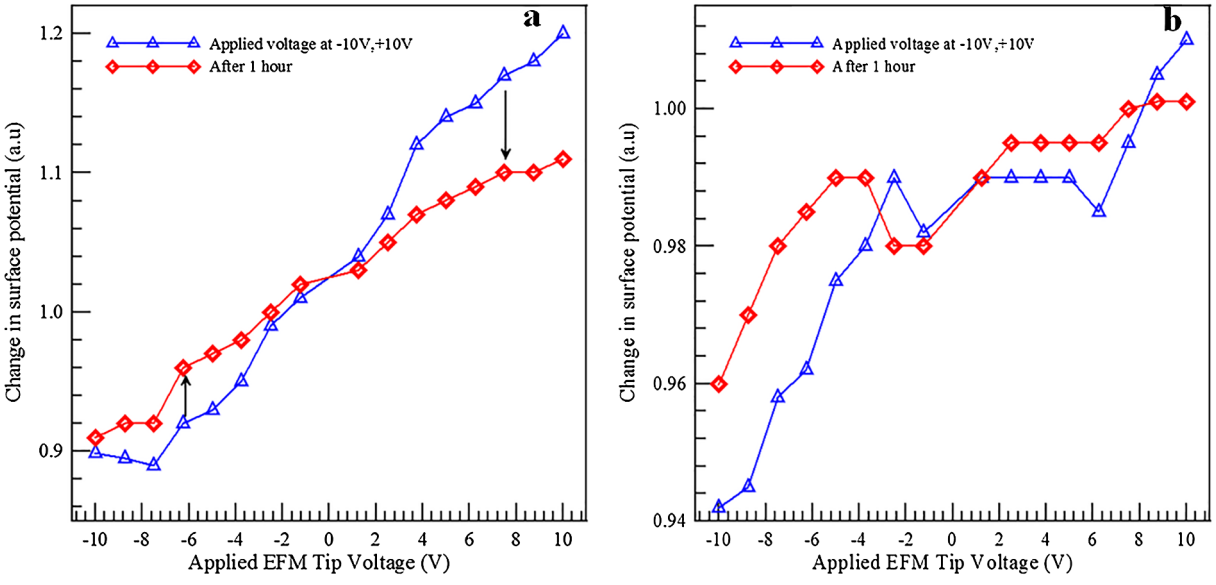

Fig. 6. Change in sample surface potential (a) 1 s EFM injection (b) 0.1 s EFM injection.

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