Fabrication of 100 nm pMOSFETs with Hybrid AFM / STM Lithography

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Introduction

Scanning probe lithography (SPL) is an emerging area of research in which the scanning tunneling microscope (STM) or atomic force microscope (AFM) is used to pattern nanometer-scale features. Four factors will dictate the viability of SPL as a patterning technology for the semiconductor industry: 1) resolution, 2) alignment accuracy, 3) reliability, and 4) throughput. We present a new SPL technique—a hybrid between the AFM and STM—to address these issues. We demonstrate its capabilities and its compatibility with semiconductor processing by fabricating a pMOSFET with an effective channel length (L_{eff}) of 100 nm and report the device characteristics.

Hybrid AFM / STM Lithography System

The Hybrid AFM / STM lithography system (Fig. 1) combines the key features of the AFM and STM by incorporating two independent feedback loops (1). One loop keeps the tip on the surface of the resist and maintains a constant force (typically 10 nN). This eliminates the problems of tip penetration into the resist while traveling over topography and minimizes the electron-beam spreading that limits the resolution of STM lithography (2). The second feedback loop maintains a constant field emission current. Without this feedback loop, any variation in resist thickness (encountered over topography) or any change in tip shape would alter the dose of electrons delivered to the resist.

Process Integration of the pMOSFETs

We used "mix and match" lithography to fabricate the pMOSFET where the gate level is patterned with Hybrid AFM / STM lithography in air. LOCOS isolation (field oxide = 450 nm) is performed followed by an arsenic channel implant (100 KeV, 1 x 10^{13} /cm^2). The gate oxide thickness is 5.7 nm and the polysilicon thickness is 100 nm. Before gate patterning, the poly is implanted with BF_2, followed by an RTA (10 sec, N_2, 1050°C) to electrically activate the dopants. The poly must be conductive for Hybrid AFM / STM lithography. 50 nm of low temperature oxide (LTO) is deposited and patterned by photolithography.

Fig 2 illustrates the gate patterning steps. Fig 2a shows the transistor structure after the gate pad formation. A negative-tone e-beam resist (SAL-601) diluted with Microposit Thinner Type A is used. The resist is nominally 60 nm thick after spin on. The resist is first imaged with the AFM in contact mode to precisely locate the position where the gate will be written. The image is then imported into the lithography software, which controls the path and the speed of the tip. The closed loop feedback used in our scanner (Park Scientific Instruments Autoprobe M5) eliminates hysteresis and enables alignment accuracy of a few nanometers. A Ti-coated silicon tip is used to expose the resist (Fig. 2b). After development (Fig 2c), the poly is etched in SF_6/Freon 115 plasma where the LTO protects the gate pad and the SAL-601 masks the gate (Fig 2d).

The resist thickness variation over the LOCOS topography caused by planarization is shown in Fig. 3a and 3b. The thickness changes abruptly from less than 30 nm to more than 90 nm within a micron. The voltage and field-emitted current during exposure are plotted in Fig 3c. The voltage required to maintain 0.05 nA ranges from 22 V to 81 V. Note that a change in voltage, $\partial V/\partial t$, generates a displacement current proportional to the capacitance between the probe and the sample. This parasitic tip-sample capacitance was reduced below 600 fF, which allowed patterning of continuous sub-100-nm features over the 180-nm of topography in a single pass. Fig. 4a is a critical dimension AFM (CD-AFM) (3) image of a 100-nm etched poly feature across the transition region from the field oxide to the active area. The scan speed was 1 μm/s and the line dose was 500 nC/cm. We have fabricated pMOSFETs with $L_{physical}$ ranging from 61 nm to 170 nm.

After gate lithography, a 35 nm oxide spacer is formed by LTO deposition and anisotropic RIE. Shallow source/drain junctions are created by BF_2 implantation (10 KeV, $1x10^{15}/cm^2$). The final processing steps are: LTO passivation, RTA (10 sec, N_2, 1050°C), furnace anneal (30 min, N_2, 800°C), contact photolithography, metallization, and a forming gas anneal. An optical micrograph of the finished structure is shown in Fig. 4b.

Device Results

The characteristics of a device with L_{eff} of 100 nm are shown in Fig 5a and 5b. A saturation current drive of 0.244 mA/μm and saturated transconductance (g_m) of 154 mS/mm are achieved at -2 V. The threshold voltage (V_t) is -0.41 V. Devices with smaller gate lengths show excessive leakage. The V_t rolloff, maximum saturated current (Id_{max},), and g_m as a function of channel length are plotted in Fig. 6a, b, and c, respectively. Transistors with gate lengths larger than 170 nm were patterned with photolithography to show the trend as a function of gate length.

Conclusions

We have demonstrated the capability of Hybrid AFM / STM lithography to fabricate pMOSFETs with $L_{physical}$ ranging from 61 nm to 170 nm and have shown the system's compatibility with semiconductor processing. Device characteristics for L_{eff} of 100 nm are presented. This new SPL technique is capable of sub-100-nm resolution and nanometer-scale alignment accuracy with reproducible patterning over significant topography. This system can be extended to high speed and multiple probe patterning and may provide an alternative technology for critical dimension patterning of 100-nm feature sizes and beyond.

References

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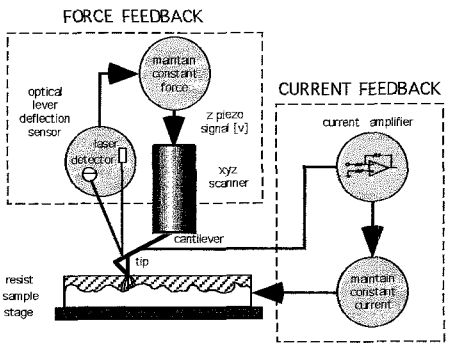


Figure 1: Schematic diagram of the Hybrid AFM / STM lithography system incorporating dual feedback loops.

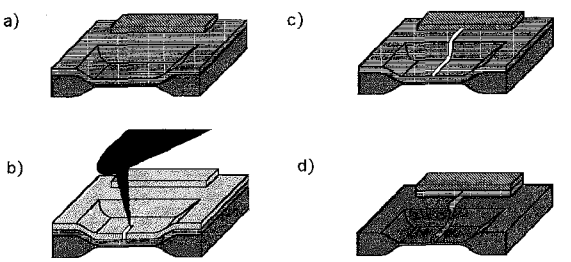


Figure 2: Schematic of the gate patterning procedure: a) LTO gate pad is photolithographically defined; b) SAL-601 resist is spun and Hybrid AFM / STM lithography is performed; c) Exposed gate remains after development; d) Poly is etched by RIE.

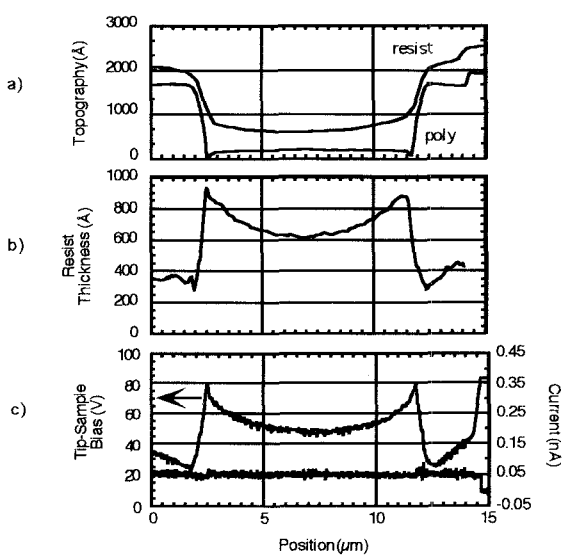
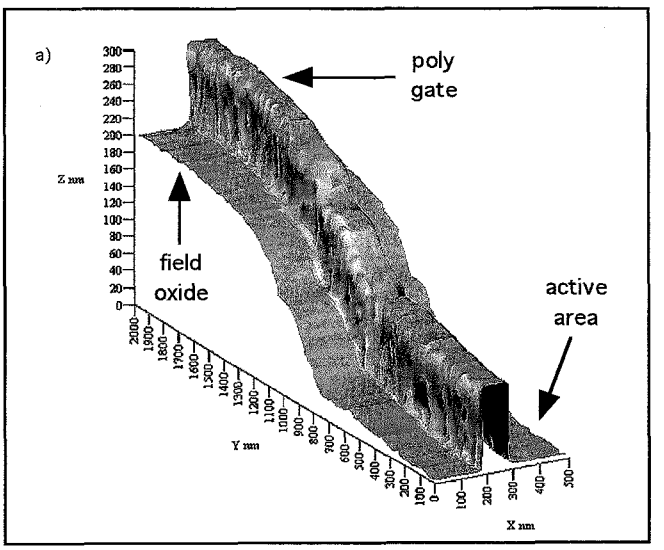


Figure 3: a) Poly and resist topography created by LOCOS isolation; b) Resist thickness variation as a function of position; c) Current and voltage during Hybrid AFM / STM lithography.



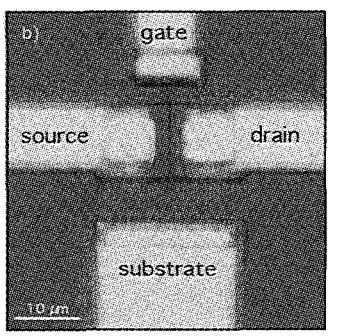


Figure 4: a) CD-AFM image of an etched 100 nm polysilicon feature over 180 nm of topography created by LOCOS isolation. The line was patterned with Hybrid AFM/STM lithography at a speed of 1 μm/s and a line dose of 500 nC/cm. b) Optical micrograph of the completed pMOSFET after metallization.

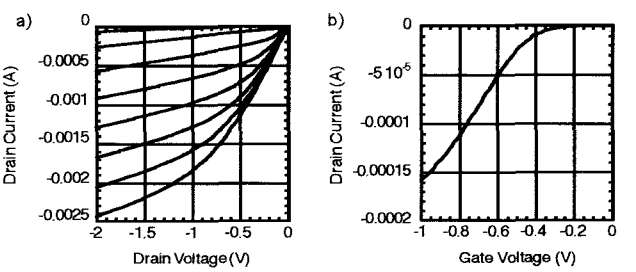


Figure 5: I-V characteristics of a 100 nm L_{eff} pMOSFET. a) I_d versus V_d where V_g was varied from 0 V to -2 V in steps of -0.25 V. b) I_d versus V_g at a V_d of -0.1 V showing V_t to be -0.41 V.

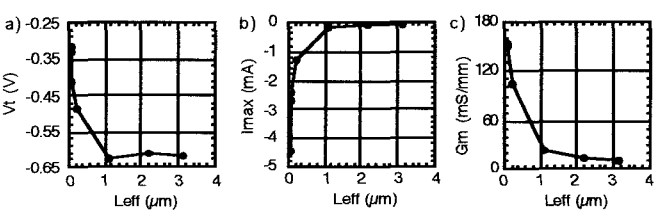


Figure 6: Electrical characteristics as a function of L_{eff} for 10-μm-wide devices: a) Threshold voltage roll-off; b) Maximum saturated current; c) Maximum saturated transconductance.

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