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TOPICAL COLLECTION: ELECTRONIC MATERIALS FOR RENEWABLE ENERGY APPLICATIONS

Electronic and Optical Properties of Atomic Layer-Deposited ZnO and TiO_2

H. ATES,[1,4] S. BOLAT,[2] F. ORUC,[2] and A.K. OKYAY[3]

1.—Department of Metallurgical and Materials Engineering, Faculty of Technology, Gazi University, 06500 Ankara, Turkey. 2.—Department of Electrical and Electronics Engineering, UNAM - National Nanotechnology Research Center, Bilkent University, 06800 Ankara, Turkey. 3.—Okyay Tech., Yenimahalle, Ankara, Turkey. 4.—e-mail: hates@gazi.edu.tr

Metal oxides are attractive for thin film optoelectronic applications. Due to their wide energy bandgaps, ZnO and TiO_2 are being investigated by many researchers. Here, we have studied the electrical and optical properties of ZnO and TiO_2 as a function of deposition and post-annealing conditions. Atomic layer deposition (ALD) is a novel thin film deposition technique where the growth conditions can be controlled down to atomic precision. ALD-grown ZnO films are shown to exhibit tunable optical absorption properties in the visible and infrared region. Furthermore, the growth temperature and post-annealing conditions of ZnO and TiO_2 affect the electrical properties which are investigated using ALD-grown metal oxide as the electron transport channel on thin film field-effect devices.

Key words: Zinc oxide, titanium oxide, atomic layer deposition, thin film transistor, semiconductor

INTRODUCTION

Thin film optoelectronics is a rapidly growing area with a demand from wearable electronics to point-of-care diagnosis and mobile health systems. The main driver, however, is still the smart devices industry which relies on screens with increasing functionality. Wide bandgap materials such as ZnO and TiO_2 typically offer low absorption in the visible spectrum. ZnO is a promising candidate for flat panel display applications thanks to its outstanding electrical and optical properties.[1–3] As-deposited ZnO naturally forms good-quality polycrystalline films even at low deposition temperatures.[4] Owing to superior bandgap properties, ZnO devices exhibit high electron mobility and are compatible with low-cost plastics as substrates thanks to low growth temperatures.[5,6] ZnO-based active matrix arrays are promising for reduced visible light sensitivity/noise, a trait not shared by a-Si counterparts.[7] In addition, the optical response of ZnO thin film transistors (TFTs) to visible photons can be tuned by a gating mechanism as was shown earlier by the authors.[8] Traditionally, ZnO has been deposited via different approaches like physical/chemical vapor deposition, solution phase deposition, molecular beam epitaxy and atomic layer deposition (ALD).[1–4,8–12] ALD is a deposition technique in which the introduction of different precursors is separated by intermittent evacuation and/or purging steps. Superior properties of ALD are precise thickness control and highly conformal deposition. TFTs made using such ALD-deposited ZnO layers exhibit on-to-off current ratios, I_{on}/I_{off}, ranging from 10 to 10^8. Reported channel mobility values are between 0.031 cm^2/V s and 56.43 cm^2/V s.[2,13–17]

TiO_2 features a relatively wide bandgap and optical transparency in the visible spectrum as well as an efficient photocatalytic effect. These remarkable characteristics make TiO_2 an attractive material for transparent thin film electronics. The first demonstration of TFTs with a thermal ALD-based TiO_2 channel semiconductor has been reported by the authors.[18] This work is a further investigation of TFT device electrical properties based on deposition and annealing conditions. The typical transistor I_{on}/

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I_{off} ratio reported for TiO_2 TFTs deposited by different techniques ranges from 10^2 to $< 5 \times 10^5$.[19–24] In this work, we present TiO_2 TFTs with I_{on}/I_{off} ratio exceeding 10^6.

MATERIALS CHARACTERIZATION

As-grown ZnO films tend to exhibit *n*-type semiconductor behavior due to crystal defects. This is attributed to oxygen vacancies and interstitial zinc, which are crystal defects. Such unintentional doping in ZnO films is not completely understood, but lower free carrier concentrations can be achieved with better control of stoichiometry. The chemical compositions of thin films grown in this work are obtained by x-ray photoelectron spectroscopy measurements (XPS; Thermo K-Alpha monochromated high-performance XPS spectrometer). XPS survey scans of ZnO films grown at different temperatures by ALD technique are plotted in Fig. 1a.

Film stoichiometry was calculated by comparing the areas under the peaks in measured survey scan data (see Tables I and II). For ZnO, film stoichiometry improves as the growth temperature decreases, which is explained by a reduced amount of oxygen vacancies and interstitial zinc.[25]

In order to determine the stoichiometry of TiO_2 films, survey scan and detailed analysis of O 1*s* spectra are used. XPS survey scan spectra of TiO_2 films annealed at different temperatures are shown in Fig. 1b. The C 1*s* spectral line, due to surface contamination, is standardized to 285.0 eV and the O 1*s* and Ti 2*p* spectra are adjusted to this energy. O 1*s* spectral lines consist of two peaks originating from O-H and O-Ti bonding states. The existence of hydroxyl groups is attributed to water vapor being used as precursor. High-resolution O 1*s* spectra are shown in Fig. 2. Two peaks that belong to O-Ti and O-H bonding states are used to fit the O 1*s* spectra. Elemental ratios obtained by fitting O 1*s* spectra are shown in Table II. Samples annealed at 475°C exhibit a Ti:O ratio closest to 1:1. This is attributed to diffusing oxygen filling vacancies at higher annealing temperatures.

Figure 3 shows XRD measurement results for ZnO and TiO_2 thin films deposited by ALD. The crystal properties of ALD-grown ZnO film are obtained from XRD (Panalytical X'pert Pro MRD) measurements. The XRD results show that ZnO films have a hexagonal wurtzite crystal structure, with no preferred orientation at low growth temperatures. At the highest growth temperature of 250°C, the intensity of the (002) peak increases significantly. The diffraction maxima occurred at (100), (002) and (101) crystallographic orientations for all ZnO films (see Fig. 3a). It is clear from the XRD results that as-deposited ZnO naturally forms good-quality polycrystalline films even at low deposition temperatures as low as 80°C. Figure 3b shows the XRD measurement results of 18-nm-thick TiO_2 films annealed at various temperatures. All

Table I. Stoichiometry of ZnO grown at different temperatures extracted from XPS analysis

T_{Growth} (°C)	Oxygen	Zinc	O/Zn
80	49.88	50.12	0.995
100	49.85	50.15	0.994
120	48.05	51.95	0.924
130	48.57	51.43	0.944
250	48.31	51.69	0.934

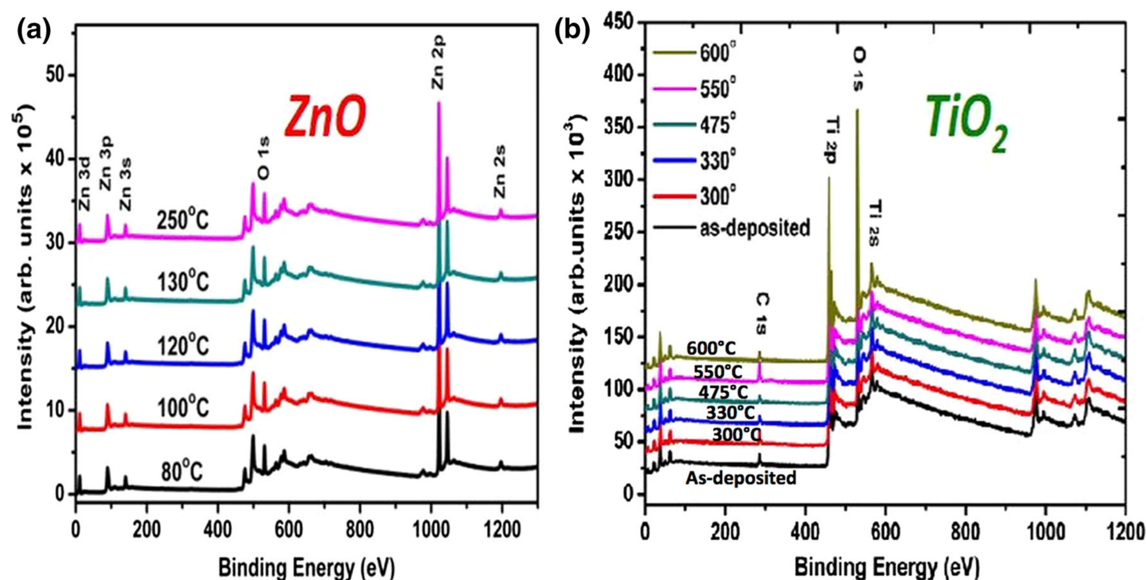

Fig. 1. XPS survey scan spectra of (a) ZnO films and (b) TiO_2 films.

diffraction peaks can be indexed to the anatase (*A*) and rutile (*R*) crystal phases of TiO_2. According to these results, the as-deposited films are in amorphous form. Anatase and rutile phases start to emerge for annealing temperatures above 300°C. Table III summarizes the anatase and rutile content in the TiO_2 films extracted using Rietveld quantitative analysis. The films are composed largely of anatase phase, and the anatase-to-rutile ratio increases with annealing temperature. The anatase phase content in annealed films is at a maximum (98.81%) at 475°C, above which the rutile content starts to increase (11.79% at 550°C). Increasing rutile content with annealing temperature is expected as the anatase-to-rutile transition in TiO_2 films is reported above 500°C in the literature.

Table II. Composition of ALD-grown titanium dioxide films annealed at various temperatures

$T_{Annealing}$ (°C)	Ti/O ratio
As-deposited	0.5546
300	0.5525
330	0.5519
475	**0.5425**
550	0.5475
600	0.5461

The ratio closest to 1:1 is shown in bold.

DEVICE FABRICATION AND CHARACTERIZATION

Starting substrates are highly conductive (c. 10 milliohm-cm) *p*-type (111) orientation silicon wafers., which were cleaned with a standard RCA clean and hydrofluoric acid HF-dip to remove native oxide on the surface. A 210-nm-thick plasma-enhanced chemical vapor deposition SiO_2 film was deposited as a field isolation layer of TFT devices. Active device areas were patterned by lithography and followed by wet etching of the SiO_2 layer using a buffered oxide etch solution (NH_4-HF, 7:1). A highly conducting Si wafer was used as the backgate electrode. The 20-nm-thick Al_2O_3 and 10-nm-thick ZnO layers were grown via ALD. The deposition temperature of the Al_2O_3 layer was 250°C. ZnO channel layers were deposited at varying temperatures (80°C, 100°C, 120°C, 130°C and 250°C). Diethylzinc (DEZn) and milli-Q water (H_2O) were used as chemical precursors. Each growth cycle consisted of a 15-ms DEZn pulse and 15-ms H_2O pulse, and purging times were adjusted according to the deposition temperature. ZnO was patterned by photolithography followed by wet etching in diluted H_2SO_4 solution to form transistor channels. An 80-

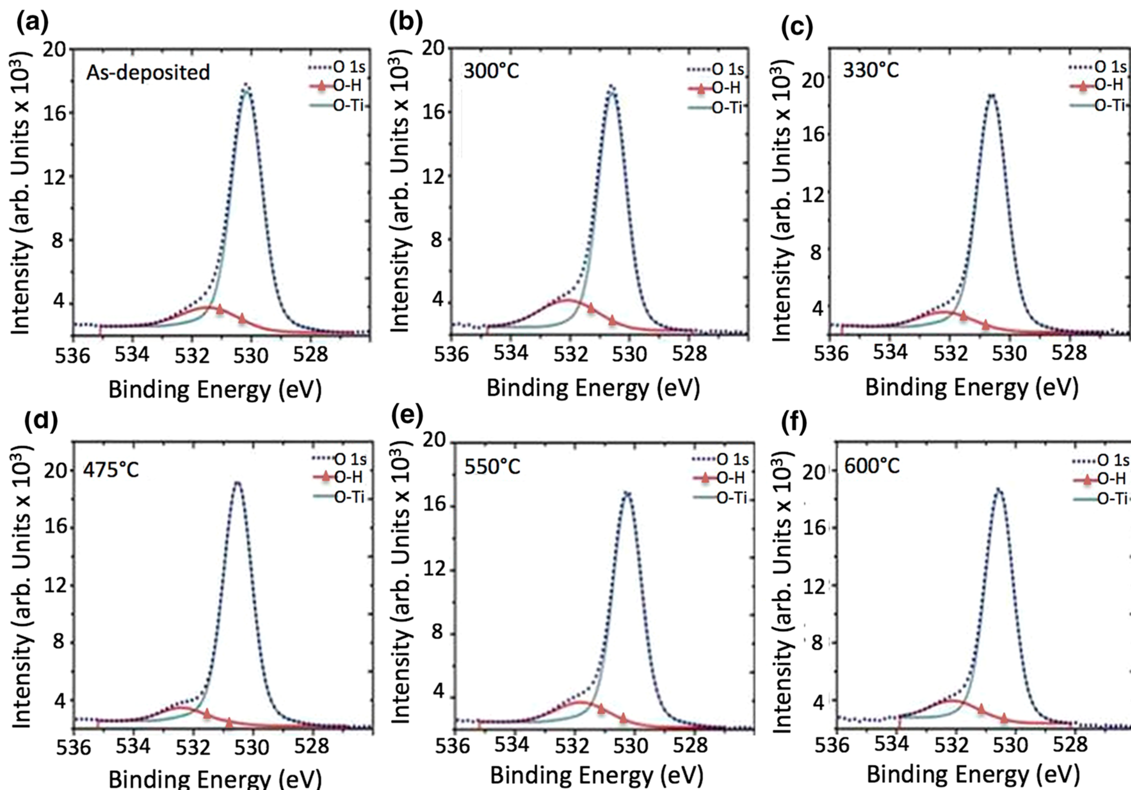

Fig. 2. Detailed O1*s* analysis of TiO_2 films (a) as-deposited and annealed at (b) 300°C, (c) 330°C, (d) 475°C, (e) 550°C, and (f) 600°C.

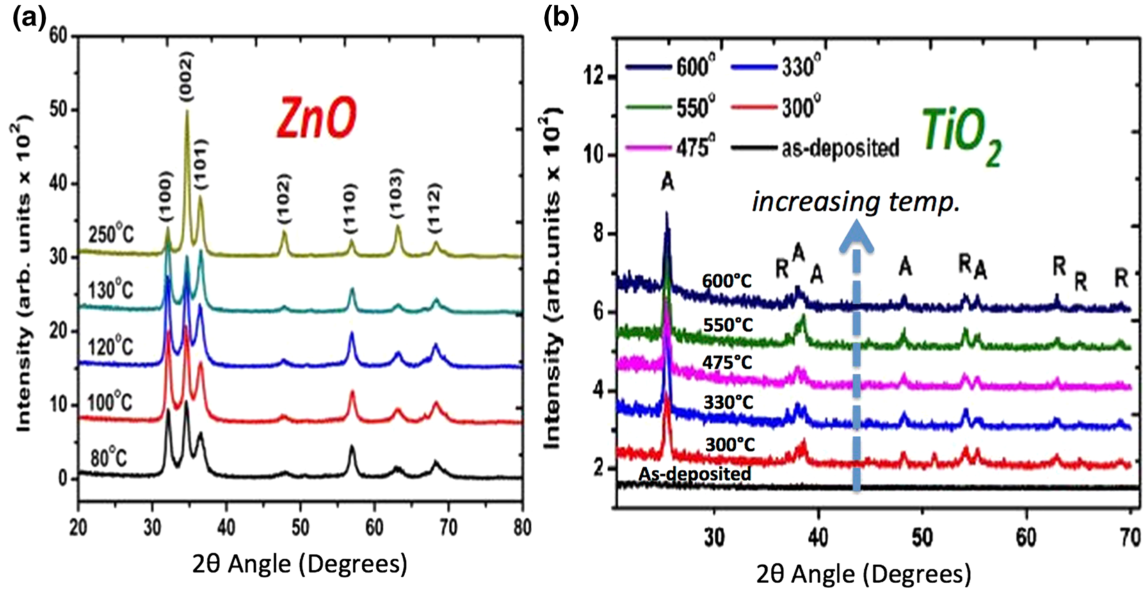

Fig. 3. Measured x-ray diffraction patterns of (a) ZnO films deposited at different temperatures and (b) TiO_2 films deposited at 150°C and post-annealed at different temperatures.

Table III. Anatase and rutile content in ALD-grown titanium dioxide films annealed at various temperatures

$T_{Annealing}$ (°C)	Anatase (%)	Rutile (%)
300	73.56	26.44
330	84.99	15.01
475	**98.81**	**1.19**
550	88.21	11.79
600	96.42	3.58

The maximum rutile content is shown in bold.

nm-thick Al layer was deposited for electrical contact pads and patterned by a lift-off technique.

TiO_2 films were deposited by ALD at 150°C using a Cambridge Nanotech, Savannah S100 reactor. The precursors for titanium and oxygen were tetrakis(dimethylamido)titanium(IV) (TDMAT) and milli-Q water (H_2O), respectively. The TDMAT precursor was kept at 75°C during the deposition. A single TiO_2 processing cycle consisted of a 100-ms TDMAT pulse and 1 min N_2 purging followed by a 15-ms H_2O pulse and 1-min N_2 purging. The extended purging periods were utilized due to the low deposition temperature. The resulting self-limiting TiO_2 film deposition rate was extracted to be 0.4 Å/cycle. All TiO_2 films in this study were deposited at 150°C and annealed subsequently at various temperatures (300°C, 330°C, 475°C, 550°C, 600°C), for 1 h in a conventional furnace in air ambient. Al_2O_3 films were deposited similar to the above. The resulting ZnO and TiO2 TFT devices are depicted and SEM images of the final devices are shown in Fig. 4.

Electrical characteristics of devices grown at 80°C are shown in Fig. 5. Transistor devices exhibit n-channel enhancement mode MOSFET characteristics as expected.

Table IV lists calculated carrier mobility, threshold voltage, subthreshold slopes, and I_{on}/I_{off} ratios of fabricated ZnO-channel transistor devices. An extrapolation method in the saturation region has been used to extract $\sqrt{I_D} - V_G$ characteristics of the devices.[25–27] Subthreshold slopes were extracted from

$$\log(I_D - V_G) \tag{1}$$

characteristics with

$$dV_G/dLog(I_D) \tag{2}$$

relation. Carrier mobility values were extracted from output $I_D - V_D$ characteristics. Oxide capacitance has been calculated using

$$C_{ox} = \varepsilon_{ox}/t_{ox} \tag{3}$$

and

$$C_{ox} = \varepsilon_0 \cdot \varepsilon_r/t_{ox} \tag{4}$$

relationships, where ε_r denotes the dielectric permittivity of ALD deposited Al_2O_3 (taken as 9 in the calculations).[28,29]

Electrical properties of TFT devices follow a similar trend as the outcome of XPS measurements. The O/Zn ratio in the film decreases with increasing deposition temperature. This results in higher effective doping (unintentional) due to defects.[30–34] At low deposition temperatures, O-H bonds passivate the defects and therefore reduce the carrier concentration and increase the I_{on}/I_{off} ratio.

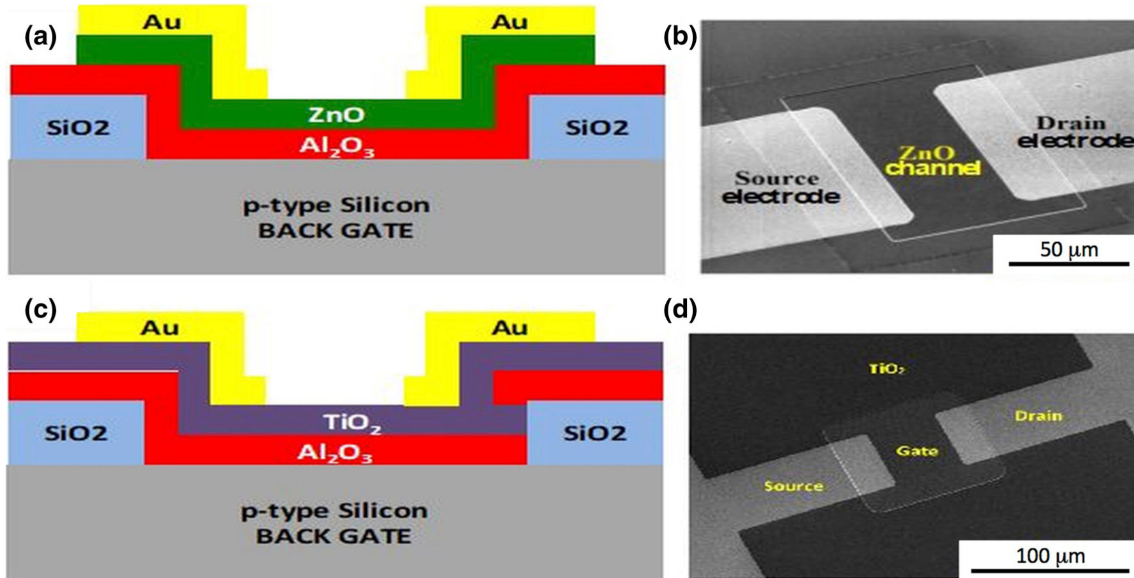

Fig. 4. Schematic of TFT device structures with (a) a ZnO channel and (c) a TiO_2 channel. Scanning electron microscope (SEM) images of a completed (b) ZnO transistor and (d) TiO_2 transistor.

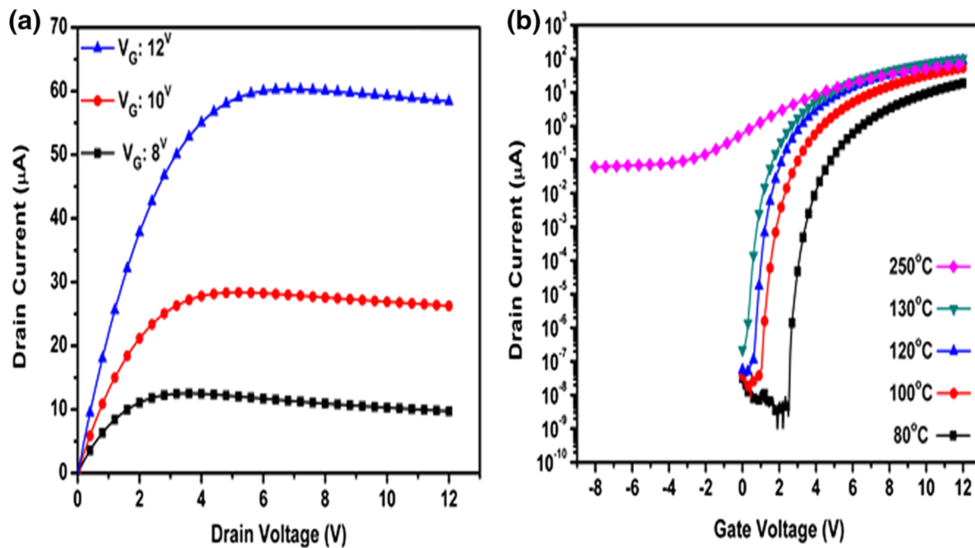

Fig. 5. (a) Measured I_D–V_{DS} characteristics of TFT devices grown at 80°C. (b) I_D–V_{GS} characteristics of devices having a ZnO channel grown at 80°C, 100°C, 120°C, 130°C, 250°C with a channel length and width of 40 μm × 50 μm, respectively.

Typical I_D–V_{DS} characteristics of a device annealed at 475°C are shown in Fig. 6a. The fabricated TFT devices exhibit n-type behavior. Figure 6b shows the subthreshold behavior of TFTs annealed at various temperatures. A maximum I_{on}/I_{off} ratio of 2.5 × 10^6 is recorded which is c. 25 times improved compared to the highest so far reported for TiO_2-channel devices. Device performance metrics are summarized in Table V. The threshold voltage has been found to be a strong function of the annealing temperature, which is a direct consequence of the effective doping in the TFT channel. The role of crystal defects as electron donors is well known in the literature for metal oxides. Films with a lower defect density are expected to exhibit a smaller effective electron concentration and therefore a larger threshold voltage. Films annealed at 475°C have the optimal Ti:O stoichiometry, hence the lowest defect density. This is in good agreement with the trend observed in the threshold voltage versus the annealing temperature, where V_{th} is the highest for TiO_2 channels annealed at 475°C.

The measured value of the sub-threshold slope is the lowest for TiO_2 channels annealed at 475°C, which is similarly attributed to low effective carrier density. Lower electron concentration in the

Table IV. Transistor characteristics with respect to ALD ZnO growth temperature

$T_{Deposition}$ (°C)	$V_{Threshold}$ (V)	I_{on}/I_{off}	Subthreshold slope (V/dec)	Mobility (cm^2/V s)
250	− 0.7	10^3	3	23
130	1.58	4.5×10^8	0.165	15.91
120	2.09	1.8×10^9	0.140	14.9
100	2.8	2×10^9	0.170	8.94
80	4.3	7.8×10^9	0.116	3.96

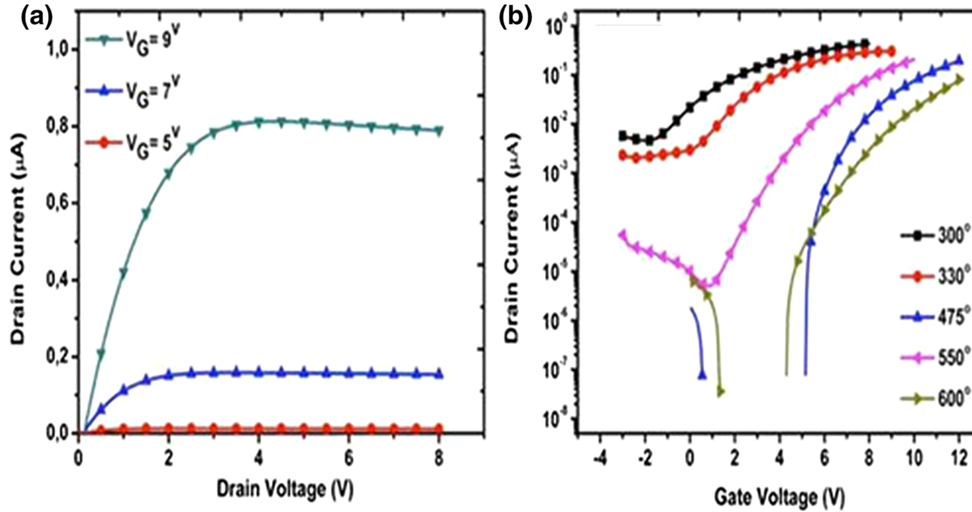

Fig. 6. (a) Typical output characteristics and (b) transfer characteristics of TiO_2 TFTs. Devices on as-deposited TiO_2 do not exhibit any gate control.

Table V. Electrical properties of ALD-grown titanium dioxide TFTs annealed at various temperatures

$T_{Deposition}$ (°C)	$V_{Threshold}$ (V)	I_{on}/I_{off}	Subthreshold slope (V/dec)	Mobility (cm^2/V s)
300	− 1.8	10^2	6.55	0.337
330	0.2	10^2	5.21	0.409
475	**6.5**	**2.5×10^6**	**0.35**	**0.672**
550	4.3	4×10^5	1.36	0.19
600	7.1	10^6	0.35	0.29

The best device performance results are shown in bold.

channel results in better gate control, which is in good agreement with the highest I_{on}/I_{off} ratio for devices annealed at 475°C. In addition, the calculated electron mobility is also the highest for films annealed at 475°C, which is attributed to reduced defect-related scattering since there are fewer defects in the film. In addition, as supporting evidence for these device performance results, anatase TiO_2 is reported to have a lower electron effective mass and inherently higher electron mobility when compared to its rutile counterpart. XRD results show that films annealed at 475°C have the highest anatase content which also contributes to higher electron mobility.

CONCLUSION

We present the fabrication and characteristics of bottom-gate ZnO and TiO_2 thin film transistors and the effect of ALD growth temperature and post-annealing conditions on electrical properties of the channel layer. The free carrier concentration is strongly influenced by the growth temperature in ZnO films. In turn, the electrical properties of TFTs are strongly influenced by the ZnO deposition temperature. As-deposited TiO_2 films grown by thermal ALD are shown to be amorphous. A post-deposition annealing step can be used to control the electrical properties of ALD-deposited TiO_2 layers. Annealed TiO_2 films transform into a

polycrystalline form containing mixed phases of anatase and rutile forms. Electrical properties of the transistors built on ALD-deposited TiO_2 films improve upon the post-growth annealing process. TiO_2 channel layers annealed at 475°C feature predominantly anatase phase, and devices fabricated using these layers exhibit the optimum electrical device characteristics.

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