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# Two-step passivation for enhanced InGaN/GaN light emitting diodes with step graded electron injectors



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### ABSTRACT

Enhancement of InGaN/GaN based light emitting diode performance with step graded electron injectors through a two-step passivation is reported. Perimeter passivation of LED dies with SiO<sub>2</sub> immediately following ICP mesa etch in addition to conventional Si<sub>3</sub>N<sub>4</sub> dielectric surface passivation leads to decrease in the reverse bias leakage current by a factor of two as well as a decrease in the shunt current under forward bias by an order of magnitude. Mitigation of the leakage currents owing to the two-step passivation leads to significant increase in the radiant intensity of LEDs by more than a factor of two compared to the conventional single step surface passivation. Further, micro-dome patterned surface of Si<sub>3</sub>N<sub>4</sub> passivation layer allow enhanced light extraction from LEDs.

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#### 1. Introduction

Light emitting diodes (LEDs) based on InGaN/GaN semiconductor structures are widely used as light sources for applications such as general lighting (both indoor and outdoor), backlighting of the display screens, and outdoor LED displays [1,2]. Standard blue LED design is featured by multiple InGaN quantum wells (QWs) separated by GaN or InGaN with relatively lower In content barrier regions, all sandwiched between highly doped n- and p-type GaN layers [1,2]. Use of native substrates for epitaxial growth of GaN films as well as device structures is very limited because of many technical problems for growing bulk GaN resulting in high cost [3]. The use of foreign substrates with lattice parameters and thermal expansion coefficients different from GaN necessitates approaches to minimize density of extended and point defects that form due to lattice and thermal mismatch and result in, among other disadvantages, increased leakage currents. The density of threading dislocations in GaN-based device structures grown by metalorganic chemical vapor deposition (MOCVD) technique on sapphire substrates can be kept below  $10^8 \text{ cm}^{-3}$  using special techniques such as epitaxial lateral overgrowth (ELO) through in situ deposited Si<sub>3</sub>N<sub>4</sub> nanoporous mask (frequently dubbed as nano-ELO technique) [4,5]. Despite such high dislocation densities,

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https://doi.org/10.1016/j.spmi.2017.11.050 0749-6036/© 2017 Elsevier Ltd. All rights reserved. InGaN/GaN heterostructures exhibit high optical efficiency due to suppression of nonradiative recombination by either localization due to In-rich nanoclusters [6–8] or blockage of carriers from reaching dislocations due to potential barriers formed around V-shaped pits [9,10].

Despite significant industrial progress in InGaN/GaN LED fabrication, problems associated with elimination of leakage currents as well as increasing light output from LED dies still require close attention. Defects and surface states on the surfaces and sidewalls of mesas in light emitters contribute to leakage currents thus degrading the injection efficiency [1]. Elimination of these leakage currents requires a carefully considered complex strategy involving growth and fabrication procedures and LED die design, among others. On the growth side, the strain in epitaxial wafers should be reduced. Otherwise, strain relaxation through defect generation degrades the material quality. The optimum LED die design intended to prevent leakage through surface states at the edge of the LED dies should take into account the limited current spreading due to low hole concentration and the associated low mobility in p-GaN. Thus, the physical distance from the contact pad to the edge of surface emitting LEDs should not be smaller than the current transfer length to prevent current leakage through surface states [11]. Finally, the mitigation of leakage through surface states requires an appropriate passivation of LED dies with dielectric layers that decreases non-radiative recombination and thus results in increased radiative efficiency. For passivation of LEDs based on InGaN/GaN MOWs Al<sub>2</sub>O<sub>3</sub> [12–15], SiO<sub>2</sub> [13–16], Si<sub>3</sub>N<sub>4</sub> [17], and SiON<sub>x</sub> [18,19] have been used. A common passivation approach is a thin layer of dielectric coating covering the entire LED die surface followed by opening windows for contact pads after metalization [12–15,17–20]. Deposition of the aforementioned dielectric layer generally can be done by plasmaenhanced chemical vapor deposition (PECVD) [13,14,17–19], sputtering [12] or atomic layer deposition (ALD) [13]. Passivation is particularly important for elimination of shortening during the packaging step which is characteristic to lateral configuration of InGaN/GaN LED dies on sapphire. These shortening can appear due to the small distance between contact pads to n- and p-type layers particularly in the common interdigitated configuration of electrodes used for high power LEDs [11,21-23].

The damage on the sidewalls of LED mesas (for lateral device configuration) fabricated by inductively coupled plasma (ICP) etching should also be taken into account. Mesa sidewalls can easily be contaminated or adsorb moisture when exposed to air [17]. It is, therefore, important to passivate the surfaces immediately after etching. This may not be an easy task for high power LEDs because of the necessity to use interdigitated configuration for LED dies employed to maximize their effective area [11,21–23].

Passivation of LED dies is also intimately related to the light extraction efficiency. The high refractive index of GaN, 2.25 [24], leads to a small escape cone. Specifically, the critical angle for total internal reflection at the GaN-air interface is equal to 26.4°. Any outward radiation outside the cone with this angle would suffer total internal reflection, which must be encountered in order to collect more of the emission emanating within the solid. In the case of flat GaN surface, only 5.2% of generated light will be emitted into air [1]. One way to improve the extraction efficiency and thus the external quantum efficiency is to roughen the GaN surface. This approach is used effectively in GaAs based LEDs utilizing plasma treatments [25]. In the case of GaN based LEDs, plasma based surface roughening is not suitable because it degrades electrical properties of p-GaN due to plasma induced damage [26]. The plasma damage manifests itself as generation of point defects, primarily nitrogen vacancies, which act as donors [27,28]. There are other ways to improve light output such as using encapsulants with high refractive indices [29,30], patterning of current spreading layer surface [21,31], using patterned sapphire substrates [13], patterning of passivation layer surface [13,14], and employing antireflection optical coatings and two-dimensional photonic crystals [12,32]. One of the practical ways for light extraction improvement of front emitting LED chip that does not degrade its electrical properties is patterning of the passivation layer [13,14].

A bilayer passivation technology with  $Al_2O_3/SiO_2$  for InGaN/GaN based LEDs was proposed in papers [13–15]. Use of ALD grown  $Al_2O_3$  as the first layer was shown to decrease leakage current by two orders of magnitude as compared to PECVD grown SiO<sub>2</sub>. Patterned PECVD deposited SiO<sub>2</sub> layer on top of  $Al_2O_3$  was used for increasing light output as material with intermediate refractive index between air and  $Al_2O_3$  [13–15]. This passivation scheme has some drawbacks, because the total internal reflection with  $Al_2O_3$  is relatively high due the fact that its refractive index is much lower than that of GaN (1.75 vs 2.25 for GaN). Silicon dioxide also looks not a good choice as its refractive index is 1.55 [33]. The difference between the refractive indices of GaN and the passivation material causes light entrapment at the layer interfaces. Light entrapping because of high refractive index of top passivation layer can be much weakened with the help of passivation layer patterning.

Using Si<sub>3</sub>N<sub>4</sub> for top emitting InGaN/GaN LEDs may be preferred because of its relatively high refractive index of 2.04 [33], which is almost equal to that of ITO (n = 2), that is commonly used as a current spreading layer on the top of p-GaN in front emitting LED chips. In such a configuration, the critical angle between ITO and Si<sub>3</sub>N<sub>4</sub> will approach 90°. In the case of Al<sub>2</sub>O<sub>3</sub> at the interface, the ITO-Al<sub>2</sub>O<sub>3</sub> critical angle is only 61.6°. We therefore conclude that use of Si<sub>3</sub>N<sub>4</sub> as a passivation layer should minimize light loss at the interface between ITO and Si<sub>3</sub>N<sub>4</sub> as compared to the ITO-Al<sub>2</sub>O<sub>3</sub> case.

In this paper, we report on the effects of two-step passivation on the electrical and light output characteristics of InGaN based front emitting LEDs. Passivation layers investigated included SiO<sub>2</sub> perimeter passivation of LED dies immediately after mesa etching and Si<sub>3</sub>N<sub>4</sub> surface LED passivation with micro-dome fabrication on its surface to improve light extraction.

#### 2. Experimental

InGaN MQW based LED structures grown by metalorganic chemical vapor deposition (MOCVD) on sapphire were used in this work. Epitaxial layers consist of 10 µm undoped GaN grown by in situ nano-ELO technique, followed by a 4 µm thick n-



Fig. 1. Crosscut fragment of interdigitated LED B structure used in this work.

GaN  $(3 \cdot 10^{18} \text{ cm}^{-3})$ , a 60 nm  $\text{In}_{0.01}$ GaN stress compensation layer, a 7 step graded  $\text{In}_x\text{Ga}_{1-x}$ N (x = 0.04 to 0.1 with 3 nm thickness for each step) electron injector layer, 6 × 2 nm  $\text{In}_{0.15}\text{Ga}_{0.85}$ N quantum wells separated by 3 nm-thick  $\text{In}_{0.06}\text{Ga}_{0.94}$ N barriers, and finally a 100 nm p-GaN ( $4 \cdot 10^{17} \text{ cm}^{-3}$ ) (see Fig. 1). The step graded electron injector (SGEI) is included in the structure to help cool the electrons prior to injection into the MQW region [34,35] and thus mitigate the electron overflow. Square mesas of ~1 mm<sup>2</sup> were formed by ICP etching (BCl<sub>3</sub>:Cl<sub>2</sub>). LEDs had interdigitated electrode patterns with distances from contact pads to the edge of etched mesa equal to 50, 100, 150 and 200 µm. Ohmic contacts to n-GaN were formed using a Ti(30 nm)/Al(50 nm)/TiB<sub>2</sub>(50 nm)/Au(70 nm) stack which was subjected to rapid thermal annealing (RTA) in N<sub>2</sub> at T = 800 °C for 30 s. For current spreading layer and ohmic contact to p-GaN, a Ni(5 nm)/Au(5 nm)/ITO(120 nm) stack was used with Ti(30 nm)/Au(50 nm) contact pads to ITO. Two samples denoted as LED A and LED B were included in this study. No passivation was employed for LED A, whereas the perimeter of LED B was passivated with PECVD-deposited SiO<sub>2</sub> of 250 nm thickness immediately after ICP mesa etching.

Both samples were then coated with 250 nm  $Si_3N_4$  deposited by the PECVD technique. For light extraction improvement, micro-domes were formed with the aid of UV lithography followed by etching in buffered oxide etchant (BOE). A schematic of this structure is shown in Fig. 1. Windows in  $Si_3N_4$  passivation layer were opened to gain access just to the contact pads on the n-GaN and contact pads on the current spreading ITO layers.

Electrical properties of fabricated LED dies were measured using a Keithley 2430 source and an HP 4142B monitor unit. Optical properties were measured by Instrument Systems spectrometer CAS 140CT. Ohmic contact resistivities were measured by using transmission line method (TLM) with linear and circular contact pad geometries [36]. For linear TLM measurements,  $75 \times 450 \ \mu\text{m}^2$  contact pads were used with separations of 20, 40, 60, 80, 100 and 150  $\ \mu\text{m}$ . For circular TLM measurements inner contact pads had diameters of 50, 80, 100 and 150  $\ \mu\text{m}$  with a constant ratio between outer and inner contact diameters of 2 [36]. The micro-dome profile was measured by DekTak XT Stylus Profiler.

#### 3. Passivation layer

The consideration for employing a passivation layer for front (top) emitting type LEDs is to address the reflections that occur at interfaces, including the layer/ambient interface, resulting in entrapping of light. In a front emitting type LED structure, there are several layers that need to be taken into account, starting with p-GaN layer. Light from GaN penetrates

through ITO layer followed by insulator passivation layer. Reflection coefficient on the two media interface for s- and ppolarized light ( $P_s$  and  $P_p$ , respectively) can be calculated by Ref. [37]:

$$P_{s} = \left| \frac{n_{1} \cos \theta_{i} - n_{2} \sqrt{1 - \left(\frac{n_{1}}{n_{2}} \sin \theta_{i}\right)^{2}}}{n_{1} \cos \theta_{i} + n_{2} \sqrt{1 - \left(\frac{n_{1}}{n_{2}} \sin \theta_{i}\right)^{2}}} \right|^{2};$$
(1)  
$$P_{p} = \left| \frac{n_{1} \sqrt{1 - \left(\frac{n_{1}}{n_{2}} \sin \theta_{i}\right)^{2}} - n_{2} \cos \theta_{i}}{n_{1} \sqrt{1 - \left(\frac{n_{1}}{n_{2}} \sin \theta_{i}\right)^{2}} + n_{2} \cos \theta_{i}} \right|^{2}.$$
(2)

where  $n_1$  and  $n_2$  are refractive indices of source and target media, respectively, and  $\theta_i$  is the angle of incidence. We can assume that light in LED is generated with circular polarization and has uniform distribution, so resulting reflection coefficient can be calculated by:

$$P = \frac{1}{2} \left( P_s + P_p \right). \tag{3}$$

To determine the best passivation layer, light propagation from GaN layer to the insulator must be considered first. As in this work, front emitting LEDs are usually coated with ITO [38], which has a refractive index of 2 compared to 2.25 for GaN. The most common choices of passivation layers on ITO are SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub> and Si<sub>3</sub>N<sub>4</sub> with refractive indices of 1.55, 1.77 and 2.04, respectively [33]. As the goal here is to have the highest light output through the insulator layer to environment, internal reflections at ITO/passivation and passivation layer/ambient interfaces should be minimized. In an effort to understand the role of reflectance on both interfaces, we conducted calculations by using equations (1)–(3). The results of these calculations are plotted in Fig. 2 in the form of reflection coefficients vs. the incident angle. The lowest reflection coefficient for light propagating from ITO layer is observed for Si<sub>3</sub>N<sub>4</sub> and the highest for Si<sub>2</sub>O as expected. The lowest reflection coefficient for the light propagating from passivation layer to air is observed for Si<sub>2</sub>O and the highest for Si<sub>3</sub>N<sub>4</sub>.

To evaluate reflected and transmitted light, we integrated dependences of reflection coefficients on the incident angle (Table 1) and assumed for convenience that the light absorption in considered layers is negligible.

One can see that after transmitting light through two interfaces, the highest percentage of the transmitted light equals 28% in the case of  $Si_3N_4$  usage. In the case of  $SiO_2$  passivation, the transmitted light is the smallest at 21% because of high light reflectance on the ITO – passivation layer interface. Use of  $Al_2O_3$  for passivation will allow transmission of 23% of light. Also we note that the amount of light transmitted through the passivation layer to air can be increased by modifying passivation layer surface by micro-dome patterning, photonic crystal deposition, or surface roughening [13,14,32]. The results of these

100 90 Reflection coefficient (%) to Air 80 from ITO 70 Si 60 Al<sub>2</sub>O 50 Si<sub>2</sub>O 40 30 20 10 0 20 50 0 10 30 40 60 70 80 90 Incidence angle (°)

Fig. 2. Internal reflection coefficients of light on incidence angle at the interface between ITO and either of Si<sub>3</sub>N<sub>4</sub>, Al<sub>2</sub>O<sub>3</sub> or SiO<sub>2</sub> and at the interface between these insulators and ambient assuming a GaN/ITO/insulator/air configuration.

Table 1	
Internal reflectance and transmittance during propagation from IT	O layer into the following insulators of LED chip

	n	P <sub>1</sub> (%)	P <sub>2</sub> (%)	T (%)
Si <sub>3</sub> N <sub>4</sub>	2.05	3.7	71.0	28.0
Al <sub>2</sub> O <sub>3</sub>	1.77	33.0	66.0	23.0
SiO <sub>2</sub>	1.55	48.0	59.0	21.0

n – refractive index,  $P_1$  – reflectance for light propagation from ITO layer to passivation layer,  $P_2$  – reflectance for light propagation from passivation layer to air, T – light transmitted to the air ambient from ITO layer through passivation layer of LED chip.



Fig. 3. IV and radiant intensities of LED dies without (LED A) (a) and with the SiO<sub>2</sub> perimeter passivation layer (LED B) (b). Equivalent LED circuit is shown in the inset.

# Table 2

<i>d</i> , (μm)	$R_s(\Omega)$			$R_{s1}(\Omega)$	$R_{s1}(\Omega)$			
	LED A	LED A1	LED B	LED B1	LED A	LED A1	LED B	LED B1
50	7.0	7.6	9.6	10.9	10.0	11.1	10.0	11.3
100	6.6	8.5	10.2	10.9	9.4	10.8	10.9	11.3
150	7.25	8.3	11.7	10.2	11.4	11.2	10.2	10.5
200	10.8	13.1	15.8	16.4	18.3	20	16.4	17.7

Series resistances of LEDs before (LED A and LED B) and after  $Si_3N_4$  micro-dome fabrication (LED A1 and LED B1).

calculations clearly show that  $Si_3N_4$  is the most appropriate material for passivation of front emitting InGaN/GaN based LEDs with ITO current spreading layer.

#### 4. Experimental results and discussion

Ohmic contact resistivity was characterized before the investigation of electrical properties of fabricated LEDs. We note that resistance of the contacts does not depend on perimeter passivation of LED dies, as was expected. The resistivity of Ti/Al/TiB<sub>2</sub>/Au ohmic contact to n-GaN layer was equal to  $3 \cdot 10^{-5} \Omega \cdot \text{cm}^2$ , and resistivity of ITO/Au/Ni/p-GaN ohmic contact was  $1.5 \cdot 10^{-2} \Omega \cdot \text{cm}^2$ . In Fig. 3, one can see current-voltage characteristics (I-V) and radiant intensities of LED dies with and without the SiO<sub>2</sub> passivation layer. These results represent the average values from 9 different measurements for each die configuration with different distance between the contact pad to p-type contact and the edge of p-n junction. The turn-on voltage for both LEDs A and B is equal to 3.5 V. Dynamic series resistance ( $R_S$ ) values for LED A without perimeter passivation extracted from the slope of I-V characteristics (Fig. 3) above the turn-on voltage are 7, 6.6, 7.25 and 10.8  $\Omega$  for dies with distances 50, 100, 150 and 200  $\mu$ m distances are higher and are 9.6, 10.2, 11.7 and 15.8  $\Omega$  for 50, 100, 150 and 200  $\mu$ m distance, respectively (Table 2).

LEDs exhibit a small but non-negligible current flow at voltages smaller than the turn-on voltage,  $V_t$  (Fig. 3). The effect of leakage current on LED I-V characteristics can be observed by practically non-zero current under reverse bias or by practically non-zero shunt current at voltages lower than the turn-on voltage [1]. A non-ideal LED can be modeled by an equivalent circuit presented in Fig. 3 inset where  $R_{s1}$  is the actual series resistance of the diode and  $R_p$  is the parallel resistance. The parallel resistance characterizes nonradiative current path that shunts the LED under test [1]. Series resistance that can be calculated from the slope of IV at voltages higher than turn-on voltage will be underestimated because of shunting current effect and we can call it dynamic series resistance. The parallel dynamic resistance  $R_p$  can be calculated from the slope of the I-V curve in the region where  $V < V_t$ . To obtain the actual LED series resistance one can use the following equation:

$$R_{s1} = \frac{R_p R_s}{R_p - R_s}.$$
(4)

Calculated  $R_p$  values are 23.2, 22.3, 19.8 and 26.4  $\Omega$  for LED A and 228, 146, 161 and 140  $\Omega$  for LED B dies with distance, d, being 50, 100, 150 and 200  $\mu$ m, respectively (Table 2). As one can see, the parallel resistance for LEDs with SiO<sub>2</sub> perimeter passivation (LED B) is one order magnitude higher than that for un-passivated LEDs (LED A). The observed leakage is evaluated by noting that the shunt current is substantially decreased by employing SiO<sub>2</sub> PECVD perimeter passivation.

After subtraction of the calculated parallel resistance, we can extract the actual device series resistance that will be higher than the dynamic series resistance calculated from the slopes of I-V characteristics for LEDs A and B. As shown in Table 2

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Leakage properties of LEDs without (LED A and LED A1) and with (LED B and LED B1) perimeter  $SiO_2$  passivation before (LED A and LED B) and after  $Si_3N_4$  micro-dome fabrication (LED A1 and LED B1).

<i>d</i> , (μm)	$R_p(\Omega)$	$R_p(\Omega)$				<i>I</i> <sub><i>l</i></sub> (at –1 V) (mA)	
	LED A	LED A1	LED B	LED B1	LED A	LED B	
50	23.2	40.3	228	333	0.60	0.04	
100	22.3	40.5	146	397	0.04	0.04	
150	19.8	32.2	161	412	0.07	0.05	
200	26.4	37.8	140	239	0.50	0.05	

actual series resistance becomes comparable for LEDs A and B. These data indicate that the main difference in their electrical properties originates from different leakage currents. This conclusion is confirmed by smaller leakage current for LED B than that for LED A measured at -1 V (Table 3).

Passivation of both LEDs was done by using PECVD-grown  $Si_3N_4$  layer. Windows were opened to get access to metal contact pads. Metal fingers deposited for realizing of interdigitated configuration of LED die were covered with  $Si_3N_4$ . An image obtained from an optical microscope is shown in Fig. 4 inset. The micro-domes, separated by 2  $\mu$ m, have in-plane diameters of 2  $\mu$ m and 130 nm average height.

Dynamic series resistances of LEDs A and B measured as the slopes of I-V characteristics at voltages higher than the turnon voltage increased after passivation. Passivation increased the parallel resistances of LEDs A and B by a factor of 2 (see Table 3) which resulted in an increase in the dynamic series resistance  $R_s$ . The actual series resistance extracted using the parallel resistance value turns out to be unaffected by passivation. We note that a significant decrease in shunt current is the main



Fig. 4. IV and radiant intensities of LED chips with Si<sub>3</sub>N<sub>4</sub> micro-domes without (LED A1) (a) and with the SiO<sub>2</sub> passivation layer (LED B1) (b). Optical microscope picture of LED die surface covered with Si<sub>3</sub>N<sub>4</sub> pillars is shown in the inset.

effect of passivation on the electrical properties of LED dies. In other words, the apparent increase in the parallel resistance is a result of the desirable decrease in the shunt current.

Comparison of the parallel resistance of LED samples under study (Fig. 5) shows that just the perimeter passivation of LEDs is more effective in suppressing the shunt current than passivation after LED chip fabrication. This observation does not depend on the distance between the contact pad and edge of p-n junction. These results can be explained by the fact that plasma-damaged LED die sidewalls are effective moisture absorbers that result in degradation, supporting the shunt current through surface states [17].



Fig. 5. Average series (a) and parallel (b) resistances of LEDs with (B, B1) and without (A, A1) perimeter passivation before (A, B) and after (A1, B1)  $Si_3N_4$  passivation.



Fig. 6. Reverse current voltage characteristics of passivated LED A1 and B1. Inset shows relative leakage current decreasing for LED with perimeter passivation.

In Fig. 6 one can see a representative leakage current in reverse polarity for LEDs with  $d = 50 \mu m$ . Investigation of leakage current difference between sample B1 and A1 obtained from reverse I-V characteristics is presented in the inset of Fig. 6. One can see that, for LED B1 with perimeter passivation, the leakage currents at -5 V are 68%, 79%, 38% and 76% smaller than those for LED A1 in LED dies with distance 50, 100, 150 and 200  $\mu m$  between contact pad and edge of p-n junction.

Consideration of light output characteristics shows that with passivation the radiant intensity at a given current density is higher as compared to unpassivated ones (Fig. 7). One can see that  $Si_3N_4$  passivation with micro-dome growth improves the radiant intensity by 45%, 30%, 6% and 8% for LED dies with characteristic distances 50, 100, 150 and 200 µm, respectively. However, according to our findings, the employment of a perimeter passivation is more efficient then surface passivation for improving the light output as well as decreasing leakage in that one can obtain 123%, 66%, 87% and 112% radiant intensity improvement for LED chips with 50, 100, 150 and 200 µm characteristic distances, respectively. Incorporation of  $Si_3N_4$  with micro-domes on the surface of perimeter passivated LED dies increases light output properties of LEDs further. As a result the radiant intensity was improved by 171%, 111%, 137% and 154% for LED dies with 50, 100, 150 and 200 µm characteristic distances, respectively.

We can surmise that lower shunt current results in better light output properties and lower shunting current in LEDs with perimeter passivation performed immediately after mesa etching. As a result, higher efficiency of LEDs with SiO<sub>2</sub> perimeter passivation than for LED with just one layer surface passivation were obtained as evidenced from Fig. 8a representing an exemplified efficiency dependence on current density for LED dies with  $d = 50 \mu m$ .

Efficiency of the perimeter passivated sample is nearly 2 times higher than not passivated one even without  $Si_3N_4$  light extraction structures on the top of LED die. For LEDs with  $Si_3N_4$  micro-domes, the efficiency is 1.7, 1.5, 2.4 and 2.8 times higher for LEDs with perimeter pre-passivation than without it. Also one can see that using of two-step passivation that include  $SiO_2$  perimeter passivation and  $Si_3N_4$  surface passivation with micro-domes light extraction structures allows one to improve efficiency by approximately 2.7 times in compareson with LED chips without passivation.

#### 5. Conclusions

We studied an effective two-step passivation for InGaN/GaN LED dies. Perimeter passivation of LED dies with PECVD SiO<sub>2</sub> layer grown immediately after ICP mesa etching leads to a decrease in the leakage current as compared with LED dies before and after Si<sub>3</sub>N<sub>4</sub> surface passivation. The perimeter passivation of LED die is more efficient in reducing the leakage current than surface passivation performed after LED die fabrication, resulting in order of magnitude higher parallel resistance (representing the leakage path) of LED dies. Additional deposition of Si<sub>3</sub>N<sub>4</sub> as the surface passivation layer for samples with perimeter passivation leads to further decrease in leakage current. As a result of leakage current reduction through two-step passivation, the light output properties of LED dies were improved by a factor of 2. Two-step passivation with micro-dome light extraction features on the surface of Si<sub>3</sub>N<sub>4</sub> passivation layer allow us to improve efficiency of LED dies by 100% in comparison with LED chips passivated in ordinary single step approach with Si<sub>3</sub>N<sub>4</sub> layer.



**Fig. 7.** Radiant intensities dependencies on current density of perimeter passivated (LED B, LED B1) and unpassivated (LED A and LED A1) LED dies with distances of 50  $\mu$ m before (LED A, LED B) and after (LED A1, LED B1) Si<sub>3</sub>N<sub>4</sub> with microdomes passivation (a) and relative radiant intensity improvement for LEDs with different characteristic distances between the contact pad and mesa edge with conventional Si<sub>3</sub>N<sub>4</sub> passivation (A1), perimeter passivation (B) and with perimeter passivation and Si<sub>3</sub>N<sub>4</sub> passivation (B1).



**Fig. 8.** Efficiencies of LED dies with (LED B, LED B1) and without (LED A, LED A1) perimeter passivation for LED dies with distance between contact pad and mesa edge equal to 50 μm (a) and relative efficiency improvement for LEDs with different characteristic distance with conventional Si<sub>3</sub>N<sub>4</sub> passivation (LED A1), perimeter passivation (LED B) and with perimeter passivation and Si<sub>3</sub>N<sub>4</sub> passivation (LED B1).

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