Current-mode tunable integrator for low voltage applications

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Indexing terms: Tuning, Integrating circuits

The Letter presents a damped integrator for the design of low-voltage (3V) tunable current-mode filters. The circuit is analysed and the tuning characteristics are discussed.

Introduction: Continuous time analogue filters are needed in many applications such as reconstruction and antialiasing filtering. The low-voltage requirement makes the design of voltage-mode filters extremely difficult owing to linearity and dynamic range limitations [1]. Current-domain signal processing allows use of highly linear circuits with a wide dynamic range operating at high frequencies and with low power supply voltages [2].

Several current-mode filters have been reported [1 – 4]. The main building block in the majority of the approaches has been assumed to be an ideal integrator. In this Letter, the basic block is a damped integrator which is suitable for low-voltage applications and tunable for the purpose of correcting the fabrication tolerances.

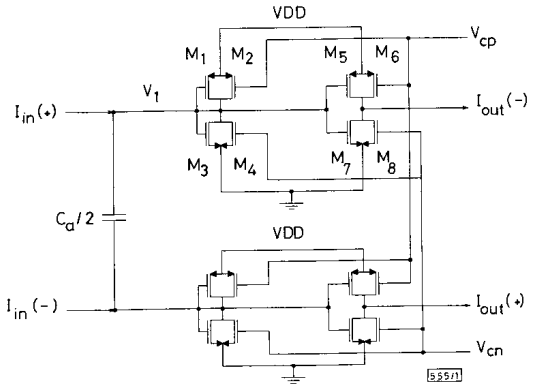

Fig. 1 *Differential damped integrator*

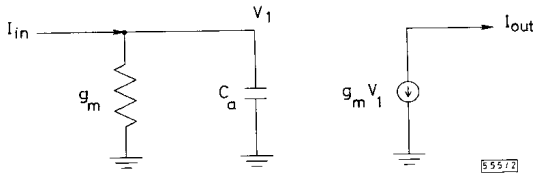

Fig. 2 *Small-signal model*

Tunable damped integrator: The circuit shown in Fig. 1 is the proposed differential damped integrator. Assume that all p-type transistors are matched to each other, and so are n-types. For $V_{cn} = 0$ and $V_{cp} = V_{dd}$, the small-signal model for the half-circuit is shown in Fig. 2, in which the output conductances and parasitic capacitances are neglected. Applying KCL at the input and output nodes yields

$$I_{in} = (sC_a + g_m)V_1 \tag{1}$$

$$I_{out} = -g_m V_1 \tag{2}$$

resulting in

$$\frac{I_{out}}{I_{in}} = -\frac{g_m/C_a}{s + g_m/C_a} \tag{3}$$

where

$$g_m = \beta_n(V_1 - V_{tn}) + \beta_p(V_{dd} - V_1 + V_{tp}) \tag{4}$$

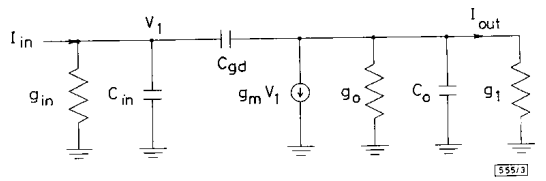

Fig. 3 *Small-signal model including parasitics*

Including the effect of output conductances and parasitic capacitances, the small-signal equivalent circuit becomes as shown in Fig. 3. KCL at input and output nodes yields

$$g_{in}V_1 + sC_{in}V_1 + sC_{gd}(V_1 - V_2) - I_{in} = 0 \tag{5}$$

$$sC_{gd}(V_2 - V_1) + g_m V_1 + g_o V_2 + sC_o V_2 + g_l V_2 = 0 \tag{6}$$

Substituting $I_{out} = g_l V_2$,

$$\frac{I_{out}}{I_{in}} = \frac{-g_l(g_m - sC_{gd})}{[sC_{ieq} + g_{in}][sC_{oeq} + g_{oeq}] + sC_{gd}(g_m - sC_{gd})} \tag{7}$$

where

$$C_{gd} = C_{gdp} + C_{gdn} \tag{8}$$

$$C_{ieq} = C_{in} + C_{gd} \tag{9}$$

$$C_{in} = C_a + C_{dbp} + C_{dbn} + 2C_{gsp} + 2C_{gsn} + 2C_{gbp} + 2C_{gbn} \tag{10}$$

$$C_{oeq} = C_o + C_{gd} \tag{11}$$

$$C_o = C_{dbp} + C_{dbn} \tag{12}$$

$$g_{oeq} = g_o + g_l \tag{13}$$

$$g_o = g_{dp} + g_{dn} \tag{14}$$

$$g_{in} = g_m + g_{dp} + g_{dn} \tag{15}$$

Tuning characteristics: Tuning is achieved by changing the bias voltage V_1 such that g_m given by eqn. 4 changes. The two control voltages V_{cn} and V_{cp} are used for this purpose. To obtain the transfer function in eqn. 3, tuning transistors should be either in the cutoff or the saturation region. For $V_{cp} = V_{dd}$ and varying V_{cn}, the states of n-type tuning transistors and a V_{cn} against g_m plot are shown in Fig. 4.

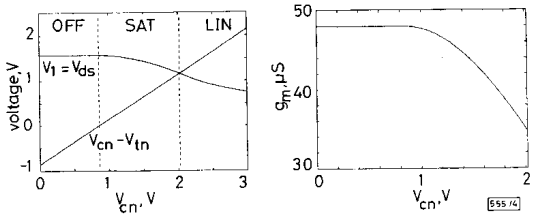

Fig. 4 *Characteristics of down-tuning*

For $V_{cn} = 0$ and varying V_{cp}, states of p-type tuning transistors and a V_{cp} against g_m plot are shown in Fig. 5.

Consequently, from Figs. 4 and 5, g_m can be decreased or increased by changing V_{cn} and V_{cp}, respectively. Note that when V_{cn} is used for tuning, V_{cp} is set to V_{dd}, and for varying V_{cp}, V_{cn} is set to zero.

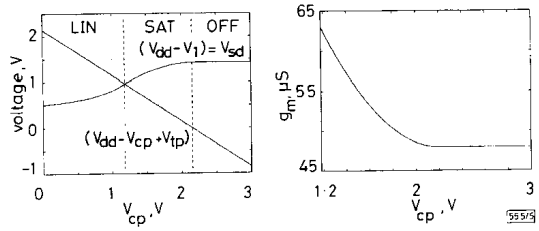

Fig. 5 *Characteristics of up-tuning*

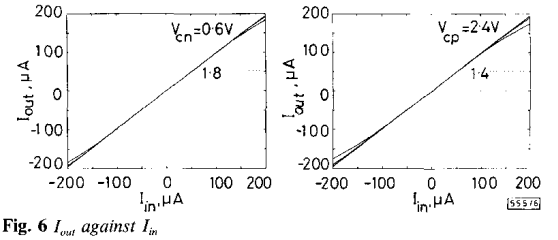

Fig. 6 *I_{out} against I_{in}*

Tuning control voltages V_{cn} and V_{cp} also affect the dynamic range of the circuit owing to finite output conductances. In Fig. 6, plots of I_{out} against I_{in} for several V_{cn} and V_{cp} values are depicted. In the Figure, a linear relationship is observed between I_{out} and I_{in} for $I_{in} \leq 100\mu A$.

Conclusion: A new current-mode damped integrator is proposed. The circuit operates at low supply voltages since only two transistors exist from supply to ground rail. Using two control voltages, the corner frequency of the integrator can be tuned.

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References

1 ZELE, R.H., ALLSTOT, D.J., and FIEZ, T.S.: 'Fully balanced CMOS current-mode circuits', *IEEE J. Solid-State Circuits*, 1993, **28**, (5), pp. 569–574
2 LEE, S.S., ZELE, R.H., ALLSTOT, D.J., and LIANG, G.: 'CMOS continuous-time current-time filters for high-frequency applications', *IEEE J. Solid-State Circuits*, 1993, **28**, (3), pp. 323–328
3 NAUTA, B.: 'A CMOS transconductance-C filter technique for very high frequencies', *IEEE J. Solid-State Circuits*, 1992, **27**, (2), pp. 142–153
4 ZELE, R.H., LEE, S.S., and ALLSTOT, D.J.: 'A 3V-125MHz CMOS continuous-time filter'. Proc. Int. Symp. on Circuits and Systems (ISCAS'93), Chicago, IL, USA, 1993, pp. 1164–1167

Digitally programmable V-I converter for application in MOSFET-C filters

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Indexing terms: Digital circuits, Transconductors, Switched capacitor filters

A compact digitally controlled V-I converter is presented. The basic element of the V-I converter is a MOSFET-only current divider (MOCD) [1]. The programmable V-I converter proposed in this work can be readily applied to MOSFET-C continuous-time amplifiers, filters and oscillators.

Introduction: One of the most successfull techniques for integrating continuous-time filters uses the so-called MOSFET-C structures [2]. These continuous-time filters are derived from classical active-RC filters, with the resistors replaced by MOS transistors operating in the triode region. Special techniques [2] have been developed to reduce the harmonic distortion caused by transistor nonlinearities. MOSFET-C filters suffer from high variability of the frequency response owing to process deviations, thermal variations and aging. This high variability requires the tuning of component values to keep the frequency response within acceptable limits. Usually, the tuning is performed on the output conductance of the MOSFET, which is controlled by the gate voltage. However, this tuning strategy changes the operating point of the MOS transistors, degrading the linearity of the filter.

We propose the application of MOCDs [1] in MOSFET-C filters. This design technique allows digital programmability without requiring much silicon area, as compared to the conventional implementation. Tuning the response of the filter does not require changes in the gate voltage, thus avoiding degradation in the linearity of the filter. Furthermore, tuning strategies such as those presented in [3, 4] can be readily applied to the new structure.

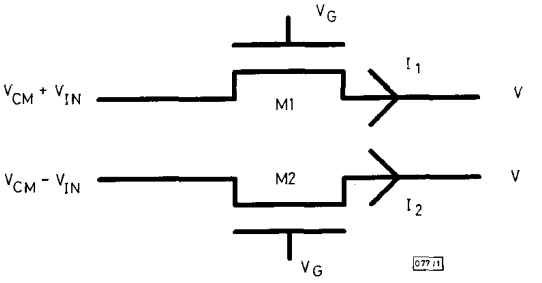

Fig. 1 *Structure of MOS linear V-I converter*

Principle of method: The proposed scheme of the digitally controlled V-I converter is based on the structure shown in Fig. 1 [2]. Assuming matched transistors, the differential output current (I_1-I_2) is free of even nonlinearities. In our proposal, M_1 and M_2 are replaced by MOCDs. The structure of the MOCDs is depicted in Fig. 2. The output current of the MOCD is a fraction, selected by a digital word, of the input current [1]. This programmable current divider has two major advantages over other digitally programmable dividers: (i) MOSFETs perform simultaneously as elements of the divider network and as switches, and (ii) the impedance of the current attenuator is independent of both the number of bits and the attenuation factor. Moreover, the high linearity of this current division technique [1] has been proved adequate for analogue signal processing.

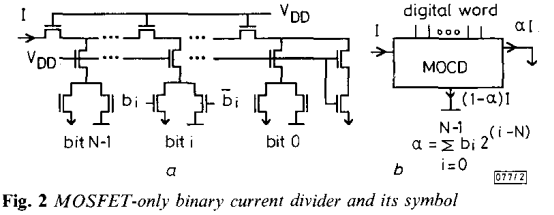

Fig. 2 *MOSFET-only binary current divider and its symbol*

a Circuit diagram
b Symbol

Fig. 3 describes the application of the proposed scheme in MOSFET-C filters. The elements in the feedback loop can be resistors or capacitors [2]. The gate voltages of the MOSFETs are kept constant at V_{DD}.

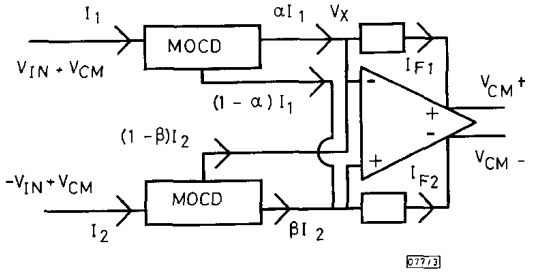

Fig. 3 *Digitally programmable V to I converter for applications in MOSFET-C filters*

We assume that the I-V characteristic of the MOSFET in the triode region is given by [6, 7]

$$I_D = \frac{\mu C'_{ox} n}{2} \frac{W}{L} [(V_P - V_S)^2 - (V_P - V_D)^2] \quad (1)$$

where V_p is the pinch-off voltage given by $V_P = (V_G - V_{TO})/n$, V_{TO} is the zero-bias threshold voltage and n is the slope factor [6, 7]. It