Design and Fabrication of CSWAP Gate Based on Nano-Electromechanical Systems

Mert Yüksel[1], Selçuk Oğuz Erbil[1], Atakan B. Arı[1], and M. Selim Hanay[1,2](✉)

[1] Department of Mechanical Engineering, Bilkent University, Bilkent, Ankara 06800, Turkey
selimhanay@bilkent.edu.tr

[2] National Nanotechnology Research Center (UNAM), Bilkent University, Bilkent, Ankara 06800, Turkey

Abstract. In order to reduce undesired heat dissipation, reversible logic offers a promising solution where the erasure of information can be avoided to overcome the Landauer limit. Among the reversible logic gates, Fredkin (CSWAP) gate can be used to compute any Boolean function in a reversible manner. To realize reversible computation gates, Nano-electromechanical Systems (NEMS) offer a viable platform, since NEMS can be produced *en masse* using microfabrication technology and controlled electronically at high-speeds. In this work-in-progress paper, design and fabrication of a NEMS-based implementation of a CSWAP gate is presented. In the design, the binary information is stored by the buckling direction of nanomechanical beams and CSWAP operation is accomplished through a mechanism which can selectively allow/block the forces from input stages to the output stages. The gate design is realized by fabricating NEMS devices on a Silicon-on-Insulator substrate.

Keywords: Reversible logic · CSWAP gate · NEMS · Buckling · Nanomechanical computation

1 Introduction

Transistor-based irreversible computation is the most commonly used paradigm for information processing which has shown a significant improvement in last few decades, especially with the adoption of complementary metal-oxide semiconductor (CMOS) transistor technology. However, further development of irreversible computing is limited by the inability to reduce heat dissipation. Landauer demonstrated that one-bit erasure of information can only be achieved with at least $k_B T ln2,$ where k_B is the Boltzmann's constant and T is the operating temperature, amount of heat dissipation to the environment during the irreversible logic operation [1], which was experimentally demonstrated in 2012 [2]. Since then, reversible computation has been receiving great attention with its ability to lower heat dissipation. It was shown that reversible logic can also be used for information processing [3].

Development of reversible logic gates is considered as a basis of the reversible computation as proposed by CSWAP (Fredkin), Toffoli, Feynman, and others. CSWAP

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gate is one of the universal reversible logic gates, meaning that all Boolean operations can be performed with a system that consists of only CSWAP gates. Mechanical implementations of logic gates were proposed before [4–6]; however, the design proposed here has higher integration density and does not require external signal generators to drive resonance motion; as a result, the cost and complexity of the proposed system is expected to be lower. Developments in NEMS technology, which allows the fabrication of mechanical systems working at high speeds [7] and at high temperatures [8], enable the realization of reversible logic gates, such as the CSWAP gate architecture presented here.

In this work-in progress paper, NEMS based implementation of CSWAP gate design is introduced and working principle of the proposed system is discussed. Proposed design is computation-wise reversible. A basic fabrication process of the architecture is also demonstrated.

2 Information Storage via Buckling

In this work, we propose to store information in NEMS devices by using the buckling of beam structures [9]. Here, each beam represents one-bit information where the buckling direction (left or right) corresponds to logic 0 or logic 1. Figure 1 demonstrates how one-bit information can be registered on NEMS structures via buckling. The beams are designed as pinned and anchored at one end. The other end, where a compressive force is applied, is free to move axially and restrained from any transverse movement in order to observe longitudinal buckling. The beam is sandwiched by two electrodes (A1/B1) which apply a preloading force to the beam in order to determine buckling direction when the voltage is applied. For instance, if 5 V is applied to the electrode on the right, an electrostatic attraction force develops which preloads the beam to the right-hand side. After the beam is directed by the electrodes, a compressive force is applied via electrostatic actuation. Upon the exertion of the compressive force, the beam buckles to the direction determined by the preloading force. In order to buckle the beam, the compressive force must exceed the critical value which is determined by:

$$F_{critical} = \frac{\pi^2 EI}{L^2} \tag{1}$$

where E is Young's Modulus, L is the length of the beam and I is the moment of inertia [10].

Threshold for the compressive force to induce buckling is calculated to be 22.5 μN for a typical device with 2μm length, 150 nm width and 250 nm thickness. This force can be produced by an electrostatic comb drive composed of capacitive gates with 350 nm gaps as demonstrated in Fig. 1. The critical voltage applied to comb drive is calculated by:

$$V_{critical} = \sqrt{\frac{2dF_{critical}}{\epsilon Nt}} \tag{2}$$

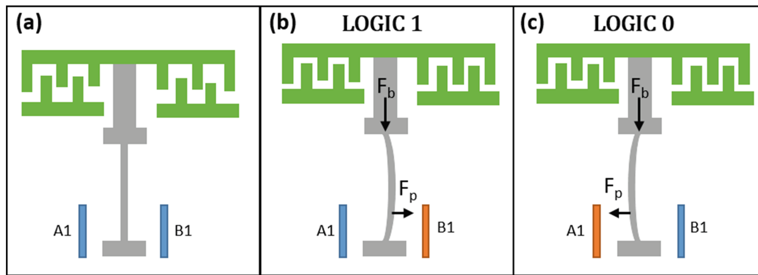

Fig. 1. Demonstration of one-bit information storage: (a) Off-state. Nano-mechanical beam is shown in gray, electrodes used to preload the data are shown in blue and the comb-drive to induce buckling is shown in green. (b) On-State Logic 1: A voltage is applied to B1 gate to first preload the beam (exerting F_p), then the beam is buckled to the right by the application of buckling force F_b. (c) On-State Logic 0: A1 gate first preloads the beam, which is then buckled to the left. (Color figure online)

where ϵ is electric permittivity, N is number of fingers, t is thickness of a finger and d is gap spacing between fingers of the comb drive [11].

Different dimensions for the beam can be considered to optimize N and $V_{critical}$. It is more convenient to have fewer fingers for comb drive for simplicity of the design. Also, having a low critical voltage is desired to decrease the power consumption. For different lengths (L) of the beam, $N - V_{critical}$ relation is shown in Fig. 2. It can be observed that for the longer lengths of the beams, it is easier to reach $F_{critical}$ with lower $V_{critical}$. Although $V_{critical}$ levels are relatively higher than voltage values commonly used in digital circuits, these voltage levels can be achieved with low power using DC-to-DC voltage converters. More importantly, triggering voltage will only be used to initiate buckling process – the actual data to be written can still be applied at the standard logic voltages such as 5.0 V or 3.3 V. In this regard, triggering voltage is similar to the clock signals of conventional digital circuits: each stage of the logic gates computes the output when a triggering voltage compresses the set of beams in turn.

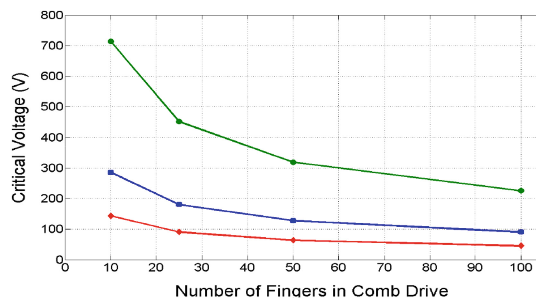

Fig. 2. Number of fingers (N) vs. critical voltage ($V_{critical}$) for beams with different lengths. Top green curve is for 2 μm, blue curve is for 5 μm and bored curve is for 10 μm long beams. (Color figure online)

3 NEMS Based CSWAP Gate

3.1 Design

Principle of the CSWAP gate is to swap the inputs when the controller bit is set (logic high), and to rehash the inputs when the controller bit is reset (logic low). In this design, inputs are applied to the gate by preloading the beams to the logic 1 or 0 states. The displacement of the input beams, after they buckle, leads to compression or tension of the spring-like structures linking inputs to outputs (Fig. 3). Through these links, the input beams exert either a push or pull force, depending on their logic state, to preload the output beams. Each output beam is connected to both input beams and the equivalent preloading force determines the eventual state of the output beam.

The symmetry of the force transmission between input beams to output beams is broken by the controller beam, C. Controller beam (C) disrupts a direct transmission of one of the input forces (A or B), by locating one of its arm to the gap found on the connecting beam. When C is logic 0, the connection between A and BO, and B and AO are disrupted, therefore the preloading will favor A for A0, and B for BO respectively, which will map the outputs in the way of A to A0 and B to B0. On the other hand, when C is logic 1, the connection between A and AO, and B and BO are disrupted by controller, consequently outputs AO and BO will swap the inputs and read B and A respectively. Thus, CSWAP gate architecture is mechanically achieved as demonstrated in Fig. 3. The required processing area for one CSWAP gate is approximately 150 μm^2 which includes the part of the comb drive transmitting buckling force. This area translates into an integration density of 200,000 gates per cm^2.

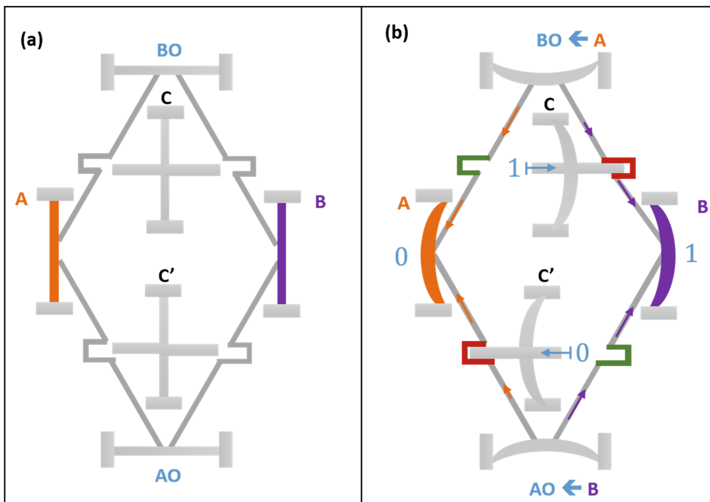

Fig. 3. NEMS based CSWAP gate (a) CSWAP architecture (b) example demonstration of CSWAP operation. Inputs are taken as A = 0, B = 1, C = 1. Outputs; AO = B = 1, BO = A = 1, C' = 1. Forces transmitted by the input stages through the springs are either blocked or uninterrupted depending on the controller bit.

3.2 Nano-Fabrication

A proof-of-principle fabrication process has been implemented using dices of a commercially available Silicon on Insulator (SOI) wafer which has a composition of: 250 nm thick p-doped Silicon on top of 3 μm buried oxide (BOX) with a 650 μm silicon base substrate. After the standard cleaning procedure, Electron-beam lithography was performed using PMMA bilayer as resist. Following the patterning, a 60 nm thick layer of SiO_2 dry etch mask was deposited via E-Beam evaporation. The sample was left in an acetone bath for lift-off overnight. For the next step, the top Silicon layer is anisotropically etched with an Inductively Coupled Plasma device, using Cl_2 plasma, until the BOX layer. Then the patterned Silicon structures were suspended by wet etching the BOX layer using a 1:7 Buffered Oxide Etch solution. Since the SiO_2 dry etch mask was also removed during the wet etching step, there was no need for an extra mask removal step (Fig. 4).

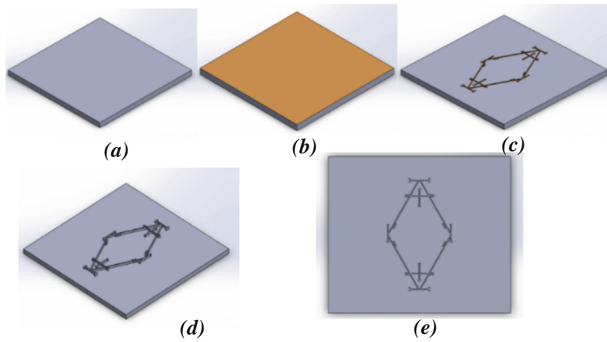

Fig. 4. Fabrication Process Flow: (a) SOI Chip, (b) after EBL and SiO_2 deposition, (c) after lift-off process, (d) after ICP etching of Si layer, (e) topside view of the system

For future progress, Au electrodes and comb drive will be fabricated on the sample respectively. Electrodes will be patterned by EBL. Following that step, a layer Au will be deposited by a Physical Thermal Deposition device and the sample will be left for lift-off. After the fabrication of the electrodes, comb drives will be fabricated using similar steps (Fig. 5).

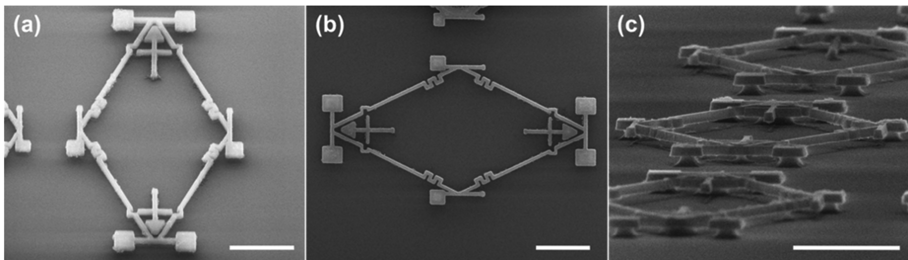

Fig. 5. SEM images of the fabricated proof-of-principle device from different perspectives. The scale bars are 3 μm in each image.

4 Conclusion

In this work-in-progress paper, logically-reversible CSWAP gates are designed using NEMS technology. One-bit data can be stored on a nano-mechanical beam depending on its direction of buckling. Basic calculations are presented for forces and voltages necessary to induce buckling in nanoscale beams. A basic nano-fabrication process is demonstrated to implement the CSWAP gate. By further integrating structures to trigger buckling process, information processing will be demonstrated in the future. With its large integration density and high speeds, NEMS technology is a promising platform to implement reversible logic operations.

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References

1. Landauer, R.: Irreversibility and heat generation in the computing process. IBM J. Res. Dev. **5**, 183–191 (1961)
2. Berut, A., Arakelyan, A., Petrosyan, A., Ciliberto, S., Dillenschneider, R., Lutz, E.: Experimental verification of Landauer's principle linking information and thermodynamics. Nature **483**, 187–189 (2012)
3. Bennet, C.H.: Logical reversibility of computation. IBM J. Res. Dev. **17**(6), 525–532 (1973)
4. Sharma, A., Ram, W.S., Amarnath, C.: Mechanical logic devices and circuits. NaCoMM **9**, 235–239 (2009)
5. Wenzler, J.S., Dunn, T., Toffoli, T., Mohanty, P.: A nanomechanical Fredkin gate. Nano Lett. **14**(1), 89–93 (2013)
6. Mahboob, I., Mounaix, M., Nishiguchi, K., Fujiwara, A., Yamaguchi, H.: A multimode electromechanical parametric resonator array. Sci. Rep. 4 (2014). Article no. 4448
7. Huang, X.M.H., Zorman, C.A., Mehregany, M., Roukes, M.L.: Nanodevice motion at microwave frequencies. Nature **421**, 496–496 (2003)
8. Lee, T.H.: Electromechanical computing at 500 °C using silicon carbide. Science **329** (5997), 1316–1318 (2010)
9. Merkle, R.C.: Two types of mechanical reversible logic. Nanotechnology **4**(2), 114 (1993)
10. Hopcroft, M.A.: What is the Young's modulus of silicon. IEEE J. Microelectromech. Syst. **19**, 229–238 (2010)
11. Legtenberg, R., Groeneveld, A.W., Elwenspoek, M.: Comb-drive actuators for large displacements. J. Micromech. Microeng. **6**, 320–329 (1996). IOPscience