Extracting the temperature distribution on a phase-change memory cell during crystallization

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Phase-change memory (PCM) devices are enabled by amorphization- and crystallization-induced changes in the devices' electrical resistances. Amorphization is achieved by melting and quenching the active volume using short duration electrical pulses (∼ns). The crystallization (set) pulse duration, however, is much longer and depends on the cell temperature reached during the pulse. Hence, the temperature-dependent crystallization process of the phase-change materials at the device level has to be well characterized to achieve fast PCM operations. A main challenge is determining the cell temperature during crystallization. Here, we report extraction of the temperature distribution on a lateral PCM cell during a set pulse using measured voltage-current characteristics and thermal modelling. The effect of the thermal properties of materials on the extracted cell temperature is also studied, and a better cell design is proposed for more accurate temperature extraction. The demonstrated study provides promising results for characterization of the temperature-dependent crystallization process within a cell. *Published by AIP Publishing.*
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I. INTRODUCTION

Phase-change memory (PCM) devices can toggle between at least two resistance states as the phase of the active volume transitions between highly resistive amorphous state and conductive crystalline state.[1,2] Amorphization is achieved by melting and quenching the active volume using short electrical pulses. Crystallization is typically achieved by annealing the amorphous volume below the melting temperature for longer durations (>50 ns). PCM devices are currently in the non-volatile memory market competing with the decades-old flash memory technology. The technology standard NAND flash memory provides high-density owing to extremely small-footprint devices and multi-/triple-level operations. Recent 3D stacking of the flash memory devices is expected to increase the competition between the flash memory and emerging non-volatile memory technologies like PCM.[3] While mainstream memory applications have been the main target of PCM technology, 2-terminal, memristor-like operation of the devices has also enabled neuromorphic applications.[4,5] As a more ambitious goal, PCM and other resistive memory technologies target replacing dynamic random access memory (DRAM), through eliminating volatility and destructive readout of current 1 transistor–1 capacitor DRAM cells. The recent announcement of a 3D, 2-terminal universal memory from Intel suggests that resistive memory technologies, including PCM, will attract more attention and witness more breakthroughs in the near future.[6] For PCM to compete with ever-improving flash memory or to find a permanent spot in the memory hierarchy, it has to overcome its limited endurance, high amorphization (reset) current, and long crystallization (set) time. Materials research and further miniaturization of the PCM devices are mainly pursued to solve the endurance and high reset current issues.[7–9] Reducing crystallization durations requires studying crystal growth velocities of phase-change materials in a wide temperature range, e.g., 300–870 K for $Ge_2Sb_2Te_5$ (GST), which is the most commonly used phase-change compound.

The crystallization process can be monitored as the gradual change in the electrical resistance of a device or the optical reflection of a film as samples are heated up to elevated temperatures.[10,11] To monitor the crystallization process properly at a certain elevated temperature, the sample temperature has to be raised quickly to the desired level before crystallization takes place.[10] The crystallization process is slow below ∼500 K, hence can be performed on a hot-plate with relatively low heating rates (∼1 K/s). Using a fast heater or an integrated micro-stage provides a larger heating rate,[12,13] hence increases the maximum temperature at which the crystallization studies can be performed up to 700 K. Alternatively, PCM devices can be reset on a hot-plate at elevated temperatures under constant resistance monitoring.[14] The ultimate device-level crystallization study, however, would require heating rates achieved in

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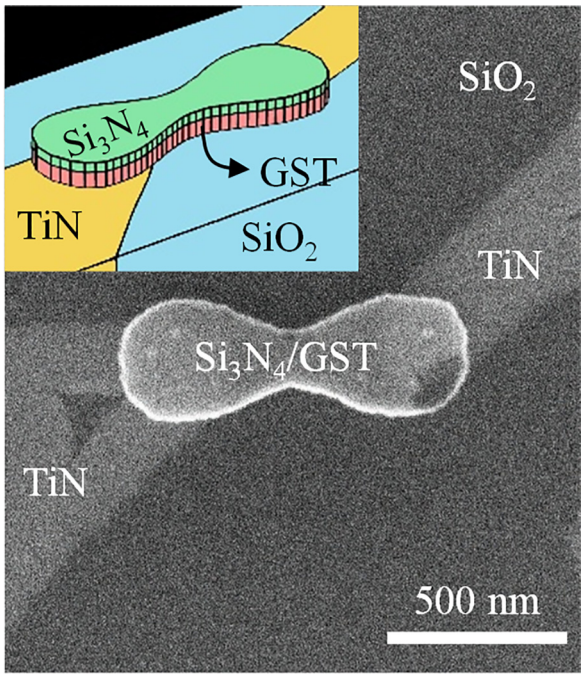

FIG. 1. Top-down scanning electron microscopy (SEM) image of a lateral PCM cell. 3D drawing of the cell showing the top Si_3N_4 layer (Inset).

an actual set operation which brings the cell temperature close to the melting temperature within nanoseconds (10^{11} K/s). The challenge with using self-heating to characterize the crystallization process is the measurement of the cell temperature. Here, we extract the temperature distribution on a lateral GST cell during various set pulses using the experimental electrical power as the heat source and modelling thermal transport on the measured cell. The proposed method requires the knowledge of the temperature-dependent thermal properties of the PCM cell layers such as GST, TiN, SiO_2, and Si_3N_4, and enables extraction of the 3D cell temperature distribution as a function of time for any set (crystallization) operation. The employed method of feeding the experimental dissipated power to the thermal transport simulations differs from what is typically done in the literature to map the cell temperature which involves solving the electrical conduction expression coupled to the thermal transport.[15–17] This method, however, is susceptible to uncertainties in the electrical conductivity of amorphous GST that can change orders of magnitude with varying temperature and electric field.[18]

II. EXPERIMENTS

The reset/set operations are performed on nanoscale lateral PCM cells. The devices consist of planarized bottom TiN contacts, 50 nm thick GST films patterned into bowtie shape, and 30 nm thick Si_3N_4 top layer (Figure 1). A detailed fabrication process is provided in Refs. 14 and 19 which report the crystallization studies up to 675 K and the extraction of the liquid GST resistivity from similar PCM cells, respectively. A small volume around the narrowest region is melted by a short-duration (10 ns) reset pulse and amorphized upon quenching. The reset pulse duration is chosen to be short to suppress the asymmetry in the molten volume due to the thermoelectric effects.[20] The short pulse duration, however, necessitates a large pulse amplitude (9 V) for melting. Both reset and set operations use the same setup: an external load resistor (R_{load}) is connected in series with the PCM cell ($R_{GST}+R_{TiN}$) which is grounded through a 50 Ω termination resistor ($R_{termination}$) (Figure 2(a)). Both the applied voltage (V_A) and voltage on the termination resistor (V_B) are monitored by an oscilloscope. The cell resistance is measured ~1 min after the pulse (reset or set) using the same setup and long duration (1 ms), small amplitude (1 V) pulses. The reset resistance is observed to drift over time as expected from melt-quenched GST ($R_{reset} \sim t^n$) with an exponent (n) of 0.1 (Ref. 14). 1 MΩ or 50 Ω is used as $R_{termination}$ for the resistance measurement depending on the cell resistance. The minimum set pulse amplitude to initiate the threshold switching is characterized to be between 4 and 5 V depending on the achieved reset resistance level. For this amplitude range, 500 ns of pulse duration crystallizes the cells unless the amorphous volume is too large. The cell exhibits a stable operation window between 10^4 and 10^7 Ω

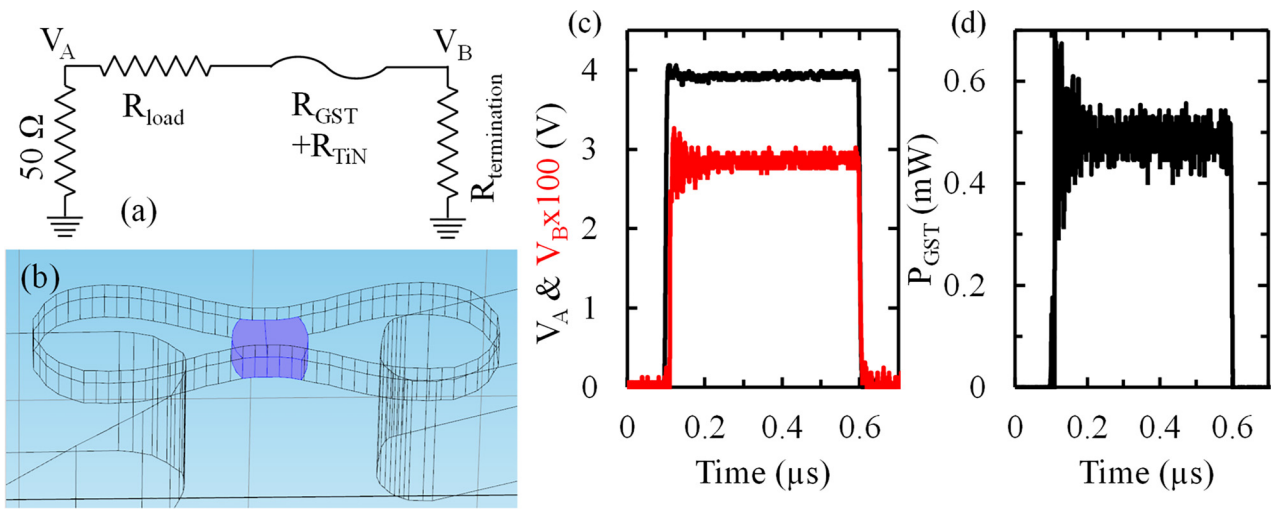

FIG. 2. (a) Circuit diagram of the measurement setup. (b) 3D illustration of the simulated structure with highlighted amorphous volume. (c) Applied set pulse and (V_A) and voltage on the termination resistor (V_B). (d) Electrical power dissipated on the GST cell.

TABLE I. Thermal conductivity, heat capacity, and density of the PCM layers. The parameters which are shown as functions of temperature are provided in supplementary Figure S4.

	κ (W/m K)	C_p (J/kg K)	d (kg/m^3)
GST	κ_{GST}(T) (Ref. 24)	C_{GST}(T) (Ref. 25)	6150 (Ref. 25)
TiN	κ_{TiN}(T) (Ref. 24)	784 (Ref. 24)	7280 (Ref. 24)
SiO_2	1.38 (Ref. 22)	703 (Ref. 22)	2203 (Ref. 22)
Si_3N_4	20 (Ref. 22)	700 (Ref. 22)	3100 (Ref. 22)

levels after an initialization phase[10] of 20 reset/set cycles and breaks after 35 cycles (supplementary Figure S1). The premature breakage of the lateral cells is attributed to the thin capping layer. The cell temperature is extracted for a set pulse (4 V, 500 ns) which brings the cell resistance to 17.6 kΩ from 19.5 MΩ.

III. THERMAL MODELLING

The extraction of the cell temperature is achieved using the experimental electrical power as the heat source in the thermal transport simulations (Eq. (1)). The measured PCM cell is drawn as accurately as possible using the top-down and cross section electron microscope images. The amorphous volume on the simulated cell is determined using steady-state electrical conduction simulations and the measured reset resistance of the cell. The amorphous volume is iteratively changed until the simulated and measured reset resistances match. While determining the amorphous volume, the resistivity of 96.4 Ω cm is used for the amorphous region which is obtained as an average value from measurements of 35 devices.[14] The curvature of the amorphous-crystalline interface as shown in Figure 2(b) is determined by simulating a reset pulse (supplementary Figure S2).

The dissipated electrical power is calculated using V_A and V_B measurements (Figure 2(c)). The total electrical power (P_{total}) is calculated as $V_A I$, where I is the current ($V_B/R_{termination}$) that flows through the load resistor, PCM cell, and the termination resistor. The power dissipated on the PCM cell (P_{GST}) is then calculated as: $P_{GST} = P_{total} R_{GST}/R_{total}$. The total resistance ($R_{total}$) is found as V_A/I, and R_{GST} is $R_{total} - (R_{load} + R_{TiN} + R_{termination})$, where R_{load} is 5.12 kΩ, R_{TiN} is measured as 200 Ω, and $R_{termination}$ is 50 Ω. P_{GST} as a function of time, calculated using measured V_A and V_B, is shown in Figure 2(d). Variations in the external resistances affect the calculated P_{GST} which has a large impact on the extracted cell temperature (supplementary Figure S3). Thus, a low-tolerance, low-capacitance surface-mount external resistor is used as the load resistor. The load resistor is attached close to the needle probing one of the contacts of the device. R_{TiN} and $R_{termination}$ are small compared to R_{load}; hence, the variations in these resistances have smaller impact on the calculated P_{GST}. R_{TiN} is measured using 4-point contact configuration and test TiN contacts.[21] The TiN/GST junction on devices with 4 individual contacts is characterized to be Ohmic with low contact resistance compared to the reset resistance levels.[14]

The time-dependent thermal transport equation is solved on the 3D geometry using P_{GST} as the heat dissipated on the amorphous volume and temperature dependent thermal parameters using COMSOL Multiphysics[22] (see Table I and supplementary Figure S4)

$$dC\frac{dT}{dt} - \nabla \cdot (\kappa \nabla T) = P_{GST}/V_{amorphous}, \tag{1}$$

where d is the density, C is the heat capacity, κ is the thermal conductivity, and $V_{amorphous}$ is the amorphous volume. A constant thermal boundary resistance (TBR) of 2×10^{-8} Km^2/W (Ref. 23) is applied on boundaries between low and high thermal conductivity materials, i.e., GST-TiN and SiO_2-TiN, using the equation: $Q = \Delta T/R_{thermal}$, where Q is the heat flux, ΔT is the temperature difference across the boundary, and $R_{thermal}$ is the thermal boundary resistance.

IV. RESULTS

The simulation results provide time evolution of the temperature distribution on the PCM cell. The temperature profile has a maximum around the wire center and decreases towards the TiN contacts (Figures 3(a) and 3(b)). Temperatures at the far ends of the TiN contacts are set to 300 K. The asymmetry in the TiN contacts geometry results in an asymmetric temperature profile. TiN contacts stay cool throughout the pulse owing to the larger thermal conductivity of TiN compared to that of GST and SiO_2. As a result, the crystalline GST regions

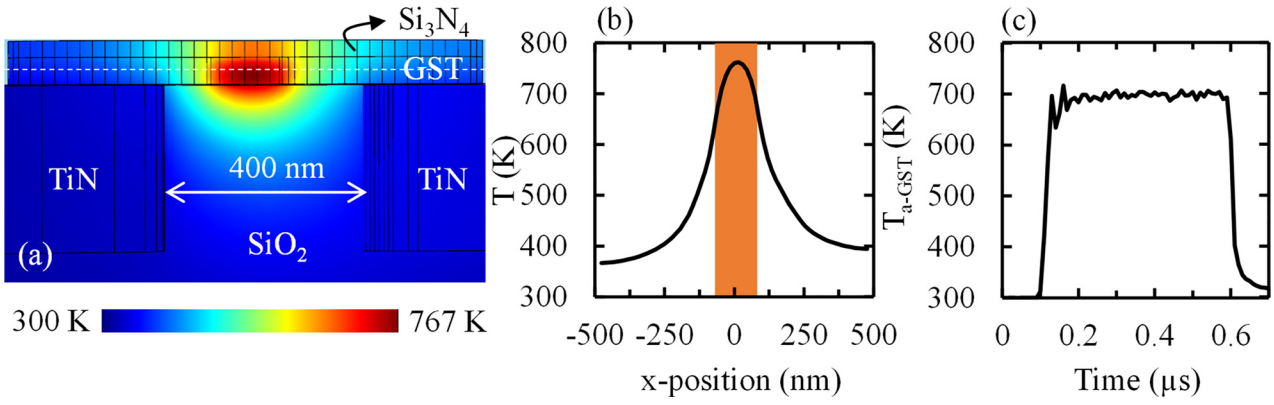

FIG. 3. (a) Temperature map across the cross-section of the cell during the set pulse. (b) Temperature profile along the GST layer (dashed line in (a)). The shaded region highlights the initial amorphous volume. (c) Volume-averaged temperature of the amorphous region during the pulse.

on top of the TiN contacts stay at low temperatures. The temperature within the amorphous volume ranges between 600 and 770 K, resulting in a volume-averaged temperature of ~700 K during the pulse (Figures 3(b) and 3(c)). The maximum temperature within the a-GST volume is close to the temperature at which the maximum crystal growth-rate is observed for melt-quenched amorphous GST.[26] This result is consistent with the measured set resistance values as lower-amplitude set pulses cannot fully set (crystallize), whereas higher-amplitude set pulses re-amorphize the cell suggesting that lower and higher amplitude set pulses bring the cell to below the-maximum-growth-rate temperature and above the melting temperature, respectively.

V. DISCUSSION

The extracted cell temperature significantly depends on the simulated geometry and the thermal parameters such as thermal conductivity and thermal boundary resistance between TiN and GST. For example, if the Si_3N_4 capping layer is ignored, the simulations incorrectly predict that the cell temperature exceeds the GST melting temperature. Therefore, care has to be taken to define the geometry and material parameters as accurately as possible. The thermal conductivity of GST and TiN is defined as functions of temperature up to the melting temperature of GST (~900 K). The thermal boundary resistance (TBR) between TiN and GST, however, is not known at high temperatures.[23] We expect the TBR between TiN-GST to decrease with increasing temperature as the electronic component of the GST thermal conductivity increases. When the thermal properties of the materials match, the TBR is expected to be very small. Therefore, to test the impact of TBR on the cell temperature, a simulation is performed ignoring the thermal boundaries which results in a maximum cell temperature of 750 K being 20 K smaller than what is estimated with TBR (Figure 4). Defining the active volume away from the TiN junctions is expected to eliminate the need for the high-temperature TBR information and the uncertainty in the estimated cell temperature. The simulations of a hypothetical wire structure with varying distance between the active volume and TiN contacts suggest that the effect of TBR between the GST and TiN layers is small ($\Delta T < 20$ K) if the active volume and the TiN contacts are more than 200 nm apart (supplementary Figure S5). The proposed method of extracting the cell temperature can be extended to any geometry, including the vertical (mushroom) geometry, after the temperature-dependent thermal boundary resistance between the contacts and phase-chase material is characterized. Otherwise, the uncertainty in the extracted temperature would be larger than what is estimated for the lateral cells studied here.

As a second study, the cell temperature extraction method is performed on the same cell for a different set pulse which brings the cell resistance to 43 kΩ from 35 MΩ (supplementary Figure S1). The amorphous volume for this case is larger (Figure 5(a)), owing to the larger reset resistance compared to the first case. The applied set pulse amplitude is 5 V, as 4 V amplitude could not initiate the threshold switching. Despite the larger set pulse amplitude, the threshold switching occurs ~100 ns after the pulse is applied, decreasing the annealing duration to ~400 ns (Figure 5(b)).[27] Owing to the larger set pulse amplitude, the resulting power dissipation is larger compared to the previous case (Figure 5(b)). However, the extracted cell temperature is smaller, since the power is also dissipated on a larger volume. Furthermore, the heat flow from the active volume towards the TiN contacts is increased as the active volume boundaries are, now, closer to the TiN contacts (Figure 5(c)). The smaller distance between the active volume and TiN contacts increases the effect of TBR in the simulations (Figures 5(d)–5(f)). The set resistance of the cell is measured as 43 kΩ, suggesting that it is not fully crystallized. The impartial crystallization of the cell is consistent with the extracted cell temperature which is lower than that of the previous case.

The method demonstrated here enables the extraction of the cell temperature distribution using the experimental electrical power and thermal transport modelling. A similar approach has recently been taken by Sebastian *et al.*[26] to extract the maximum-growth-rate-temperature within vertical (mushroom) PCM cells. The mentioned report uses a single pulse with varying amplitude to melt and crystallize the PCM cells. The power required for full crystallization is determined at various ambient temperatures. When the linear relationship between the ambient temperature and crystallization power is extrapolated to zero power, the maximum growth-rate temperature is extracted as ~750 K. This method, however, can only extract the maximum-growth-rate temperature and melting temperature. In contrast, our method can extract the 3D temperature profile within a cell for any given power dissipation. Another advantage of our method is the use of a single set of voltage-current measurements at any ambient condition. Furthermore, the reset and set pulses in our study are applied separately similar to the typical PCM operation. The drawback of the demonstrated

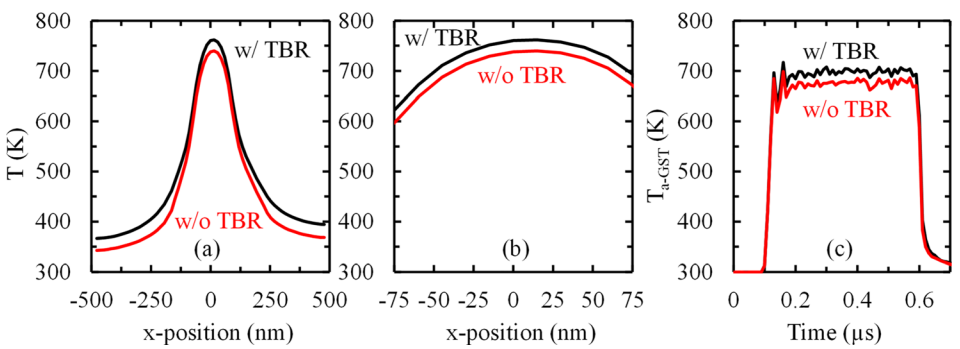

FIG. 4. Simulation results with and without TBR. Temperature profiles (a) along the GST layer and (b) along the amorphous volume. (c) Volume-averaged temperature of the amorphous region during the pulse.

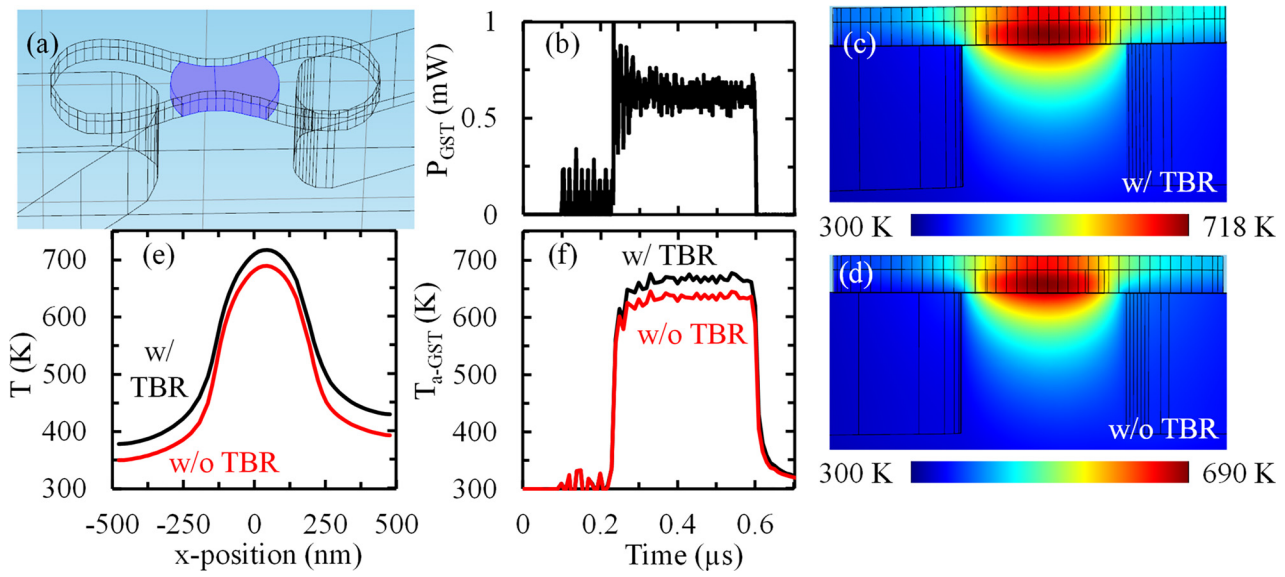

FIG. 5. (a) 3D illustration of the simulated structure with a larger amorphous volume (highlighted in blue). (b) Electrical power dissipated on the GST cell. Temperature map across the cross-section of the cell during the set pulse (c) with TBR and (d) without TBR. (e) Temperature profiles along the GST layer. (f) Volume-averaged temperature of the amorphous region during the pulse.

method, however, is its strong dependence on the thermal parameters of the cell layers, especially the TBR between GST and TiN (or any other material used to form the electrical contacts). This problem can be avoided by designing the active volume farther away from the heat sinks like TiN or metal contacts. The thermal properties of the cell in the report by Sebastian *et al.*[26] is not an input as in ours but a result of the temperature extraction method. The thermal resistance of the whole cell (R_{TH}), which accounts for the heat flow in all directions, i.e., top and bottom TiN, and surrounding c-GST and SiO_2, is extracted as the slope of the linear relationship between the ambient temperature and crystallization power. R_{TH} is extracted as $\sim$1.5 K/μW by the authors,[26] whereas it is calculated as 0.8 K/μW for our study using the extracted cell temperature and dissipated power. These R_{TH} values are on the same order despite the architecture difference between the mushroom cells in Ref. 26 and our lateral cells. R_{TH} is calculated as 0.6 K/μW for the larger amorphous volume case in Figure 5(a), being smaller as a result of the greater heat loss to the surroundings.

VI. CONCLUSIONS

In conclusion, the cell temperature within a nanoscale lateral PCM device during the set operation is extracted using the experimental power dissipation and modelling of thermal transport. Power dissipated on the cell is calculated using the measured voltage and current during the set pulse. The extracted cell temperature is close to the maximum growth-rate temperature for the melt-quenched GST. For the demonstrated method, it is crucial to define the simulated geometry and the thermal parameters as accurately as possible. This study is compared to a recent report of extraction of the maximum crystal-growth-rate temperature within a cell. While the mentioned report can extract the maximum-growth-temperature or melting temperature accurately, it requires an extensive electrical characterization of the devices. In contrast, our work can extract the temperature distribution within a cell as a function of time for any given set pulse. The extracted cell temperature, however, is only as accurate as the temperature-dependent thermal parameters used for the thermal modelling. The demonstrated method for PCM cell temperature extraction can be used to characterize the temperature-dependent crystallization process within a PCM cell.

SUPPLEMENTARY MATERIAL

See supplementary material for PCM endurance test, RESET pulse simulation, the effect of the load resistance, the temperature dependent materials parameters, and the effect of distance to the contacts.

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