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Citation: Journal of Applied Physics **116**, 234507 (2014);
View online: https://doi.org/10.1063/1.4904746
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JOURNAL OF APPLIED PHYSICS 116, 234507 (2014)

Suppression of thermoelectric Thomson effect in silicon microwires under large electrical bias and implications for phase-change memory devices

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(Received 27 October 2014; accepted 7 December 2014; published online 18 December 2014)

We have observed how thermoelectric effects that result in asymmetric melting of silicon wires are suppressed for increasing electric current density (J). The experimental results are investigated using numerical modeling of the self-heating process, which elucidates the relative contributions of the asymmetric thermoelectric Thomson heat ($\sim J$) and symmetric Joule heating ($\sim J^2$) that lead to symmetric heating for higher current levels. These results are applied in modeling of the self-heating process in phase-change memory devices. While, phase-change memory devices show a clearly preferred operation polarity due to thermoelectric effects, nearly symmetric operation can be achieved with higher amplitude and shorter current pulses, which can lead to design of improved polarity-invariant memory circuitry. © *2014 AIP Publishing LLC.*
[http://dx.doi.org/10.1063/1.4904746]

I. INTRODUCTION

Current-carrying conductors heat up due to conversion of electrical potential energy (qV) to heat, commonly known as Joule heating or self-heating. For a symmetric resistor structure, the electric field profile ($\boldsymbol{E} = -\nabla V$), hence current ($\boldsymbol{J} = \sigma \boldsymbol{E}$), is expected to be symmetric, resulting in a symmetric Joule heating ($\boldsymbol{E} \cdot \boldsymbol{J}$) profile. Besides electrical potential energy, charges also carry kinetic and chemical potential energies, the sum of which corresponds to $q\Pi$, where Π is the thermoelectric Peltier coefficient.[1] The energy transferred by charge carriers can be observed as thermoelectric Seebeck, Peltier, or Thomson effects.[2] Seebeck and Peltier effects appear as an open-circuit voltage in the presence of a temperature gradient and heating/cooling at junctions of dissimilar materials under an electrical current, respectively. Thermoelectric devices are typically formed by two dissimilar materials connected in series electrically and in parallel thermally.[2] Thomson effect is observed along self-heating homogeneous (junction-less) structures as skewed (asymmetric) temperature profiles as charge carriers absorb or release energy along the thermal gradient depending on the material $\Pi(T)$.[3–7] We have previously demonstrated that Thomson effect causes significant asymmetry in heating and melting of Si microwires biased with microsecond voltage pulses.[8,9] The electrical current polarity dependence of the heating profiles was demonstrated using low frequency AC biases causing the hottest spot on the wires to alternate between left and right locations.[8,9] For these Si wires, the main mechanism behind the asymmetry is understood as energy transfer from hotter to cooler regions of the wire through minority carrier generation and recombination (further discussed in Ref. 9). During further experiments on self-heating of Si wires through electrical pulses, we have found that the asymmetries disappear when the wires are subjected to larger amplitude, shorter duration electrical pulses. Here, we report the experimental results and elucidate the suppression of asymmetric heating using 3D numerical modeling of electrothermal transport in a Si wire. Implications of the observed phenomenon for phase-change memory (PCM) devices, the operation of which is based on self-heating, are also studied through modeling of the most common geometry (mushroom cell) for various electrical bias conditions.

II. EXPERIMENTS AND MODELLING OF SELF-HEATED SILICON MICROWIRES

The Si wires were formed by patterning highly phosphorus-doped nanocrystalline Si (nc-Si) films (t $\sim$ 50 nm). The nc-Si films were deposited on thermally oxidized single-crystal silicon wafers (SiO_2: $\sim$750 nm) in a low-pressure chemical vapor deposition system at 580 °C with high *in-situ* phosphorus concentration. Grain sizes are estimated to be 10–50 nm based on the scanning electron micrographs. The room-temperature resistivity, electron density, and mobility of the films were measured as 20.8 mΩ.cm, $(6 \pm 2) \times 10^{19}$ cm^{-3} and 4.4 ± 1.5 cm^{2}V^{-1}s^{-1} using a homemade Hall measurement setup (B: 0.8 T). The wires were released from the underlying SiO_2 using buffered oxide etch, remaining anchored to the substrate by the two large contacts. The fabrication process and temperature-dependent physical parameters of these wires were previously reported in Ref. 10. Wire lengths range from 1 to 5 μm and widths range from 0.2 to 1 μm. In the experiments, tungsten probes made direct contact with large Si pads $\sim$50 μm away from the wires. Three different pulse durations were used for the experiments: 30, 100 ns and 1 μs with 10 ns rise/fall time. For a given pulse duration, various pulse amplitudes were used to produce a variety of results from wire breakage to no structural change. As previously demonstrated, 1 μs pulses result in asymmetric wire modification and melting/crystallization (Figures 1(a)–1(d)) as a result of strong asymmetric self-heating (J: 5–10 MA/cm^2). For

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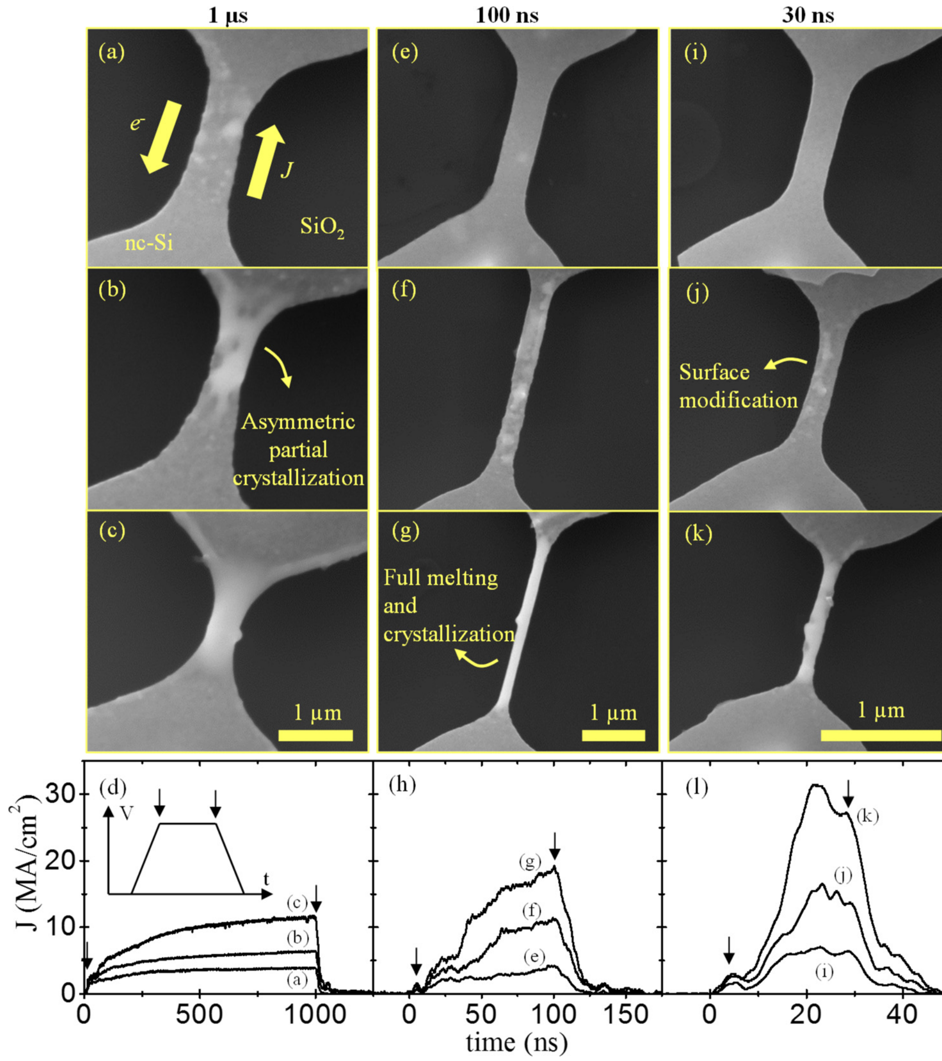

FIG. 1. SEM images of pulsed nc-Si wires for pulse durations of 1 μs (a)-(c), 100 ns (e)-(g), and 30 ns (i)-(k). Electric current and electron flow directions during the voltage pulses are shown in (a). Each column shares the same pulse duration and scale bar. (d), (h), and (l) Resulting current densities on the wires during the voltage pulses. Inset in (d) shows schematic of an applied pulse with 10 ns rise/fall time. Arrows in (d), (h), and (l) mark the pulse edges.

lower durations (30 and 100 ns), however, pulse amplitudes (J: 15–30 MA/cm^2) that are large enough to cause structural changes on the wires result in symmetric melting and crystallization (Figures 1(e)–1(l)). These results show that asymmetric self-heating and melting of the wires due to Thomson effect is suppressed for higher current levels.

To elucidate how asymmetric heating due to Thomson effect is suppressed at high electrical currents, the heat transfer and electrical conduction equations are solved simultaneously using COMSOL Multiphysics. The total current density consists of drift and diffusion currents and current continuity along the wires is assumed[11]

$$\nabla \cdot J = \nabla \cdot \left(\underbrace{\frac{-\nabla V}{\rho}}_{\text{Drift}} + \underbrace{\frac{-S\nabla T}{\rho}}_{\text{Diffusion}} \right) = 0, \tag{1}$$

where J is the electrical current density, V is the electrical potential, T is the temperature, ρ is the resistivity, and S is the Seebeck coefficient. The heat transfer expression accounts for the temperature change over time, heat transfer through conduction and heat generation through Joule and thermoelectric heating[12]

$$\underbrace{dC_P \frac{dT}{dt}}_{\text{Heat absorbed}} \underbrace{-\nabla \cdot (\kappa \nabla T)}_{\substack{\text{Heat loss}\\ \text{through}\\ \text{conduction}}} = \underbrace{\rho J^2}_{\substack{\text{Joule}\\ \text{Heat}}} + \underbrace{-TJ \cdot \nabla S}_{\substack{\text{Thermoelectric}\\ \text{Heat}}}, \tag{2}$$

where d is the mass density, C_P is the specific heat under constant pressure, and κ is the thermal conductivity. At junctions between different materials at uniform temperature (Peltier effect), the thermoelectric heat is due to the difference between the Seebeck coefficients of each material. In a uniform material, as in these silicon wires, the thermoelectric heat is due to the temperature gradient along the wires and temperature dependence of Seebeck coefficient ($\nabla S = dS/dT\ \nabla T$).[2] Joule heating depends on the current density (constant for a uniform cross section) and resistivity profile of the wires, which, in turn, depends on temperature. Thus, for a symmetric structure Joule heating results in a symmetric temperature profile with the hottest spot in the middle of the wires. Thomson heat, however, switches sign along the wire (causing heat absorption or additional heat generation) depending on the sign of the Seebeck coefficient gradient, which results in an asymmetric temperature profile. When current and temperature are weakly coupled (through

temperature-dependent material properties), as in the case of externally heated structures, Thomson heat ($\sim J$) is expected to dominate over Joule heat ($\sim J^2$) as J decreases[2] (see Thomson heat discussion in supplementary material[13]). In self-heating processes, however, current and temperature distribution are strongly coupled and the relative contributions of Joule and Thomson heat are expected to depend on specific geometry and bias conditions. In this work, we study these relative contributions in Si microwires self-heated by voltage pulses with varying amplitudes and durations.

The magnitude of the asymmetry (impact of Thomson heating on total heating) is quantitatively studied here using a 3D model for a wire similar to the ones used in the experiments (L: 2.5 μm, W: 0.5 μm) (Figure 2). A 20 kΩ load resistor in series with the wire is used to account for the resistance of the contact pads which are not drawn to keep the modelled structure small for practical computation times. For the same reason, the Si substrate is drawn thinner (5 μm) than it actually is (500 μm). Thermal boundaries (300 K at all times) are defined at the electrical contacts and bottom of the substrate. Although these are closer to the wire than they are in the experiments, they are far enough as not to affect the self-heating process. The voltage pulse amplitude is varied between 25 and 100 V in the simulations. Duration for each amplitude is kept just long enough to observe melting of most of the wire. Temperature dependent material parameters for nc-Si layer and constant parameters for SiO_2 and single crystalline silicon substrate layers are given in supplementary material.

The distance between the hottest spot location and the wire center (Δx) is used to quantitatively analyze the asymmetry in self-heating. Simulation results show that, as expected, Δx is larger for lower voltage (current) pulses (Figure 3) for the same maximum temperatures (close to melting). More interestingly, the simulations also show that significantly broader temperature profiles are obtained for

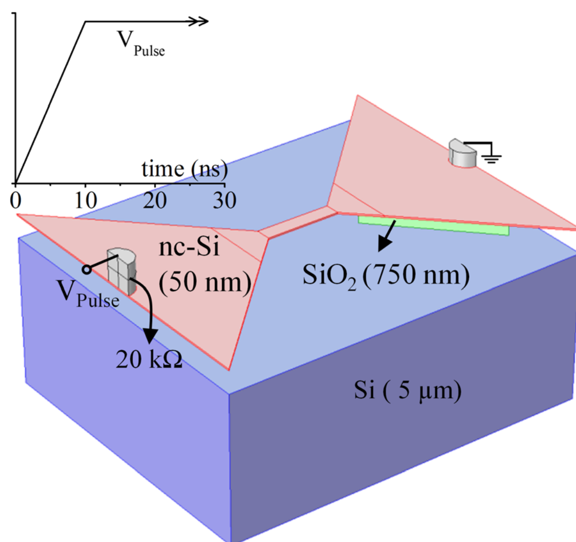

FIG. 2. 3D view of the modeled structure (L: 2.5 μm, W: 0.5 μm). The wire is released from the underlying SiO_2 layer by isotropically etching 0.9 μm of SiO_2. Layer thicknesses are given in parentheses. (Inset) Applied voltage pulse shape.

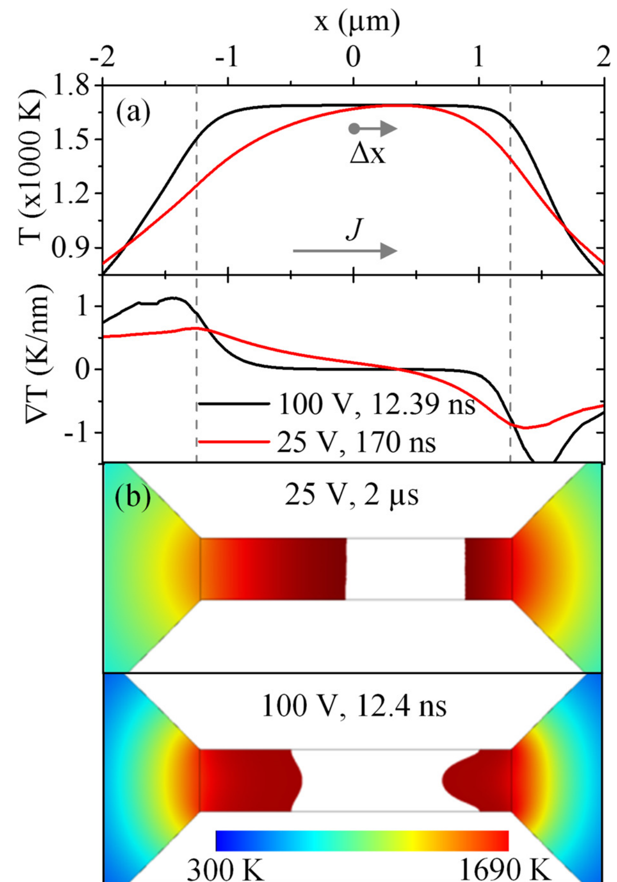

FIG. 3. Simulation results: (a) Temperature and temperature gradient profiles along the wire at the onset of melting for 25 and 100 V pulses. The magnitude and direction of the shift (Δx) in the hottest spot location is shown for the 25 V pulse. Vertical dashed lines mark the wire ends (x: ± 1.25 μm). (b) Temperature map on the wire for the indicated conditions. The melting regions (T > 1690 K) are shown in white. See time evolution of temperature on the wire for the 25 V case. (Multimedia view) [URL: http://dx.doi.org/10.1063/1.4904746.1]

high amplitude voltage pulses (Figure 3(a)), which further suppress thermoelectric heat for these conditions due to the smaller temperature gradient, hence smaller Seebeck coefficient gradient, along the wire. The broader temperature profiles are attributed to heat diffusion time constants (extracted as ~24 ns for a 2.5 μm long wire—see supplementary material) larger than or on the order of the pulse durations. The broader temperature profiles on the wire give rise to steeper temperature gradients near the wire ends, but since here the current density is small due to larger cross-section area of the contact pads and temperatures are lower, Thomson heat near the wire ends is insignificant. The contrast in the temperature profiles for low and high voltage pulses is more visible at the end of the pulses as shown by the temperature maps in Figure 3(b).

Figure 4(a) summarizes asymmetries (Δx) observed in the simulations. The largest Δx for a given voltage pulse condition is observed at the onset of melting. Δx increases up to the onset of melting due the rising temperature profile, hence the temperature gradient profile, which, in turn, increases the current through the wire. The smallest voltage pulse amplitude required to melt the wire (25 V) shows the largest Δx,

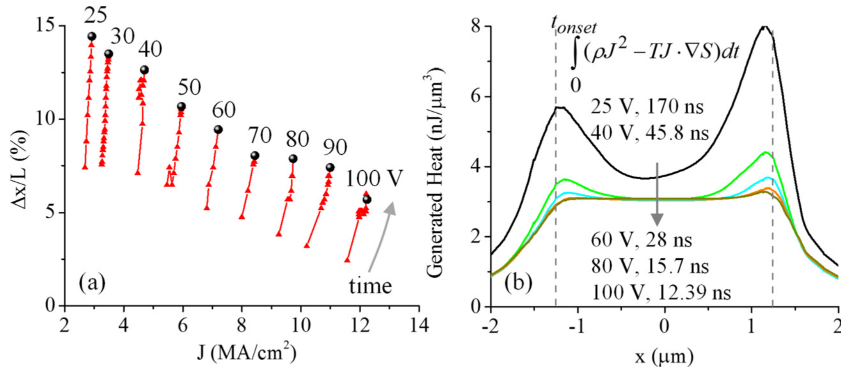

FIG. 4. Simulation results: (a) Shift in the hottest spot location (Δx) scaled with the wire length as a function of current density prior to melting. Black dots show values at the onset of melting. Pulse amplitudes are shown next to each curve. (b) Total generated heat (sum of Joule and Thomson heat) along the wire up to the onset of melting for indicated voltage levels and time steps. Vertical lines indicate the wire ends. Every other voltage pulse amplitude is skipped for clarity.

owing to the maximum ratio of asymmetric thermoelectric heating to symmetric Joule heating. This is illustrated by comparing the total generated heat (Joule + Thermoelectric heat) up to the onset of melting for various voltage pulse amplitudes (Figure 4(b)). More heat is generated at the ends of the wire (cooler regions) due to the higher electrical resistivity of Si wires at low temperatures. The difference between these peaks at the ends of the wire leads to the asymmetry in the temperature profiles. Lower amplitude pulses result in more total heat generation due to longer pulse durations despite the smaller current levels.

Transient simulation results shed more light on the self-heating process: Current through the wire increases sharply in the first 10 ns due to the rising voltage (Figure 5(a)) and keeps increasing for the constant voltage owing to decreasing wire resistance with increasing temperature (negative temperature coefficient of resistivity—material parameters provided in supplementary material). For all voltage pulse cases, after a small portion of the wire starts melting, the liquid-solid interface advances in both directions leading to a slowly growing molten region (see supplementary video). As the wire melts, temperature within the melting region stays between 1690 and 1700 K (Figure 5(b)) due to the large latent heat incorporated in the heat capacity function in this temperature range. The hottest spot is located in the middle of the wire (Δx: 0) (Figure 5(c)) at the beginning of the pulse. Then, it slightly skews towards the higher potential end—outlet for electrons—for peak temperatures smaller than 1100 K (Figures 5(c)–5(e)), as electrons release their excess energy, gained at hotter regions of the wire, before leaving the wire (Figure 5(f)). This mechanism is captured in the Seebeck coefficient, which is increasing in magnitude with temperature up to 1100 K. Beyond this temperature, thermal generation of minority carriers dominates resulting in net thermoelectric heat carried towards the lower potential end—outlet of holes—causing the hottest spot to shift towards this end. We have referred to this process as generation–transport–recombination (GTR) of minority carriers as introduced and analyzed in detail in Ref. 9. The process of GTR is captured in the overall Seebeck coefficient, which decreases in magnitude beyond 1100 K. Once the wire starts melting, the hottest spot is assumed to be at the center of the melting region (1690 K < T < 1700 K) for tracing the time evolution of the asymmetry in the temperature profiles. Pulse durations for the large voltage pulses are kept short since the simulations tend to diverge as the wire melts due to the sudden changes in the material parameters.

III. IMPLICATIONS FOR PHASE-CHANGE MEMORY DEVICES

Suppression of thermoelectric effects in self-heating can be useful in PCM devices, where it has been shown that thermoelectric effects play an important role and result in a preferred operation direction.[14–18] In PCM devices a small active volume is toggled between high resistance amorphous

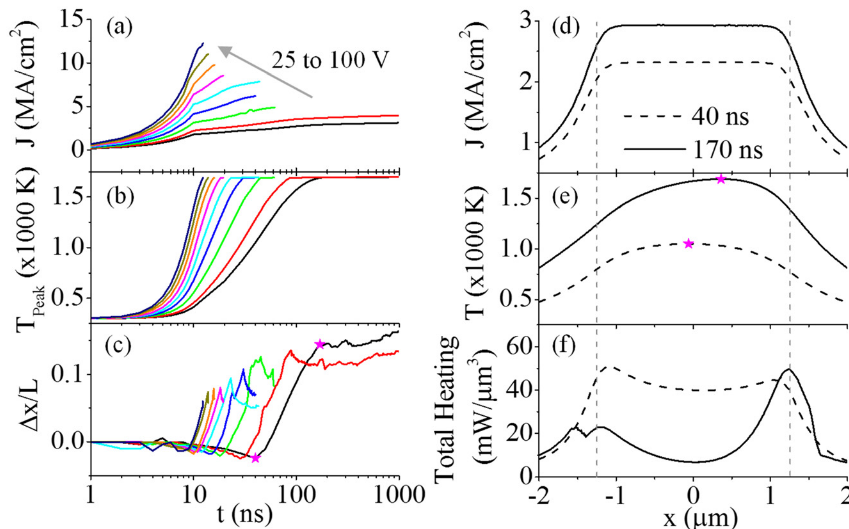

FIG. 5. Simulation results: Transient response of (a) current density, (b) peak temperature on the wire, and (c) shift in the hottest spot location for voltage pulse amplitudes of 25, 30, 40, 50, 60, 70, 80, 90, and 100 V. Two symbols in (c) mark the largest shift towards the higher potential end (40 ns) and the shift at the onset of melting (170 ns) for the 25 V pulse case. (d) Current density, (e) temperature, and (f) total heat profiles along the wire for the 25 V pulse at time steps marked in (c) (40 and 170 ns). Vertical lines mark the wire ends. Two symbols in (e) mark the peaks.

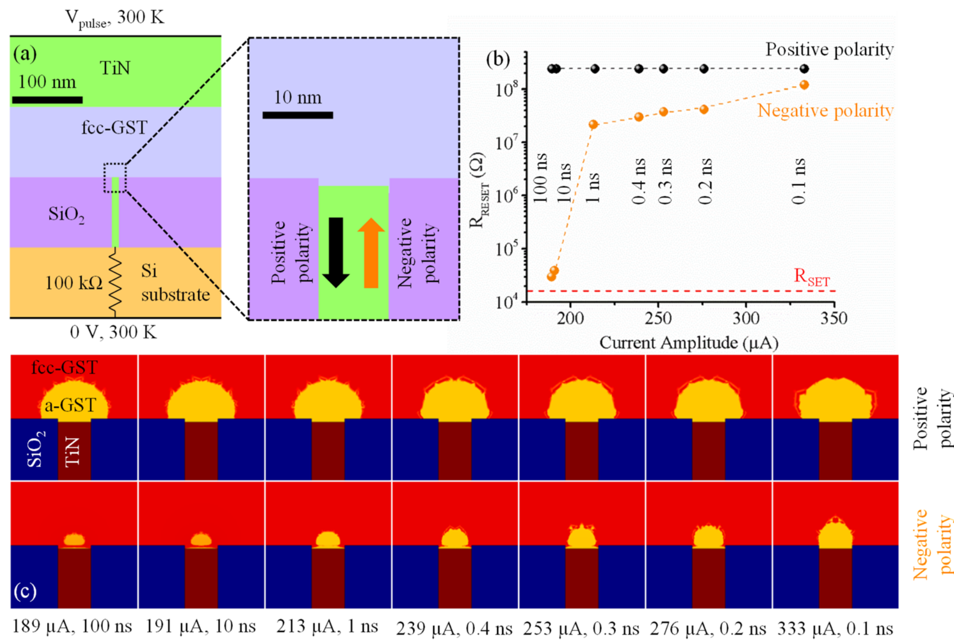

FIG. 6. (a) Cartoon illustration of the simulated phase-change memory cell (cross-section view) in SET (low resistance) state showing the layers forming the cell and electrical/thermal boundary conditions. An external 100 kΩ resistor is connected in series with the cell to limit the current. Close-up shows the active region with the recessed heater (1 nm) and current directions for the positive/negative voltage polarity configurations. (b) RESET cell resistance after pulses with indicated pulse conditions: polarity, current amplitude, pulse duration. SET resistance level is marked with a red dashed line. (c) Resistivity map of the cell around the active region after the RESET pulse for the indicated pulse conditions.

phase and low resistance crystalline phase using self-heating.[19] The most common PCM structure, mushroom cell (Figure 6(a)), is asymmetric along the current path in contrast to symmetric Si wire structures. As a result of this asymmetry, the phase-change material on top of the narrow bottom electrode (heater) heats up the most due to the current confinement around the heater. The effect of thermoelectric transport in these structures is observed when the current direction is reversed, which leads to different amounts of self-heating, hence molten (and amorphized) volume[14–18] in the active region. The amorphized volume during RESET determines the high resistance (RESET) state, hence the resistance ratio for the memory cell. We have recently shown that when the current flow is directed from top (large) to bottom (narrow) electrode, thermoelectric heating (Peltier heat at the junction and Thomson heat within the phase-change material) adds to Joule heating.[17] When the current direction is reversed, thermoelectric cooling within the active volume counters the Joule heating resulting in a smaller molten, hence amorphous volume. The same resistance ratio can therefore be achieved with lower power consumption if the preferred polarity is used. Interestingly, it has been observed that this same polarity also leads to reduced void formation and elemental segregation, hence improved device reliability, a major difficulty with PCM devices.[20,21] A preferred operation polarity, however, restricts memory array circuit schemes. Although the geometry of a mushroom cell is distinctly different from that of the Si wires, both of them use self-heating, which is captured by Eqs. (1) and (2) in the simulations. Hence, Joule heating is expected to dominate over thermoelectric heating with increased current in phase-change memory cells, as well as in any other self-heated structures.

The effect of thermoelectric transport in a mushroom PCM cell biased with increasing voltage pulse amplitudes is studied here. The geometry, material parameters, and physical models from our previous computational work[17] are used. The PCM simulations use the same set of equations (Eqs. (1) and (2)). The thermoelectric heat is defined as Thomson heat within the GST and TiN layers and as Peltier heat at the GST-TiN interfaces. The electrical resistivity for fcc-GST uses a metastable approach, where the material does not transition to hcp phase with increasing temperature but keeps its fcc phase up to the melting temperature. Electronic contribution in the thermal conductivity is accounted for using the Wiedemann-Franz law. The Seebeck coefficient of GST is measured up to 650 K and extrapolated up to the melting temperature of GST. Owing to its confined geometry, the temperature-dependent thermal boundary resistances between GST-TiN, GST-SiO_2, and SiO_2-TiN interfaces are included in the simulations. Reference 17 provides a complete study of thermoelectric effects on a PCM cell. In this previous work, current is controlled using a transistor, available in the simulation tool's SPICE module, connected in series with the PCM cell. This method, however, yields slightly different current amplitudes for opposite voltage polarities. Hence, here, a 100 kΩ load resistor is used to limit the current, while varying the pulse amplitude (Figure 6(a)). For the positive polarity configuration, the electrical pulse amplitudes are chosen such that the same RESET resistance is achieved for various pulse durations (0.1 to 100 ns) (see supplementary material for applied voltage pulse amplitudes and resulting currents). The same electrical pulse configurations (amplitude and duration) are then used for the negative polarity resulting in smaller amorphous volumes, hence RESET resistances (Figures 6(b) and 6(c)). The difference between the RESET resistances for positive and negative polarities decreases with increasing voltage amplitudes, due to dominant Joule heating, suggesting that symmetric operation of PCM cells is possible when large amplitude, short duration pulses are used (Figures 6(b) and 6(c)).

IV. CONCLUSIONS

In summary, it is shown that asymmetric self-heating of silicon microwires under microsecond pulses due to thermoelectric Thomson heat is suppressed when higher amplitude electrical pulses are used and Joule heating dominates. Numerical simulations elucidate the relative contributions of Thomson and Joule heat for the different bias conditions and show that thermoelectric heat on the wire is further suppressed for larger currents due to broader temperature profiles, hence smaller temperature gradients within the wires. Broader temperature profiles result from characteristic heat diffusion time constants that are comparable to the short pulse durations used for the large amplitude pulses. These observations are applied to study the effects of pulse amplitude and duration on the self-heating process in phase change memory devices. While these devices show a preferred operation polarity under normal operating conditions due to thermoelectric transport, nearly symmetric operation can be achieved through the use of larger amplitude, shorter duration voltage pulses. Polarity invariant operation of phase-change memory may allow more efficient memory array programming schemes and peripheral circuitry.

ACKNOWLEDGMENTS

This work was supported by the U.S. Department of Energy Office of Basic Energy Sciences (DE-SC0005038). Gokhan Bakan also acknowledges the support through TUBITAK Bideb-2232 fellowship (114C063) during the preparation of this manuscript. The authors thank Azer Faraclas for providing his previous phase-change memory device simulation files and Lhacene Adnane for characterizing the temperature-dependent resistivity and Seebeck coefficient of nc-Si.

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