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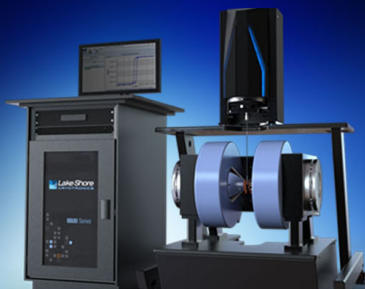
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Voltage contrast X-ray photoelectron spectroscopy reveals graphene-substrate interaction in graphene devices fabricated on the C- and Si- faces of SiC

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We report on an X-ray photoelectron spectroscopy (XPS) study of two graphene based devices that were analyzed by imposing a significant current under +3 V bias. The devices were fabricated as graphene layer(s) on hexagonal SiC substrates, either on the C- or Si-terminated faces. Position dependent potential distributions (IR-drop), as measured by variations in the binding energy of a C1s peak are observed to be sporadic for the C-face graphene sample, but very smooth for the Si-face one, although the latter is less conductive. We attribute these sporadic variations in the C-face device to the incomplete electrical decoupling between the graphene layer(s) with the underlying buffer and/or substrate layers. Variations in the Si2p and O1s peaks of the underlayer(s) shed further light into the electrical interaction between graphene and other layers. Since the potential variations are amplified only under applied bias (voltage-contrast), our methodology gives unique, chemically specific electrical information that is difficult to obtain by other techniques. © 2015 AIP Publishing LLC.

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Graphene, with its superb properties, has been the focus of intense investigations for over a decade.^{1–19} Attention paid to graphene grown on SiC has been more intense due to its potential adoptability into silicon technology, and wafer-scale graphene integrated circuits have already been fabricated with superior properties, which are expected to be improved further.^{13,14} In this work, we focus on two devices made out of graphene grown on SiC(0001), referred to as Si-face or Si-terminated substrate SiC, and SiC(000 $\bar{1}$), so-called C-face or C-terminated SiC. The layer structure and electrical properties of graphene films grown on two faces have been reported to be quite different from each other.⁹ For instance, growth rate of the epitaxial graphene (EG) is much faster on C-face so that at the same growth temperature, multiple layers of graphene are more readily formed on the C-face than on the Si-face substrates.¹⁵ Electrical properties of graphene are strongly related to morphology, and epitaxial graphene structures contain disorders and defects.^{10,16,17} Several successful experimental strategies have been developed to reduce this unavoidable graphene substrate chemical/electrical interaction using intercalating agents and thermal treatments.^{17–20} In general, additional chemical/physical treatments are also implemented for fabrication of devices derived from them, and each process introduces further defects, impurities, etc. For this reason, graphene-substrate interaction, as well as role of defects within graphene layer(s) should be well understood and characterized for the final device, preferably under working conditions.

Optical absorption and reflection, Raman spectroscopy, and scanning probe microscopy techniques have also been extensively used to assess electrical properties.^{21–27} However,

all of these techniques can only provide indirect information about the variations in the charge density and the Fermi energy and do not have significant chemical specificity. Microscopic techniques, such as scanning Kelvin-probe, are powerful in terms of probing electrical variations, with a resolution down to 1 meV, but are also incapable of yielding chemical information.²⁸

Ultra-Violet (UPS), X-ray (XPS), and synchrotron-based photoemission techniques have been utilized for probing the nature of graphene layers grown on different faces of SiC, revealing important, but at the same time somewhat conflicting, information.^{29–39} In addition to its superb chemical specificity, an important but under-utilized aspect of XPS is its ability to detect shifts in the position of the peaks as a result of developed or imposed voltage stresses, which has been used by our group to extract chemically specific electrical properties of material surfaces and devices.⁴⁰ We showed that the potential drop across the entire surface of a pristine graphene sheet was uniform between two gold electrodes by imposing a d.c. bias across the device, and observed that the uniformity was lost after mild oxidation, because of defects and cracks created during the oxidation process.⁴¹ We also reported on similar observations on a gate-tunable graphene layer on Si₃N₄/Si substrate, where tuning was evidenced by the shifts in peak positions of the C1s of the graphene sheet and the Si2p (or N1s) of the substrate.⁴² The present report extends our work concentrating mostly on similarities and differences of the measured voltage variations between graphene layer(s) on C- and Si-face of SiC substrate. As in our previous study, the local voltage variations are detected as binding energy shifts in the corresponding core levels, while the device is operating under a current imposed by application of +3 V across the gold electrodes. This experimental variant drastically amplifies and sheds important light onto

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graphene-substrate electrical interactions, which is not possible to harvest by other techniques.

Samples, consisting of epitaxial graphene grown at 1600 °C by the CVD technique,¹⁹ on (10 × 10) mm² nominally on-axis 4H-SiC (0001) Si-face and C-face, chemo-mechanically polished substrates, were used. Graphene layers were grown under an argon laminar flow within a hot-wall Aixtron VP508 reactor. The process relies critically on creation of dynamic flow conditions in the reactor that control the Si sublimation rate and enable the mass transport of hydrocarbon (propane) to the SiC substrate.

Devices were fabricated using various lithographic techniques.^{43,44} Ohmic contacts were incorporated with the reverse lithography technique. After development, 20 nm titanium and 100 nm gold layers were deposited with an e-beam evaporator, followed with the standard lift-off process. The base pressure of the e-beam evaporator is 8×10^{-6} mbar. The samples were not exposed to air in between depositions of Ti/Au gold pair. Gold was evaporated right after titanium deposition inside the same chamber. The mesa lithography step was performed in order to preserve the active graphene region, while etching rest of graphene on the surface with O₂ plasma. After etching, a 500 μm × 1100 μm active graphene region was retained. Finally, devices were bonded for electrical and XPS measurements, having resistances of 400 and 700 Ω for the C- and Si-face samples, respectively. I-V data of the two devices are given in the supplemental material as Figure S1(d).⁴⁷ Raman spectra of the two samples are given in Figures S2(a) and S2(b). The spectra of the two materials, as produced, are very similar. However, after fabrication steps, we were able to record a reasonable Raman spectrum of graphene only for the C-face device as shown in Figure S2(c). Only SiC peaks are evident for the Si-face device after fabrication [Figure S2(d)]. AFM images of the samples are also given as Figures S4 and S5.

XPS measurements are carried out using Thermo-Fisher K-Alpha spectrometer with monochromatic AlK α x-rays. Take-off angle for the photoelectrons is normal to the sample surface. The system is modified to allow external biasing of the sample. High-resolution spectra of elemental peaks were recorded with 0.1 eV steps. Spectra were also recorded in the line scan or in the areal mapping modes with variable X-Ray spot as well as step-sizes, from 30 to 400 μm. For the data presented in this paper, all spectra were recorded with an X-ray beam size of 30 μm. Data acquisition and analyses are controlled by Avantage software.

Conventional XPS analysis carried out on two samples are shown in Figure 1 for the C1s, Si2p, and O1s regions. For the C-face, C1s peaks representing the graphene layer(s) and the SiC substrate are well-separated from each other and slightly oxidized features broaden the graphene component on the high binding energy side, but the corresponding peaks for the Si-face can only be resolved by curve-fitting. Intensity and position of the peaks are consistent with published data.^{15,30–39} For the C-face, the intensity ratio of the C1s peaks of the graphene to the carbide is used to estimate the thickness of the graphene as 2.5 nm. This confirms its multilayered structure, as opposed to 1.6 nm for the Si-face, suggesting a thinner graphene layer.¹⁵ Details of the thickness estimation are given in the supplemental material.⁴⁷

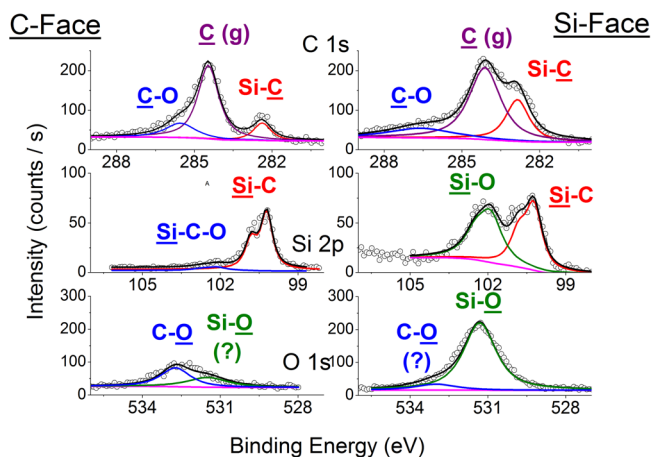


FIG. 1. Conventional scanned XPS spectra; C1s, Si2p, and O1s regions of the C- and Si-face samples. Data given as counts/s are only meaningful for the same sample, but direct comparison between samples is not valid due to variations in photon intensity.

Si2p doublet corresponding to the carbide is very sharp for the C-face, and has only a small oxidized component, since it was well protected from oxidation in the post treatments. The difference in the Si region of the Si-face is the existence of a large oxidized component in the high-binding energy side, with a large corresponding O1s peak, pointing to a stoichiometric SiO₂ layer. This feature forms during the device fabrication steps, since we did not observe such a component for the corresponding sample before device fabrication, as shown in Figure S3 of the supplemental material.⁴⁷ No significant component exists for the C-face. Hence, we can now draw a partial conclusion that the formation of an oxidized silicon buffer/intercalation layer between the graphene layer and the SiC substrate is successful only for the Si-face sample, and the graphene layers protected the substrate from oxidation for the C-face one, in accordance with the literature.^{8–19} All of these parameters contribute critically to the performance of the final device and information related to them is of utmost importance.

Extension of the measurements to the entire surface of the sample is possible but takes much longer, hence the snapshot mode of data collection is used for the displayed areal maps of Au4f, C1s, and Si2p peaks, using a 30 μm X-ray spot-size with 30 μm steps, shown in Figures 2(a)–2(c), respectively, for the C-face device, and Figures 2(d)–2(f) for the Si-face one. A cursory visual analysis reveals information related to uniformity and/or presence of morphological defects, like the one appearing in Figure 2(b) for the C-face sample, as a less intense “spot” in the C1s map, and a darker one in the Si2p map. Note, however, that the presence of this “spot” is not detrimental to the device’s performance, since the overall resistance of it is 400 Ω, lower than the more uniform Si-face device, as shown in Figure 2(e), which has a higher overall resistance of 700 Ω.

The results of the measurements by application of a bias between the two electrodes are shown in Figure 3 as areal maps of the position of the peaks starting from the first electrode at +3.00 V towards the grounded one. Variations in the measured binding energies of C1s peak of the C-face are depicted in panels (b) and (c), and for the Si-face in (d) and (e), as well as those

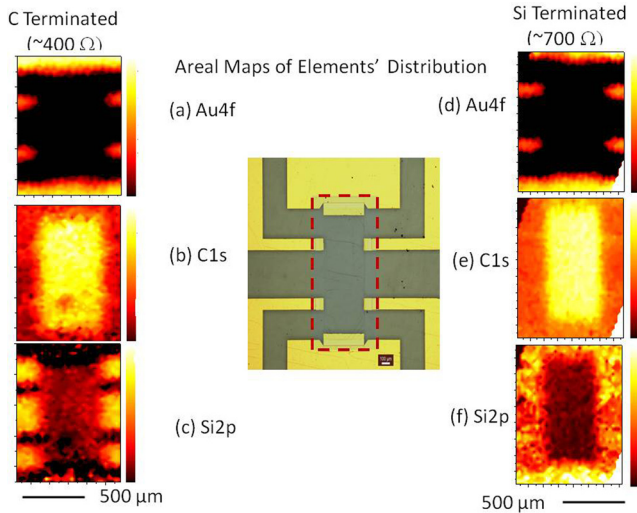


FIG. 2. Areal maps of the intensity of (a) Au4f, (b) C1s, and (c) Si2p signals for the C-face, and (d)–(f) for the Si-face devices.

of the Au4f in (a) of the electrodes. Imposing a steady-state current amplifies morphological defects as well as voltage variations since such irregularities are now projected onto the voltage-space. The collected data are vast (Au4f, C1s, Si2p, and O1s spectra for each sample at $30 \times 50 = 1500$ spots) and require careful analysis. However, we will concentrate only on

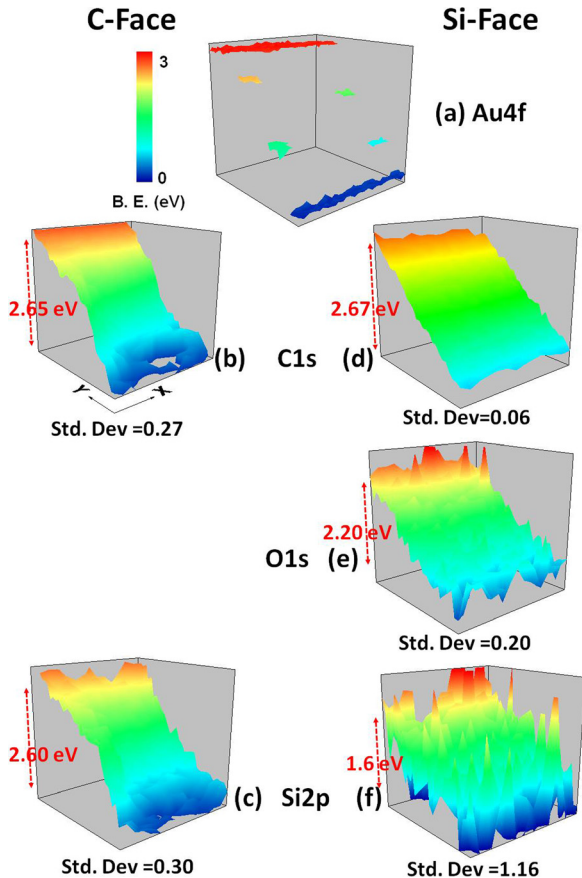


FIG. 3. (a) Summary of the XPS measurements under an external bias of +3 V. Areal maps of the measured binding energies: (a) Au4f_{7/2}, (b) and (d) C1s, (c) and (f) Si2p of the entire sample for the C- and Si-faces, (e) O1s for the Si-face only. Measured overall shifts, as well as the computed standard deviations for each case are also shown.

points, regarding mostly; (i) the overall voltage drop across the metal electrodes, (ii) their variations from the mean, quantified by computed standard deviations, and (iii) correlations between the sets of spectra,⁴⁷ as computed by the correlation coefficients, as given in Table I. Here, it is also important to stress that the probe depth of XPS is ~ 10 nm, hence, both graphene and also underlayers are probed. Furthermore, as we pointed out previously, although it is generally difficult to analyze insulating layers with XPS due to charging, graphene overcomes this difficulty by providing a conductivity blanket to the underlayer it is in contact with.⁴¹

As indicated in Figure 3, the voltage drop is measured as 2.95 eV on Au4f_{7/2} peak for both samples, well within experimental uncertainty of the applied +3.00 V, validating applicability of our technique. Voltage drops measured on C1s for C- and Si-faces are 2.65 and 2.67 eV, respectively, and are lower than 2.95 eV. This small but significant difference is due to contact resistance between gold electrode(s) and graphene layer(s)^{45,46} and will not be dwelled upon further in this work. However, the fact that the overall full voltage drop, save for the contact resistance, is measured in the C1s for both samples is indicative of a graphene layer acting as a faithful resistive element in both devices. In contrast, although the measured Si2p voltage drop is also full and has the value of 2.60 eV for the C-face, it is only 1.6 eV for the Si-face, which can be interpreted as the Si-underlayer being in good electrical contact in the C-face device only. The O1s drop is 2.20 eV, measurable only for the Si-face, which is a value in between those of C1s and Si2p. Hence, the electrical contact between the graphene and the underlayer is weak for the Si-face sample.

On the other hand, variations in the measured binding energies of the C 1s across the graphene layer(s), as revealed by their computed standard deviations, are much larger for the C-face (0.27) compared with the Si-face (0.06). Interestingly, the Si2p variations are similar to that of the C1s for the C-face (0.30) but are very large for the Si-face (1.16), and those for the O1s is in between that of C1s and Si2p for the same sample. These observations are consistent with the above-mentioned findings. The most interesting outcome of such analyses is that despite the fact that geometrical and morphological irregularities/asperities are much more pronounced and sporadic in the C-face device when compared to the Si-face one, the former has a smaller overall electrical resistance.

Reproducibility checks were performed for both samples but are shown for the Si-face one by recording exactly the same data but without using the flood-gun in Figure S6 of the supplemental material, yielding the same variations as those using the flood gun as also shown in the same figure (same data as in Figure 3).⁴⁷ For checking the consistency of our measurements, we repeated the C1s measurements under

TABLE I. Computed correlation coefficients between the sets of measured binding energies.

	C1s/Si2p	C1s/O1s	Si2p/O1s
C-face	0.98	-	-
Si-face	0.62	0.92	0.56

+6 V, as shown in Figure S7.⁴⁷ Although, the absolute value of the voltage variations is doubled in comparison to those displayed in Figure 3(d), they are also very smooth throughout the entire surface, and moreover, they display exactly the same average standard deviation of 0.06. However, when the chemical integrity of the same surface is intentionally degraded with a mild (~ 200 eV) Ar⁺ etching, which is known to partially destroy the graphene honeycomb structure, the resistance jumped to 22.2 k Ω , and the measured C1s energy variations became discontinuous as also shown in Figure S7.⁴⁷ At the same time, the standard deviation of the C1s peak positions increased more than one order of magnitude to 0.63.⁴⁷

Parallel and supportive findings also emerge from the computed correlation coefficients given in Table I. Whereas the correlation coefficient between the C1s and Si2p sets of data for the C-face is very large (0.98), for the Si-face it is only 0.62 and approaches 0.92 between C 1s and O 1s sets. We can also infer that there is a significant correlation of the electrical properties between graphene and underlayer(s) for the C-face, and the lack of it for the Si-face.

Combining all these findings and the well-known difference between the graphene layers of the C- and Si-faces,^{9–21} we are now bolstered to postulate that current is limited to transport predominantly through graphene layer in the Si-face (2D transport), such that the voltage drop is more or less constant and uniform laterally along the perpendicular direction, and changes linearly in parallel with the direction of the current. In stark contrast, current transport is chaotic, involving both 2D and 3D components for the C-face, leading to the observed sporadic variations. We attribute these observations to the presence of a successful buffer and/or intercalation layer under the graphene in the Si-face, and the lack of it in the C-face. Naturally, more work is needed to comprehend nature and magnitude of the various electrical and chemical interactions tapped for improving material and device properties, but one thing is clear that the voltage contrast XPS analysis gives us a unique and fresh perspective. We also hope that this will initiate further theoretical studies to accurately relate the transport properties of real-life graphene samples to these measurements.

In summary, we used a variant of XPS to analyze two devices fabricated from graphene grown on C-face and Si-face of SiC substrates by imposing +3 V across gold electrodes with graphene in between. This method introduces changes in the binding energy positions of core levels of graphene, as well as the layers below, including that of the SiC substrate. These changes reveal vital electrical information about the graphene, as well as its interaction with the substrate. For the two devices analyzed, we found that the C1s binding energy variations are much larger for the C-face device when compared to the Si-face one, although the former has a lower resistance. This surprising result is attributed to the reduced graphene-substrate interaction in the Si-face device, realized by successful incorporation of the buffer layer. This claim is further supported by the variations measured on the Si2p and O1s peak positions representing the underlayers. Thus, by imposing potential stress while recording XPS data, one is able to probe the otherwise hidden electrical properties of surface structures in a chemically specific way,

which can be of utmost importance especially for assessment of device performance(s).

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