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## Enhanced memory effect via quantum confinement in 16 nm InN nanoparticles embedded in ZnO charge trapping layer

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In this work, the fabrication of charge trapping memory cells with laser-synthesized indium-nitride nanoparticles (InN-NPs) embedded in ZnO charge trapping layer is demonstrated. Atomic layer deposited Al<sub>2</sub>O<sub>3</sub> layers are used as tunnel and blocking oxides. The gate contacts are sputtered using a shadow mask which eliminates the need for any lithography steps. High frequency C-V<sub>gate</sub> measurements show that a memory effect is observed, due to the charging of the InN-NPs. With a low operating voltage of 4 V, the memory shows a noticeable threshold voltage (V<sub>t</sub>) shift of 2 V, which indicates that InN-NPs act as charge trapping centers. Without InN-NPs, the observed memory hysteresis is negligible. At higher programming voltages of 10 V, a memory window of 5 V is achieved and the V<sub>t</sub> shift direction indicates that electrons tunnel from channel to charge storage layer.

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In recent years, indium-nitride nanoparticles (InN-NPs) have gained a growing attention owing to their excellent optoelectronic properties such as high electron mobility, high saturation velocity due to their low effective mass,<sup>1,2</sup> small band gap, terahertz/near-infrared emission, and high surface electron accumulation.<sup>3-5</sup> In addition, InN-NPs have the largest electron affinity among all semiconductors, which is estimated to be 5.5–6.1 eV with respect to the vacuum level.<sup>6,7</sup> This large electron affinity is a desired property for charge trapping materials in memory devices because it increases the energy barrier for electrons stored in the InN-NPs, which exponentially reduces the charge leakage; therefore, the retention characteristic of the charge trapping memory cell is improved.

In order to compare the InN NPs performance directly with other materials, the gate stack of the memory structure has to be similar, since the tunnel oxide thickness and material have great impact on the memory performance, specifically on the retention characteristic of the memory device. As a matter of fact, in our previous work,<sup>8</sup> a charge trapping memory with 2-nm Si nanoparticles (Si-NPs) embedded in ZnO was demonstrated. The memory showed hole trapping with a 41% loss of the initial charge in 10 yr and a reduced operating voltage. The very small electron affinity of the Si-NPs supports the observed results. In this work, the performance of the memory with laser-synthesized InN-NPs, which have a much larger electron affinity, is demonstrated. In this memory device, n-type ZnO grown by Atomic layer deposition (ALD)<sup>9-13</sup> is also used as charge trapping layer. In addition to enhancing the electric field across the tunnel oxide, ZnO layer adds additional trap states, which reduce the required operating voltage in order to achieve the memory effect. The charge trapping characteristics of InN-NPs are

explored using high frequency C-V<sub>gate</sub> measurements on MOS charge trapping memory cells.

Colloidal InN-NPs were prepared by laser ablation process using a commercial nanosecond pulsed neodymium-doped: yttrium aluminium garnet (Nd:YAG) laser (Empower Q-Switched Laser, Spectral Physics).<sup>14</sup> The laser was operated at 527 nm with a pulse duration of 100 ns and a repetition rate of 1 kHz. Laser output power of 16 W and a pulse energy of 16 mJ were used. The target was placed in a glass vial filled with 20 ml ethanol solution. The laser beam was focused on the target using a plano-convex lens with a focal length of 50 mm. The height of liquid layer over InN target is 5 mm and the laser ablation lasted for 5 min. A TEM image of the 16 nm average sized spherical InN-NPs is depicted in Fig. 1.

The MOS memory cells were fabricated on an n<sup>+</sup>-type (111) (antimony doped, 15–20 mΩ·cm) Si wafer. 3.6-nm-thick Al<sub>2</sub>O<sub>3</sub> tunnel oxide followed by 2-nm-thick ZnO charge trapping layer were deposited at 250 °C using

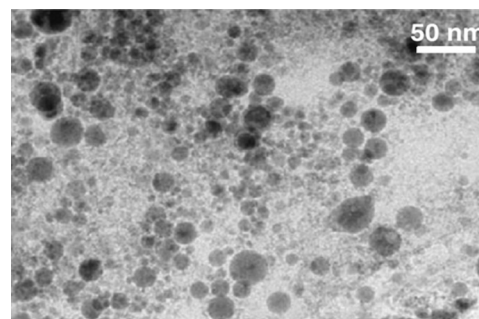


FIG. 1. TEM image of the laser-synthesized non-agglomerate InN nanoparticles.

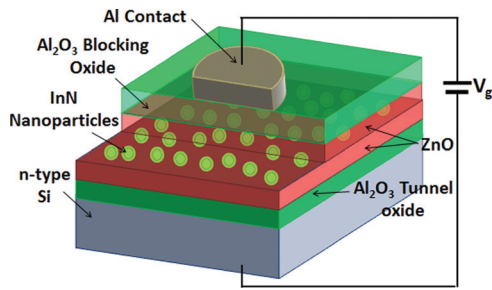


FIG. 2. Schematic cross-section of the fabricated charge trapping memory cell with embedded InN nanoparticles.

Cambridge Nanotech Savannah-100 ALD system. The InN-NPs in solution was then spin casted on to the substrates with a spin speed of 700 rpm, 250 rpm/s ramp rate for 10 s and samples were left to dry for 5 min on hot-plate. Then a 2-nm-thick ZnO charge trapping layer followed by a 15-nm-thick Al<sub>2</sub>O<sub>3</sub> blocking oxide were deposited at 250 °C by ALD. Finally, using a shadow mask with 1 mm openings, a 400-nm-thick Al layer was sputtered as the gate contact. It is worth to mention that the use of the shadow mask eliminates the need for additional photolithography steps which further reduce the cost of fabrication of such memory structures. Fig. 2 shows a cross-sectional illustration of the final device structure with InN-NPs.

In order to analyze the charge trapping characteristics of the InN-NPs, C-V<sub>gate</sub> measurements at high frequency (1 MHz) were conducted on the memory cells using the Agilent-Sigatone B1505A probe station-semiconductor device analyzer. The gate voltage of MOS memory cells was first swept from -2 V to 2 V, which is too low to achieve any noticeable charging and the threshold voltage (V<sub>t</sub>) shift was indeed zero. Then, by sweeping the gate voltage from -10 V to 10 V, the same curve was obtained, which indicates the erased state as depicted in Fig. 3. Sweeping the gate voltage in the opposite direction from 10 V to -10 V shows a shifted version of the erased state curve to the right, which indicates that electrons are being stored and a 5.5 V V<sub>t</sub> shift is achieved as shown in Fig. 3. The analysis of the C-V<sub>gate</sub> curves indicates that InN-NPs are trapping only electrons and not mixed charges unlike typical charge trapping materials.<sup>11,15</sup>

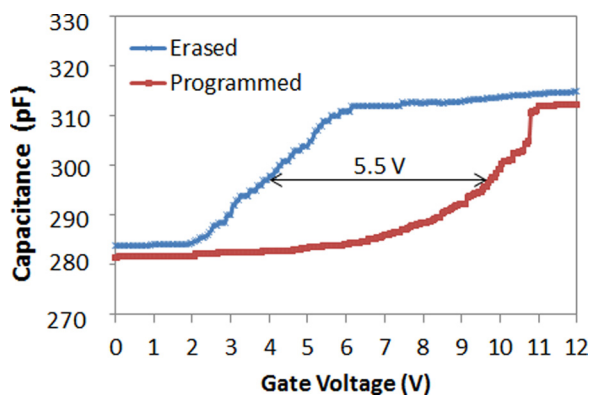


FIG. 3. Hysteresis measurement using high frequency C-V<sub>g</sub> characteristics showing the obtained V<sub>t</sub> shift with InN nanoparticles. The curves are obtained by sweeping the gate voltage from -10 V to 10 V forward and backward.

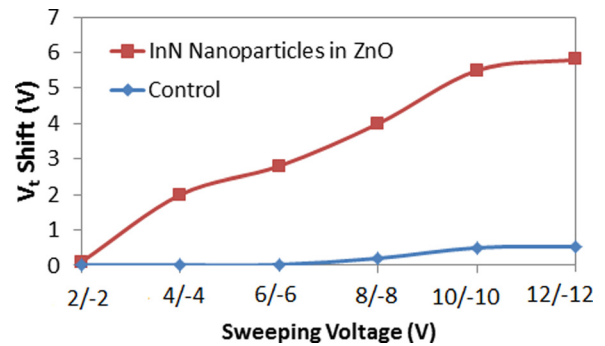


FIG. 4. V<sub>t</sub> shift vs. gate voltage sweeping with InN nanoparticles.

Furthermore, the C-V<sub>gate</sub> characteristic shows a flat-band voltage which is significantly shifted to the right. This confirms the n-type nature of ALD-deposited ZnO due to native crystallographic defects, such as oxygen vacancies and zinc interstitials, which act as electrons donors.<sup>9,10,17</sup> The obtained V<sub>t</sub> shift at different gate sweeping voltages was measured and plotted in Fig. 4. The plot shows that with InN-NPs, the measured memory hysteresis is much larger than in the case of control devices which only have ZnO charge trapping layer without NPs. At a very low operating voltage of -4/4 V, a 2 V V<sub>t</sub> shift is obtained. This confirms that InN-NPs act as charge trapping centers with high charge trapping density within the bandgap of ZnO. Since the control device with only ZnO charge trapping layer is showing a negligible memory window, the charge trap states density of the InN-NPs can be calculated using the following equation:<sup>16</sup>

$$N_t = \frac{C_t \times \Delta V_t}{q}, \quad (1)$$

where  $C_t$  is the capacitance of the charge trapping layer per unit area,  $\Delta V_t$  is the threshold voltage shift, and  $q$  is the elementary charge. At a gate voltage sweeping of -10/10 V and with  $C_t = 39.9 \text{ nF/cm}^2$ ,  $\Delta V_t$  is 5.5 V and corresponds to a charge trap states density of  $1.37 \times 10^{12} \text{ cm}^{-2}$  or equivalently  $2.29 \times 10^{-7} \text{ C/cm}^2$ , and at a gate voltage sweeping of -4/4 V, the  $\Delta V_t$  is 2 V, which corresponds to a charge trap states density of  $4.78 \times 10^{11} \text{ cm}^{-2}$  or  $7.98 \times 10^{-8} \text{ C/cm}^2$ .

Additionally, the retention characteristic of the memory was characterized by plotting the measured V<sub>t</sub> shift vs. time. The plot depicted in Fig. 5 shows an excellent retention characteristic where 22% of the initial charge is lost in 10 yr or a

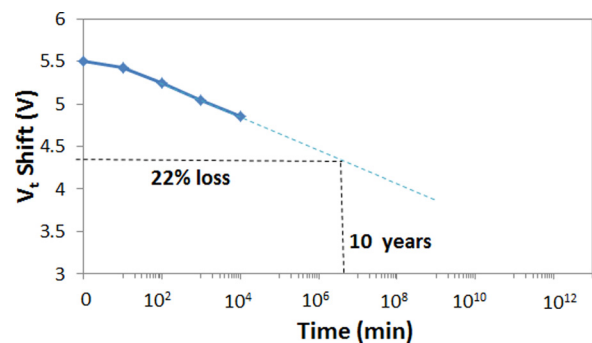


FIG. 5. V<sub>t</sub> shift vs time measured for the memory structures with InN nanoparticles at room temperature. The plot shows a remarkable retention characteristic.

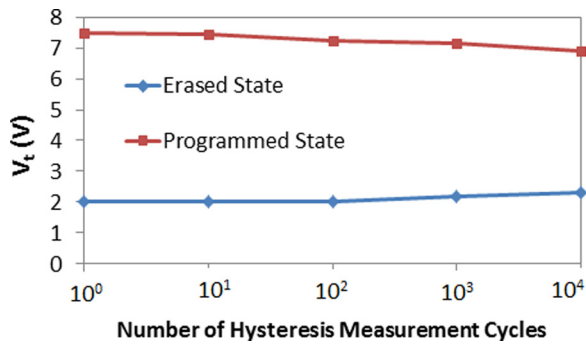


FIG. 6.  $V_t$  vs number of hysteresis measurement cycles. The plot shows excellent endurance characteristic.

reduction from 5.5 V to 4.4 V  $V_t$  shift after 10 yr. Compared to our previous work,<sup>8</sup> the retention of the memory with InN-NPs instead of Si-NPs is much improved. The larger electron affinity of the InN plays a major role in enhancing the retention property. InN differs from Si not only in terms of electron affinity and bandgap but also in terms of lattice spacing: 3.2 Å for Si NPs<sup>18</sup> while 2.7 Å for InN NPs.<sup>14</sup> Moreover, these differences in material properties account for the differences in the device performance.

Also, the endurance characteristic of the memory device was studied by plotting the threshold voltage vs. number of memory hysteresis measurement cycle. The measurements were made up to  $10^4$  cycles where the initial  $V_t$  shift of 5.5 V reduced to 4.9 V which means a loss of 11.8% of the initial charge as shown in Fig. 6, which highlights the good reliability of such memory structure.

In order to understand and explain the physics of InN-NPs based memory cell, the energy band diagram of the memory structure is plotted in Fig. 7 using the reported materials properties for InN, ZnO, and  $\text{Al}_2\text{O}_3$ .<sup>6–10</sup> First of all, the analysis of the energy band diagram shows a much smaller conduction band offset between Si channel and  $\text{Al}_2\text{O}_3$  tunnel oxide ( $\Delta E_c = 1.47 \text{ eV} \ll \Delta E_v = 4.08 \text{ eV}$ ), which makes the electrons tunneling probability much higher than holes tunneling probability. This analysis supports the observed electrons storage in the memory using C- $V_{\text{gate}}$  measurements. Additionally, the addition of the InN-NPs to ZnO increases the energy barrier for electrons during discharge due to the large electron affinity of the InN. This energy barrier increases from 1.9 eV to 3.25 eV, which exponentially reduces the back-tunneling (or charge leakage), therefore enhances the retention characteristic of the fabricated memory devices. The outstanding retention characteristic, shown in Fig. 5, is thus attributed to the large barrier for electrons stored in the InN-NPs owing to the very large electron affinity of the InN semiconductor. In addition, the

ZnO acts as a spacer (extra physical thickness) which electrons must overcome in order to discharge. This will further exponentially reduce the back tunneling of electrons, which will further enhance the retention of data in this memory structure. On the other hand, the required erase voltage for the memory cell might be increased due to this large barrier and might become larger than the applied programming voltage in the absolute value. However, the n-type nature of the ZnO helps to overcome this problem because it enhances the electric field across the tunnel oxide when a negative gate voltage is applied (during the erase operation); therefore, the required erase voltage can be reduced further. Since the C- $V_{\text{gate}}$  measurements of the erased state at different gate sweeping voltages are overlapping with the C- $V_{\text{gate}}$  curve of the memory at low sweeping voltage ( $-2/2 \text{ V}$ ), this indicates that the memory is being fully erased at all applied erase voltages, which confirms that the ZnO is indeed overcoming the effect of the large barrier on the needed erase voltage.

Moreover, the trap lifetime of the electrons confined in the InN-NPs between the barriers formed by  $\text{Al}_2\text{O}_3$  tunnel and blocking oxides is calculated. The ground state energy of the electrons confined in 16-nm InN-NPs is first calculated by adopting the following equation:<sup>19</sup>

$$E_0 = \frac{\hbar^2 \pi^2}{2m_0 L^2}, \quad (2)$$

where  $\hbar$  is the reduced Planck's constant,  $m_0$  is the electron effective mass in InN,<sup>20</sup> and  $L$  is the thickness of the InN-NPs. The ground state energy ( $E_0$ ) is calculated and found to be  $E_0 = 13.4 \text{ meV}$ . The tunneling probability can be then approximated using the following equation:<sup>18</sup>

$$T = 16 \times \left(\frac{E_0}{V_0}\right) \times \left(1 - \frac{E_0}{V_0}\right) \times e^{-2d \frac{\sqrt{2m_0(V_0 - E_0)}}{\hbar}}, \quad (3)$$

where  $V_0$  is the potential energy of the barrier (3.25 eV) and  $d$  is the thickness of the barrier. The transmission probability is found to be  $T = 5.837 \times 10^{-22}$ . The attempt frequency  $\nu$  can be estimated from  $\nu = \frac{E_0}{2\pi\hbar} = 3.24 \times 10^{12} \text{ s}^{-1}$ , and the trap lifetime of an electron confined in InN-NPs between the barriers would be  $\tau = (\nu T)^{-1} = 5.287 \times 10^8 \text{ s} = 16.754 \text{ yr}$ . The results support the observed long retention characteristic ( $>10 \text{ yr}$ ) of the memory structure with InN-NPs.

In conclusion, a charge trapping memory device with InN-NPs embedded in ZnO trapping layer is demonstrated. Using C- $V_{\text{gate}}$  hysteresis measurements, the memory showed a large  $V_t$  shift at reduced operating voltages. The charge trapping characteristics of the InN-NPs is quantified and the analysis of the energy band diagram supported the observed electrons storage in the InN-NPs and confirmed the

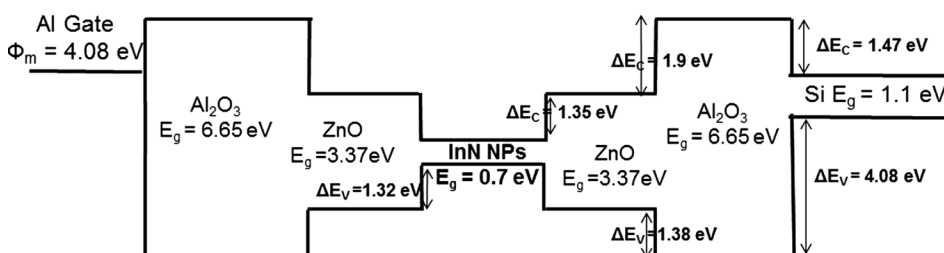


FIG. 7. Energy band diagram of the memory structure with InN nanoparticles with zero applied bias.



remarkable retention characteristic owing to the good confinement of charges in InN-NPs. Finally, the good reliability of the memory structure and the compatibility of the fabrication with current semiconductor processing technology highlight the potential of InN-NPs in future reliable, low-cost, and low operating voltage of charge trapping memory devices.

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